

Z80180 Z180 MPU

FEATURES:

- Operating Frequency to 12.5 MHz
- On-Chip MMU Supports Extended Address Space
- Two DMA Channels
- On-Chip Wait State Generators
- Two UART Channels
- Two 16-Bit Timer Channels
- On-Chip Interrupt Controller
- On-Chip Clock Oscillator/Generator
- Clocked Serial I/O Port
- Code Compatible with Zilog Z80 CPU
- Extended Instructions
- 6 MHz Version Supports 6.144 MHz CPU Clock Operation

GENERAL DESCRIPTION:

Based on a microcoded execution unit and an advanced CMOS manufacturing technology, the Z80180 is an 8-bit MPU which provides the benefits of reduced system costs and low power operation while offering higher performance and maintaining compatibility with a large base of industry standard software written around the Zilog Z80 CPU.

Higher performance is obtained by virtue of higher operating frequencies, reduced instruction execution times, an enhanced instruction set, and an on-chip memory management unit (MMU) with the capability of addressing up to 1 Mbyte of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several "glue"

functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Not only does the Z80180 consume a low amount of power during normal operation, but it also provides two operating modes that are designed to drastically reduce the power consumption even further. The SLEEP mode reduces power by placing the CPU into a "stopped" state, thereby consuming less current, while the on-chip I/O device is still operating. The SYSTEM STOP mode places both the CPU and the on-chip peripherals into a "stopped" mode, thereby reducing power consumption even further.

When combined with other CMOS VLSI devices and memories, the Z80180 provides an excellent solution to system applications requiring high performance, and low power operation.

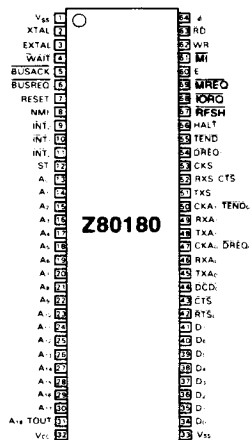


Figure 1. 64 Pin DIP

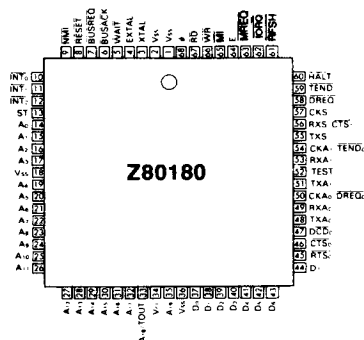


Figure 2. 68 Pin PLCC

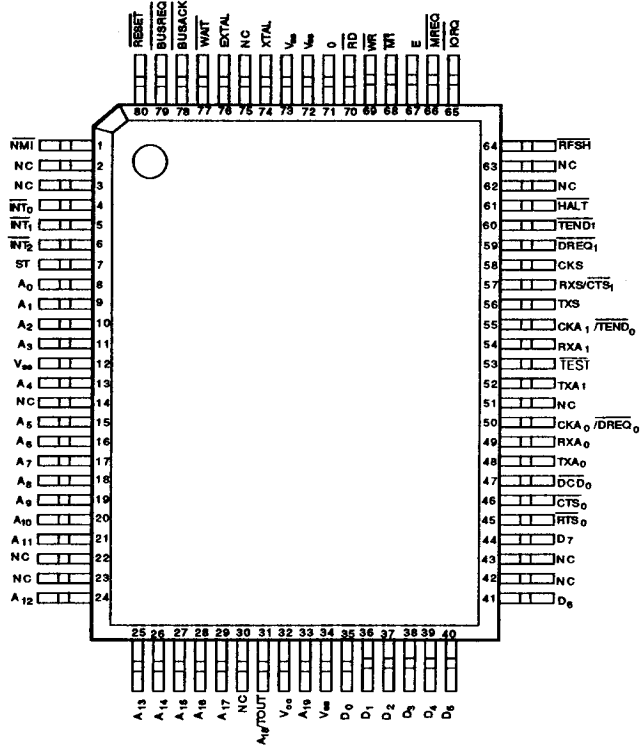


Figure 2b. 80-pin Quad Flat Pack

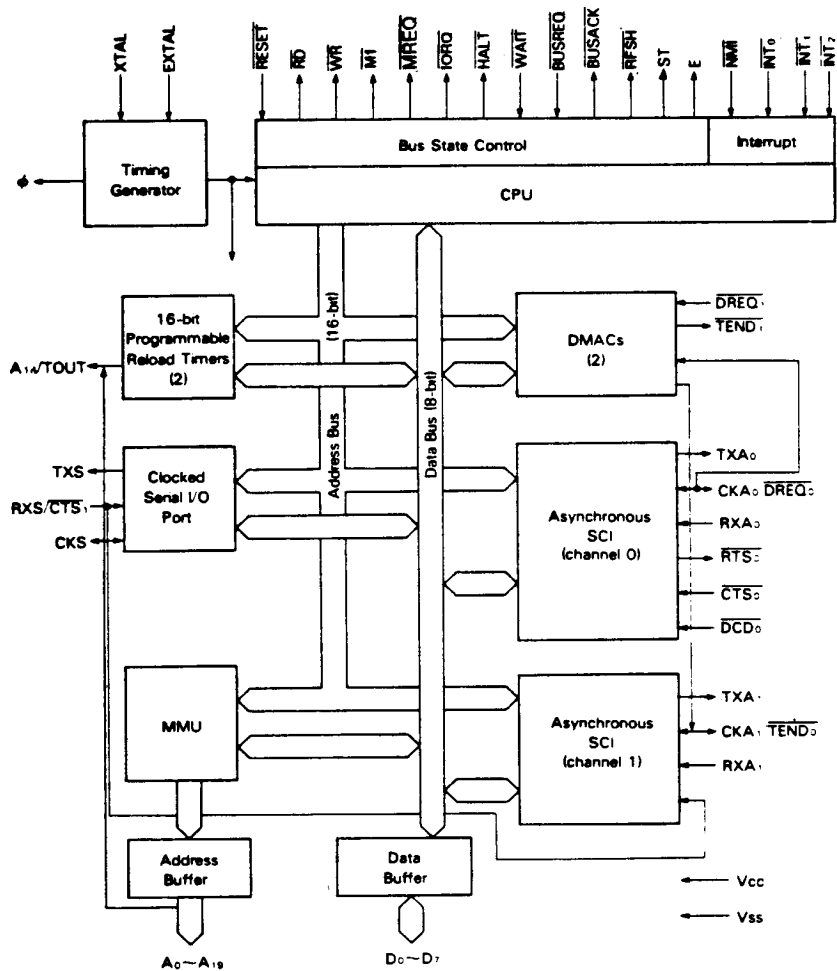


Figure 3. Block Diagram

PIN DESCRIPTION:

A₀-A₁₉. Address Bus (Output, active High, 3-state). A₀-A₁₉ form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges, up to 1 Mbyte, and I/O data bus exchanges, up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles. Address line A₁₈ is multiplexed with the output of PRT channel 1 (TOUT, selected as address output on reset) and address line A₁₉ is not available in DIP versions of the Z80180.

BUSACK. Bus Acknowledge (Output, active Low). BUSACK indicates the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

BUSREQ. Bus Request (Input, active Low). This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address and data buses, and other control signals, into the high impedance state.

CKA₀, CKA₁. Asynchronous Clock 0 and 1 (Bidirectional, active High). These pins are the transmit and receive clocks for the synchronous channels. CKA₀ is multiplexed with DREQ₀ and CKA₁ is multiplexed with TEND₀.

CKS. Serial Clock (Bidirectional, active High). This line is clock for the CSIO channel.

CLOCK. System Clock (Output, active High). The output is used as a reference clock for the MPU and the external system. The frequency of this output is equal to one-half that of the crystal or input clock frequency.

CTS₀-CTS₁. Clear to Send 0 and 1 (Inputs, active Low). These lines are modem control signals for the ASCII channels. CTS₁ is multiplexed with RXS.

D₀-D₇. Data Bus (Bidirectional, active High, 3-state). D₀-D₇ constitute an 8-bit bidirectional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles.

DCD₀. Data Carrier Detect 0 (Input, active Low). This is a programmable modem control signal for ASCII channel 0.

DREQ₀, DREQ₁. DMA Request 0 and 1 (Input, active Low). DREQ is used to request a DMA transfer from one of the on-chip DMA channels. The DMA channels monitor these inputs to determine when an external device is ready for a read or write operation. These inputs can be programmed to be either level or edge sensed. DREQ₀ is multiplexed with CKA₀.

E. Enable Clock (Output, active High). Synchronous machine cycle clock output during bus transactions.

EXTAL. External Clock/Crystal (Input, active High). Crystal oscillator connection. An external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt triggered.

HALT. Halt/Sleep Status (Output, active Low). This output is asserted after the CPU has executed either the HALT or SLP instruction, and is waiting for either non-maskable or maskable interrupt before operation can resume. It is also used with the M₁ and ST signals to decode status of the CPU machine cycle.

INT₀. Maskable Interrupt Request 0 (Input, active Low). This signal is generated by external I/O devices. The CPU will honor this request at the end of the current instruction cycle as long as the NMI and BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the M₁ and IORQ signals will become active.

INT₁, INT₂. Maskable Interrupt Requests 1 and 2 (Inputs, active Low). This signal is generated by external I/O devices. The CPU will honor these requests at the end of the current instruction cycle as long as the NMI, BUSREQ, and INT₀ signals are inactive. The CPU will acknowledge these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgement for INT₀, during this cycle neither the M₁ or IORQ signals will become active.

IORQ. I/O Request (Output, active Low, 3-state). IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. IORQ is also generated, along with M₁, during the acknowledgement of the INT₀ input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

M₁. Machine Cycle 1 (Output, active Low). Together with MREQ, M₁ indicates that the current cycle is the opcode fetch cycle of an instruction execution. Together with IORQ, M₁ indicates that the current cycle is for an interrupt acknowledge. It is also used with the HALT and ST signal to decode status of the CPU machine cycle. This signal is analogous to the LIR signal of the Z64180.

MREQ. Memory Request (Output, active Low, 3-state). MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the ME signal of the Z64180.

NMI. Non-maskable Interrupt (Input, negative edge triggered). NMI has a higher priority than INT and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066H.

RD. *Read (Output, active Low, 3-state).* RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

RFSH. *Refresh (Output, active Low).* Together with MREQ, RFSH indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7-A0) contain the refresh address.

This signal is analogous to the REF signal of the Z64180.

RTS₀. *Request to Send 0 (Output, active Low).* This is a programmable modem control signal for ASCII channel 0.

RXA₀, RXA₁. *Receive Data 0 and 1 (Inputs, active High).* These signals are the receive data to the ASCII channels.

RXS. *Clocked Serial Receive Data (Input, active High).* This line is the receiver data for the CSIO channel. RXS is multiplexed with the CTS₁ signal for ASCII channel 1.

ST. *Status (Output, active High).* This signal is used with the M1 and HALT output to decode the status of the CPU machine cycle.

Note that the output from M1 is affected by the status of the M1E bit in OMCR register. Table 1 shows the status while M1E = 1.

ST	HALT	M1	Operation
0	1	0	CPU operation (1st op-code fetch)
1	1	0	CPU operation (2nd op-code and 3rd op-code fetch)
1	1	1	CPU operation (MC except for op-code fetch)
0	X	1	DMA operation
0	0	0	HALT mode
1	0	1	SLEEP mode (including SYSTEM STOP mode)

NOTE X: Don't care
MC: Machine cycle

Table 1. Status Summary

TEND₀, TEND₁. *Transfer End 0 and 1 (Outputs, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. TEND₀ in multiplexed with CKA₁.

TEST (Output): This pin is for test and is left open.

TOUT. *Timer Out (Output, active High).* TOUT is the pulse output from PRT channel 1. This line is multiplexed with A₁₈ of the address bus.

TXA₀, TXA₁. *Transmit Data 0 and 1 (Outputs, active High).* These signals are the transmitted data from the ASCII channels. Transmitted data changes are with respect to the falling edge of the transmit clock.

TXS. *Clocked Serial Transmit Data (Output, active High).* This line is the transmitted data from the CSIO channel.

WAIT. *Wait (Input, active Low).* WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The WAIT input is sampled on the falling edge of T₂ (and subsequent wait states). If the input is sampled low, then additional wait states are inserted until the WAIT input is sampled high, at which time execution will continue.

WR. *Write (Output, active Low, 3-state).* WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

XTAL. *Crystal (Input, active High).* Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

Multiplexed pin descriptions

A₁₈/TOUT

During RESET, this pin is initialized as A₁₈ pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, TOUT function is selected. If TOC1 and TOC0 bits are cleared to 0, A₁₈ function is selected.

CKA₀/DREQ₀

During RESET, this pin is initialized as CKA₀ pin. If either DM1 or SM1 in DMA Mode Register (DMODE) is set to 1, DREQ₀ function is always selected.

CKA₁/TEND₀

During RESET, this pin is initialized as CKA₁ pin. If CKA1D bit in ASCII control register ch 1 (CNTLA1) is set to 1, TEND₀ function is selected. If CKA1D bit is set to 0, CKA₁ function is selected.

RXS/CTS₁

During RESET, this pin is initialized as RXS pin. If CTS1E bit in ASCII status register ch1 (STAT1) is set to 1, CTS₁ function is selected. If CTS1E bit is set to 0, RXS function is selected.

ARCHITECTURE:

The Z80180 combines a high performance CPU core with a variety of system and I/O resources useful in a broad range of applications. The CPU core consists of five functional blocks: clock generator, bus state controller (including dynamic memory refresh), interrupt controller, memory management unit (MMU), and the central processing unit (CPU). The integrated I/O resources make up the remaining four functional blocks: direct memory access (DMA) control (2 channels), asynchronous serial communications interface (ASCI, 2 channels), programmable reload timers (PRT, 2 channels), and a clock serial I/O (CSIO) channel.

Clock Generator. This logic generates the system clock from either an external crystal or clock input. The external clock is divided by two and provided to both internal and external devices.

Bus State Controller. This logic performs all of the status and bus control activity associated with both the CPU and some on-chip peripherals. This includes wait state timing, reset cycles, DRAM refresh, and DMA bus exchanges.

Interrupt Controller. This block monitors and prioritizes the variety of internal and external interrupts and traps to provide the correct responses from the CPU. To remain compatible with the Z80 CPU, three different interrupt modes are supported.

Memory Management Unit. The MMU allows the user to "map" the memory used by the CPU (logically only 64K) into the 1M Byte addressing range supported by the Z80180. The organization of the MMU object code compatibility with the Z80 CPU while offering access to an extended memory space. This is accomplished by using an effective "common area - banked area" scheme.

Central Processing Unit. The CPU is microcoded to provide a core that is object code compatible with the Z80 CPU. It also provides a superset of the Z80 instruction set, including 8-bit multiply and divide. This core has been enhanced to allow many of the instructions to execute in fewer clock cycles.

DMA Controller. The DMA controller provides high speed transfers between memory and I/O devices. Transfer operations supported are memory to memory, memory to/from I/O, and I/O to I/O. Transfer modes supported are request, burst, and cycle steal. DMA transfers can access the full 1 Mbyte addressing range with a block length up to 64K bytes, and can cross over 64K boundaries.

Asynchronous Serial Communications Interface (ASCI). The ASCI logic provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels can also support a multiprocessor communications format.

Programmable Reload Timer (PRT). This logic consists of two separate channels, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is derived from the system clock (divided by 20) before reaching the counter. PRT channel 1 provides an optional output to allow for waveform generation.

Clocked Serial I/O (CSIO). The CSIO channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another microprocessor or microcomputer.

OPERATION MODES:

The Z80180 can be configured to operate like the 64180. This is accomplished by allowing the user to have control over the $\overline{M1}$, \overline{IORQ} , \overline{WR} , and \overline{RD} signals. The Operation Mode Control Register (OMCR) determines the $\overline{M1}$ options; the timing of the \overline{IORQ} , \overline{RD} , and \overline{WR} signals; and the RETI operation.

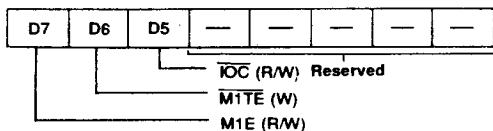


Figure 4. Operation Mode Control Register
(I/O Address = 3 EH)

$\overline{M1E}$ ($\overline{M1}$ Enable): This bit controls the $\overline{M1}$ output and is set to a 1 during reset.

When $\overline{M1E}=1$, the $\overline{M1}$ output is asserted LOW during the opcode fetch cycle, the $\overline{INT0}$ acknowledge cycle, and the first machine cycle of the \overline{NMI} acknowledge. This will also cause the $\overline{M1}$ signal to be active during both fetches of the RETI instruction sequence, which may cause corruption of the external interrupt daisy chain. Hence, this bit should be set to 0 for the Z80180. When $\overline{M1E}=0$, the $\overline{M1}$ output is normally inactive and asserted LOW only during the refetch of the RETI instruction sequence and during the $\overline{INT0}$ acknowledge cycle.

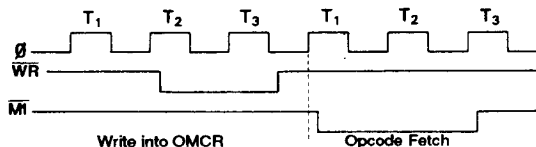


Figure 5. $\overline{M1}$ Temporary Enable Timing

$\overline{M1TE}$ ($\overline{M1}$ Temporary Enable): This bit controls the temporary assertion of the $\overline{M1}$ signal. It is always read back as

a '1' and is set to 1 during reset. This function is used to "arm" the internal interrupt structure of the Z80PIO. When a control word is written to the Z80PIO to enable interrupts, no enable actually takes place until the PIO sees an active $\overline{M\overline{I}}$ signal. When $\overline{M\overline{I}TE}=1$, there is no change in the operation of the $\overline{M\overline{I}}$ signal and $\overline{M\overline{I}E}$ controls its function. When $\overline{M\overline{I}TE}=0$, the $\overline{M\overline{I}}$ output will be asserted during the next opcode fetch cycle regardless of the state programmed into the $\overline{M\overline{I}E}$ bit. This is only momentary (one time) and the user need not reprogram a 1 to disable the function (See Figure 5).

$\overline{IO\overline{C}}$: this bit controls the timing of the \overline{IORQ} and \overline{RD} signals. It is set to 1 by reset.

When $\overline{IO\overline{C}}=1$, the \overline{IORQ} and \overline{RD} signals function the same as the Z64180.

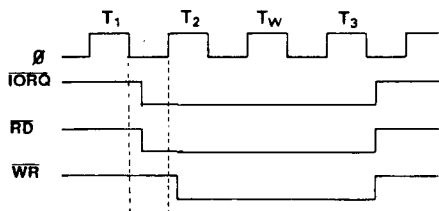


Figure 6. I/O Read and Write Cycles with $\overline{IO\overline{C}}=1$

When $\overline{IO\overline{C}}=0$, the timing of the \overline{IORQ} and \overline{RD} signals match the timing required by the Z80 family of peripherals. The \overline{IORQ} and \overline{RD} signals will go active as a result of the rising edge of T2. This allows the Z80180 to satisfy the setup times required by the Z80 peripherals on those two signals.

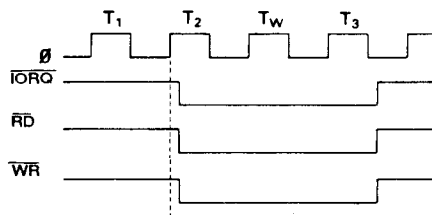


Figure 7. I/O Read and Write Cycles with $\overline{IO\overline{C}}=0$

For the rest of this manual, it is assumed that $\overline{M\overline{I}E}=0$ and $\overline{IO\overline{C}}=0$. The user must program the Operation Mode Control Register before the first I/O instruction is executed.

TIMING:

This section explains the Z80180 CPU timing for the following operations:

- Instruction (op-code) fetch timing.
- Operand and data read/write timing.
- I/O read/write timing.
- Basic instruction (fetch and execute) timing.
- RESET timing.
- BUSREQ/BUSACK bus exchange timing.

The basic CPU operation consists of one or more "Machine Cycles" (MC). A machine cycle consists of three system clocks, T1, T2, and T3 while accessing memory or I/O, or it consists of one system clock (T1) during CPU internal operations. The system clock is half the frequency of the Crystal oscillator (e.g., an 8 MHz crystal produces 4 MHz or 250 nsec). For interfacing to slow memory or peripherals, optional wait states (Tw) may be inserted between T2 and T3.

Instruction (op-code) Fetch Timing. Fig. 8 shows the instruction (op-code) fetch timing with no wait states. An op-code fetch cycle is externally indicated when the $\overline{M\overline{I}}$ output pin is LOW.

In the first half of T1, the address bus (A0-A19) is driven

from the contents of the Program Counter (PC). Note that this is the translated address output of the Z80180 on-chip MMU.

In the second half of T1, the \overline{MREQ} (Memory Request) and \overline{RD} (Read) signals are asserted LOW, enabling the memory.

The op-code on the data bus is latched at the rising edge of T3 and the bus cycle terminates at the end of T3.

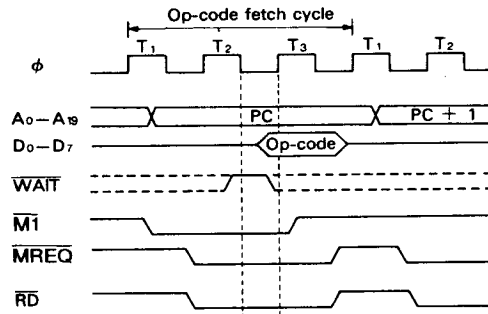


Figure 8. Opcode Fetch timing (Without Wait State)

Fig. 9 illustrates the insertion of wait states (T_w) into the op-code fetch cycle. Wait states (T_w) are controlled by the external WAIT input combined with an on-chip programmable wait state generator.

At the falling edge of T_2 the combined WAIT input is sampled. If WAIT input is asserted LOW, a wait state (T_w) is inserted. The address bus, MREQ, RD and MI are held stable during wait states. When the WAIT is sampled inactive HIGH at the falling edge of T_w , the bus cycle enters T_3 and completes at the end of T_3 .

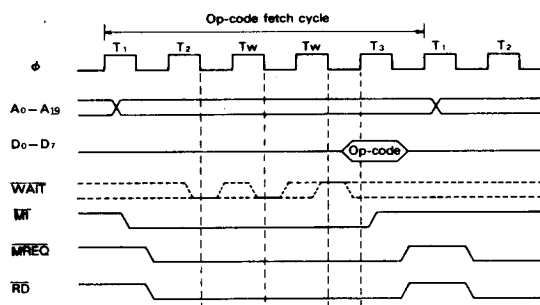


Figure 9. Opcode Fetch Timing (With Wait State)

Operand and Data Read/Write Timing. The instruction operand and data read/write timing differs from op-code fetch timing in two ways. First, the MI output is held inactive. Second, the read cycle timing is relaxed by one-half clock cycle since data is latched at the falling edge of T_3 .

Instruction operands include immediate data, displacement, and extended addresses, and have the same timing as memory data reads.

During memory write cycles the MREQ signal goes active in the second half of T_1 . At the end of T_1 , the data bus is driven with the write data.

At the start of T_2 , the WR signal is asserted LOW enabling the memory. MREQ and WR go inactive in the second half of T_3 followed by disabling of the write data on the data bus.

Wait states (T_w) are inserted as previously described for op-code fetch cycles. Fig. 10 illustrates the read/write timing without wait states (T_w), while Fig. 11 illustrates read/write timing with wait states (T_w).

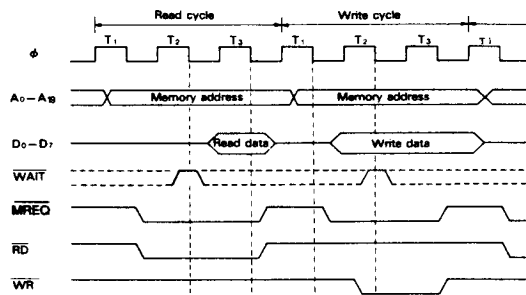


Figure 10. Memory Read/Write Timing (Without Wait State)

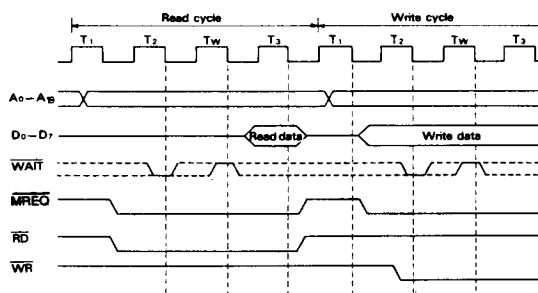


Figure 11. Memory Read/Write Timing (With Wait State)

I/O Read/Write Timing. I/O instructions cause data read/write transfers which differ from memory data transfers in the following three ways:

1. The IORQ (I/O Request) signal is asserted LOW instead of the MREQ signal.
2. The 16-bit I/O address is not translated by the MMU.
3. A16-A19 are held LOW.

At least one wait state (T_w) is always inserted for I/O read and write cycles (except internal I/O cycles).

Fig. 12 shows I/O read/write timing with the automatically inserted wait state (T_w).

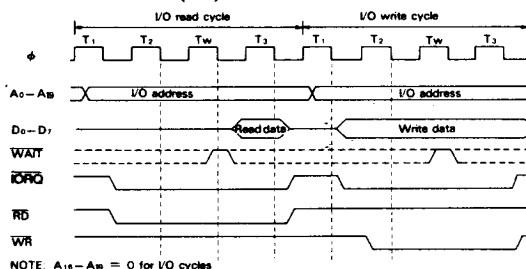


Figure 12. I/O Read/Write Timing

Basic Instruction Timing. An instruction may consist of a number of machine cycles including op-code fetch, operand fetch, and data read/write cycles. An instruction may also include cycles for internal processes which make the bus idle.

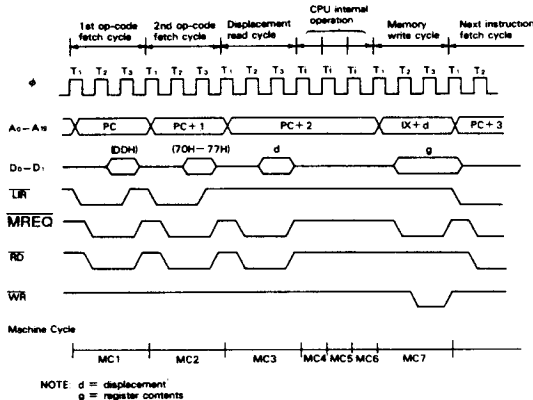


Figure 13. Instruction Timing

The example in Fig. 13 illustrates the bus timing for the data transfer instruction LD (IX+d),g. This instruction moves the contents of a CPU register (g) to the memory location with address computed by adding a signed 8-bit displacement (d) to the contents of an index register (IX).

The instruction cycle starts with the two machine cycles to read the two byte instruction op-code as indicated by \overline{MREQ} LOW. Next, the instruction operand (d) is fetched.

The external bus is idle while the CPU computes the effective address. Finally, the computed memory location is written with the contents of the CPU register (g).

RESET Timing. Fig. 14 shows the Z80180 hardware RESET timing. If the \overline{RESET} pin is LOW for six or more than six clock cycles, processing is terminated and the Z80180 restarts execution from (logical and physical) address 00000H.

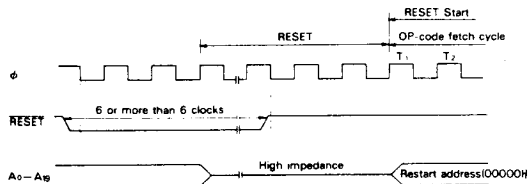


Figure 14. Reset Timing

BUSREQ/BUSACK Bus Exchange Timing. The Z80180 can coordinate the exchange of control, address and data bus ownership with another bus master. The alternate bus master can request the bus release by asserting the \overline{BUSREQ} (Bus Request) input LOW. After the Z80180 releases the bus, it relinquishes control to the alternate bus master by asserting the \overline{BUSACK} (Bus Acknowledge) output LOW.

The bus may be released by the Z80180 at the end of each machine cycle. In this context, a machine cycle consists of a minimum of 3 clock cycles (more if wait states are inserted) for op-code fetch, memory read/write, and I/O read/write cycles. Except for these cases, a machine cycle corresponds to one clock cycle.

When the bus is released, the address (A_0-A_{19}), data (D_0-D_7), and control (\overline{MREQ} , \overline{IORQ} , \overline{RD} , and \overline{WR}) signals are placed in the high impedance state.

Note that dynamic RAM refresh is not performed when the Z80180 has released the bus. The alternate bus master must provide dynamic memory refreshing if the bus is released for long periods of time.

Fig. 15 illustrates $\overline{BUSREQ}/\overline{BUSACK}$ bus exchange during a memory read cycle. Fig. 16 illustrates bus exchange when the bus release is requested during a Z80180 CPU internal operation. \overline{BUSREQ} is sampled at the falling edge of the system clock prior to T_3 , T_1 and T_x (BUS RELEASE state). If \overline{BUSREQ} is asserted LOW at the falling edge of the clock state prior to T_x , another T_x is executed.

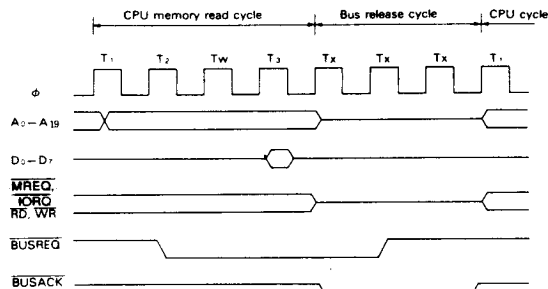


Figure 15. Bus Exchange Timing

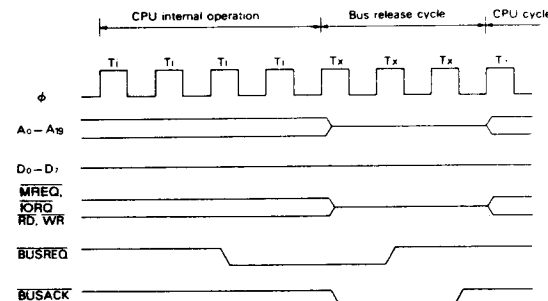


Figure 16. Bus Exchange Timing

WAIT State Generator

To ease interfacing with slow memory and I/O devices, the Z80180 uses wait states (T_w) to extend bus cycle timing. A wait state(s) is inserted based on the combined (logical OR) state of the external $\overline{\text{WAIT}}$ input and an internal programmable wait state (T_w) generator. Wait states (T_w) can be inserted in both CPU execution and DMA transfer cycles.

When the external $\overline{\text{WAIT}}$ input is asserted LOW, wait state(s) (T_w) are inserted between T_2 and T_3 to extend the bus cycle duration. The $\overline{\text{WAIT}}$ input is sampled at the falling edge of the system clock in T_2 or T_w . If the $\overline{\text{WAIT}}$ input is asserted LOW at the falling edge of the system clock in T_w , another T_w is inserted into the bus cycle. Note that $\overline{\text{WAIT}}$ input transitions must meet specified set-up and hold times. This can easily be accomplished by externally synchronizing $\overline{\text{WAIT}}$ input transitions with the rising edge of the system clock.

Dynamic RAM refresh is not performed during wait states (T_w) and thus system designs which use the automatic

refresh function must consider the affects of the occurrence and duration of wait states (T_w). Figure 17 shows WAIT timing.

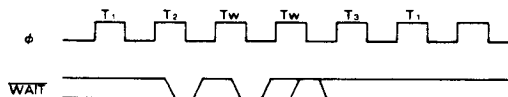


Figure 17. $\overline{\text{WAIT}}$ Timing

Programmable Wait State Insertion. In addition to the $\overline{\text{WAIT}}$ input, wait states (T_w) can also be inserted by program using the Z80180 on-chip wait state generator. Wait state (T_w) timing applies for both CPU execution and on-chip DMAC cycles.

By programming the four significant bits of the DMA/ $\overline{\text{WAIT}}$ Control Register (DCNTL) the number of wait states, (T_w) automatically inserted in memory and I/O cycles, can be separately specified.

HALT and Low Power Operation Modes

The Z80180 can operate in 4 different modes. HALT mode, IOSTOP mode and 2 low power operation modes - SLEEP and SYSTEM STOP. Note that in all operating modes, the basic CPU clock (XTAL, EXTAL) must remain active.

HALT mode. HALT mode is entered by execution of the HALT instruction (op-code = 76H) and has the following characteristics.

- (1) The internal CPU clock remains active.
- (2) All internal and external interrupts can be received.
- (3) Bus exchange ($\overline{\text{BUSREQ}}$ and $\overline{\text{BUSACK}}$) can occur.
- (4) Dynamic RAM refresh cycle ($\overline{\text{RFSH}}$) insertion continues at the programmed interval.
- (5) I/O operations (ASCII, CSI/O and PRT) continue.
- (6) The DMAC can operate.
- (7) The $\overline{\text{HALT}}$ output pin is asserted LOW.
- (8) The external bus activity consists of repeated "dummy" fetches of the op-code following the HALT instruction.

Essentially, the Z80180 operates normally in HALT mode, except that instruction execution is stopped.

HALT mode can be exited in the following two ways.

RESET Exit from HALT mode. If the $\overline{\text{RESET}}$ input is as-

serted LOW for at least 6 clock cycles, HALT mode is exited and the normal RESET sequence (restart at address 00000H) is initiated.

Interrupt Exit from HALT mode. When an internal or external interrupt is generated, HALT mode is exited and the normal interrupt response sequence is initiated.

If the interrupt source is masked (individually by enable bit, or globally by IEF1 state), the Z80180 remains in HALT mode. However, $\overline{\text{NMI}}$ interrupt will initiate the normal $\overline{\text{NMI}}$ interrupt response sequence independent of the state of IEF1.

HALT timing is shown in Fig 18.

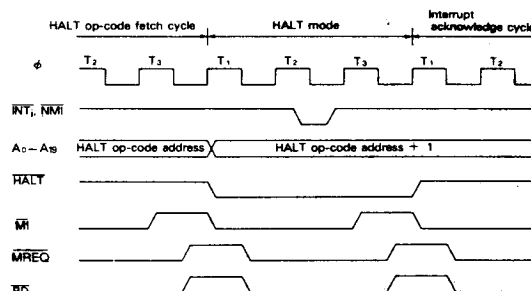


Figure 18. HALT Timing

SLEEP mode. SLEEP mode is entered by execution of the 2 byte SLP instruction. SLEEP mode has the following characteristics.

- (1) The internal CPU clock stops, reducing power consumption.
- (2) The internal crystal oscillator does not stop.
- (3) Internal and external interrupt inputs can be received.
- (4) DRAM refresh cycles stop.
- (5) I/O operations using on-chip peripherals continue.
- (6) The internal DMAC stop.
- (7) $\overline{\text{BUSREQ}}$ can be received and acknowledged.
- (8) Address outputs go HIGH and all other control signal output become inactive HIGH.
- (9) Data Bus, 3-state.

SLEEP mode is exited in one of two ways as shown below.

RESET Exit from SLEEP mode. If the $\overline{\text{RESET}}$ input is held LOW for at least 6 clock cycles, it will exit SLEEP mode and begin the normal RESET sequence with execution starting at address (logical and physical) 00000H.

Interrupt Exit from SLEEP mode. The SLEEP mode is exited by detection of an external (NMI, INT_0 - INT_2) or internal (ASCI, CSI/O, PRT) interrupt.

In case of NMI, SLEEP Mode is exited and the CPU begins the normal NMI interrupt response sequence.

In the case of all other interrupts, the interrupt response depends on the state of the global interrupt enable flag (IEF_1) and the individual interrupt source enable bit.

If the individual interrupt condition is disabled by the corresponding enable bit, occurrence of that interrupt is ignored and the CPU remains in the SLEEP state.

Assuming the individual interrupt condition is enabled, the response to that interrupt depends on the global interrupt enable flag (IEF_1). If interrupts are globally enabled

($\text{IEF}_1=1$) and an individually enabled interrupt occurs, SLEEP mode is exited and the appropriate normal interrupt response sequence is executed.

If interrupts are globally disabled ($\text{IEF}_1=0$) and an individually enabled interrupt occurs, SLEEP mode is exited and instruction execution begins with the instruction following the SLP instruction. Note that this provides a technique for synchronization with high speed external events without incurring the latency imposed by an interrupt response sequence.

Figure 19 shows SLEEP timing.

I/O STOP mode. I/O STOP mode is entered by setting the IOSTOP bit of the I/O Control Register (ICR) to 1. In this case, on-chip I/O (ASCI, CSI/O, PRT) stops operating. However, the CPU continues to operate. Recovery from IOSTOP mode is by resetting the IOSTOP bit in ICR to 0.

SYSTEM STOP mode. SYSTEM STOP mode is the combination of SLEEP and IOSTOP modes. SYSTEM STOP mode is entered by setting the IOSTOP bit in ICR to 1 followed by execution of the SLP instruction. In this mode, on-chip I/O and CPU stop operating, reducing power consumption. Recovery from SYSTEM STOP mode is the same as recovery from SLEEP mode, noting that internal I/O sources (disabled by IOSTOP) cannot generate a recovery interrupt.

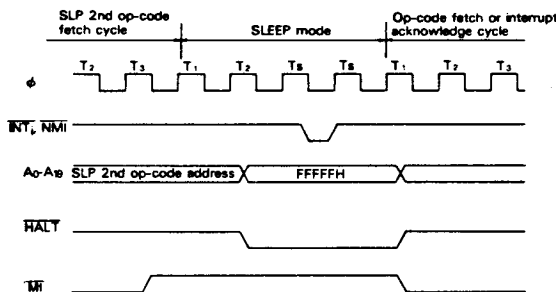


Figure 19. SLEEP Timing

Trap and Interrupts

The Z80180 CPU has twelve interrupt sources, 4 external and 8 internal, with fixed priority. (Reference Figure 20).

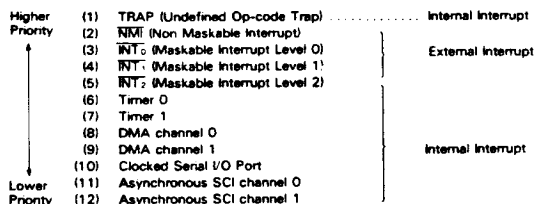


Figure 20. Interrupt Sources

TRAP Interrupt. The Z80180 generates a non-maskable TRAP interrupt when an undefined op-code fetch occurs. This feature can be used to increase software reliability, implement an "extended" instruction set, or both. TRAP may occur during op-code fetch cycles and also if an undefined op-code is fetched during the interrupt acknowledge cycle for $\overline{\text{INT}}_0$ when Mode 0 is used.

When a TRAP interrupt occurs the Z80180 operates as follows.

- (1) The TRAP bit in the Interrupt TRAP/Control (ITC) register is set to 1.
- (2) The current PC (Program Counter) value, reflecting location of the undefined op-code, is saved on the stack.
- (3) The Z80180 vectors to logical address 0. Note that if logical address 0000H is mapped to physical address 00000H, the vector is the same as for RESET. In this case, testing the TRAP bit in ITC will reveal whether the restart at physical address 00000H was caused by RESET or TRAP.

External Interrupts. The Z80180 has four external hardware interrupt inputs.

- (1) $\overline{\text{NMI}}$ - Non-maskable Interrupt
- (2) $\overline{\text{INT}}_0$ - Maskable Interrupt Level 0
- (3) $\overline{\text{INT}}_1$ - Maskable Interrupt Level 1
- (4) $\overline{\text{INT}}_2$ - Maskable Interrupt Level 2

$\overline{\text{NMI}}$, $\overline{\text{INT}}_1$ and $\overline{\text{INT}}_2$ have fixed interrupt response modes. $\overline{\text{INT}}_0$ has 3 different software programmable interrupt response modes - Mode 0, Mode 1 and Mode 2.

$\overline{\text{NMI}}$ - Non-Maskable Interrupt. The $\overline{\text{NMI}}$ interrupt input is edge sensitive and cannot be masked by software. When $\overline{\text{NMI}}$ is detected, the Z80180 operates as follows.

- (1) DMAC operation is suspended by the clearing of the DME (DMA Main Enable) bit in DCNTL.
- (2) The PC is pushed onto the stack.
- (3) The contents of IEF₁ are copied to IEF₂. This saves the interrupt reception state that existed prior to $\overline{\text{NMI}}$.
- (4) IEF₁ is cleared to 0. This disables all external and internal maskable interrupts (i.e. all interrupts except $\overline{\text{NMI}}$ and TRAP).
- (5) Execution commences at logical address 0066H.

The last instruction of an $\overline{\text{NMI}}$ service routine should be RETN (Return from Non-maskable Interrupt). This restores the stacked PC, allowing the interrupted program to continue.

$\overline{\text{INT}}_0$ - Maskable Interrupt Level 0

The next highest priority external interrupt after $\overline{\text{NMI}}$ is $\overline{\text{INT}}_0$. $\overline{\text{INT}}_0$ is sampled at the falling edge of the clock state prior to T₃ or T₁ in the last machine cycle. If $\overline{\text{INT}}_0$ is asserted LOW at the falling edge of the clock state prior to T₃ or T₁ in the last machine cycle, $\overline{\text{INT}}_0$ is accepted. The interrupt is masked if either the IEF₁ flag or the ITE₀ (Interrupt Enable 0) bit in ITC are reset to 0.

The $\overline{\text{INT}}_0$ interrupt is unique in that 3 programmable interrupt response modes are available - Mode 0, Mode 1 and Mode 2. The specific mode is selected with the IM 0, IM 1 and IM 2 (Set Interrupt Mode) instructions. During RESET, the Z80180 is initialized to use Mode 0 for $\overline{\text{INT}}_0$. The 3 interrupt response modes for $\overline{\text{INT}}_0$ are:

- (1) Mode 0 - Instruction fetch from data bus.
- (2) Mode 1 - Restart at logical address 0038H.
- (3) Mode 2 - Low byte vector table address fetch from data bus.

$\overline{\text{INT}}_0$ Mode 0

During the interrupt acknowledge cycle, an instruction is fetched from the data bus (D₀-D₇) at the rising edge of T₃. Often, this instruction is one of the eight single byte RST (RESTART) instructions which stack the PC and restart execution at a fixed logical address. However, multibyte instructions can be processed if the interrupt acknowledging device can provide a multibyte response. Unlike all other interrupts, the PC is not automatically stacked.

Note that TRAP interrupt will occur if an invalid instruction is fetched during Mode 0 interrupt acknowledge.

$\overline{\text{INT}}_0$ Mode 1

When $\overline{\text{INT}}_0$ is received, the PC is stacked and instruction execution restarts at logical address 0038H. Both IEF₁ and IEF₂ flags are reset to 0, disabling all maskable interrupts. The interrupt service routine should normally terminate with the EI (Enable Interrupts) instruction followed by the RETI (Return from Interrupt) instruction, to reenables the interrupts.

$\overline{\text{INT}}_0$ Mode 2

This method determines the restart address by reading the contents of a table residing in memory. The vector table consists of up to 128 two-byte restart addresses stored in low byte, high byte order.

The vector table address is located on 256 byte boundaries in the 64K byte logical address space programmed in the 8-bit Interrupt Vector Register (I).

During the $\overline{\text{INT}}_0$ Mode 2 acknowledge cycle, the low-order 8 bits of the vector is fetched from the data bus at the rising edge of T₃ and the CPU acquires the 16-bit vector.

Next, the PC is stacked. Finally, the 16-bit restart address is fetched from the vector table and execution begins at that address.

Note that external vector acquisition is indicated by both $\overline{M1}$ and \overline{IORQ} LOW. Two wait states (T_w) are automatically inserted for external vector fetch cycles.

INT₁, INT₂

The operation of external interrupts INT₁ and INT₂ is a vector mode similar to INT₀ Mode 2. The difference is that INT₁ and INT₂ generate the low-order byte of vector table address using the IL (Interrupt Vector Low) register rather than fetching it from the data bus. This is also the interrupt response sequence used for all internal interrupts (except TRAP).

Internal Interrupts. Internal interrupts (except TRAP) use the same vectored response mode as INT₁ and INT₂. Internal interrupts are globally masked by IEF₁ = 0. Individual internal interrupts are enabled/disabled by programming each individual I/O (PRT, DMAC, CSI/O, ASCI) control register. The lower vector of INT₁, INT₂ and internal interrupt are summarized in Table 2.

Interrupt Source	Priority	IL	Fixed Code
INT ₁	Highest	b ₇ b ₆ b ₅	b ₄ b ₃ b ₂ b ₁ b ₀
INT ₂		* * *	0 0 0 0 0
PRT channel 0		* * *	0 0 1 0 0
PRT channel 1		* * *	0 0 1 1 0
DMA channel 0		* * *	0 1 0 0 0
DMA channel 1		* * *	0 1 0 1 0
CSI/O		* * *	0 1 1 0 0
ASCI channel 0		* * *	0 1 1 1 0
ASCI channel 1	Lowest	* * *	1 0 0 0 0

* Programmable

Table 2. Vector Table

RETI Instruction Sequence:

When the EDH/4DH sequence is fetched by the Z80180, it is recognized as the RETI instruction sequence. The Z80180 will then refetch the RETI instruction with 4 T-states in the EDH cycle to allow the Z80 peripherals time to decode that cycle (See Figure 21). This allows the internal interrupt structure of the peripheral to properly decode the instruction and behave accordingly.

The M1E bit of the Operation Mode Control Register (OMCR) should be set to 0 so that $\overline{M1}$ signal is active only during the refetch of the RETI instruction sequence. This is the desired operation when Z80 peripherals are connected to the Z80180.

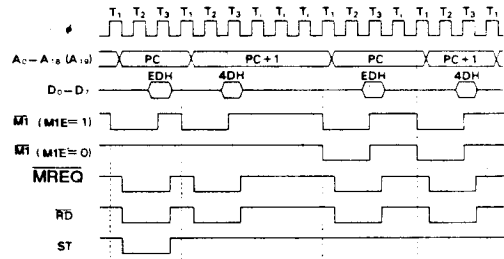


Figure 21. RETI Instruction Sequence

The RETI instruction takes 22 T-states and 10 machine cycles.

Interrupt Control Registers and Flags. The Z80180 has three registers and two flags which are associated with interrupt processing.

Function	Name	Access Method
(1) Interrupt Vector High	I	LD A, I and LD I, A instructions
(2) Interrupt Vector Low	IL	I/O instruction (addr=33H)
(3) Interrupt/Trap Control	ITC	I/O instruction (addr=34H)
(4) Interrupt Enable Flag	IEF ₁ , IEF ₂	EI and DI

Interrupt Enable/Disable Operation

Two flags, IEF₁ and IEF₂, are used to signal the Z80180 CPU interrupt status. IEF₁ controls the overall enabling and disabling of all internal and external maskable interrupts (i.e. all interrupts except NMI and TRAP).

If IEF₁ = 0, all maskable interrupts are disabled. IEF₁ can be reset to 0 by the DI (Disable Interrupts) instruction and set to 1 by the EI (Enable Interrupts) instruction.

The purpose of IEF₂ is to correctly manage the occurrence of NMI. During NMI, the prior interrupt reception state is saved and all maskable interrupts are automatically disabled (IEF₁ copied to IEF₂ and then IEF₁ cleared to 0). At the end of the NMI interrupt service routine, execution of the RETN (Return from Non-maskable Interrupt) will automatically restore the interrupt receiving state (by copying IEF₂ to IEF₁) prior to the occurrence of NMI.

IEF₂ state can be reflected in the P/V bit of the CPU Status Register by executing LD A, I or LD A, R instructions.

CPU Operation	IEF ₁	IEF ₂	REMARKS
RESET	0	0	Inhibits the interrupt except NMI and TRAP
NMI	0	IEF ₁	Copies the contents of IEF ₁ to IEF ₂
RETN	IEF ₂	not affected	Returns from the NMI service routine
Interrupt except NMI and TRAP	0	0	Inhibits the interrupt except NMI and TRAP
RETI	not affected	not affected	
TRAP	not affected	not affected	
EI	1	1	
DI	0	0	
LD A, I	not affected	not affected	Transfers the contents of IEF ₂ to P/V flag
LD A, R	not affected	not affected	Transfers the contents of IEF ₂ to P/V flag

Table 3. State of IEF₁ and IEF₂

Internal I/O Registers

The Z80180 internal I/O Registers occupy 64 I/O addresses (including reserved addresses). These registers access the internal I/O modules (ASCI, CSI/O, PRT) and control functions (DMAC, DRAM refresh, interrupts, wait state generator, MMU and I/O relocation).

To avoid address conflicts with external I/O, the Z80180 internal I/O addresses can be relocated on 64 byte boundaries within the bottom 256 bytes of the 64K byte I/O address space.

Internal I/O Registers

By programming IOA7 and IOA6 in the I/O control register, internal I/O register addresses are relocatable within ranges from 0000H to 00FFH in the I/O address space.

REGISTER	MNEMONICS	ADDRESS	REMARKS																								
ASCII Control Register A Channel 0 : CNTLA0	0 0	bit	<table><tr><td>MPE</td><td>RE</td><td>TE</td><td>RTS0</td><td>MPBR/EFB</td><td>MOD2</td><td>MOD1</td><td>MOD0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>invalid</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table>	MPE	RE	TE	RTS0	MPBR/EFB	MOD2	MOD1	MOD0	0	0	0	1	invalid	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		MPE	RE	TE	RTS0	MPBR/EFB	MOD2	MOD1	MOD0																		
0	0	0	1	invalid	0	0	0																				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W																				
			<div><div>during RESET</div><div><div>MODE Selection</div><div>Multi Processor Bit Receive/ Error Flag Reset</div><div>Request To Send</div><div>Transmit Enable</div><div>Receive Enable</div><div>Multi Processor Enable</div></div></div>																								
ASCII Control Register A Channel 1 : CNTLA1	0 1	bit	<table><tr><td>MPE</td><td>RE</td><td>TE</td><td>CKA1D</td><td>MPBR/EFB</td><td>MOD2</td><td>MOD1</td><td>MOD0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>invalid</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table>	MPE	RE	TE	CKA1D	MPBR/EFB	MOD2	MOD1	MOD0	0	0	0	1	invalid	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		MPE	RE	TE	CKA1D	MPBR/EFB	MOD2	MOD1	MOD0																		
0	0	0	1	invalid	0	0	0																				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W																				
			<div><div>during RESET</div><div><div>MODE Selection</div><div>Multi Processor Bit Receive/ Error Flag Reset</div><div>CKA1 Disable</div><div>Transmit Enable</div><div>Receive Enable</div><div>Multi Processor Enable</div></div></div>																								
		MOD2, 1, 0																									
		0 0 0	Start + 7 bit Data + 1 Stop																								
		0 0 1	Start + 7 bit Data + 2 Stop																								
		0 1 0	Start + 7 bit Data + Parity + 1 Stop																								
		0 1 1	Start + 7 bit Data + Parity + 2 Stop																								
		1 0 0	Start + 8 bit Data + 1 Stop																								
		1 0 1	Start + 8 bit Data + 2 Stop																								
		1 1 0	Start + 8 bit Data + Parity + 1 Stop																								
		1 1 1	Start + 8 bit Data + Parity + 2 Stop																								
ASCII Control Register B Channel 0 : CNTLB0	0 2	bit	<table><tr><td>MPBT</td><td>MP</td><td>CTS/PS</td><td>PEO</td><td>DR</td><td>SS2</td><td>SS1</td><td>SS0</td></tr><tr><td>invalid</td><td>0</td><td>*</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table>	MPBT	MP	CTS/PS	PEO	DR	SS2	SS1	SS0	invalid	0	*	0	0	1	1	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		MPBT	MP	CTS/PS	PEO	DR	SS2	SS1	SS0																		
invalid	0	*	0	0	1	1	1																				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W																				
			<div><div>during RESET</div><div><div>Clock Source and Speed Select</div><div>Divide Ratio</div><div>Parity Even or Odd</div><div>Clear To Send/Prescale</div><div>Multi Processor</div><div>Multi Processor Bit Transmit</div></div></div>																								
			<div><div>* CTS : Depending on the condition of CTS Pin.</div><div>PS : Cleared to 0.</div></div>																								

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS							
ASCI Control Register B Channel 1 : CNTLB1		0 3	bit							
			during RESET							
			R/W							
			MPBT	MP	CTS/PS	PEO	DR	SS2	SS1	SS0
			invalid	0	0	0	0	1	1	1
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			Clock Source and Speed Select							
			Divide Ratio							
			Parity Even or Odd							
			Clear To Send/Prescale							
Multi Processor										
Multi Processor Bit Transmit										
General divide ratio		PS = 0 (divide ratio = 10)		PS = 1 (divide ratio = 30)						
SS2, 1, 0		DR = 0 (× 16)		DR = 1 (× 64)		DR = 0 (× 16)		DR = 1 (× 64)		
0 0 0		φ + 160		φ + 640		φ + 480		φ + 1920		
0 0 1		+ 320		+ 1280		+ 960		+ 3840		
0 1 0		+ 640		+ 2560		+ 1920		+ 7680		
0 1 1		+ 1280		+ 5120		+ 3840		+ 15360		
1 0 0		+ 2560		+ 10240		+ 7680		+ 30720		
1 0 1		+ 5120		+ 20480		+ 15360		+ 61440		
1 1 0		+ 10240		+ 40960		+ 30720		+ 122880		
1 1 1		External clock (frequency < φ + 40)								
ASCI Status Register Channel 0 : STAT0		0 4	bit							
			during RESET							
			R/W							
			RDRF	OVRN	PE	FE	RIE	DCD0	TDRE	TIE
			0	0	0	0	0	*	**	0
			R	R	R	R	R/W	R	R	R/W
			Transmit Interrupt Enable							
			Transmit Data Register Empty							
			Data Carrier Detect							
			Receive Interrupt Enable							
Framing Error										
Parity Error										
Over Run Error										
Receive Data Register Full										
* DCD0 : Depending on the condition of DCD0 Pin.										
** CTS0 Pin										
L 1										
H 0										
ASCI Status Register Channel 1 : STAT1		0 5	bit							
			during RESET							
			R/W							
			RDRF	OVRN	PE	FE	RIE	CTS1E	TDRE	TIE
			0	0	0	0	0	0	1	0
			R	R	R	R	R/W	R/W	R	R/W
			Transmit Interrupt Enable							
			Transmit Data Register Empty							
			CTS1 Enable							
			Receive Interrupt Enable							
Framing Error										
Parity Error										
Over Run Error										
Receive Data Register Full										

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS																																		
ASCII Transmit Data Register Channel 0	: TDR0	0 6																																			
ASCII Transmit Data Register Channel 1	: TDR1	0 7																																			
ASCII Receive Data Register Channel 0	: TSRO	0 8																																			
ASCII Receive Data Register Channel 1	: TSR1	0 9																																			
CS/O Control Register	: CNTR	0 A	<div>bit during RESET</div> <table><tr><td>EF</td><td>EIE</td><td>RE</td><td>TE</td><td>—</td><td>SS2</td><td>SS1</td><td>SS0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td><td></td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table> <div>End Flag End Interrupt Enable Receive Enable Transmit Enable Speed Select</div>	EF	EIE	RE	TE	—	SS2	SS1	SS0	0	0	0	0	1	1	1	1	R	R/W	R/W	R/W		R/W	R/W	R/W										
EF	EIE	RE	TE	—	SS2	SS1	SS0																														
0	0	0	0	1	1	1	1																														
R	R/W	R/W	R/W		R/W	R/W	R/W																														
			<table><tr><th>SS2,1,0</th><th>Baud Rate</th><th>SS2,1,0</th><th>Baud Rate</th></tr><tr><td>000</td><td>$\phi + 20$</td><td>100</td><td>$\phi + 320$</td></tr><tr><td>001</td><td>+ 40</td><td>101</td><td>+ 640</td></tr><tr><td>010</td><td>+ 80</td><td>110</td><td>+ 1280</td></tr><tr><td>011</td><td>+ 160</td><td>111</td><td>External (frequency < + 20)</td></tr></table>	SS2,1,0	Baud Rate	SS2,1,0	Baud Rate	000	$\phi + 20$	100	$\phi + 320$	001	+ 40	101	+ 640	010	+ 80	110	+ 1280	011	+ 160	111	External (frequency < + 20)														
SS2,1,0	Baud Rate	SS2,1,0	Baud Rate																																		
000	$\phi + 20$	100	$\phi + 320$																																		
001	+ 40	101	+ 640																																		
010	+ 80	110	+ 1280																																		
011	+ 160	111	External (frequency < + 20)																																		
CS/O Transmit/Receive Data Register	: TRDR	0 B																																			
Timer Data Register Channel OL	: TMDROL	0 C																																			
Timer Data Register Channel OH	: TMDROH	0 D																																			
Timer Reload Register Channel OL	: RLDROL	0 E																																			
Timer Reload Register Channel OH	: RLDROH	0 F																																			
Timer Control Register	: TCR	1 0	<div>bit during RESET</div> <table><tr><td>TIF1</td><td>TIF0</td><td>TIE1</td><td>TIE0</td><td>TOC1</td><td>TOC0</td><td>TDE1</td><td>TDE0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R</td><td>R</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table> <div>Timer Interrupt Flag 1,0 Timer Interrupt Enable 1,0 Timer Output Control 1,0 Timer Down Count Enable 1,0</div> <table><tr><th>TOC1,0</th><th>A₁₅/TOUT</th></tr><tr><td>00</td><td>Inhibited</td></tr><tr><td>01</td><td>Toggle</td></tr><tr><td>10</td><td>0</td></tr><tr><td>11</td><td>1</td></tr></table>	TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0	0	0	0	0	0	0	0	0	R	R	R/W	R/W	R/W	R/W	R/W	R/W	TOC1,0	A ₁₅ /TOUT	00	Inhibited	01	Toggle	10	0	11	1
TIF1	TIF0	TIE1	TIE0	TOC1	TOC0	TDE1	TDE0																														
0	0	0	0	0	0	0	0																														
R	R	R/W	R/W	R/W	R/W	R/W	R/W																														
TOC1,0	A ₁₅ /TOUT																																				
00	Inhibited																																				
01	Toggle																																				
10	0																																				
11	1																																				

(to be continued)

REGISTER	MINEMONICS	ADDRESS	REMARKS																									
Timer Data Register Channel 1L : TMDR1L		1 4																										
Timer Data Register Channel 1H : TMDR1H		1 5																										
Timer Reload Register Channel 1L : RLDR1L		1 6																										
Timer Reload Register Channel 1H : RLDR1H		1 7																										
Free Running Counter : FRC		1 8	read only																									
DMA Source Address Register Channel 0L : SAROL		2 0																										
DMA Source Address Register Channel 0H : SAROH		2 1																										
DMA Source Address Register Channel 0B : SAROB		2 2	Bits 0-2 (3) are used for SAROB. <table><tr><th>A₁₉*</th><th>A₁₈</th><th>A₁₇</th><th>A₁₆</th><th>DMA Transfer Request</th></tr><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>DREQ₀ (external)</td></tr><tr><td>X</td><td>X</td><td>0</td><td>1</td><td>RDRO (ASCIO)</td></tr><tr><td>X</td><td>X</td><td>1</td><td>0</td><td>RDR1 (ASC11)</td></tr><tr><td>X</td><td>X</td><td>1</td><td>1</td><td>Not Used</td></tr></table>	A ₁₉ *	A ₁₈	A ₁₇	A ₁₆	DMA Transfer Request	X	X	0	0	DREQ ₀ (external)	X	X	0	1	RDRO (ASCIO)	X	X	1	0	RDR1 (ASC11)	X	X	1	1	Not Used
A ₁₉ *	A ₁₈	A ₁₇	A ₁₆	DMA Transfer Request																								
X	X	0	0	DREQ ₀ (external)																								
X	X	0	1	RDRO (ASCIO)																								
X	X	1	0	RDR1 (ASC11)																								
X	X	1	1	Not Used																								
DMA Destination Address Register Channel 0L : DAROL		2 3																										
DMA Destination Address Register Channel 0H : DAROH		2 4																										
DMA Destination Address Register Channel 0B : DAROB		2 5	Bits 0-2 (3) are used for DAROB. <table><tr><th>A₁₉*</th><th>A₁₈</th><th>A₁₇</th><th>A₁₆</th><th>DMA Transfer Request</th></tr><tr><td>X</td><td>X</td><td>0</td><td>0</td><td>DREQ₀ (external)</td></tr><tr><td>X</td><td>X</td><td>0</td><td>1</td><td>TDRO (ASCIO)</td></tr><tr><td>X</td><td>X</td><td>1</td><td>0</td><td>TDR1 (ASC11)</td></tr><tr><td>X</td><td>X</td><td>1</td><td>1</td><td>Not Used</td></tr></table>	A ₁₉ *	A ₁₈	A ₁₇	A ₁₆	DMA Transfer Request	X	X	0	0	DREQ ₀ (external)	X	X	0	1	TDRO (ASCIO)	X	X	1	0	TDR1 (ASC11)	X	X	1	1	Not Used
A ₁₉ *	A ₁₈	A ₁₇	A ₁₆	DMA Transfer Request																								
X	X	0	0	DREQ ₀ (external)																								
X	X	0	1	TDRO (ASCIO)																								
X	X	1	0	TDR1 (ASC11)																								
X	X	1	1	Not Used																								
DMA Byte Count Register Channel 0L : BCROL		2 6																										
DMA Byte Count Register Channel 0H : BCROH		2 7																										
DMA Memory Address Register Channel 1L : MAR1L		2 8																										
DMA Memory Address Register Channel 1H : MAR1H		2 9																										
DMA Memory Address Register Channel 1B : MAR1B		2 A	Bits 0-2 (3) are used for MAR1B.																									
DMA I/O Address Register Channel 1L : IAR1L		2 B																										
DMA I/O Address Register Channel 1H : IAR1H		2 C																										

to be continued

* In the R1 and Z Mask, these DMAC registers are expanded from 4 bits to 3 bits in the package version of CP-68 and FP-80.

REGISTER	MNEMONICS	ADDRESS	REMARKS																																																												
DMA Byte Count Register Channel 1L	: BCR1L	2 E	<div>bit during RESET</div> <table><tr><td>DE1</td><td>DE0</td><td>DWE1</td><td>DWE0</td><td>DE1</td><td>DIE0</td><td>—</td><td>DME</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td>W</td><td>W</td><td>R/W</td><td>R/W</td><td></td><td>R</td></tr></table> <div>DMA Master Enable</div> <div>DMA Enable Bit Write Enable 1,0</div> <div>DMA Enable ch 1,0</div>	DE1	DE0	DWE1	DWE0	DE1	DIE0	—	DME	0	0	1	1	0	0	1	0	R/W	R/W	W	W	R/W	R/W		R																																				
DE1	DE0	DWE1		DWE0	DE1	DIE0	—	DME																																																							
0	0	1		1	0	0	1	0																																																							
R/W	R/W	W	W	R/W	R/W		R																																																								
DMA Byte Count Register Channel 1H	: BCR1H	2 F																																																													
DMA Status Register	: DSTAT	3 0																																																													
DMA Mode Register	: DMODE	3 1	<div>bit during RESET</div> <table><tr><td>—</td><td>—</td><td>DM1</td><td>DM0</td><td>SM1</td><td>SM0</td><td>MMOD</td><td>—</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td></td><td></td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td></td></tr></table> <div>Memory MODE Select</div> <div>Ch 0 Source Mode 1,0</div> <div>Ch 0 Destination Mode 1,0</div> <div><table><tr><th>DM1, 0</th><th>Destination</th><th>Address</th><th>SM1, 0</th><th>Source</th><th>Address</th></tr><tr><td>0 0</td><td>M</td><td>DAR0+1</td><td>0 0</td><td>M</td><td>SAR0+1</td></tr><tr><td>0 1</td><td>M</td><td>DAR0-1</td><td>0 1</td><td>M</td><td>SAR0-1</td></tr><tr><td>1 0</td><td>M</td><td>DAR0 fixed</td><td>1 0</td><td>M</td><td>SAR0 fixed</td></tr><tr><td>1 1</td><td>I/O</td><td>DAR0 fixed</td><td>1 1</td><td>I/O</td><td>SAR0 fixed</td></tr></table><table><tr><th>MMOD</th><th>Mode</th></tr><tr><td>0</td><td>Cycle Steal Mode</td></tr><tr><td>1</td><td>Burst Mode</td></tr></table></div>	—	—	DM1	DM0	SM1	SM0	MMOD	—	1	1	0	0	0	0	0	1			R/W	R/W	R/W	R/W	R/W		DM1, 0	Destination	Address	SM1, 0	Source	Address	0 0	M	DAR0+1	0 0	M	SAR0+1	0 1	M	DAR0-1	0 1	M	SAR0-1	1 0	M	DAR0 fixed	1 0	M	SAR0 fixed	1 1	I/O	DAR0 fixed	1 1	I/O	SAR0 fixed	MMOD	Mode	0	Cycle Steal Mode	1	Burst Mode
—	—	DM1	DM0	SM1	SM0	MMOD	—																																																								
1	1	0	0	0	0	0	1																																																								
		R/W	R/W	R/W	R/W	R/W																																																									
DM1, 0	Destination	Address	SM1, 0	Source	Address																																																										
0 0	M	DAR0+1	0 0	M	SAR0+1																																																										
0 1	M	DAR0-1	0 1	M	SAR0-1																																																										
1 0	M	DAR0 fixed	1 0	M	SAR0 fixed																																																										
1 1	I/O	DAR0 fixed	1 1	I/O	SAR0 fixed																																																										
MMOD	Mode																																																														
0	Cycle Steal Mode																																																														
1	Burst Mode																																																														

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS																																																																	
DMA/WAIT Control Register	: DCNTL	3 2	<div><div>bit during RESET R/W</div><table><tr><td>MW11</td><td>MW10</td><td>W11</td><td>W10</td><td>DMS1</td><td>DMS0</td><td>DIM1</td><td>DIM0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table><div><div>DMA Ch 1 I/O Memory Mode Select DREQi Select, i = 1,0</div><div>I/O Wait Insertion Memory Wait Insertion</div></div><table><tr><th>MW11,0</th><th>The number of wait states</th><th>W11,0</th><th>The number of wait states</th></tr><tr><td>00</td><td>0</td><td>00</td><td>0</td></tr><tr><td>01</td><td>1</td><td>01</td><td>2</td></tr><tr><td>10</td><td>2</td><td>10</td><td>3</td></tr><tr><td>11</td><td>3</td><td>11</td><td>4</td></tr></table><table><tr><th>DMSi</th><th>Sense</th></tr><tr><td>1</td><td>Edge sense</td></tr><tr><td>0</td><td>Level sense</td></tr></table><table><tr><th>DIM1,0</th><th>Transfer Mode</th><th>Address Increment/Decrement</th></tr><tr><td>00</td><td>M→I/O</td><td>MAR1+1 IAR1 fixed</td></tr><tr><td>01</td><td>M→I/O</td><td>MAR1-1 IAR1 fixed</td></tr><tr><td>10</td><td>I/O→M</td><td>IAR1 fixed MAR1+1</td></tr><tr><td>11</td><td>I/O→M</td><td>IAR1 fixed MAR1-1</td></tr></table></div>	MW11	MW10	W11	W10	DMS1	DMS0	DIM1	DIM0	1	1	1	1	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	MW11,0	The number of wait states	W11,0	The number of wait states	00	0	00	0	01	1	01	2	10	2	10	3	11	3	11	4	DMSi	Sense	1	Edge sense	0	Level sense	DIM1,0	Transfer Mode	Address Increment/Decrement	00	M→I/O	MAR1+1 IAR1 fixed	01	M→I/O	MAR1-1 IAR1 fixed	10	I/O→M	IAR1 fixed MAR1+1	11	I/O→M	IAR1 fixed MAR1-1
MW11	MW10	W11	W10	DMS1	DMS0	DIM1	DIM0																																																													
1	1	1	1	0	0	0	0																																																													
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W																																																													
MW11,0	The number of wait states	W11,0	The number of wait states																																																																	
00	0	00	0																																																																	
01	1	01	2																																																																	
10	2	10	3																																																																	
11	3	11	4																																																																	
DMSi	Sense																																																																			
1	Edge sense																																																																			
0	Level sense																																																																			
DIM1,0	Transfer Mode	Address Increment/Decrement																																																																		
00	M→I/O	MAR1+1 IAR1 fixed																																																																		
01	M→I/O	MAR1-1 IAR1 fixed																																																																		
10	I/O→M	IAR1 fixed MAR1+1																																																																		
11	I/O→M	IAR1 fixed MAR1-1																																																																		
Interrupt Vector Low Register	: IL	3 3	<div><div>bit during RESET R/W</div><table><tr><td>IL7</td><td>IL6</td><td>IL5</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr></table><div>Interrupt Vector Low</div></div>	IL7	IL6	IL5	—	—	—	—	—	0	0	0	0	0	0	0	0	R/W	R/W	R/W																																														
IL7	IL6	IL5	—	—	—	—	—																																																													
0	0	0	0	0	0	0	0																																																													
R/W	R/W	R/W																																																																		
INT/TRAP Control Register	: ITC	3 4	<div><div>bit during RESET R/W</div><table><tr><td>TRAP</td><td>UFO</td><td>—</td><td>—</td><td>—</td><td>ITE2</td><td>ITE1</td><td>ITE0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>R/W</td><td>R</td><td></td><td></td><td></td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table><div><div>TRAP</div><div>Undefined Fetch Object</div><div>INT Enable 2,1,0</div></div></div>	TRAP	UFO	—	—	—	ITE2	ITE1	ITE0	0	0	1	1	1	0	0	1	R/W	R				R/W	R/W	R/W																																									
TRAP	UFO	—	—	—	ITE2	ITE1	ITE0																																																													
0	0	1	1	1	0	0	1																																																													
R/W	R				R/W	R/W	R/W																																																													
Refresh Control Register	: RCR	3 6	<div><div>bit during RESET R/W</div><table><tr><td>REFE</td><td>REFW</td><td>—</td><td>—</td><td>—</td><td>—</td><td>CYC1</td><td>CYC0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td></td><td></td><td></td><td></td><td>R/W</td><td>R/W</td></tr></table><div><div>Refresh Wait State</div><div>Refresh Enable</div><div>Cycle Select</div></div><table><tr><th>CYC1,0</th><th>Interval of Refresh Cycle</th></tr><tr><td>00</td><td>10 States</td></tr><tr><td>01</td><td>20</td></tr><tr><td>10</td><td>40</td></tr><tr><td>11</td><td>80</td></tr></table></div>	REFE	REFW	—	—	—	—	CYC1	CYC0	1	1	1	1	1	1	0	0	R/W	R/W					R/W	R/W	CYC1,0	Interval of Refresh Cycle	00	10 States	01	20	10	40	11	80																															
REFE	REFW	—	—	—	—	CYC1	CYC0																																																													
1	1	1	1	1	1	0	0																																																													
R/W	R/W					R/W	R/W																																																													
CYC1,0	Interval of Refresh Cycle																																																																			
00	10 States																																																																			
01	20																																																																			
10	40																																																																			
11	80																																																																			

(to be continued)

REGISTER	MNEMONICS	ADDRESS	REMARKS																								
MMU Common Base Register : CBR	3 8	bit during RESET R/W	<table><tr><td>CB7*</td><td>CB6</td><td>CB5</td><td>CB4</td><td>CB3</td><td>CB2</td><td>CB1</td><td>CB0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table> <p>MMU Common Base Register</p>	CB7*	CB6	CB5	CB4	CB3	CB2	CB1	CB0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CB7*	CB6	CB5	CB4	CB3	CB2	CB1	CB0																				
0	0	0	0	0	0	0	0																				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W																				
MMU Bank Base Register : BBR	3 9	bit during RESET R/W	<table><tr><td>BB7*</td><td>BB6</td><td>BB5</td><td>BB4</td><td>BB3</td><td>BB2</td><td>BB1</td><td>BB0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table> <p>MMU Bank Base Register</p>	BB7*	BB6	BB5	BB4	BB3	BB2	BB1	BB0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BB7*	BB6	BB5	BB4	BB3	BB2	BB1	BB0																				
0	0	0	0	0	0	0	0																				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W																				
MMU Common/Bank Area Register : CBAR	3 A	bit during RESET R/W	<table><tr><td>CA3</td><td>CA2</td><td>CA1</td><td>CA0</td><td>BA3</td><td>BA2</td><td>BA1</td><td>BA0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td><td>R/W</td></tr></table> <p>MMU Common Area Register</p> <p>MMU Bank Area Register</p>	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0	1	1	1	1	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0																				
1	1	1	1	0	0	0	0																				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W																				
Operation Mode Control Register : OMCR	3 E	bit during RESET R/W	<table><tr><td>M1E</td><td>MTTE</td><td>IOC</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>R/W</td><td>W</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr></table> <p>I/O Compatibility</p> <p>M1 Temporary Enable</p> <p>M1 Enable</p>	M1E	MTTE	IOC	—	—	—	—	—	1	1	1	1	1	1	1	1	R/W	W	R/W					
M1E	MTTE	IOC	—	—	—	—	—																				
1	1	1	1	1	1	1	1																				
R/W	W	R/W																									
I/O Control Register : ICR	3 F	bit during RESET R/W	<table><tr><td>IOA7</td><td>IOA6</td><td>IOSTP</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>R/W</td><td>R/W</td><td>R/W</td><td></td><td></td><td></td><td></td><td></td></tr></table> <p>I/O Address</p> <p>I/O Stop</p>	IOA7	IOA6	IOSTP	—	—	—	—	—	0	0	0	1	1	1	1	1	R/W	R/W	R/W					
IOA7	IOA6	IOSTP	—	—	—	—	—																				
0	0	0	1	1	1	1	1																				
R/W	R/W	R/W																									

These MMU registers are expanded from 7 bits to 8 bits in the PLCC package

Memory Management Unit (MMU)

The Z80180 has an on-chip MMU which performs the translation of the CPU 64K byte (16-bit addresses 0000H to FFFFH) logical memory address space into a 1024K byte (20-bit addresses 00000H to FFFFFH) physical memory address space. Address translation occurs internally in parallel with other CPU operation.

Logical Address Spaces. The 64K byte CPU logical address space is interpreted by the MMU as consisting of up to three separate logical address areas, Common Area 0, Bank Area, and Common Area 1.

As shown in Fig. 22, a variety of logical memory configurations are possible. The boundaries between the Common and Bank Areas can be programmed with 4K byte resolution.

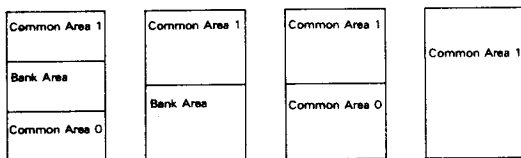


Figure 22. Logical Address Mapping Examples

Whether address translation takes place depends on the type of CPU cycle as follows.

(1) Memory Cycles

Address Translation occurs for all memory access cycles including instruction and operand fetches, memory data reads and writes, hardware interrupt vector fetch, and software interrupt restarts.

(2) I/O Cycles

The MMU is logically bypassed for I/O cycles. The 16-bit logical I/O address space corresponds directly with the 16-bit physical I/O address space. The four high-order bits (A16-A19) of the physical address are always 0 during I/O cycles.

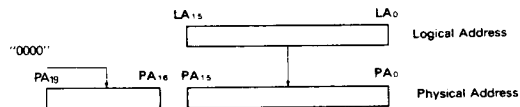


Figure 23. I/O Address Translation

(3) DMA Cycles

When the Z80180 on-chip DMAC is using the external bus, the MMU is physically bypassed. The 20-bit source and destination registers in the DMAC are directly output on the physical address bus (A0-A19).

Physical address translation. Fig. 24 shows the way in which physical addresses are generated based on the contents of CBAR, CBR and BBR. MMU comparators classify an access by logical area as defined by CBAR. Depending on which of the three potential logical areas (Common Area 1, Bank Area, or Common Area 0) is being accessed, the appropriate 8-bit base address is added to the high-order 4 bits of the logical address, yielding a 20-bit physical address. CBR is associated with Common Area 1 accesses. Common Area 0, if defined, is always based at physical address 00000H.

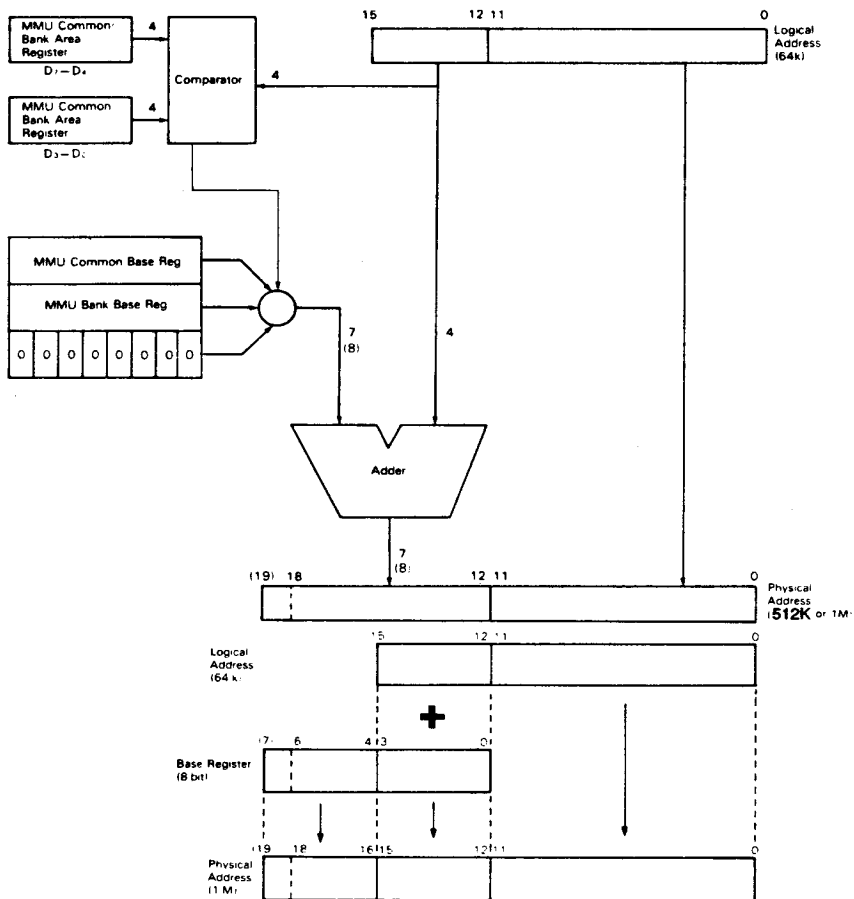


Figure 24. Physical Address Generation

Dynamic RAM Refresh Control

The Z80180 incorporates a dynamic RAM refresh control circuit including 8-bit refresh address generation and programmable refresh timing. This circuit generates asynchronous refresh cycles inserted at the programmable interval independent of CPU program execution. For systems which do not use dynamic RAM, the refresh function can be disabled.

When the internal refresh controller determines that a refresh cycle should occur, the current instruction is interrupted at the first breakpoint between machine cycles. The refresh cycle is inserted by placing the refresh address on A₀-A₇ and the $\overline{\text{RFSH}}$ output is driven LOW.

Refresh cycles may be programmed to be either 2 or 3 clock cycles in duration by programming the REFW (Refresh Wait) bit in the Refresh Control Register (RCR). Note that the external WAIT input and the internal wait state generator are not effective during refresh.

Fig. 25 shows the timing of a refresh cycle with a refresh wait (TRW) cycle.

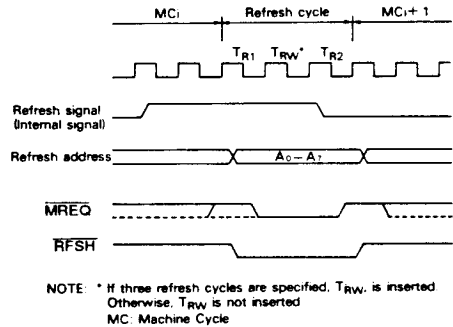


Figure 25. Refresh Cycle Timing

DMA Controller (DMAC)

The Z80180 contains a two-channel DMA (Direct Memory Access) controller which supports high speed data transfer. Both channels (channel 0 and channel 1) have the following capabilities.

Memory Address Space. Memory source and destination addresses can be directly specified anywhere within the 1024K byte physical address space using 20-bit source and destination memory addresses. In addition, memory transfers can arbitrarily cross 64K byte physical address boundaries without CPU intervention.

I/O Address Space. I/O source and destination addresses can be directly specified anywhere within the 64K byte I/O address space (16-bit source and destination I/O addresses).

Transfer Length. Up to 64K bytes are transferred based on a 16-bit byte count register.

$\overline{\text{DREQ}}$ Input. Level and edge sense DREQ input detection are selectable.

$\overline{\text{TEND}}$ Output. Used to indicate DMA completion to external devices.

Transfer Rate. Each byte transfer can occur every 6 clock cycles. Wait states can be inserted in DMA cycles for slow memory or I/O devices. At the system clock (ϕ) = 6 MHz, the DMA transfer rate is as high as 1.0 megabytes/second (no wait states).

There is an additional feature disc for DMA interrupt request by DMA END. Each channel has the following additional specific capabilities.

Channel 0

Memory \leftrightarrow memory, memory \leftrightarrow I/O, memory \leftrightarrow memory mapped I/O transfers.

- Memory address increment, decrement, no-change.
- Burst or cycle steal memory to/from memory transfers.
- DMA to/from both ASCI channels.
- Higher priority than DMAC channel 1.

Channel 1

Memory \leftrightarrow I/O transfer.

Memory address increment, decrement

DMAC Registers

Each channel of the DMAC (channel 0, 1) has three registers specifically associated with that channel.

Channel 0

SAR0 - Source Address Register
DAR0 - Destination Address Register
BCR0 - Byte Count Register

Channel 1

MAR1 - Memory Address Register
IAR1 - I/O Address Register
BCR1 - Byte Count Register

The two channels share the following three additional registers in common.

DSTAT - DMA Status Register
DMODE - DMA Mode Register
DCNTL - DMA Control Register

DMAC Block Diagram. Fig.26 shows the Z64180 DMAC Block Diagram.

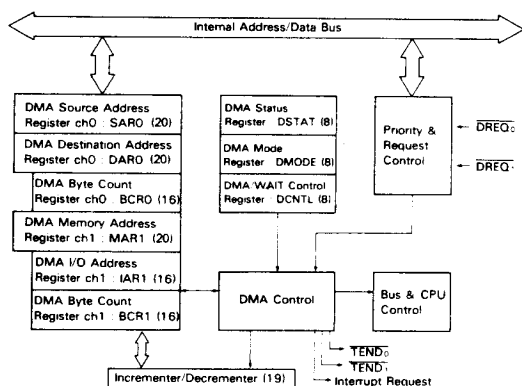


Figure 26. DMAC Block Diagram

Asynchronous Serial Communication Interface (ASCI)

The Z80180 on-chip ASCI has two independent full-duplex channels. Based on full programmability of the following functions, the ASCI directly communicates with a wide variety of standard UARTs (Universal Asynchronous Receiver/Transmitter) including the Z8440 SIO and the Z8530 SCC.

The key functions for ASCI are shown below. Each channel is independently programmable.

- Full-duplex communication.
- 7- or 8-bit data length.
- Program controlled 9th data bit for multiprocessor communication.
- 1 or 2 stop bits.
- Odd, even, no parity.
- Parity, overrun, framing error detection.
- Programmable baud rate generator, /16 and /64 modes.
- Speed to 38.4K bits per second (CPU fc = 6.144 MHz).
- Modem control signals - Channel 0 has DCD₀, CTS₀ and RTS₀ Channel 1 has CTS₁.
- Programmable interrupt condition enable and disable.
- Operation with on-chip DMAC.

ASCI Block Diagram. Fig. 27 shows the ASCI Block Diagram.

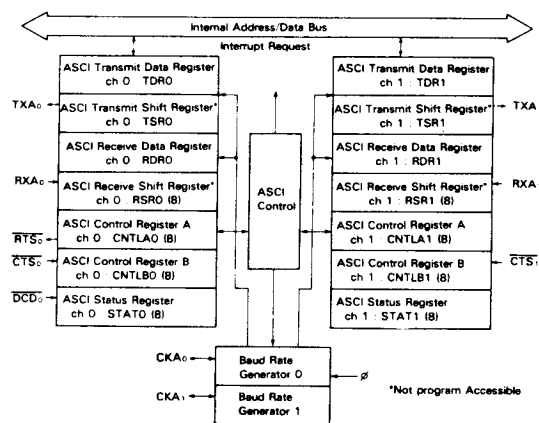


Figure 27. ASCI Block Diagram

Clocked Serial I/O Port (CSI/O)

The Z80180 includes a simple, high speed clock, synchronous serial I/O port. The CSI/O includes transmit/receive (half-duplex), fixed 8-bit data, and internal or external data clock selection. High speed operation (baud rate 200K bits/second at $f_C = 4$ MHz) is provided. The CSI/O is ideal for implementing a multiprocessor communication link between multiple Z80180s. These secondary devices may typically perform a portion of the system I/O processing, i.e. keyboard scan/decode, LDC interface, etc.

CSI/O Block Diagram. The CSI/O block diagram is shown in Fig. 28. The CSI/O consists of two registers - the Transmit/Receive Data Register (TRDR) and Control Register (CNTR).

CSI/O Transmit/Receive Data Register (TRDR: I/O Address = 0BH). TRDR is used for both CSI/O transmission and reception. Thus, the system design must insure that the constraints of half-duplex operation are met (Transmit and receive operation cannot occur simultaneously). For example, if a CSI/O transmission is attempted while the CSI/O is receiving data, a CSI/O will not work. Also note that TRDR is not buffered. Therefore, attempting to perform a CSI/O transmit while the previous transmit data is still being shifted out causes the shift data to be immediately updated, thereby corrupting the transmit operation in

progress. Similarly, reading TRDR while a transmit or receive is in progress should be avoided.

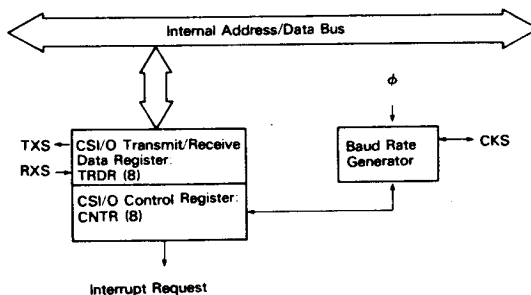


Figure 28. CSI/O Block Diagram

CSI/O Register Description

CSI/O Control/Status Register (CNTR: I/O Address = 0AH). CNTR is used to monitor CSI/O status, enable and disable the CSI/O, enable and disable interrupt generation, and select the data clock speed and source.

Programmable Reload Timer (PRT)

The Z80180 contains a two channel 16-bit Programmable Reload Timer. Each PRT channel contains a 16-bit down counter and a 16-bit reload register. The down counter is directly read and written and a down counter overflow interrupt can be programmably enabled or disabled. Also, PRT channel 1 has a TOUT output pin (pin 31 - multiplexed with A18) which can be set HIGH, LOW, or toggled. Thus, PRT1 can perform programmable output waveform generation.

PRT block diagram. The PRT block diagram is shown in Fig. 29. The two channels have separate timer data and reload registers and a common status/control register. The PRT input clock for both channels is equal to the system clock divided by 20.

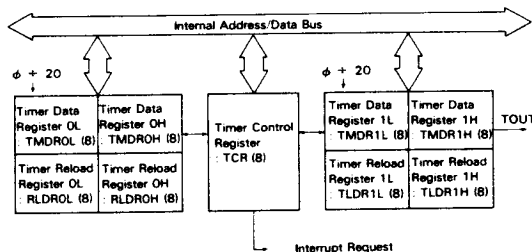


Figure 29. PRT Block Diagram

Secondary Bus Interface

E clock Output Timing. The Z80180 also has a secondary bus interface that allows it to easily interface with other peripheral families.

These devices require connection with the Z80180

synchronous E clock output. The speed (access time) required for the peripheral devices are determined by the Z80180 clock rate. Table 19, and Figures 80-82 define E clock output timing.

On-Chip Clock Generator

The Z80180 contains a crystal oscillator and system clock generator. A crystal can be directly connected or an external clock input can be provided. In either case, the system clock is equal to one-half the input clock. For example, a crystal or external clock input of 8 MHz corresponds with a system clock rate of 4 MHz.

The following table shows the AT cut crystal characteristics (Co, Rs) and the load capacitance (CL1, CL2) required for various frequencies of Z80180 operation.

Clock Frequency	4MHz	4MHz < f ≤ 12MHz	12MHz < f ≤ 16MHz
Item			
Co	< 7 pF	< 7 pF	< 7 pF
Rs	< 60 Ω	< 60 Ω	< 60 Ω
CL1, CL2	10 to 22 pF ± 10%	10 to 22 pF ± 10%	10 to 22 pF ± 10%

Table 4.

If an external clock input is used instead of a crystal, the waveform (twice the clock rate) should exhibit a $50\% \pm 10\%$ duty cycle. Note that the minimum clock input HIGH voltage level is $V_{CC}-0.6V$. The external clock input is connected to the EXTAL pin, while the XTAL pin is left open. Fig. 30 shows external clock interface.

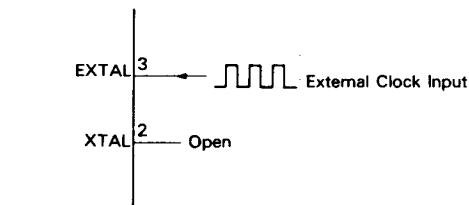


Figure 30. External Clock Interface

Miscellaneous

Free Running Counter (I/O Address = 18H)

Read only 8-bit free running counter without control registers and status registers. The contents of the 8-bit free running counter is counted down by one with an interval of 10 clock cycles. The free running counter continues counting down without being affected by the read operation.

If data is written into the free running counter, the interval of DRAM refresh cycle and baud rates for the ASCII and CSI/O are not guaranteed.

In IOSTOP mode, the free running counter continues counting down. It is initialized to FFH during RESET.

SOFTWARE ARCHITECTURE

Instruction Set. The Z80180 is object code compatible with the Z80 CPU, refer to the Z80 CPU Technical Manual or the Z80 Assembly Language Programming Manual for further details.

<u>New Instructions</u>	<u>Operation</u>
SLP	Enter SLEEP mode
MLT	8-bit multiply with 16-bit result
INO g, (m)	Input contents of immediate I/O address
OUT0 (m), g	Output register contents to immediate I/O address
OTIM	Block output - increment
OTIMR	Block output - increment and repeat
OTDM	Block output - decrement
OTDMR	Block output - decrement and repeat
TSTIO m	Non-destructive AND, I/O port, and accumulator
TST g	Non-destructive AND, register, and accumulator
TST m	Non-destructive AND, immediate data and accumulator.
TST (HL)	Non-destructive AND, memory data, and accumulator.

SLP - Sleep. The SLP instruction causes the Z80180 to enter the SLEEP low power consumption mode. See section 2.4 for a complete description of the SLEEP state.

MLT - Multiply. The MLT performs unsigned multiplication on two 8-bit numbers yielding a 16-bit result. MLT may specify BC, DE, HL or SP registers. In all cases, the 8-bit

operands are loaded into each half of the 16-bit register and the 16-bit result is returned in that register.

OTIM, OTIMR, OTDM, OTDMR - Block I/O. The contents of memory pointed to by HL is output to the I/O address in (C). The memory address (HL) and I/O address (C) are incremented in OTIM and OTIMR and decremented in OTDM and OTDMR, respectively. The B register is decremented. The OTIMR and OTDMR variants repeat the above sequence until register B is decremented to 0. Since the I/O address (C) is automatically incremented or decremented, these instructions are useful for block I/O (such as Z80180 on-chip I/O) initialization. When I/O is accessed, 00H is output in high-order bits of address automatically.

TSTIO m - Test I/O Port. The contents of the I/O port addressed by C are ANDed with immediately specified 8-bit data and the status flags are updated. The I/O port contents are not written (non-destructive AND). When I/O is accessed, 00H is output in higher bits of address automatically.

TST g - Test Register. The contents of the specified register are ANDed with the accumulator (A) and the status flags are updated. The accumulator and specified register are not changed (non-destructive AND).

TST m - Test Immediate. The contents of the immediately specified 8-bit data are ANDed with the accumulator (A) and the status flags are updated. The accumulator is not changed (non-destructive AND).

TST (HL) - Test Memory. The contents of memory pointed to by HL are ANDed with the accumulator (A) and the status flags are updated. The memory contents and accumulator are not changed (non-destructive AND).

INO g, (m) - Input, Immediate I/O address. The contents of immediately specified 8-bit I/O address are input into the specified register. When I/O is accessed, 00H is output in high-order bits of the address automatically.

OUT0 (m), g - Output, immediate I/O address. The contents of the specified register are output to the immediately specified 8-bit I/O address. When I/O is accessed, 00H is output in high-order bits of the address automatically.

CPU Registers

The Z80180 CPU registers consist of Register Set GR, Register Set GR' and Special Registers.

The Register Set GR consists of 8-bit Accumulator (A), 8-bit Flag Register (F), and three General Purpose Registers (BC, DE, and HL) which may be treated as 16-bit registers (BC, DE, and HL) or as individual 8-bit registers (B, C, D, E, H, and L) depending on the instruction to be executed. The Register Set GR' is alternate register set of Register Set GR and also contains Accumulator (A'), Flag Register (F') and three General Purpose Registers (BC', DE', and HL'). While the alternate Register Set GR' contents are not directly accessible, the contents can be programmably exchanged at high speed with those of Register Set GR.

The Special Registers consist of 8-bit Interrupt Vector Register (I), 8-bit R Counter (R), two 16-bit Index Registers (IX and IY), 16-bit Stack Pointer (SP), and 16-bit Program Counter (PC).

Fig. 31 shows CPU registers configuration.

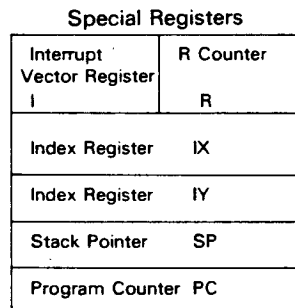
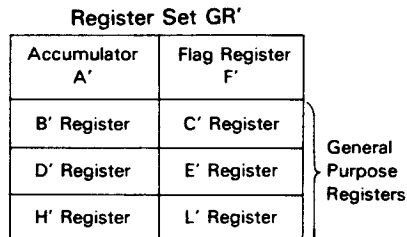
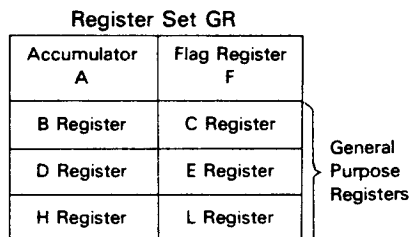


Figure 31. CPU Registers

Z80180 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	$-0.3 \sim +7.0$	V
Input Voltage	V_{in}	$-0.3 \sim V_{CC}+0.3$	V
Operating Temperature	Standard	Topr	0 - 70
	Extended	Topr	-40 - 85
Storage Temperature	T_{stg}	$-55 \sim +150$	°C

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

DC CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, over specified temperature range, unless otherwise noted.)

Symbol	Item	Condition	min	typ	max	Unit
V_{IH1}	Input "H" Voltage RESET, EXTAL, NMI		$V_{CC}-0.6$	-	$V_{CC}+0.3$	V
V_{IH2}	Input "H" Voltage Except RESET, EXTAL, NMI		2.0	-	$V_{CC}+0.3$	V
V_{IL1}	Input "L" Voltage RESET, EXTAL, NMI		-0.3	-	0.6	V
V_{IL2}	Input "L" Voltage Except RESET, EXTAL, NMI		-0.3	-	0.8	V
V_{OH}	Output "H" Voltage All outputs	$I_{OH} = -200\mu A$	2.4	-	-	V
		$I_{OH} = -20\mu A$	$V_{CC}-1.2$	-	-	
V_{OL}	Output "L" Voltage All Outputs	$I_{OL} = 2.2\text{ mA}$	-	-	0.45	V
I_L	Input Leakage Current All Inputs Except XTAL, EXTAL	$V_{in} = 0.5 \sim V_{CC}-0.5$	-	-	1.0	μA
I_{TL}	Three State Leakage Current	$V_{in} = 0.5 \sim V_{CC}-0.5$	-	-	1.0	μA
I_{CC}^*	Power Dissipation* (Normal Operation)	$f = 6\text{ MHz}$	-	15	40	mA
		$f = 8\text{ MHz}$	-	20	50	
		$f = 10\text{ MHz}$	-	25	60	
		$f = 12\text{ MHz}$	-	30	70	
	Power Dissipation* (SYSTEM STOP mode)	$f = 6\text{ MHz}$	-	3.8	12.5	
		$f = 8\text{ MHz}$	-	5	15.0	
		$f = 10\text{ MHz}$	-	6.3	17.5	
		$f = 12\text{ MHz}$	-	TBD	20	
C_p	Pin Capacitance	$V_{in} = 0V, f = 1\text{ MHz}$ $T_a = 25^\circ C$	-	-	12	pF

* $V_{IHmin} = V_{CC}-1.0V$, $V_{ILmax} = 0.8V$ (all output terminals are at no load)
 $V_{CC}=5.00V$

Z80180 AC CHARACTERISTICS

($V_{cc}=5V \pm 10\%$, $V_{ss}=0V$, over specified temperature range, unless otherwise noted.)

No	Sym	Parameter	Z018006		Z8018008		Z8018010		Z8018012 [3,4]		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
1	t _{cy}	Clock Cycle time	162	2000	125	2000	100	2000	80	2000	ns	[1]
2	t _{CHW}	Clock Pulse width (high)	65		55		40		35		ns	[1]
3	t _{CLW}	Clock Pulse width (low)	65		55		40		35		ns	[1]
4	t _{cf}	Clock Fall time		15		15		10		5	ns	[1]
5	t _{cr}	Clock Rise time		15		15		10		5	ns	[1]
6	t _{AD}	Address valid from Clock Rise		90		80		70		50	ns	
7	t _{AS}	Address valid to /MREQ, /IORQ Fall	30		20		10		10		ns	
8	t _{MED1}	Clock Fall to /MREQ Fall delay		60		50		50		45	ns	
9	t _{RDD1}	Clock Fall to /RD Fall (/IOC=1)		60		50		50		45	ns	
		Clock Rise to /RD Fall (/IOC=0)		65		60		55		50	ns	
10	t _{M1D1}	Clock Rise to /M1 Fall delay		80		70		60		50	ns	
11	t _{AH}	Address Hold time (/MREQ, /IORQ, /RD, /WR)	35		20		10		10		ns	
12	t _{MED2}	Clock Fall to /MREQ Rise Delay		60		50		50		45	ns	
13	t _{RDD2}	Clock Fall to /RD Rise delay		60		50		50		45	ns	
14	t _{M1D2}	Clock Rise to /M1 Rise delay		80		70		60		50	ns	
15	t _{DRS}	Data Read Setup Time	40		30		25		20		ns	
16	t _{DRH}	Data Read Hold time	0		0		0		0		ns	
17	t _{STD1}	Clock Edge to ST Fall		90		70		60		50	ns	
18	t _{STD2}	Clock Edge to ST Rise		90		70		60		50	ns	
19	t _{WS}	/WAIT setup time to Clock Fall	40		40		30		20		ns	
20	t _{WH}	/WAIT Hold time from Clock Fall	40		40		30		20		ns	
21	t _{WDZ}	Clock Rise to Data Float Delay		95		70		60		60	ns	
22	t _{WRD1}	Clock Rise to /WR Fall delay		65		60		50		30	ns	
23	t _{WDD}	Clock Fall to Write Data Delay		90		80		60		50	ns	
24	t _{WDS}	Write Data Setup time to /WR	40		20		15		10		ns	
25	t _{WRD2}	Clock Fall to /WR Rise		80		60		50		45	ns	
26	t _{WRP}	/WR Pulse Width (Memory Write Cycles)	170		130		110		85		ns	
26a		/WR Pulse Width (I/O Write Cycles)	332		225		210		165		ns	
27	t _{WDH}	Write Data Hold time from /WR Rise	40		15		10		10		ns	
28	t _{IOD1}	Clock Fall to /IORQ Fall delay (/IOC=1)		60		50		50		45	ns	
		Clock Rise to /IORQ Fall delay (/IOC=0)		65		60		55		50	ns	
29	t _{IOD2}	Clock Fall /IOQR Rise Delay		60		50		50		50	ns	
30	t _{IOD3}	/M1 Fall to /IORQ Fall delay	340		250		200		160		ns	
31	t _{INTS}	/INT Setup Time to Clock Fall	40		40		30		20		ns	
32	t _{INTH}	/INT Hold Time from Clock Fall	40		40		30		20		ns	
33	t _{NMIW}	/NMI Pulse width	120		100		80		60		ns	
34	t _{BRS}	/BUSREQ Setup Time to Clock Fall	40		40		30		20		ns	
35	t _{BRH}	/BUSREQ Hold Time from Clock Fall	40		40		30		20		ns	
36	t _{BAD1}	Clock Rise to /BUSACK Fall delay		95		70		60		50	ns	
37	t _{BAD2}	Clock Fall to /BUSACK Rise delay		95		70		60		50	ns	
38	t _{BZD}	Clock Rise to Bus Floating Delay Time		125		90		80		60	ns	
39	t _{MEWH}	/MREQ Pulse Width (High)	110		90		70		60		ns	
40	t _{MEWL}	/MREQ Pulse Width (LOW)	125		100		80		60		ns	

Z80180 AC CHARACTERISTICS (Continued)

($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, over specified temperature range, unless otherwise noted.)

No	Sym	Parameter	Z018006		Z8018008		Z8018010		Z8018012 [3,4]		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
41	tRFD1	Clock Rise to /RFSH Fall Delay		90		80		60		40	ns	
42	tRFD2	Clock Rise to /RFSH Rise Delay		90		80		60		40	ns	
43	tHAD1	Clock Rise to /HALT Fall Delay		90		80		50		30	ns	
44	tHAD2	Clock Rise to /HALT Rise Delay		90		80		50		30	ns	
45	tDRQS	/DREQi Setup Time to Clock Rise	40		40		30		20		ns	
46	tDRQH	/DREQi Hold Time from Clock Rise	40		40		30		20		ns	
47	tTED1	Clock Fall to /TENDi Fall Delay		70		60		50		50	ns	
48	tTED2	Clock Fall to /TENDi Rise Delay		70		60		50		50	ns	
49	tED1	Clock Rise to E Rise Delay		95		70		60		40	ns	
50	tED2	Clock Edge to E Fall Delay		95		70		60		40	ns	
51	PWEH	E Pulse Width (High)	75		65		55		45		ns	
52	PWEL	E Pulse Width (Low)	180		130		110		90		ns	
53	tEr	Enable Rise Time		20		20		20		10	ns	
54	tEf	Enable Fall Time		20		20		20		10	ns	
55	tTOD	Clock Fall to Timer Output Delay		300		200		150		120	ns	
56	ISTDI	CSI/O Tx Data Delay Time (Internal Clock Operation)		200		200		150		120	ns	
57	ISTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5tcyc+300		7.5tcyc+200		7.5tcyc+150		7.5tcyc+120	ns	
58	ISRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)	1		1		1		1		tcyc	
59	ISRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)	1		1		1		1		tcyc	
60	ISRSE	CSI/O Rx Data Setup Time (External Clock Operation)	1		1		1		1		tcyc	
61	ISRHE	CSI/O Rx Data Hold Time (External Clock Operation)	1		1		1		1		tcyc	
62	IRES	/RESET Setup time to Clock Fall	120		100		80		60		ns	
63	IREH	/RESET Hold time from Clock Fall	80		70		50		45		ns	
64	tOSC	Oscillator Stabilization Time		20		20		20		20	ms	
65	tEXr	External Clock Rise Time (EXTAL)		25		25		15		10	ns	
66	tEXf	External Clock Fall Time (EXTAL)		25		25		15		10	ns	
67	tRr	/RESET Rise Time		50		50		50		50	ms	[2]
68	tRf	/RESET Fall Time		50		50		50		50	ms	[2]
69	tIr	Input Rise Time (Except EXTAL, /RESET)		100		100		100		80	ns	[2]
70	tIf	Input Fall Time (Except EXTAL, /RESET)		100		100		100		80	ns	[2]

Notes:

[1] $tcyc = tCHW + tCLW + tcf + tcr$

[2] This parameter has to be modified if other specification(s) can not be met.

[3] For Z8018012, V_{CC} range is limited to $\pm 5\%$.

[4] Numbers are preliminary and subject to change without notice.

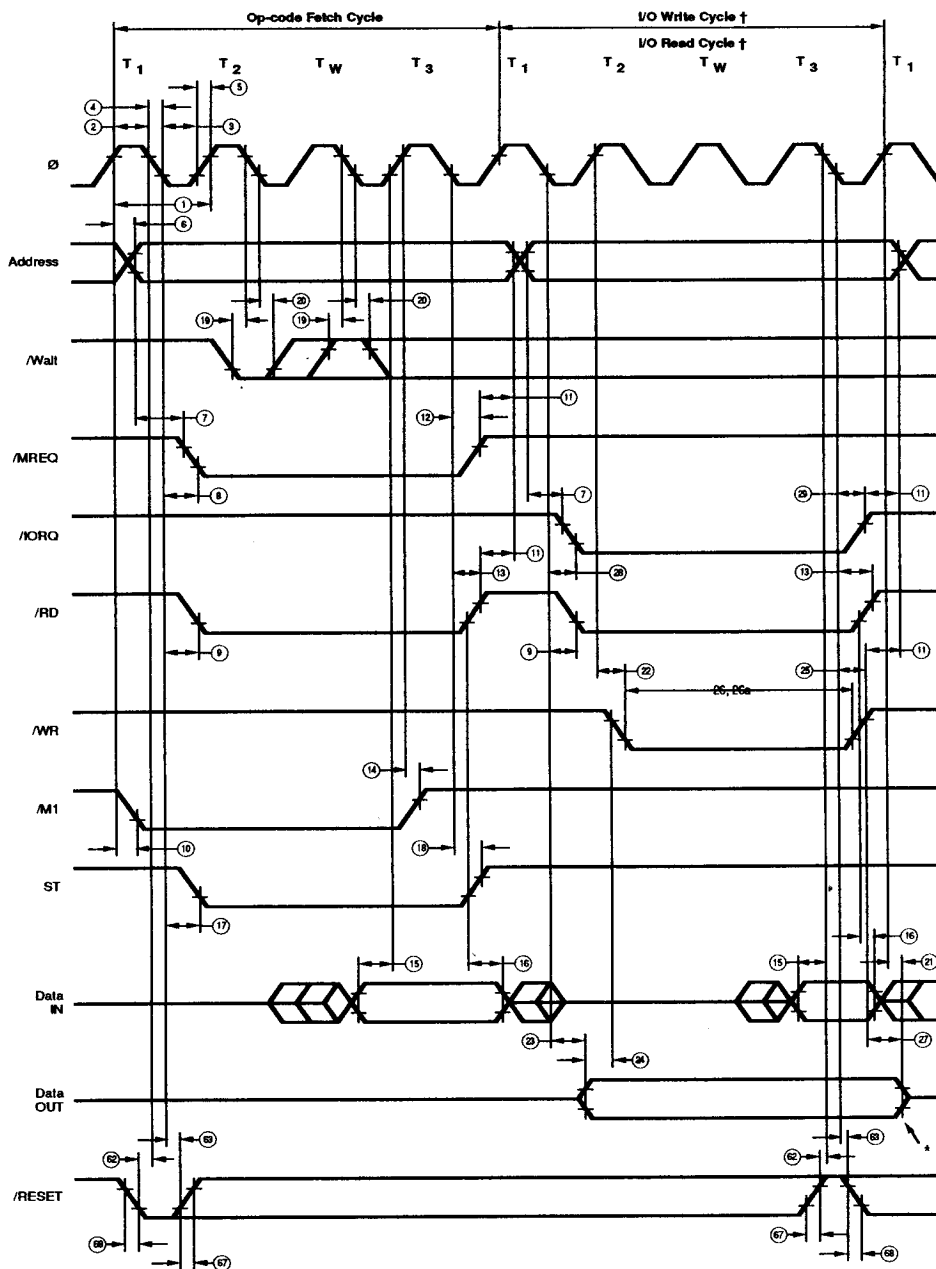


Figure 5a. Z80180 Timing Diagram

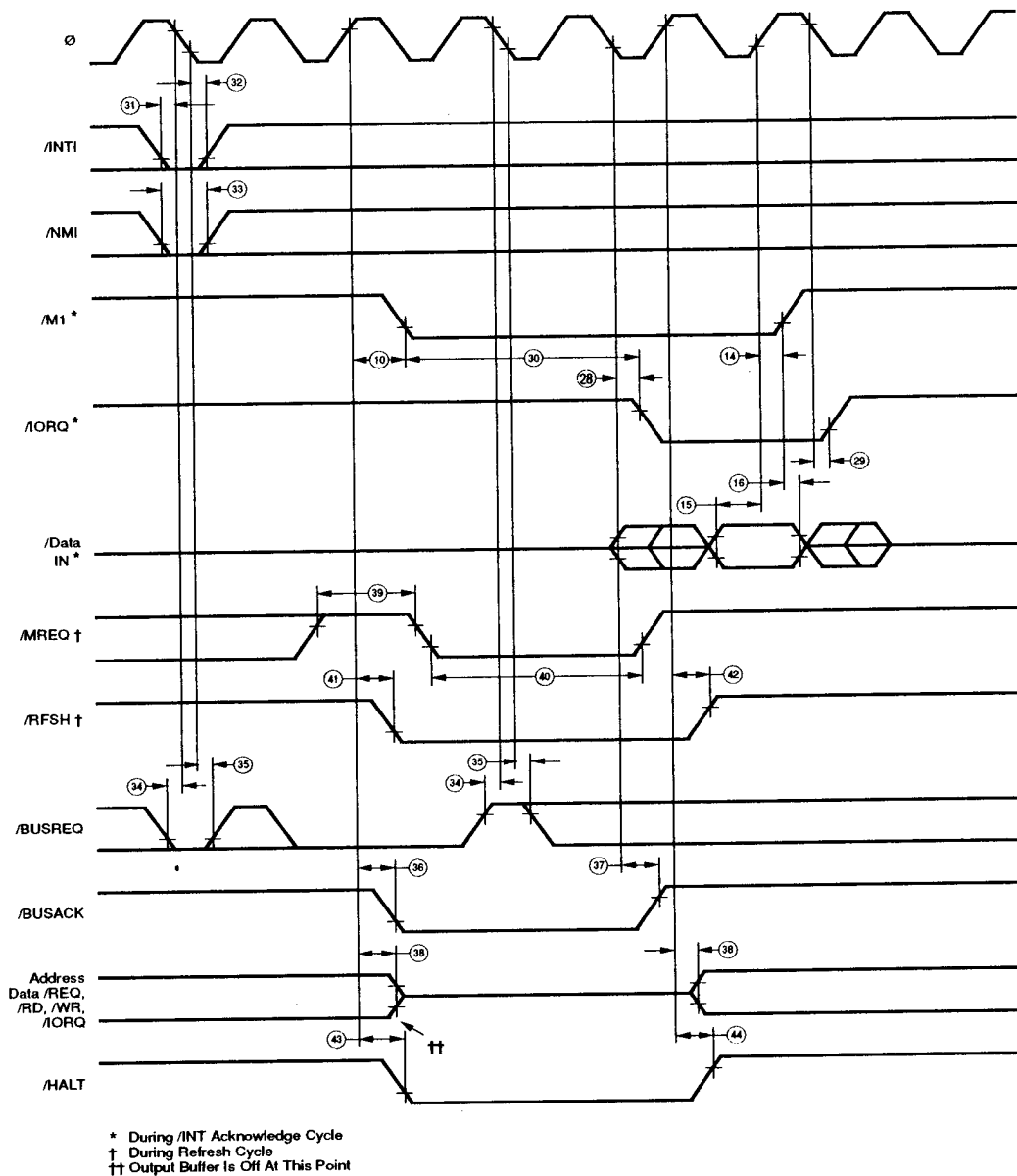
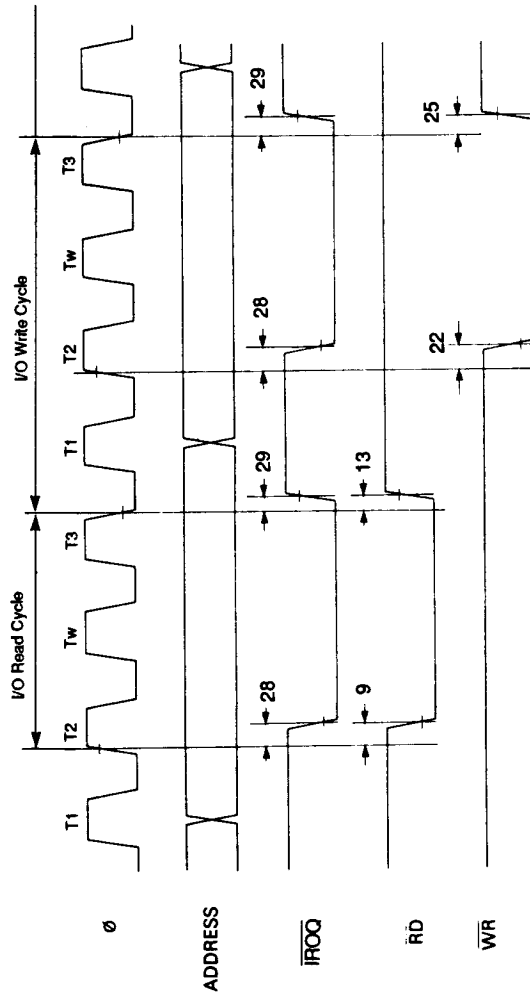
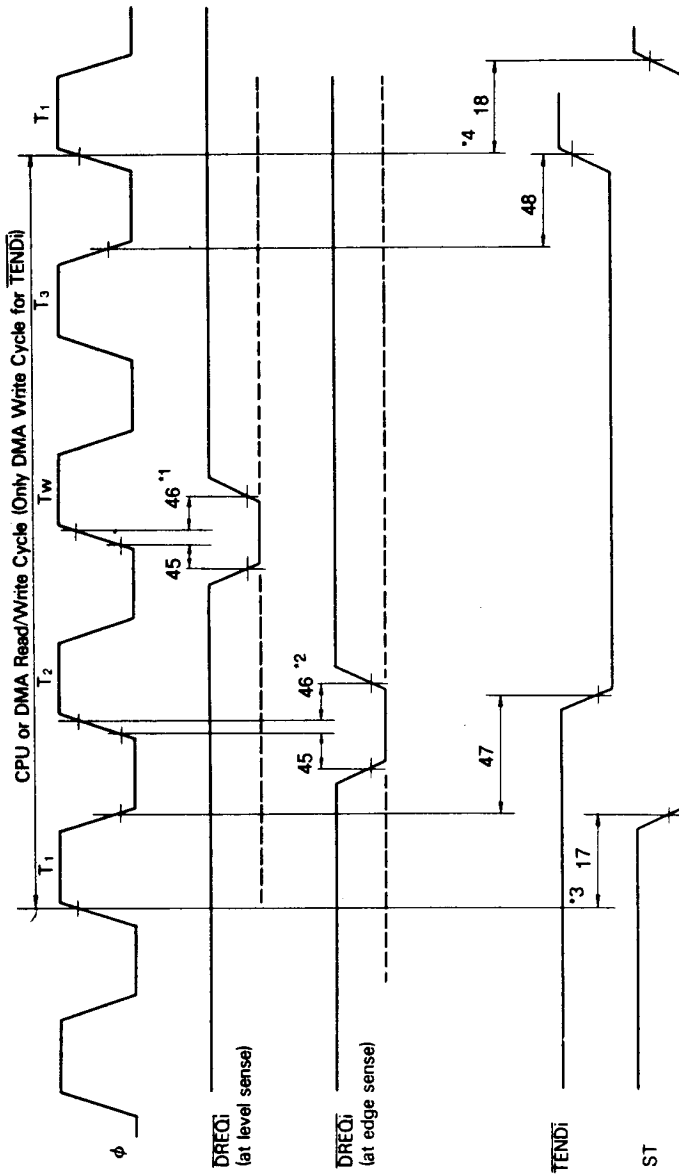


Figure 5b. Z80180 Timing Diagram



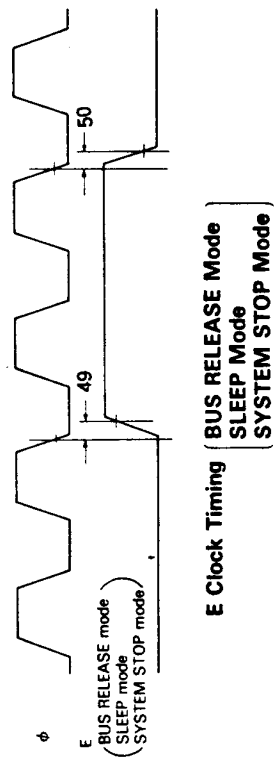
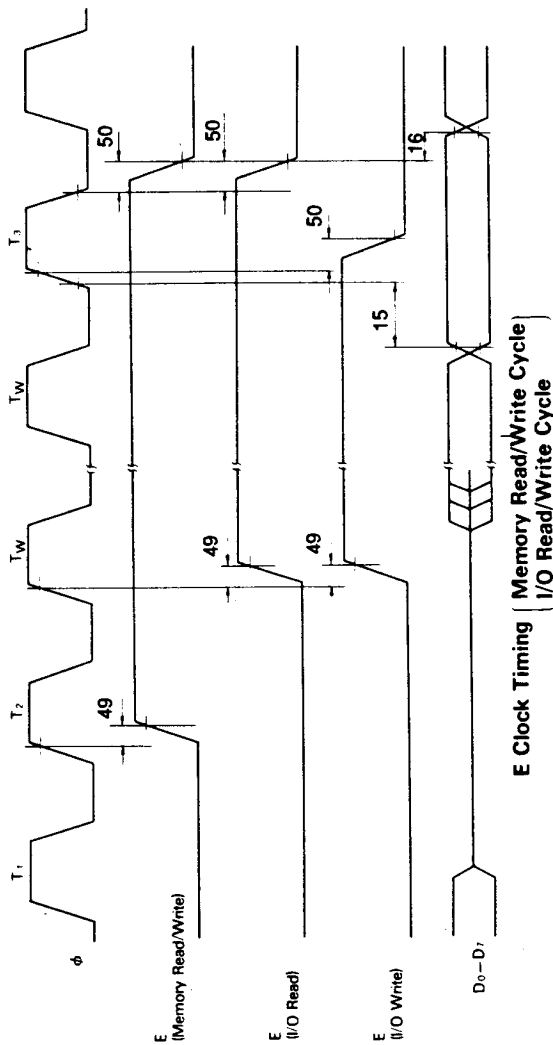
CPU Timing ($\overline{IOC}=0$)

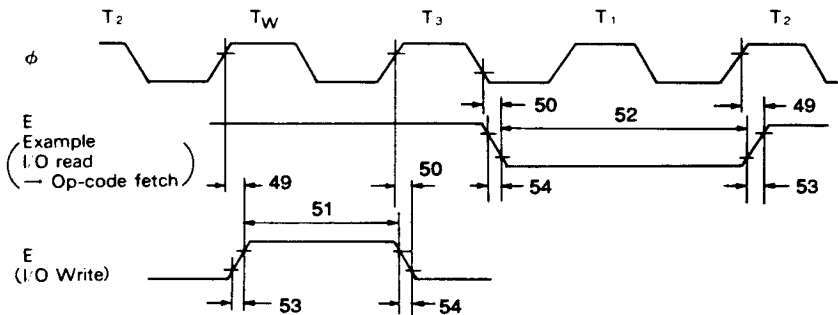
{ I/O Read Cycle
I/O Write Cycle }



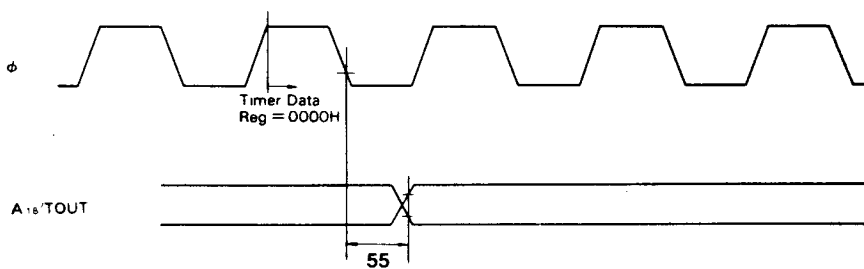
DMA Control Signals

- *1 t_{BQDS} and t_{BQDH} are specified for the rising edge of clock followed by T_3 .
- *2 t_{BQDS} and t_{BQDH} are specified for the rising edge of clock.
- *3 DMA cycle starts.
- *4 CPU cycle starts.

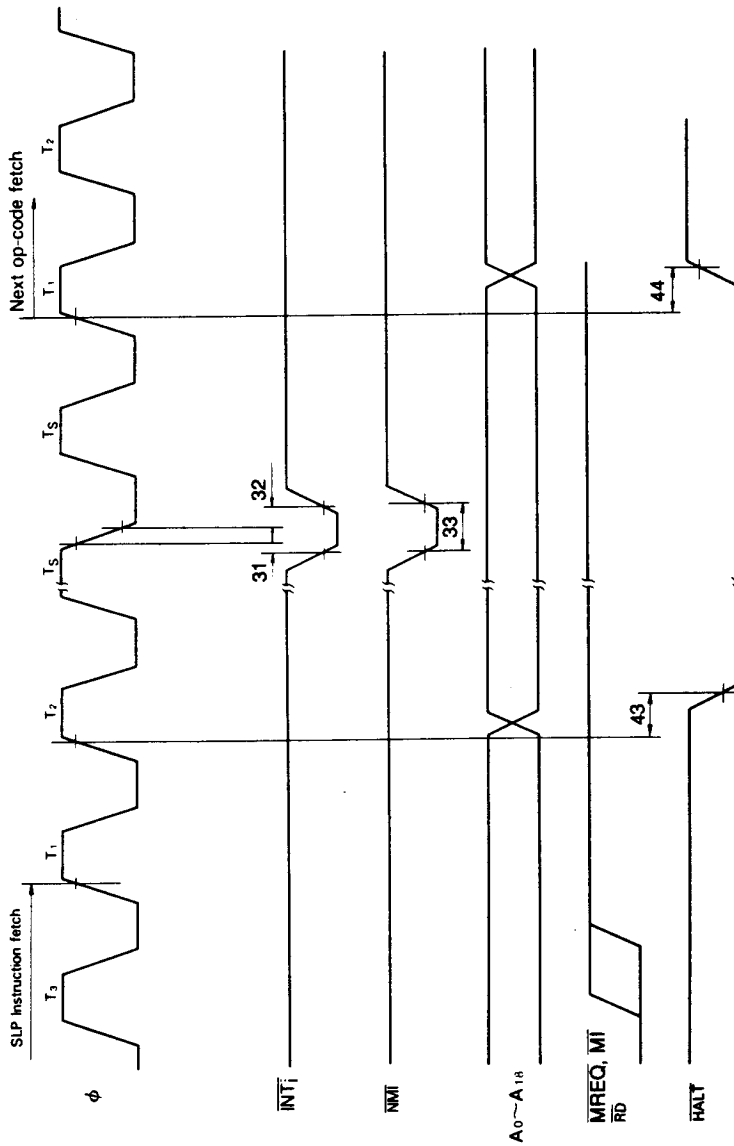




E Clock Timing (Minimum timing example of P_{WEL} and P_{WEH})



Timer Output Timing



SLP Execution Cycle

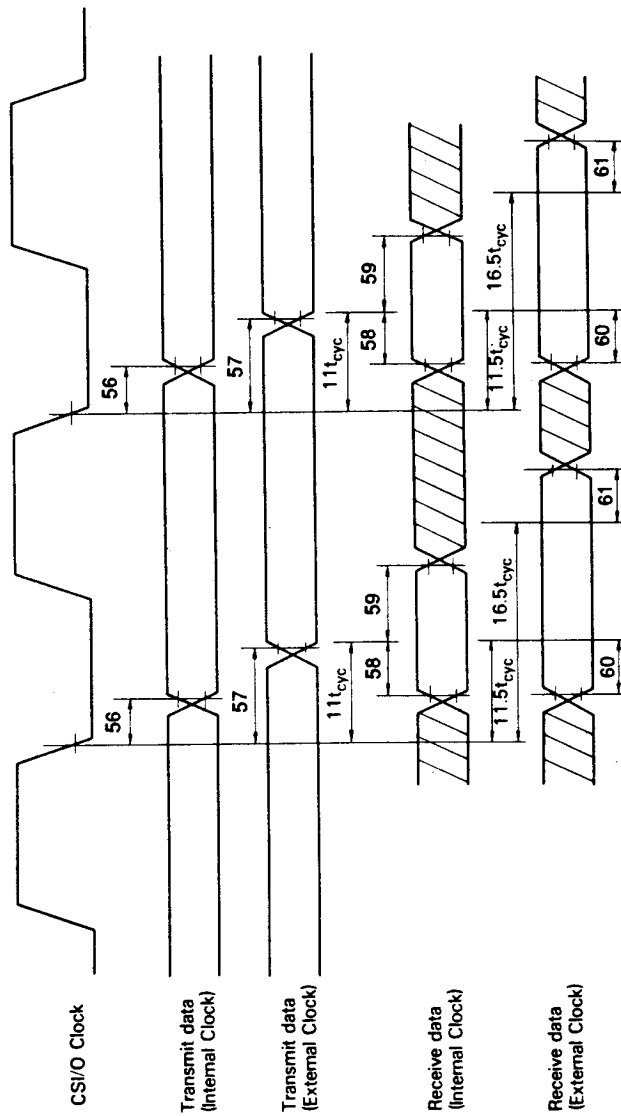
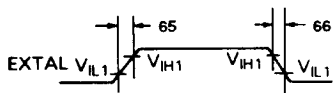
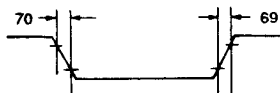


Figure 68. CSI/O Receive/Transmit Timing



External Clock Rise Time and Fall Time



**Input Rise Time and Fall Time
(Except EXTAL, RESET)**

STANDARD TEST CONDITIONS:

The DC Characteristics and Capacitance sections above apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows in to the referenced pin.

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for the address and control lines. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

