

# **Compound Field Effect Power Transistor**

# $\mu$ PA1572B

# N-CHANNEL POWER MOS FET ARRAY SWITCHING INDUSTRIAL USE

#### **DESCRIPTION**

The  $\mu$ PA1572B is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

#### **FEATURES**

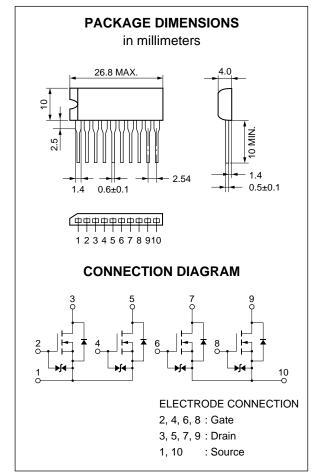
- Full Mold Package with 4 Circuits
- 4 V driving is possible
- Low On-state Resistance 
  $$\label{eq:RDS(on)} \begin{split} \text{RDS(on)} &= 0.6~\Omega~\text{MAX.}~\text{(VGS} = 10~\text{V, ID} = 1~\text{A)} \\ \text{RDS(on)} &= 0.8~\Omega~\text{MAX.}~\text{(VGS} = 4~\text{V, ID} = 1~\text{A)} \end{split}$$
- Low Input Capacitance Ciss = 110 pF TYP.

#### **ORDERING INFORMATION**

Type Number	Package
μPA1572BH	10Pin SIP

## ABSOLUTE MAXIMUM RATINGS (TA = 25 $^{\circ}$ C)

Drain to Source Voltage (Vgs = 0)	VDSS	60	V
Gate to Source Voltage (VDS = 0)	VGSS (AC)	±20	V
Drain Current (DC)	ID (DS)	±2.0	A/unit
Drain Current (pulse)	ID (pulse) *1	±6.0	A/unit
Total Power Dissipation	P <sub>T1</sub> *2	20	W
Total Power Dissipation	P <sub>T2</sub> *3	3.0	W
Channel Temperature	Тсн	150	°C
Storage Tempreature	T <sub>stg</sub> –	55 to +	150°C
Single Avalanche Current	las *4	5.0	Α
Single Avalanche Energy	Eas *4	0.1	mJ



Build-in Gate Diodes are for protection from static electricity in handing. In case high voltage over VGSs is applied, please append gate protection circuits.

The information in this document is subject to change without notice.

<sup>\*1</sup> PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 % \*2 4 Circuits Tc = 25 °C



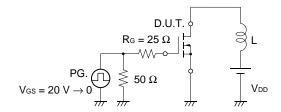
# ELECTRICAL CHARACTERISTICS (TA = 25 °C)

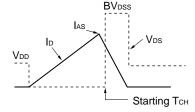
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Drain Leakage Current	IDSS			10	μΑ	Vps = 60 V, Vgs = 0
Gate Leakage Current	Igss			±10	μΑ	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Gate Cutoff Voltage	VGS (off)	1.0		2.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 mA
Forward Transfer Admittance	Y <sub>fs</sub>	0.5			S	Vps = 10 V, lp = 1.0 A
Drain to Source ON-Resistance	RDS (on)1		0.3	0.6	Ω	Ves = 10 V, Ip = 1.0 A
Drain to Sourse ON-Resistance	RDS (on)2		0.4	0.8	Ω	Ves = 4.0 V, ID = 1.0 A
Input Capacitance	Ciss		110		pF	Vps = 10 V, Vgs = 0, f = 1.0 MHz
Output Capacitance	Coss		70		pF	
Reverse Transfer Capacitance	Crss		25		pF	
Turn-on Delay Time	td (on)		30		ns	$I_D$ = 1.0 A, $V_{GS (on)}$ = 10 V, $V_{DD}$ = 30 V, $R_L$ = 30 $\Omega$
Rise Time	tr		200		ns	
Turn-off Delay Time	td (off)		100		ns	
Fall Time	tf		160		ns	
Total Gate Charge	QG		5.4		nC	VGS = 10 V, ID = 2.0 A, VDD = 48 V
Gate to Source Charge	Qgs		0.7		nC	
Gate to Drain Charge	Q <sub>GD</sub>		2.0		nC	
Body Diode Forward Voltage	V <sub>F</sub> (S-D)		1.0		V	IF = 2.0 A, VGS = 0
Reverse Recovery Time	trr		130		ns	$I_F = 2.0 \text{ A}, \text{ V}_{GS} = 0, \text{ di/dt} = 50 \text{ A}/\mu\text{s}$
Reverse Recovery Charge	Qrr		110		nC	

2

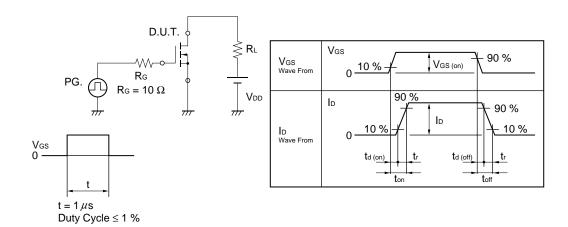


# **Test Circuit 1 Avalanche Capability**

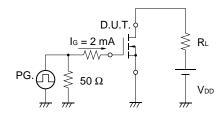




# **Test Circuit 2 Switching Time**



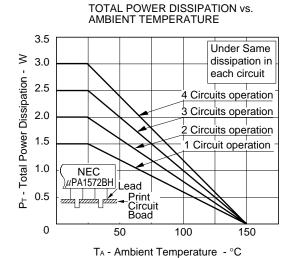
# **Test Circuit 3 Gate Charge**



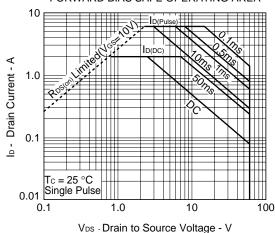
3



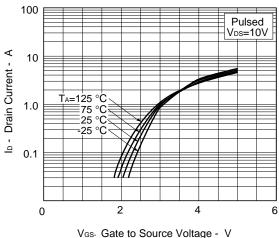
## CHARACTERISTICS (TA = 25 °C)



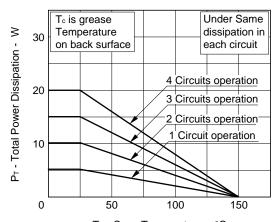
#### FORWARD BIAS SAFE OPERATING AREA



FORWARD TRANSFER CHARACTERISTICS

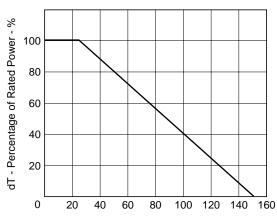


#### TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



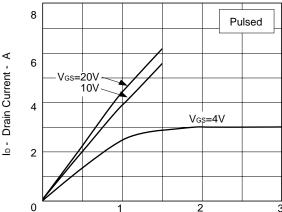
Tc - Case Temperature - °C

#### DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



Tc - Case Temperature - °C

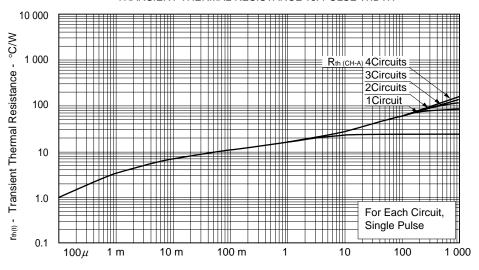
# DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



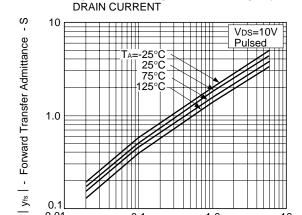
V<sub>DS</sub> - Drain to Source Voltage - V



#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



PW - Pulse Width - s



0.1

ID- Drain Current - A

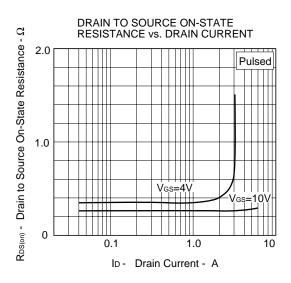
1.0

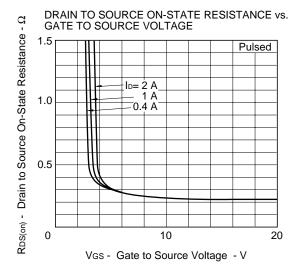
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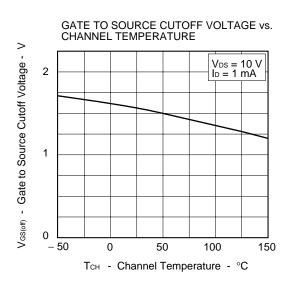
0.1

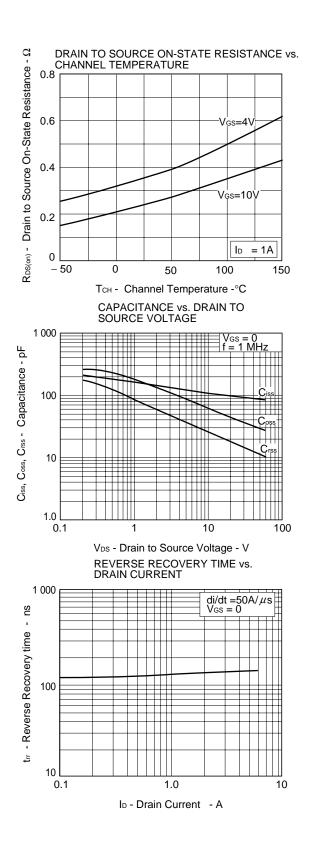
0.01

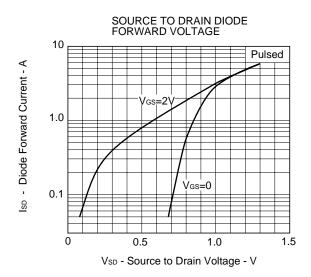
FORWARD TRANSFER ADMITTANCE vs.

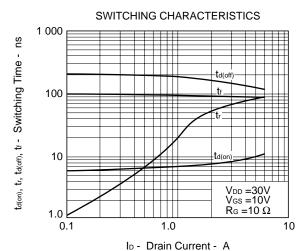


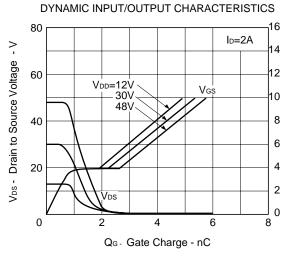




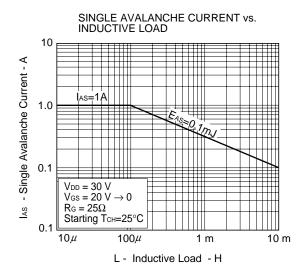


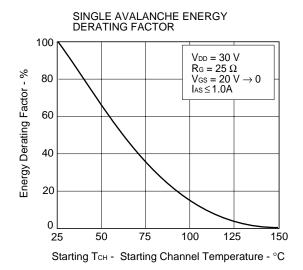












### **REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.