To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

COMPOUND FIELD EFFECT POWER TRANSISTOR

μPA1501

N-CHANNEL POWER MOS FET ARRAY SWITCHING TYPE

DESCRIPTION

The μPA1501 is N-channel Power MOS FET Array that built in 4 circuits and surge absorber designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Low On-state Resistance
  $R_{DS(on)} \leqq 0.42\ \Omega$ MAX. (V_{GS} = 10 V, I_D = 2 A)
  $R_{DS(on)} \leqq 0.49\ \Omega$ MAX. (V_{GS} = 4 V, I_D = 2 A)
- Surge Absorber, built in.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPA1501H	12-Pin SIP	Standard

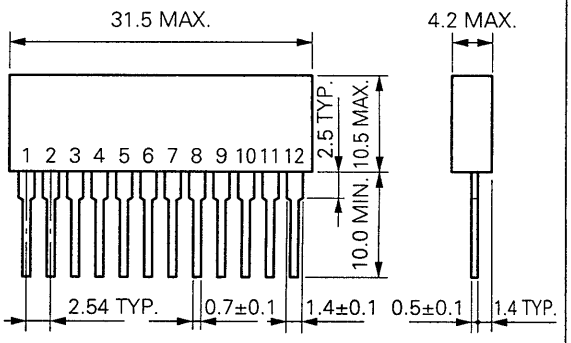
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	120	V
Gate to Source Voltage	$V_{GSS(AC)}$	+20, −10	V
Drain Current (DC)	$I_{D(DC)}$	±3.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$*	±12	A/unit
Repetitive Peak Reverse Voltage	V_{RRM}	140	V
Diode Forward Current	$I_{F(AV)}$	3.0	A/unit
Total Power Dissipation (4 circuits)	P_T	4.0	W
<T_a = 25 °C>			
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

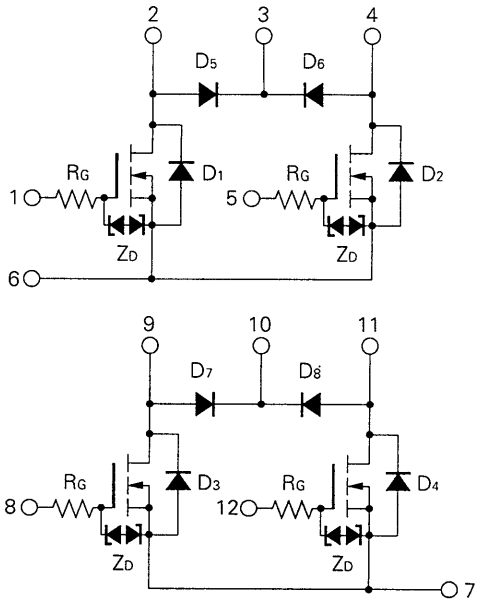
PACKAGE DIMENSIONS
(in millimeters)



ELECTRODE CONNECTION

1, 5, 8, 12	GATE
2, 4, 9, 11	DRAIN, ANODE
6, 7	SOURCE
3, 10	CATHODE

PIN CONNECTION



D_1 to D_4 : Body Diode
D_5 to D_8 : Surge Absorber
Z_D : Gate to Source Protection
R_G : Gate Input Resistance
450 Ω TYP.

Document No. IC-3327
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Date Published December 1993 M
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 120 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	$V_{GS} = {}^{+20}_{-10}$ V, V_{DS} = 0
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	2.2			S	V_{DS} = 10 V, I_D = 2 A
Drain to Source On-state Resistance	$R_{DS(on)1}$		0.42	0.55	Ω	V_{GS} = 10 V, I_D = 2 A
Drain to Source On-state Resistance	$R_{DS(on)2}$		0.49	0.65	Ω	V_{GS} = 4 V, I_D = 2 A
Input Capacitance	C_{iss}		620		pF	V_{DS} = 10 V V_{GS} = 0 f = 1.0 MHz
Output Capacitance	C_{oss}		140		pF	
Reverse Transfer Capacitance	C_{rss}		10		pF	
Turn-On Delay Time	$t_{d(on)}$		75		ns	I_D = 2 A V_{GS} = 10 V V_{DD} = 30 V R_L = 15 Ω See Fig. 1
Rise Time	t_r		60		ns	
Turn-Off Delay Time	$t_{d(off)}$		900		ns	
Fall Time	t_f		200		ns	
Total Gate Charge	Q_G		13		nC	V_{GS} = 10 V I_D = 3 A V_{DD} = 48 V See Fig. 2
Gate to Source Charge	Q_{GS}		3		nC	
Gate to Drain Charge	Q_{GD}		2		nC	

SURGE ABSORBER (Diode, built in) 1 Unit

Repetitive Peak Reverse Current	I_{RRM}			10	μA	V_R = 140 V
Diode Forward Voltage	V_F		1.2		V	I_F = 3 A, V_{GS} = 0

Fig. 1 Switching Test Circuit

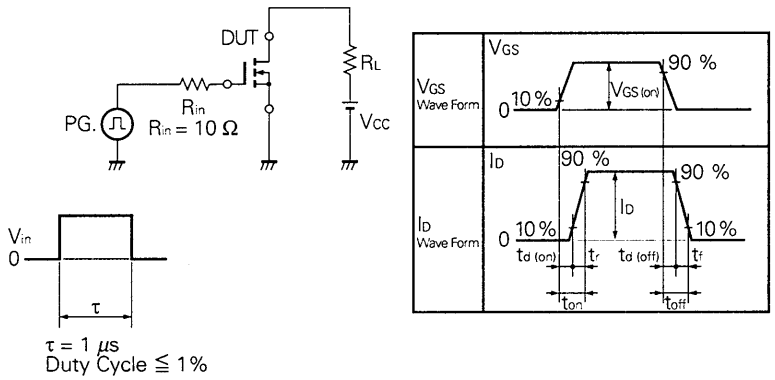
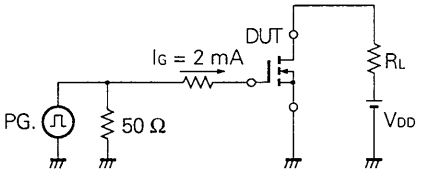
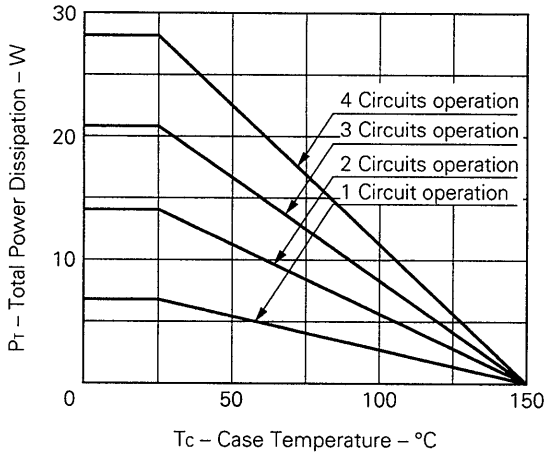


Fig. 2 Gate Charge Test Circuit

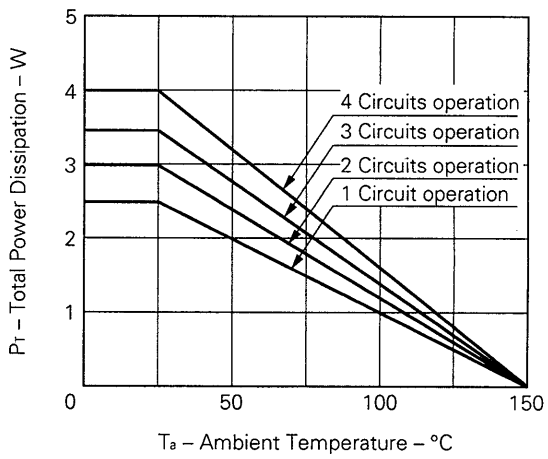


TYPICAL CHARACTERISTICS (T_a = 25 °C)

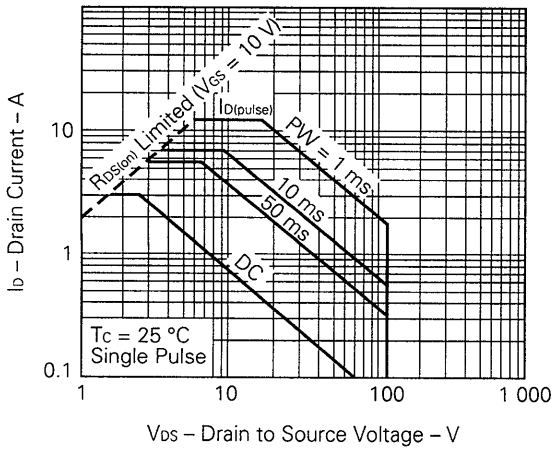
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



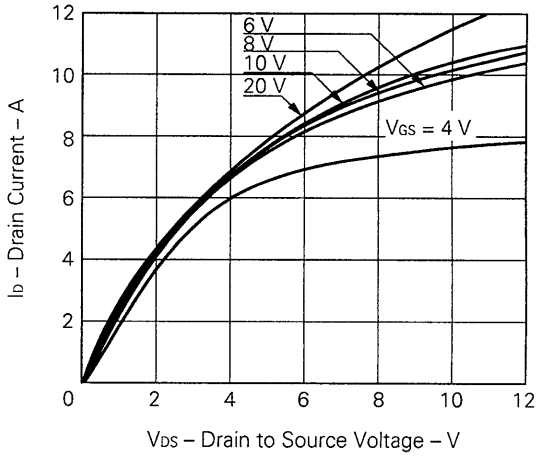
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



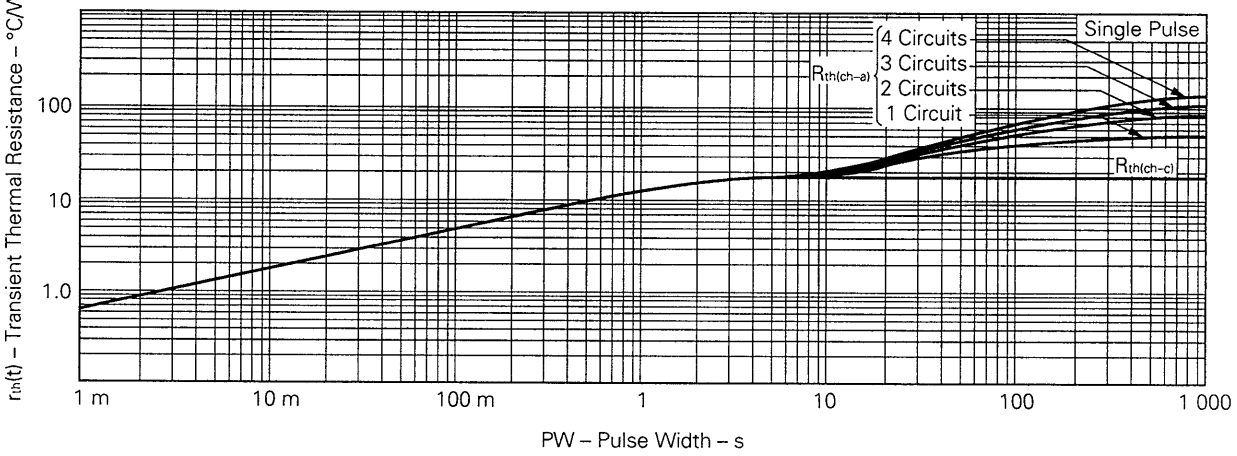
FORWARD BIAS SAFE OPERATING AREA



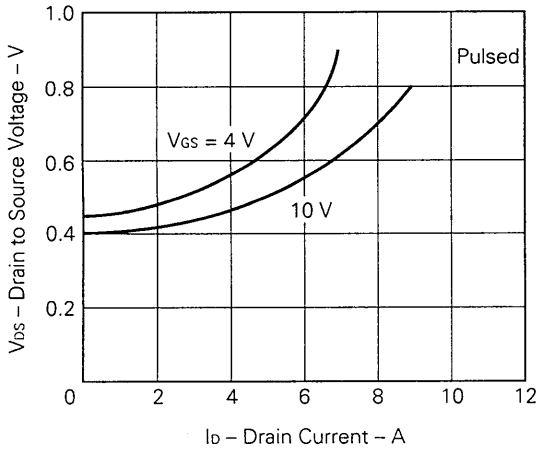
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



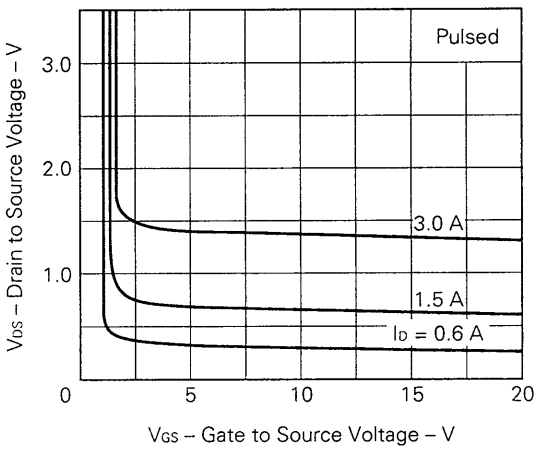
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



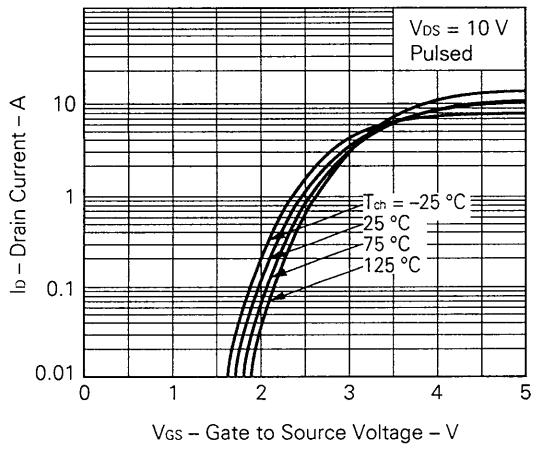
DRAIN TO SOURCE VOLTAGE vs. DRAIN CURRENT



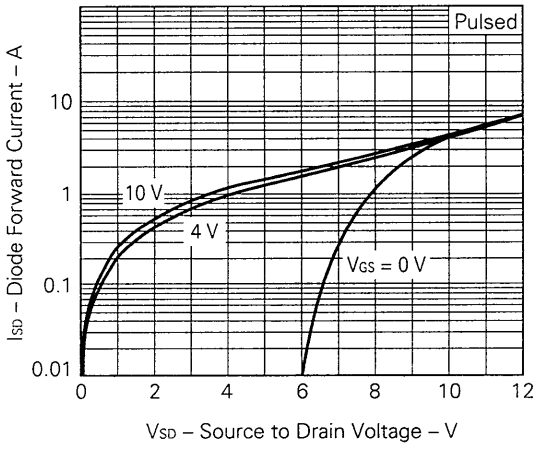
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE



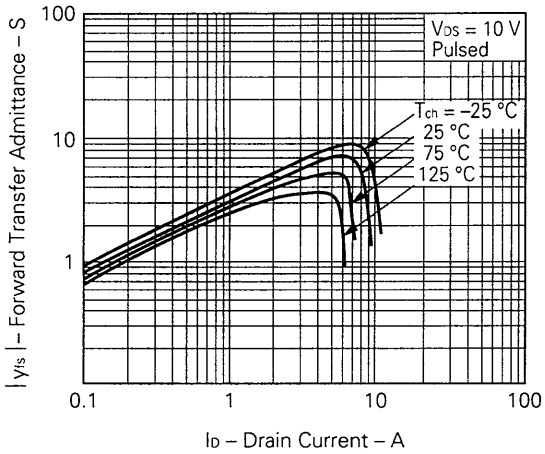
TRANSFER CHARACTERISTIC



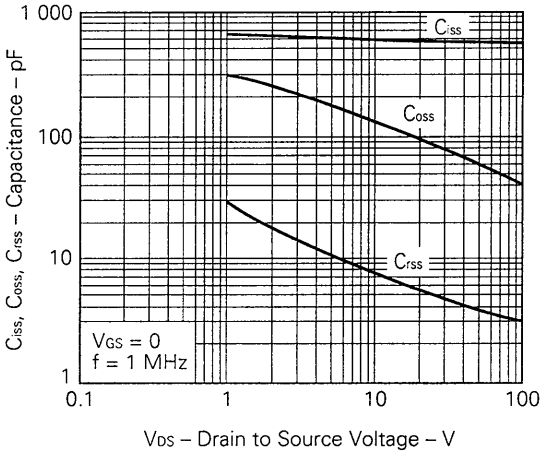
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



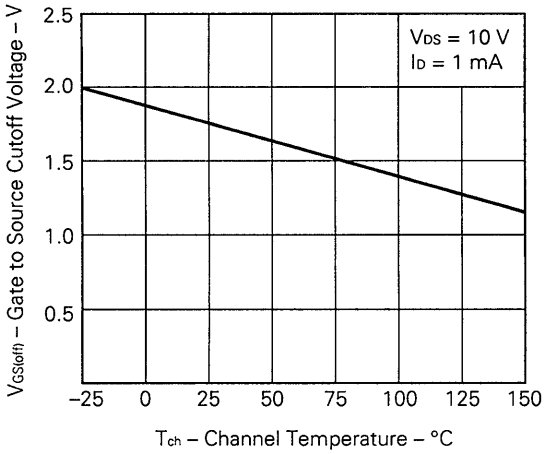
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



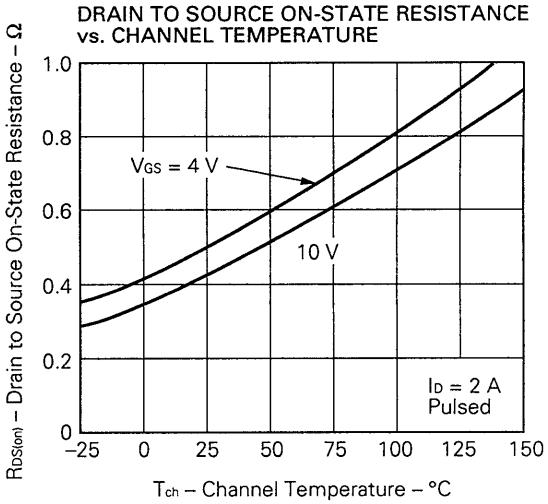
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



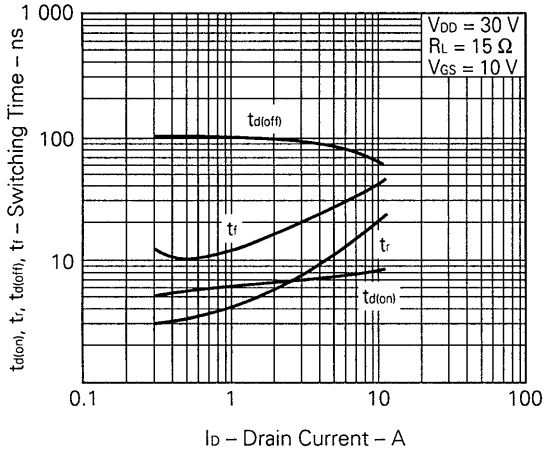
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



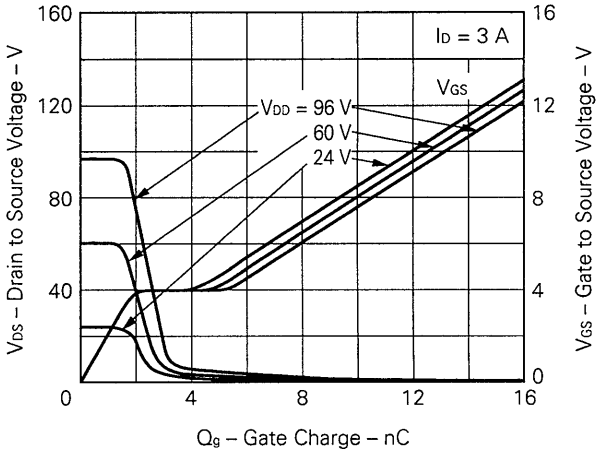
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



SWITCHING TIME vs. DRAIN CURRENT



DYNAMIC INPUT CHARACTERISTIC



Reference

Application note name	No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Application circuit using Power MOS FET	TEB-1035

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