

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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Not recommended  
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Dual N-CHANNEL MOSFET

**DESCRIPTION**

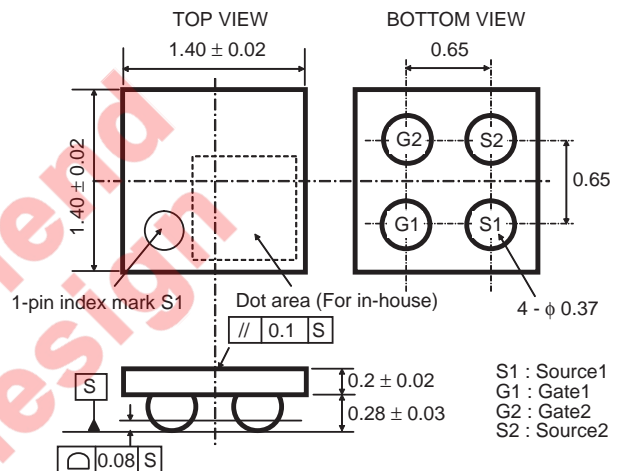
The μPA2352 is a Dual N-channel MOSFET designed for Lithium-Ion battery protection circuit.

Ecologically Flip chip MOSFET for Lithium-Ion battery Protection (EFLIP).

**FEATURES**

- Monolithic Dual MOSFET  
Connecting the Drains on the circuit board is not required because the Drains of the FET1 and the FET2 are internally connected.
- 2.5 V drive available and low on-state resistance  
 $R_{SS(on)1} = 43.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_S = 2.0 \text{ A)}$   
 $R_{SS(on)2} = 45.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_S = 2.0 \text{ A)}$   
 $R_{SS(on)3} = 55.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 3.1 \text{ V, } I_S = 2.0 \text{ A)}$   
 $R_{SS(on)4} = 67.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 2.5 \text{ V, } I_S = 2.0 \text{ A)}$
- Built-in G-S protection diode against ESD
- Pb-free bump

**OUTLINE DRAWING (Unit: mm)**



**ORDERING INFORMATION**

PART NUMBER	PACKAGE
μPA2352T1G-E4-A <sup>Note</sup>	4 PIN EFLIP

**Note** "-A" indicates Pb-free (This product does not contain Pb in external electrode and other parts). "-E4" indicates the unit orientation (-E4 only).

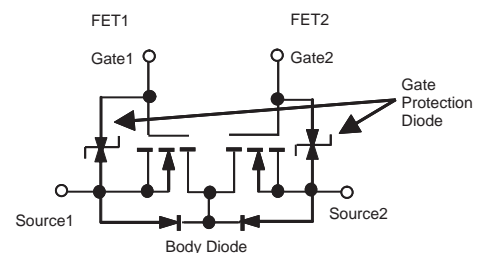
**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)**

Source to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>SSS</sub>	24	V
Gate to Source Voltage (V <sub>SS</sub> = 0 V)	V <sub>GSS</sub>	±12	V
Source Current (DC) <sup>Note1</sup>	I <sub>S(DC)</sub>	±4.0	A
Source Current (pulse) <sup>Note2</sup>	I <sub>S(pulse)</sub>	±40	A
Total Power Dissipation (2units) <sup>Note1</sup>	P <sub>T</sub>	0.75	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

**Notes 1.** Mounted on BT resin board of 40.5 mm x 25 mm x 1.5 mm

**2.** PW ≤ 100 μs, Duty Cycle ≤ 1%

**EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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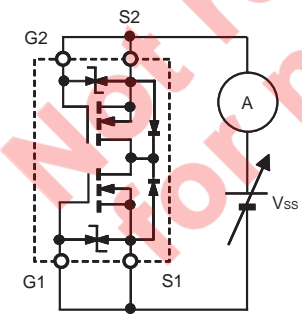
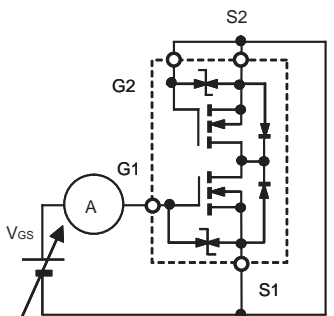
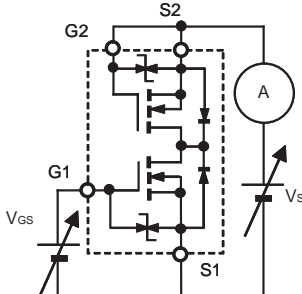
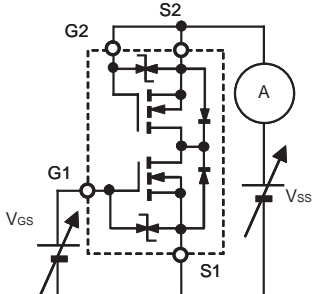
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**ELECTRICAL CHARACTERISTICS (TA = 25°C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Source Current	I <sub>SSS</sub>	V <sub>SS</sub> = 24.0 V, V <sub>GS</sub> = 0 V, TEST CIRCUIT 1			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±12.0 V, V <sub>SS</sub> = 0 V, TEST CIRCUIT 2			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>SS</sub> = 10.0 V, I <sub>S</sub> = 1.0 mA, TEST CIRCUIT 3	0.5	1.0	1.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>SS</sub> = 10.0 V, I <sub>S</sub> = 2.0 A, TEST CIRCUIT 4	2.5			S
Source to Source On-state Resistance <sup>Note</sup>	R <sub>SS(on)1</sub>	V <sub>GS</sub> = 4.5 V, I <sub>S</sub> = 2.0 A, TEST CIRCUIT 5	24.0	35.0	43.0	mΩ
	R <sub>SS(on)2</sub>	V <sub>GS</sub> = 4.0 V, I <sub>S</sub> = 2.0 A, TEST CIRCUIT 5	25.0	37.0	45.0	mΩ
	R <sub>SS(on)3</sub>	V <sub>GS</sub> = 3.1 V, I <sub>S</sub> = 2.0 A, TEST CIRCUIT 5	31.5	42.0	55.0	mΩ
	R <sub>SS(on)4</sub>	V <sub>GS</sub> = 2.5 V, I <sub>S</sub> = 2.0 A, TEST CIRCUIT 5	33.5	50.0	67.0	mΩ
Input Capacitance	C <sub>iSS</sub>	V <sub>SS</sub> = 10.0 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		330		pF
Output Capacitance	C <sub>oss</sub>	TEST CIRCUIT 7		80		pF
Reverse Transfer Capacitance	C <sub>rSS</sub>			55		pF
Turn-on Delay Time	t <sub>d(on)</sub>		I <sub>S</sub> = 4.0 A, V <sub>GS</sub> = 4.0 V, V <sub>DD</sub> = 20.0 V,		22	
Rise Time	t <sub>r</sub>	R <sub>G</sub> = 6.0 Ω, TEST CIRCUIT 8		132		ns
Turn-off Delay Time	t <sub>d(off)</sub>			183		ns
Fall Time	t <sub>f</sub>			216		ns
Gate to Source Charge	Q <sub>G</sub>	V <sub>G1S1</sub> = 4.0 V, I <sub>S</sub> = 4.0 A, V <sub>DD</sub> = 20.0 V, TEST CIRCUIT 9		5.7		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-S)</sub>	I <sub>F</sub> = 4.0 A, V <sub>GS</sub> = 0 V, TEST CIRCUIT 6		1.0		V

**Note** Pulsed

Both the FET1 and the FET2 are measured. Test circuits are example of measuring the FET1 side.

<p><b>TEST CIRCUIT 1</b> I<sub>SSS</sub></p> 	<p><b>TEST CIRCUIT 2</b> I<sub>GSS</sub></p> <p>When FET1 is measured, between GATE and SOURCE of FET2 are shorted.</p> 
<p><b>TEST CIRCUIT 3</b> V<sub>GS(off)</sub></p> <p>When FET1 is measured, between GATE and SOURCE of FET2 are shorted.</p> 	<p><b>TEST CIRCUIT 4</b>  y<sub>fs</sub> </p> <p>ΔI<sub>S</sub>/ΔV<sub>GS</sub></p> 

**TEST CIRCUIT 5  $R_{ss(on)}$**

$V_{ss}/I_s$

**TEST CIRCUIT 6  $V_{F(s-s)}$**

When FET1 is measured, FET2 is added  $V_{GS} +4.5 V$ .

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**TEST CIRCUIT 7**

$C_{iss}$

$C_{oss}$

$C_{riss}$

---

**TEST CIRCUIT 8  $t_{d(on)}$ ,  $t_r$ ,  $t_{d(off)}$ ,  $t_f$**

$V_{GS}$  Wave Form

$V_{SS}$  Wave Form

$\tau = 1 \mu s$   
Duty Cycle  $\leq 1\%$

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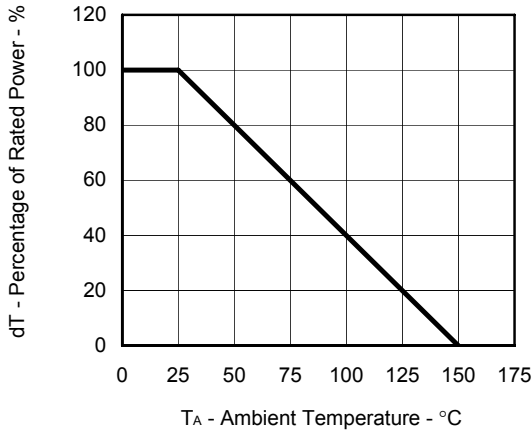
**TEST CIRCUIT 9  $Q_G$**

$I_e = 2 mA$

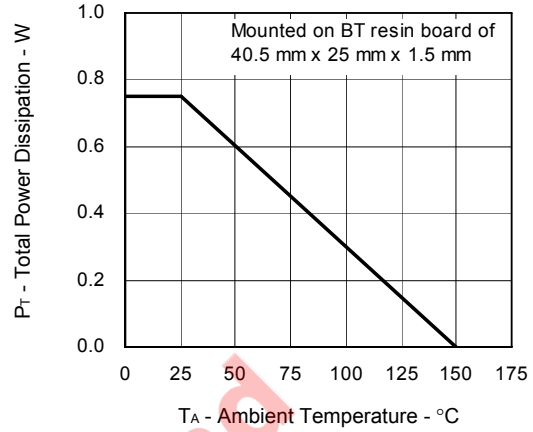
$50 \Omega$

TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

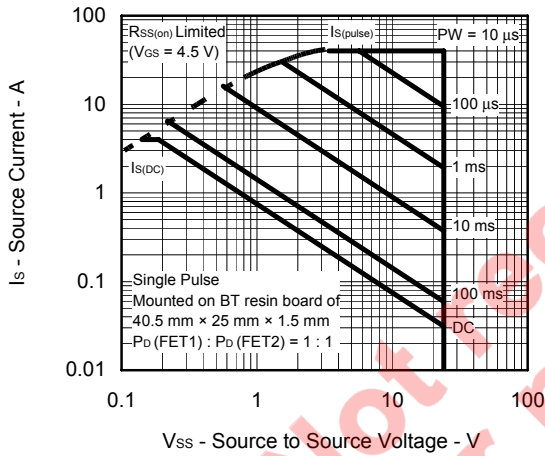
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



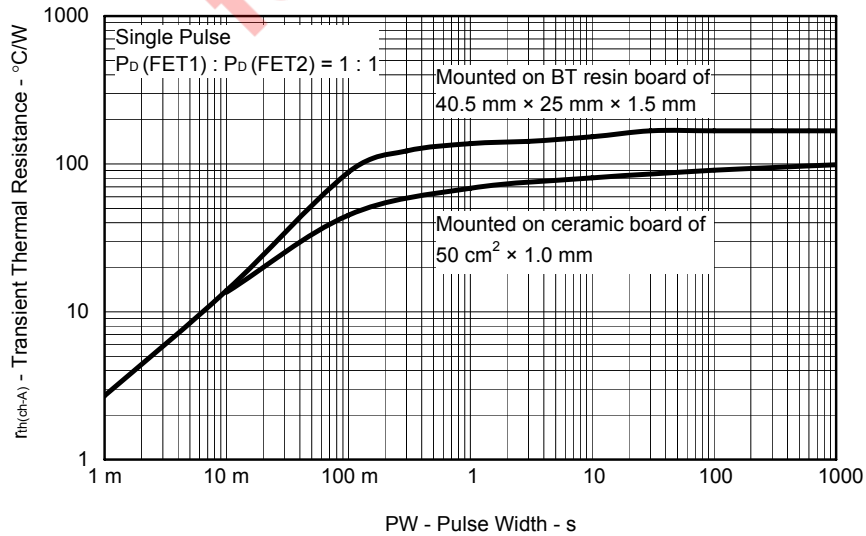
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



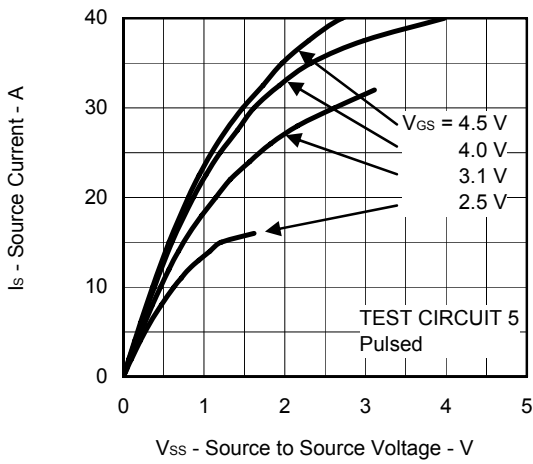
<R> FORWARD BIAS SAFE OPERATING AREA



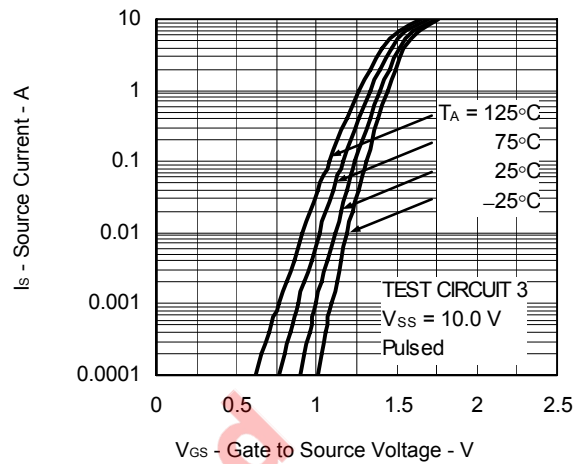
<R> TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



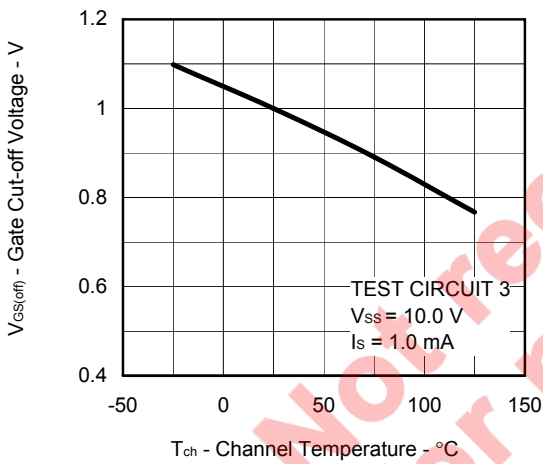
SOURCE CURRENT vs. SOURCE TO SOURCE VOLTAGE



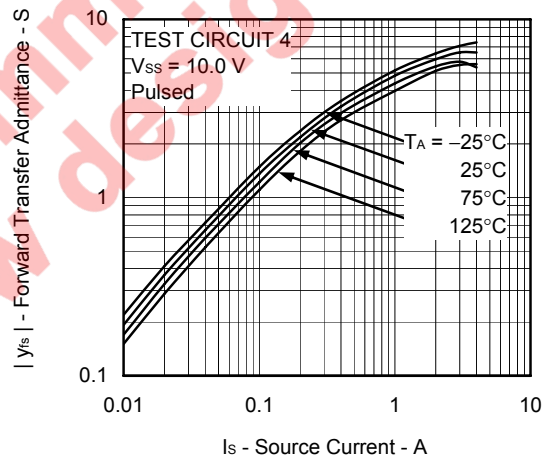
FORWARD TRANSFER CHARACTERISTICS



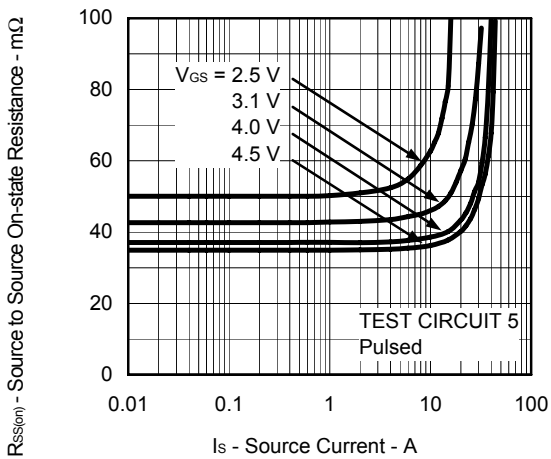
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



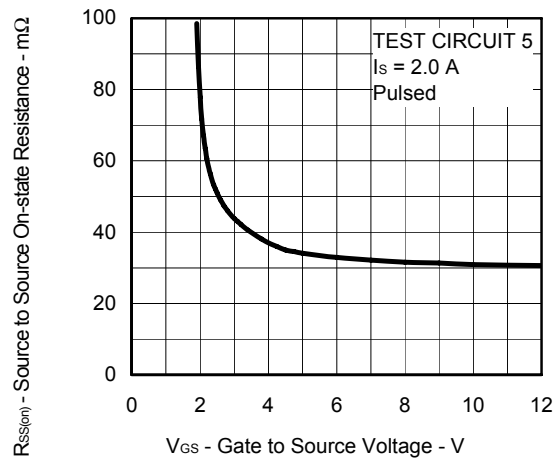
FORWARD TRANSFER ADMITTANCE vs. SOURCE CURRENT



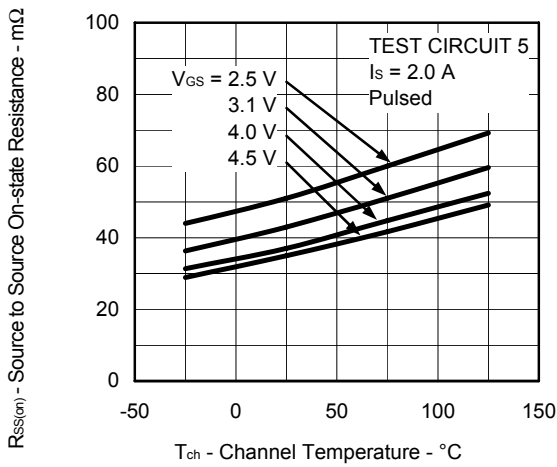
SOURCE TO SOURCE ON-STATE RESISTANCE vs. SOURCE CURRENT



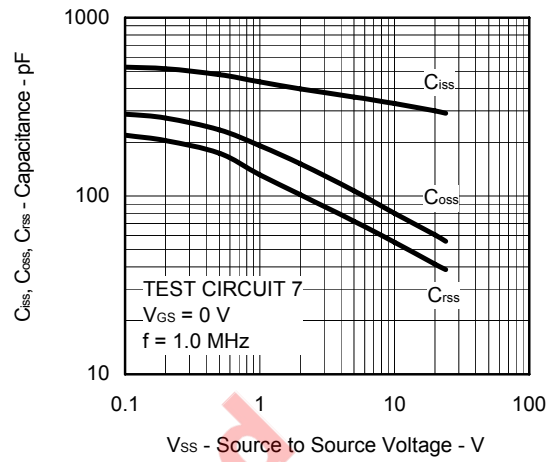
SOURCE TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



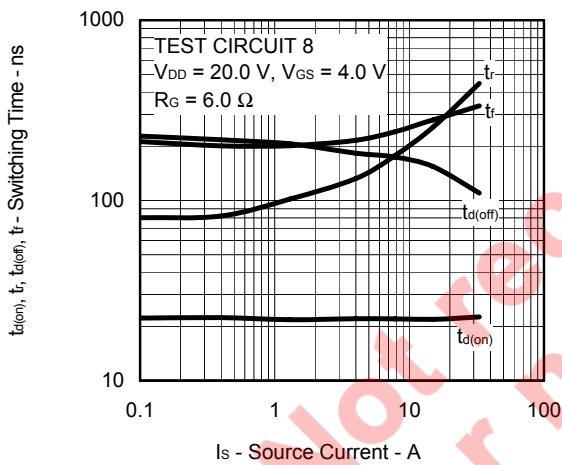
SOURCE TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



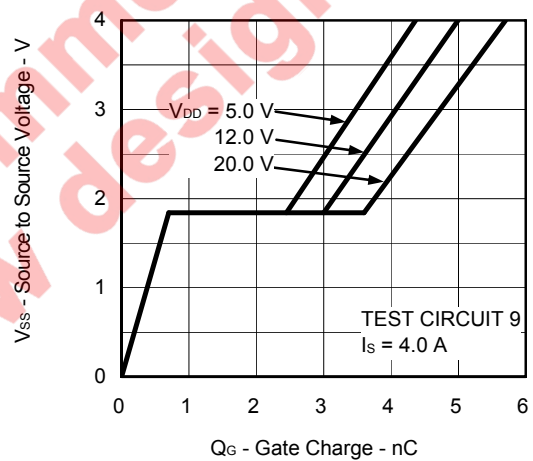
<R> CAPACITANCE vs. SOURCE TO SOURCE VOLTAGE



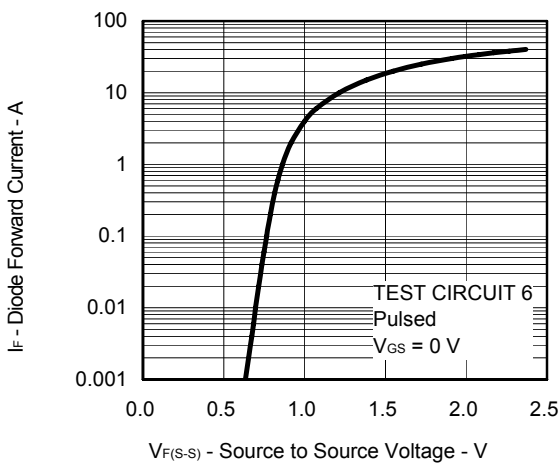
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO SOURCE DIODE FORWARD VOLTAGE





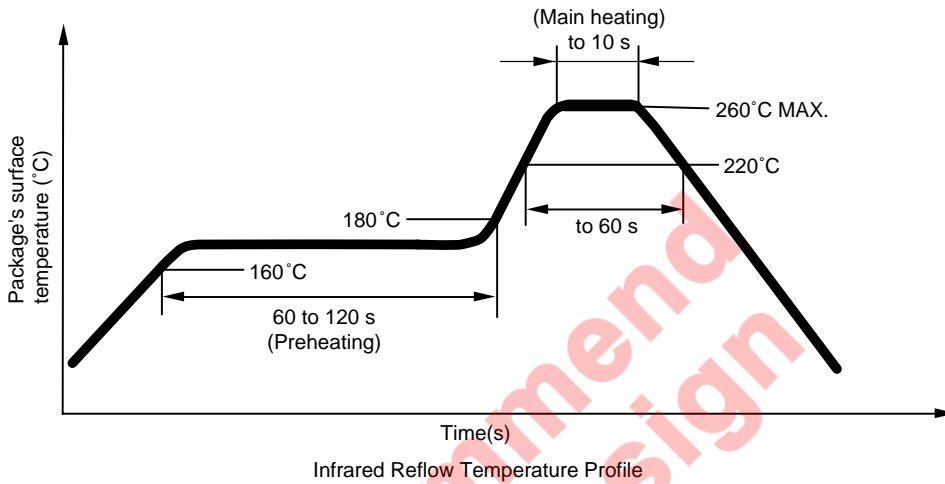
**<Notes for using this device safely>**

**When you use this device, in order to prevent a customer's hazard and damage, use it with understanding the following contents. If used exceeding recommended conditions, there is a possibility of causing the device and characteristic degradation.**

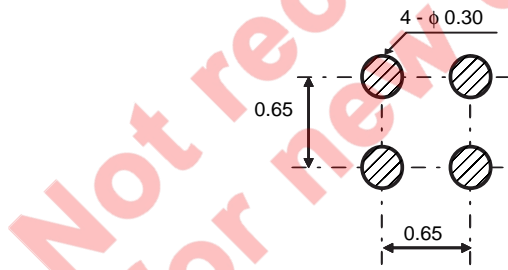
1. This device is very thin device and should be handled with caution for mechanical stress. The rate of distortion applied to the device should become below 2000  $\mu\epsilon$ . If the rate of distortion exceeds 2000  $\mu\epsilon$ , the characteristic of a device may be degraded and it may result in failure.
2. Please do not damage the device when you handle it. The use of metallic tweezers has the possibility of giving the wound. And mounting with the nozzle with clean point is recommended.
3. When you mount the device on a substrate, carry out within our recommended soldering conditions of infrared reflow. If mounted exceeding the conditions, the characteristic of a device may be degraded and it may result failure.
4. When you wash the device mounted the board, carry out within our recommended conditions. If washed exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.
5. When you use ultrasonic wave to substrate after the device mounting, prevent from touching a resonance directly. If it touches, the characteristic of a device may be degraded and it may result in failure.
6. When you coat the device after mounted on the board, please consult our company. NEC Electronics recommends the epoxy resin of the semiconductor grade as a coating material.
7. Please refer to Figure 2 as an example of the Mounting Pad. Optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.
8. The marking side of this device is an internal electrode. Please neither contact with terminals of other parts nor take out the electrode.

**Figure 1 Recommended soldering conditions of INFRARED REFLOW**

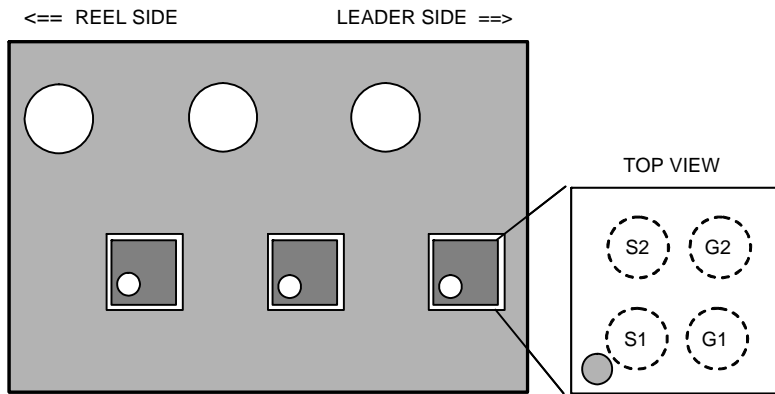
Maximum temperature (Package's surface temperature)	: 260°C or below
Time at maximum temperature	: 10 s or less
Time of temperature higher than 220°C	: 60 s or less
Preheating time at 160 to 180°C	: 60 to 120 s
Maximum number of reflow processes	: 3 times
Maximum chlorine content of rosin flux (Mass percentage)	: 0.2% or less



**Figure 2 The example of the Mounting Pad**



**Figure 3 The unit orientation**



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