



## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- ▶ Low threshold - 2.0V max.
- ▶ High input impedance
- ▶ Low input capacitance - 50pF typical
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage
- ▶ Complementary N- and P-channel devices

### Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

### General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

Device	Package Option	BV <sub>DSS</sub> /BV <sub>DGS</sub> (V)	R <sub>DS(ON)</sub> (max) (Ω)	I <sub>D(ON)</sub> (min) (A)	V <sub>GS(th)</sub> (max) (V)
	TO-92				
TN0106	TN0106N3-G	60	3.0	2.0	2.0

-G indicates package is RoHS compliant ('Green')



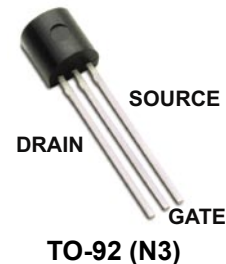
### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV <sub>DSS</sub>
Drain-to-gate voltage	BV <sub>DGS</sub>
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

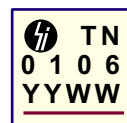
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* Distance of 1.6mm from case for 10 seconds.

### Pin Configurations



### Product Marking



YY = Year Sealed  
 WW = Week Sealed  
 \_\_\_\_\_ = "Green" Packaging

**TO-92 (N3)**

## Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup> (mA)	$I_D$ (pulsed) (A)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	$\theta_{jc}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{ja}$ ( $^\circ\text{C}/\text{W}$ )	$I_{DR}^\dagger$ (mA)	$I_{DRM}$ (A)
TO-92	350	2.0	1.0	125	170	350	2.0

**Notes:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

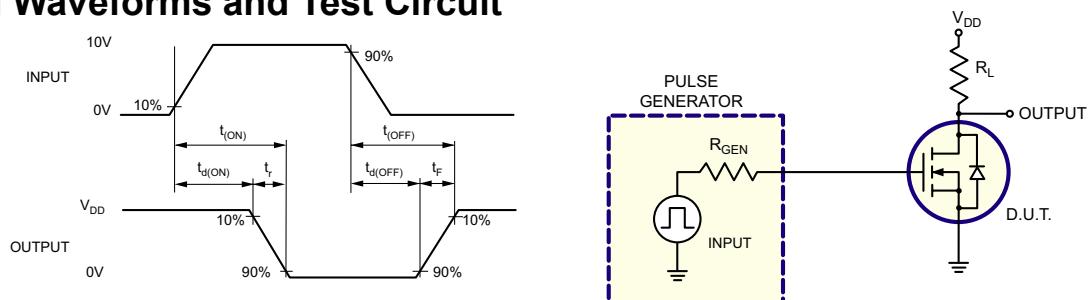
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	60	-	-	V	$V_{GS} = 0V, I_D = 1.0mA$
$V_{GS(th)}$	Gate threshold voltage	0.6	-	2.0	V	$V_{GS} = V_{DS}, I_D = 0.5mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.2	-5.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0mA$
$I_{GSS}$	Gate body leakage	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate voltage drain current	-	-	10	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
		-	-	500		$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	0.75	1.4	-	A	$V_{GS} = 5.0V, V_{DS} = 25V$
		2.0	3.4	-		$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	2.0	4.5	$\Omega$	$V_{GS} = 4.5V, I_D = 250mA$
		-	1.6	3.0		$V_{GS} = 10V, I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.6	1.1	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 500mA$
$G_{FS}$	Forward transductance	225	400	-	mmho	$V_{DS} = 25V, I_D = 500mA$
$C_{ISS}$	Input capacitance	-	50	60	pF	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	25	35		
$C_{RSS}$	Reverse transfer capacitance	-	4.0	8.0		
$t_{d(ON)}$	Turn-on delay time	-	2.0	5.0	ns	$V_{DD} = 25V,$ $I_D = 1.0A,$ $R_{GEN} = 25\Omega$
$t_r$	Rise time	-	3.0	5.0		
$t_{d(OFF)}$	Turn-off delay time	-	6.0	7.0		
$t_f$	Fall time	-	3.0	6.0		
$V_{SD}$	Diode forward voltage drop		1.0	1.5	V	$V_{GS} = 0V, I_{SD} = 500mA$
$t_{rr}$	Reverse recovery time	-	400	-	ns	$V_{GS} = 0V, I_{SD} = 500mA$

**Notes:**

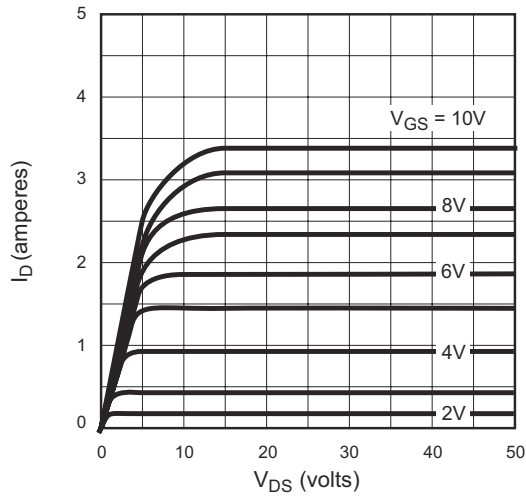
1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

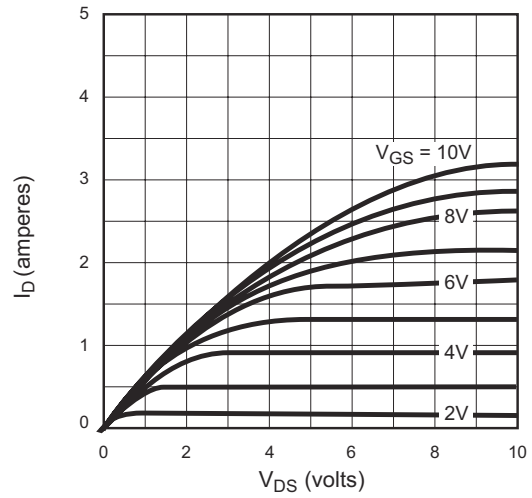


# Typical Performance Curves

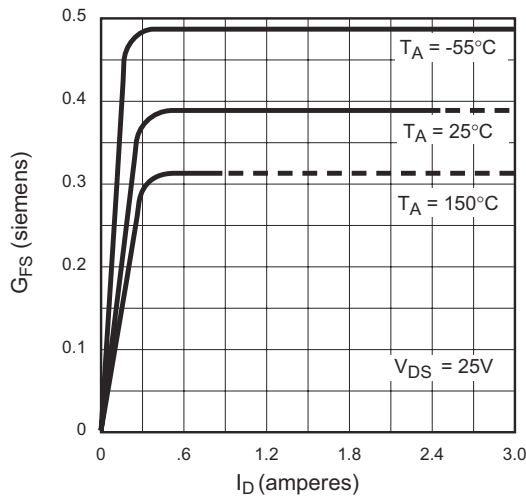
Output Characteristics



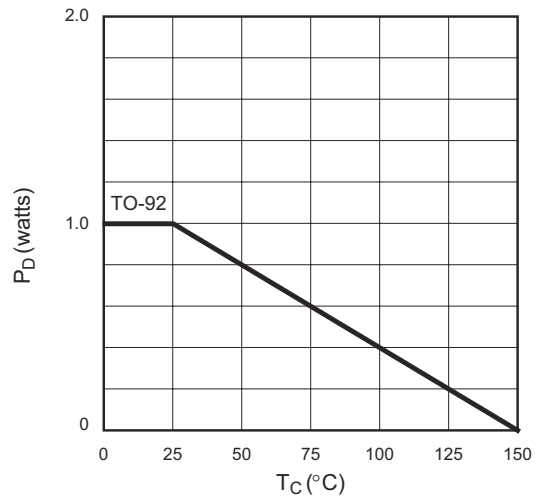
Saturation Characteristics



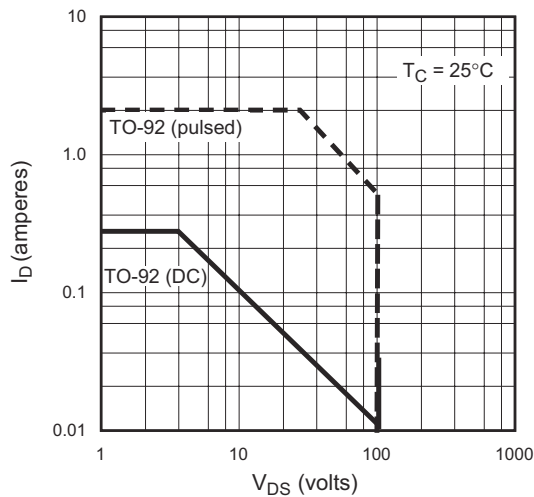
Transconductance vs. Drain Current



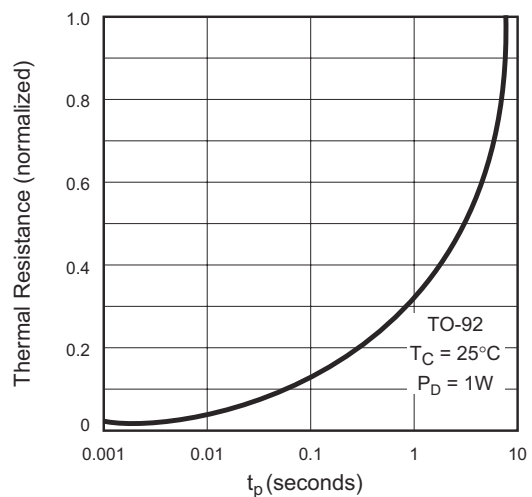
Power Dissipation vs. Case Temperature



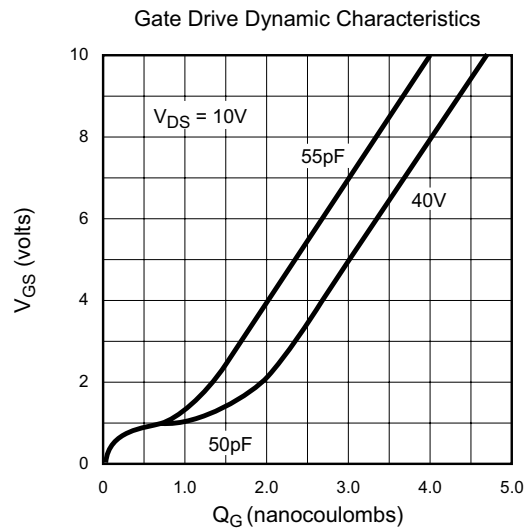
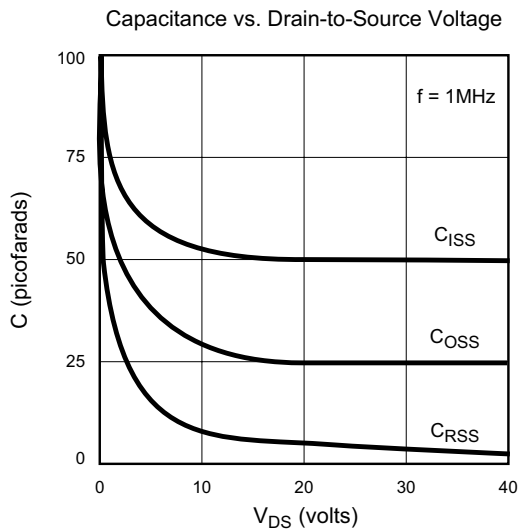
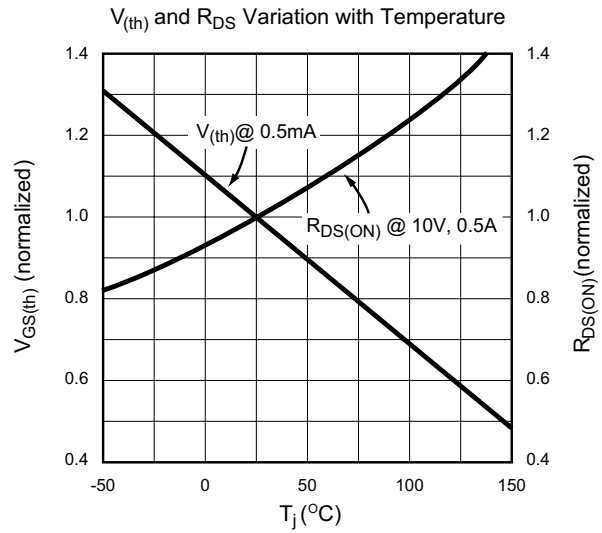
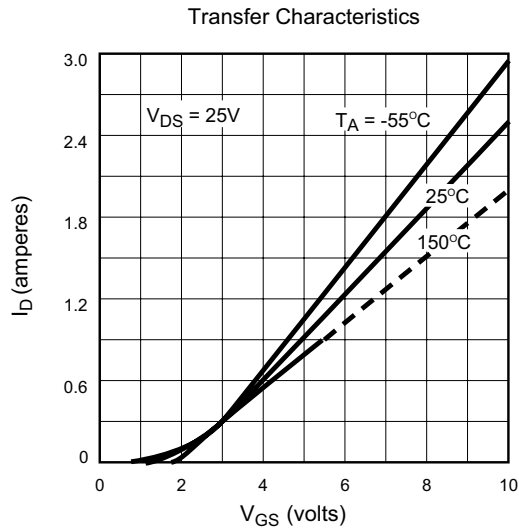
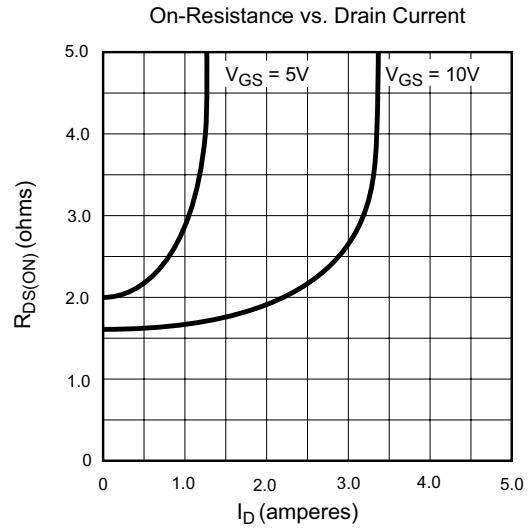
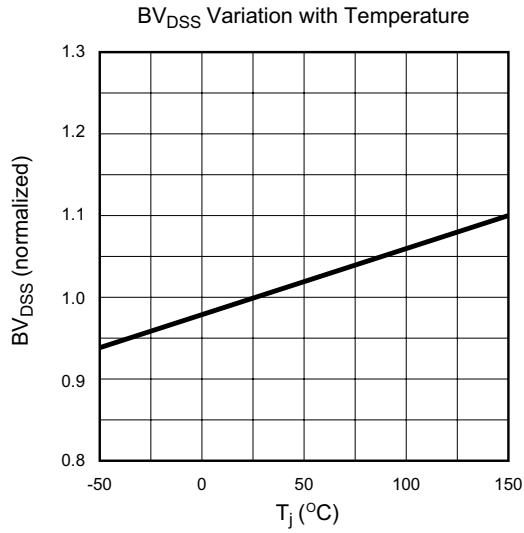
Maximum Rated Safe Operating Area



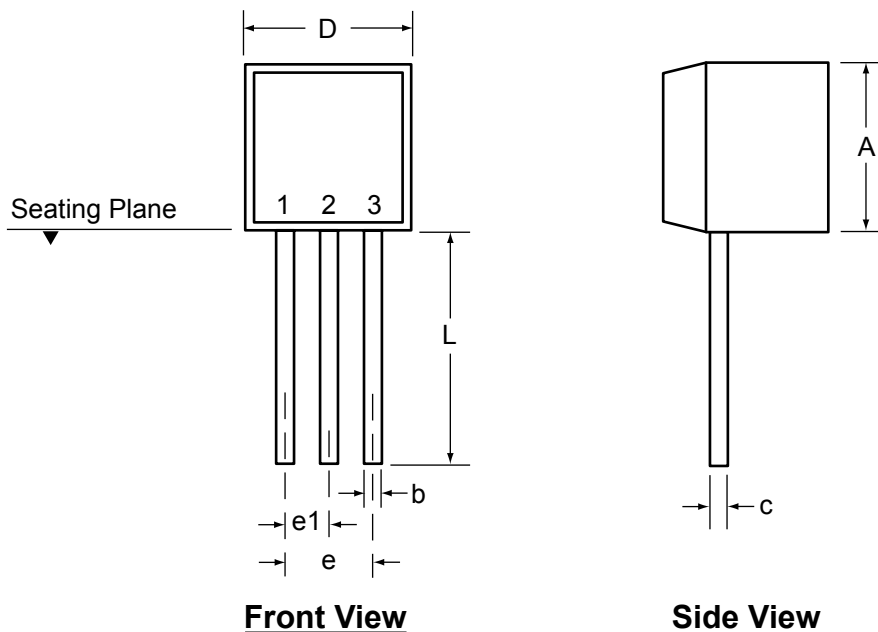
Thermal Response Characteristics



Typical Performance Curves (cont.)



### 3-Lead TO-92 Package Outline (N3)



Symbol	A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

† This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version D080408.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. website: <http://www.supertex.com>.