THCV213 and 214

LVDS SerDes transmitter and receiver

General Description

THCV213 and 214 are designed to support pixel data transmission between the Host and Display. The chipset can transmit 18bit data and 4bit control data through only a single differential cable at a pixel clock frequency from 5MHz to 40MHz.

By V-by-One® technologies, unique encoding scheme and proprietary CDR technique, a link synchronization is achieved without any external frequency reference such as a crystal oscillator. It drastically improves the cost and space of PCBs of a display system.

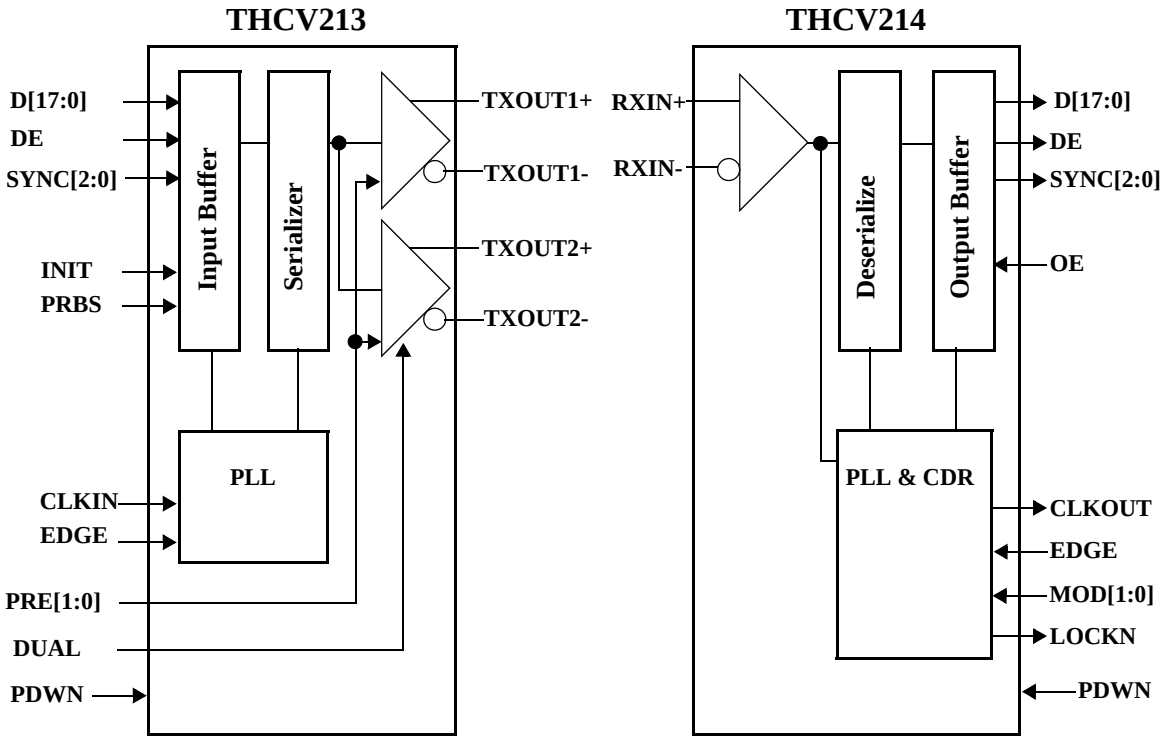
THCV213 transmitter converts input data into a single LVDS serial data stream with the embedded clock. It supports pre-emphasis for a long cable transmission. 214 receiver extracts the clock from the embedded clock and transforms the serial data stream back into the parallel data.

To confirm the reliability of the link, several functions are supported. THCV213 can transmit the SYNC pattern which expedites the link establishment. 214 has an indicator of its PLL status.

Features

- Transmit 18bit data and 4bit control data via a single differential cable
- Wide frequency range: 5MHz to 40MHz
- Support SYNC pattern and LOCK indicator
- Pre Emphasis mode
- Clock edge selectable
- Dual Display mode
- Power Down mode
- Low power single 3.3V CMOS design
- 48pin TQFP

Block Diagram

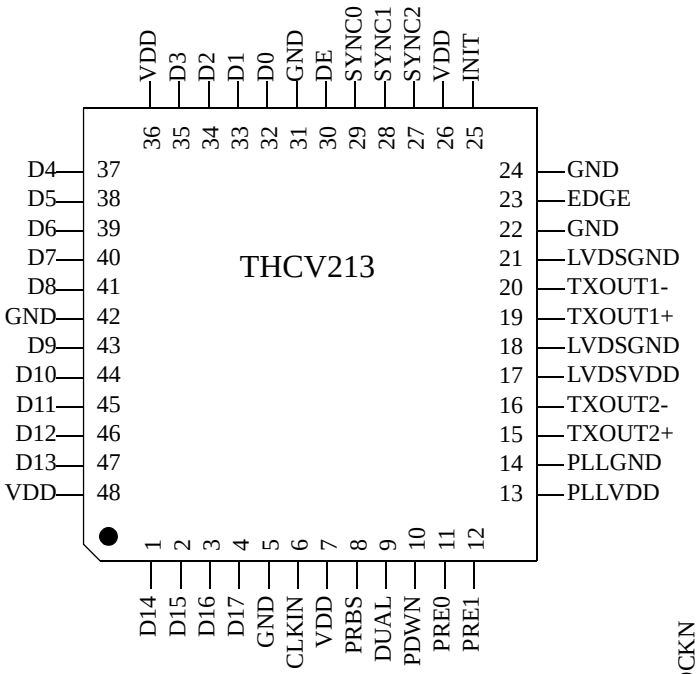


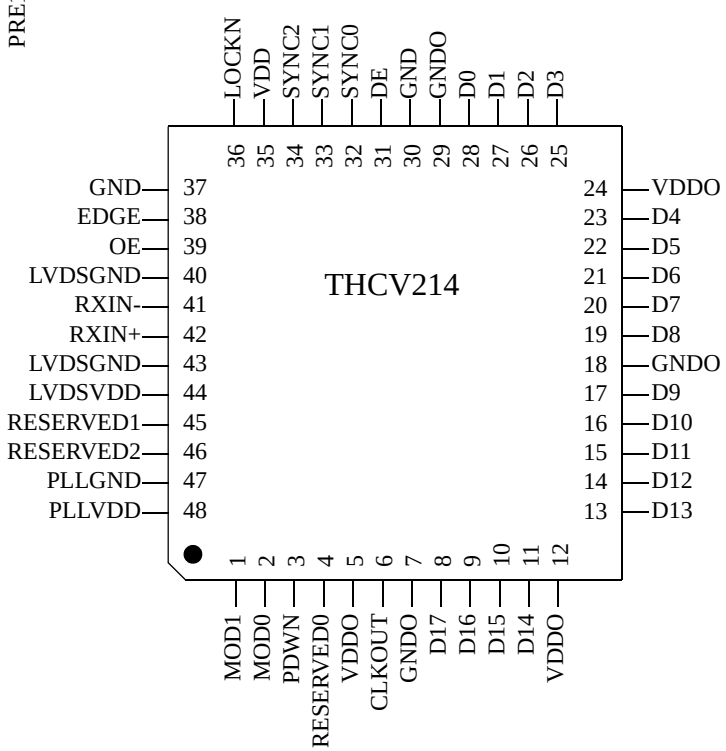
Package Information

PART	TEMP. RANGE	PACKAGE
THCV213-1TTN	0°C to 70°C	48pin TQFP
THCV214-1TTN	0°C to 70°C	48pin TQFP
THCV213-5TTN	-40°C to 85°C	48pin TQFP
THCV214-5TTN	-40°C to 85°C	48pin TQFP

Pin Out

48Pin TQFP





Pin Description

THCV213 Pin Description

Pin Name	Pin #	type	Description
TXOUT1-, TXOUT1+	20, 19	LVDSOUT	LVDS output.
TXOUT2-, TXOUT2+	16, 15	LVDSOUT	LVDS output for Dual Display mode. Identical to TXOUT1+/-. Hi-Z when Normal operation.
D0~D17	32~35, 37~41, 43~47, 1~4	IN	Data input. Active if input DE=High
SYNC2~SYNC0	27~29	IN	Sync input. Active if input DE =Low. Input sync data pulse must be wider than or equal to two input clock periods.
DE	30	IN	Data Enable (DE) input. Refer to Tabe2 for requirements.
CLKIN	6	IN	Clock input. 5 MHz to 40MHz.
PDWN	10	IN	H: Normal operation. L: Power Down, TXOUT1+/-, (TXOUT2+/-) are Hi-Z.
EDGE	23	IN	Input clock triggering edge select. H: Rise edge, L: Fall edge.
PRE0,PRE1	11, 12	IN	Select the level of pre-emphasis. PRE1 / PRE0 / Description L / L / w/o Pre-Emphasis L / H / w/ 25% Pre Emphasis H / L / w/ 50% Pre Emphasis H / H / w/ 100% Pre Emphasis
INIT	25	IN	H: Triggers SYNC pattern output fromTXOUT1+/- and (TXOUT2+/-), normally used in Shake Hand mode. L: Normal operation.
DUAL	9	IN	H: Dual Display mode Both TXOUT1-/+ and TXOUT2-/+ enabled. L: Normal operation Only TXOUT1-/+ enabled.

Pin Name	Pin #	type	Description
PRBS	8	IN	H: Internal test pattern generator is enabled. Pseud-Random Bit Sequence (PRBS) is generated and is fed into input data latches. Normally used for debug. L: Normal operation.
VDD	7,26,36,48	Power	Power supply pins for digital circuitry.
GND	5,22,24, 31,42,	Power	Ground pins for digital circuitry.
LVDSVDD	17	Power	Power supply pin for LVDS input.
LVDSGND	18, 21	Power	Ground pins for LVDS input.
PLLVDD	13	Power	Power supply pin for PLL circuitry.
PLLGND	14	Power	Ground pin for PLL circuitry.

214 Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>type</th><th>Description</th></tr>
<tr><td>RXIN-, RXIN+</td><td>41, 42</td><td>LVDSIN</td><td>LVDS input.</td></tr>
<tr><td>D17~D0</td><td>8~11,
13~17,
19~23,
25~28</td><td>OUT</td><td>Data outputs.</td></tr>
<tr><td>SYNC0~SYNC2</td><td>32~34</td><td>OUT</td><td>Sync output.</td></tr>
<tr><td>DE</td><td>31</td><td>OUT</td><td>Data Enable (DE) output.</td></tr>
<tr><td>CLKOUT</td><td>6</td><td>OUT</td><td>Clock output.</td></tr>
<tr><td>LOCKN</td><td>36</td><td>OUT</td><td>Lock detect output.
H: Unlock, L: Lock.
Can be used as an input signal detector, too.</td></tr>
<tr><td>PDWN</td><td>3</td><td>IN</td><td>H: Normal operation.
L: Power Down, all outputs except LOCKN and CLK-OUT are held low. Refer to Fig9 for details(Note1.)</td></tr>
<tr><td>EDGE</td><td>38</td><td>IN</td><td>Output clock triggering edge select.
H: Rise edge, L: Fall edge.</td></tr>
<tr><td>OE</td><td>39</td><td>IN</td><td>Output Enable.
(DE, SYNC0~SYNC2, D0~D17,CLKOUT)
H: Output disabled, all outputs are Hi-Z.
L: Output enabled. (Note1)</td></tr>
<tr><td>MOD1, MOD0</td><td>1, 2</td><td>IN</td><td>Select operation mode
Both must be tied to GND.
<table><tr><td>MOD0</td><td>MOD1</td><td></td></tr><tr><td>L</td><td>L</td><td>Normal Mode
Shake Hand Mode</td></tr><tr><td colspan="2">Others</td><td>Not Available</td></tr></table></td></tr>
<tr><td>RESERVED0</td><td>4</td><td>IN</td><td>Must be tied to GND.</td></tr>
<tr><td>RESERVED1</td><td>45</td><td>IN</td><td>Must be tied to LVDSGND.</td></tr>
<tr><td>RESERVED2</td><td>46</td><td>IN</td><td>Must be tied to LVDSGND.</td></tr>
<tr><td>VDD</td><td>35</td><td>Power</td><td>Power supply pin for digital circuitry.</td></tr>
<tr><td>GND</td><td>30,37</td><td>Power</td><td>Ground pins for digital circuitry.</td></tr>
<tr><td>LVDSVDD</td><td>44</td><td>Power</td><td>Power supply pin for LVDS input.</td></tr>
<tr><td>LVDSGND</td><td>40,43</td><td>Power</td><td>Ground pins for LVDS input.</td></tr>
<tr><td>PLLVDD</td><td>48</td><td>Power</td><td>Power supply pin for PLL circuitry.</td></tr>
<tr><td>PLLGND</td><td>47</td><td>Power</td><td>Ground pin for PLL circuitry.</td></tr>
<tr><td>VDDO</td><td>5,12,24</td><td>Power</td><td>Power supply pins for TTL output.</td></tr>
<tr><td>GNDO</td><td>7,18,29</td><td>Power</td><td>Ground pins for TTL output.</td></tr>
</table>

Note1: The state of outputs determined by the combination of OE and PDWN is as follow

Table 1 Output State determined by OE and PDWN

OE	PDWN	Output State
L	H	Normal Operation.
L	L	All outputs except LOCKN and CLKOUT are held low. LOCKN is held high while CLKOUT is driven high when EDGE input is high and is driven low when EDGE input is low.
H	H	All outputs are Hi-Z.
H	L	All outputs are Hi-Z.

Table 2 Requirements for DE input

Operation Mode	DE = High	DE = Low
Normal	Min. $2t_{TCIP}$ (See Fig5 for t_{TCIP}) Max. 80 μsec	Min. 50 t_{TCIP} (See Fig5 for t_{TCIP})
ShakeHand	Min. $2t_{TCIP}$ (See Fig5 for t_{TCIP})	Min. $2t_{TCIP}$ (See Fig5 for t_{TCIP})

Absolute Maximum Ratings

Supply Voltage (V_{DD})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{DD} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{DD} + 0.3V)
LVDS Receiver Input Voltage	-0.3V ~ (V_{DD} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Reflow Peak Temperature / Time	+260°C / 10sec.
Maximum Power Dissipation @+25°C	1.9W

Operation Condition

Parameter	**Consumer**			**Industrial**			
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**
All Supply Voltage	3.0	3.3	3.6	3.0	3.3	3.6	V
Operating Ambient Temperature	0		70	-40		85	°C

Electrical Characteristics

CMOS/TTL DC Specifications

Transmitter: V_{DD}=VDD=LVDSVDD=PLLVDD, Receiver: V_{DD}=VDD=VDDO=LVDSVDD=PLLVDD

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	V_{DD}= 3.0V ~ 3.6V I_{OH} = -4mA	2.4			V
V_{OL}	Low Level Output Voltage	V_{DD} = 3.0V ~ 3.6V I_{OL} = 4mA			0.4	V
I_{IIL}	Input Leak Current	$0V \le V_{IN} \le V_{CC}$			±10	μA

THCV213 DC Specifications

V_{DD}=VDD=LVDSVDD=PLLVDD

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω, PRE<1:0>=L,L	250	350	450	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω, PRE<1:0>=L,L			35	mV
VOC	Common Mode Voltage	RL=100Ω, PRE<1:0>=L,L	1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states	RL=100Ω, PRE<1:0>=L,L			35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=0V,RL=100Ω			24	mA
I_{OZ}	Output TRI-STATE Current	PDWN=L, V_{OUT}=0V to V_{DD}			±10	μA

214 DC Specifications

V_{DD}=VDD=VDDO=LVDSVDD=PLLVDD

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{TH}	Differential Input High Threshold	VIC = +1.2V			100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
I_{ILD}	Differential Input Leakage Current	V_{IN} = +2.4V/0V V_{DD} = 3.6V			±10	μA

THCV213 Supply Current

V_{DD}=VDD=LVDSVDD=PLLVDD

Symbol	Parameter	Condition	Typ.	Max.	Units
I_{TCCW1}	Transmitter Supply Current (Worst Case Pattern) (Fig. 1)	Normal Operation f_{CLKIN} =40MHz V_{DD}=3.3V		60	mA
I_{TCCW2}	Transmitter Supply Current (Worst Case Pattern) (Fig. 1)	Dual Display Mode f_{CLKIN} =40MHz V_{DD}=3.3V		90	mA
I_{TCCS}	Transmitter Power Down Supply Current	PDWN = L		10	μA

214 Supply Current

V_{DD}=VDD=VDDO=LVDSVDD=PLLVDD

Symbol	Parameter	Condition	Typ.	Max.	Units
I_{RCCW}	Receiver Supply Current (Worst Case Pattern) (Fig. 1)	f_{CLKOUT} = 40MHz V_{DD}=3.3V CL=8pF (Fig. 4)		70	mA
I_{RCCS}	Receiver Power Down Supply Current	PDWN = L		10	μA

Worst Case Pattern

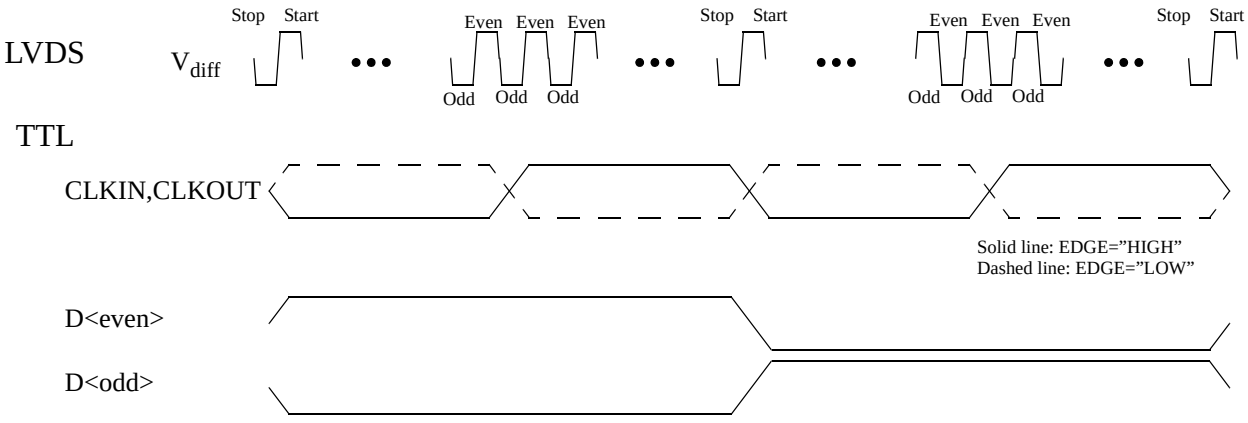


Fig. 1 Test Pattern

Switching Characteristics

THCV213 Switching Characteristics

V_{DD}=VDD=LVDSVDD=PLLVDD

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{TCIP}	CLKIN Period (Fig. 5)	25		200	ns
t_{TCP}	TXOUT Period (Fig. 5)		t_{TCIP}		ns
t_{TCH}	CLKIN High Time (Fig. 5)	$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TCL}	CLKIN Low Time (Fig. 5)	$0.35t_{TCIP}$	$0.5t_{TCIP}$	$0.65t_{TCIP}$	ns
t_{TS}	TTL Data Setup to CLKIN (Fig. 5)	5			ns
t_{TH}	TTL Data Hold from CKLIN (Fig. 5)	0			ns
t_{TO}	CLK IN to TXOUT+/- Delay (Fig. 5)	$3\frac{17}{21}t_{TCIP}$	.	$3\frac{17}{21}t_{TCIP}+7$	ns
t_{TLH}	TTL Input Low to High Transition Time (Fig. 2)		3.0	5.0	ns
t_{THL}	TTL Input High to Low Transition Time (Fig. 2)		3.0	5.0	ns
t_{TLVT}	LVDS Differential Output Transition Time (Fig. 3)		0.6	1.5	ns
t_{TPLL}	Phase Lock Loop Set Time (Fig. 7)			10.0	ms
t_{THZ}	PDWN Low to Output Hi-Z Set Delay (Fig. 7)		3.6		ns
t_{TSYNC1}	INIT High to Sync Pattern Output Delay (Fig. 8)		$\frac{17}{21}t_{TCIP}+3$		ns
t_{TSYNC2}	INIT Low to Normal Pattern Output Delay (Fig. 8)		$1026\frac{17}{21}t_{TCIP}+3$		ns

214 Switching Characteristics

V_{DD}=VDD=VDDO=LVDSVDD=PLLVDD

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{RCIP}	RXIN Period (Fig. 6)	25		200	ns
t_{RCP}	CLKOUT Period (Fig. 6)		t_{RCIP}		ns
t_{RCH}	CLKOUT High Time (Fig. 6)		$\frac{t_{RCP}}{2}$		ns
t_{RCL}	CKLOUT Low Time (Fig. 6)		$\frac{t_{RCP}}{2}$		ns
t_{RS}	TTL Data Setup to CLKOUT (Fig. 6)	$0.3t_{RCP}$			ns
t_{RH}	TTL Data Hold from CKLOUT (Fig. 6)	$0.3t_{RCP}$			ns
t_{RO}	RXIN+/- to CLKOUT Delay (Fig. 6)	$4\frac{13.5}{21}t_{RCP}$		$4\frac{13.5}{21}t_{RCP} + 7$	ns
t_{RLH}	TTL Output Low to High Transition Time (Fig. 4)		3.0	5.0	ns
t_{RHL}	TTL Output High to Low Transition Time (Fig. 4)		3.0	5.0	ns
t_{RPLL1}	Phase Lock Loop Set (Fig. 9)			10.0	ms
t_{RPDD}	Power-Down Delay (Fig. 9)		9		ns
t_{RDO}	LOCKN transition to TTL Data Output Delay (Fig. 9)		2		clock cycles
t_{RCOL}	Beginning of Clock Output to LOCKN transition Time(Fig. 9)	10			clock cycles
t_{RLCS}	LOCKN transition to Stop of Clock Output Time(Fig. 9)	3			clock cycles
t_{RPLL2}	Phase Lock Loop Set (Fig. 10)			10.0	ms
t_{RLN}	Data Stop to LOCKN Transition Delay (Fig. 10)		7		ns

AC Timing Diagram and Test Circuits

Transmitter Input/Output Switching Characteristics

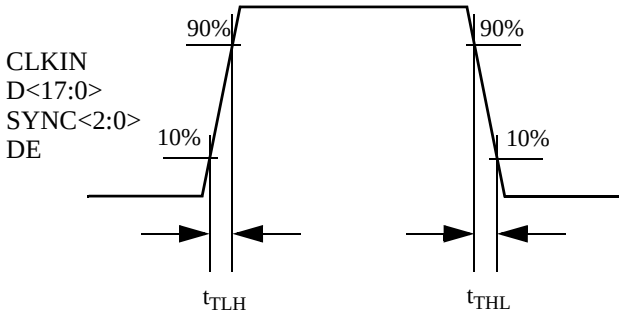


Fig. 2 CMOS/TTL Inputs Transition Time

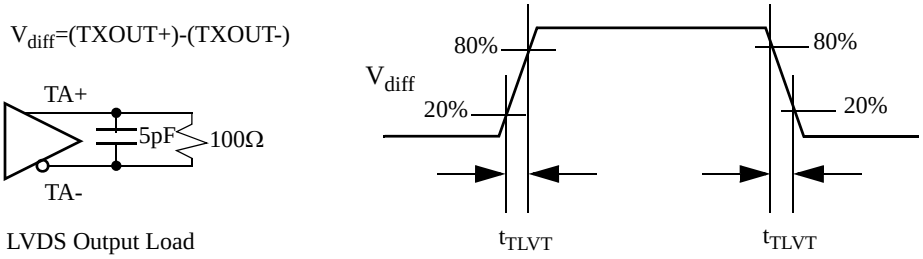


Fig. 3 LVDS Outputs Transition Time

Receiver Output Switching Characteristics

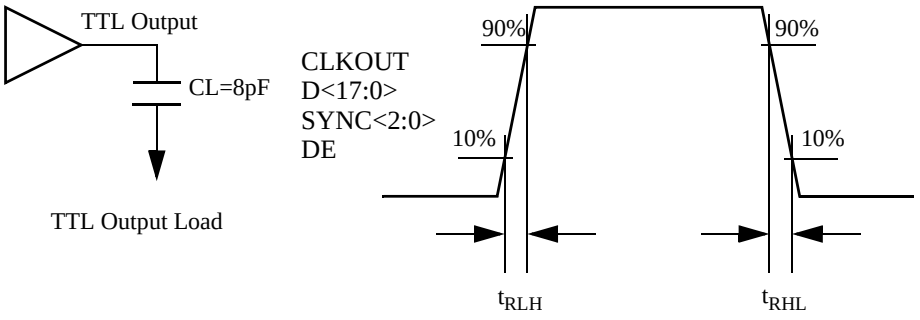


Fig. 4 CMOS/TTL Outputs Load and Transition Time

AC Timing Diagram and Test Circuits (Continued)

Transmitter Output timing

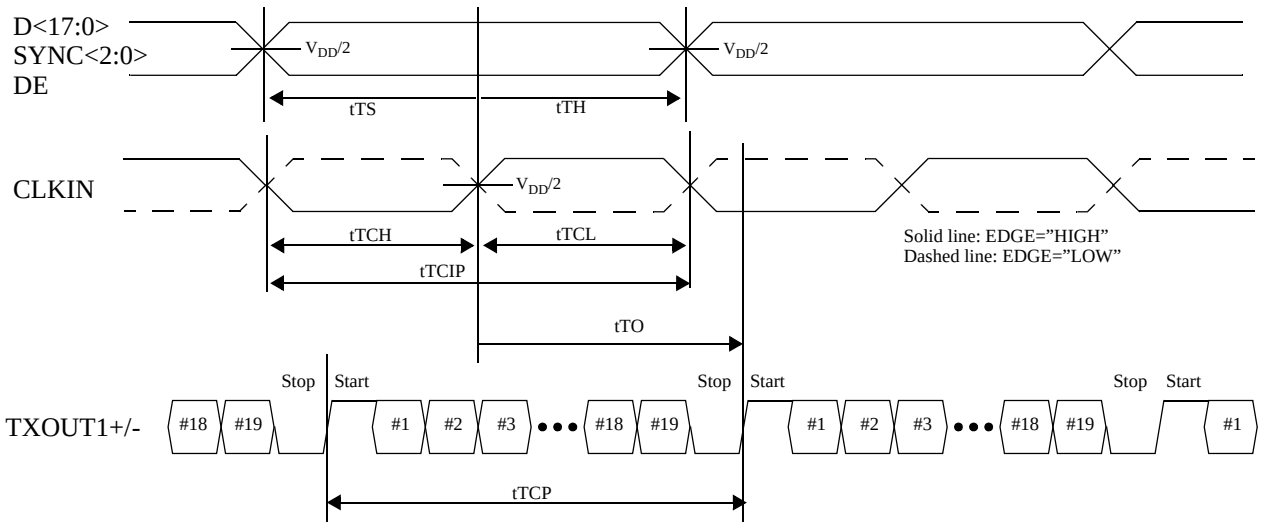


Fig. 5 Transmitter Output Timing

Receiver Output timing

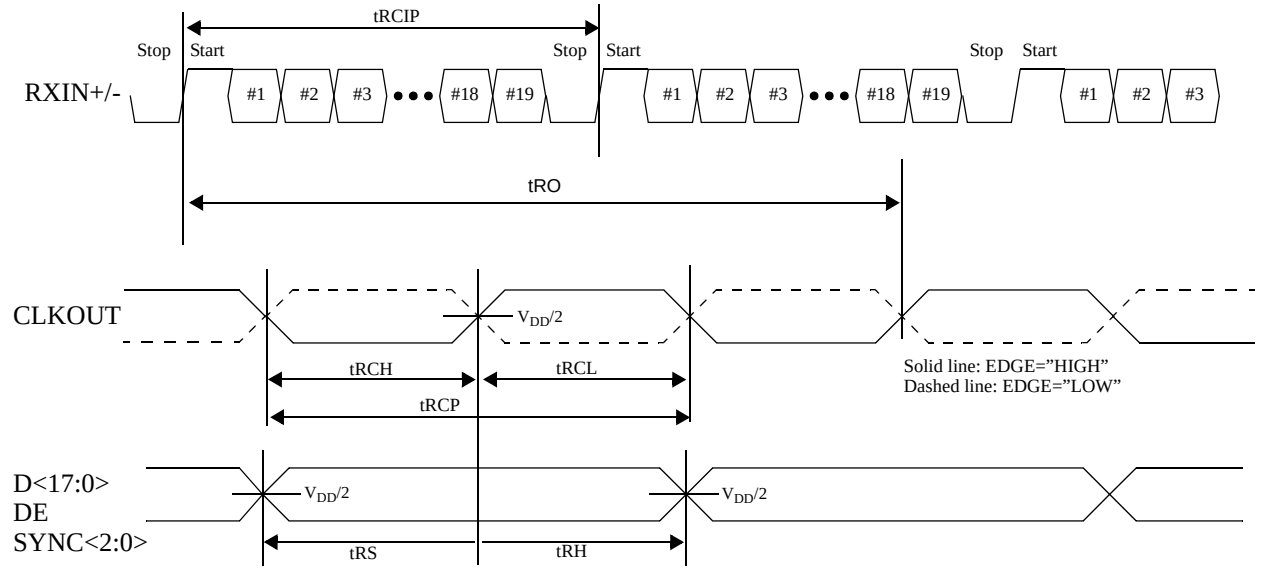


Fig. 6 Receiver Output Timing

AC Timing Diagram and Test Circuits (Continued)

Transmitter Start-up and Power-down Sequence

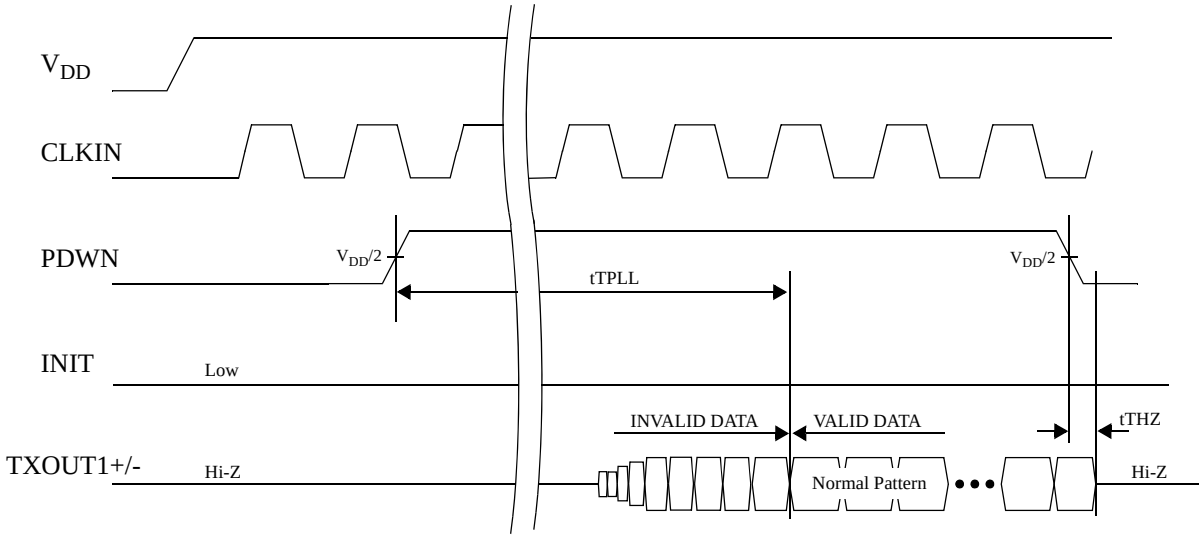


Fig. 7 Transmitter Start-up and Power-down Sequence

Transmitter Lock Recovery Sequence

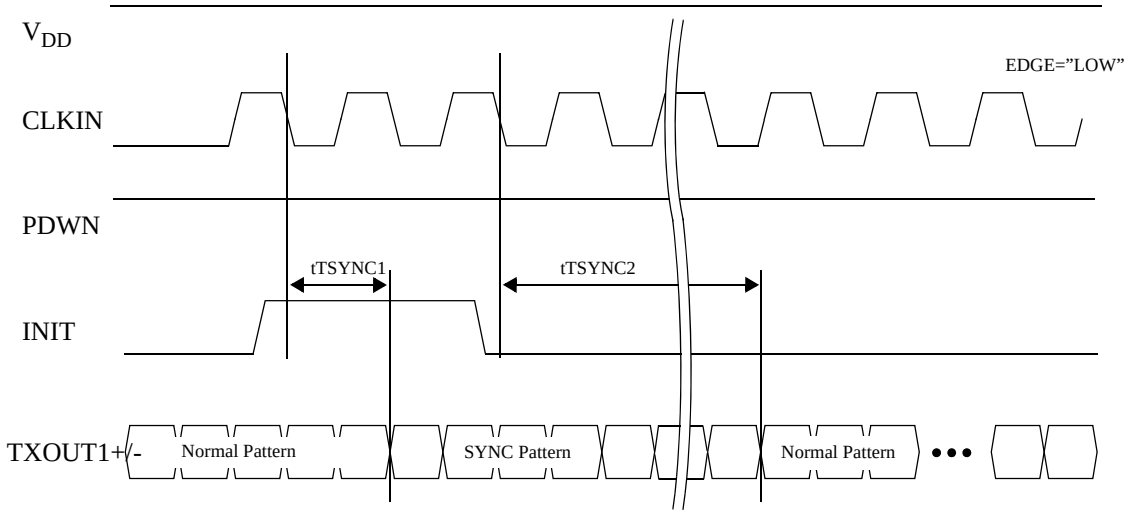


Fig. 8 Transmitter Lock Recovery Sequence

AC Timing Diagram and Test Circuits (Continued)

Receiver Start-up and Power-down Sequence

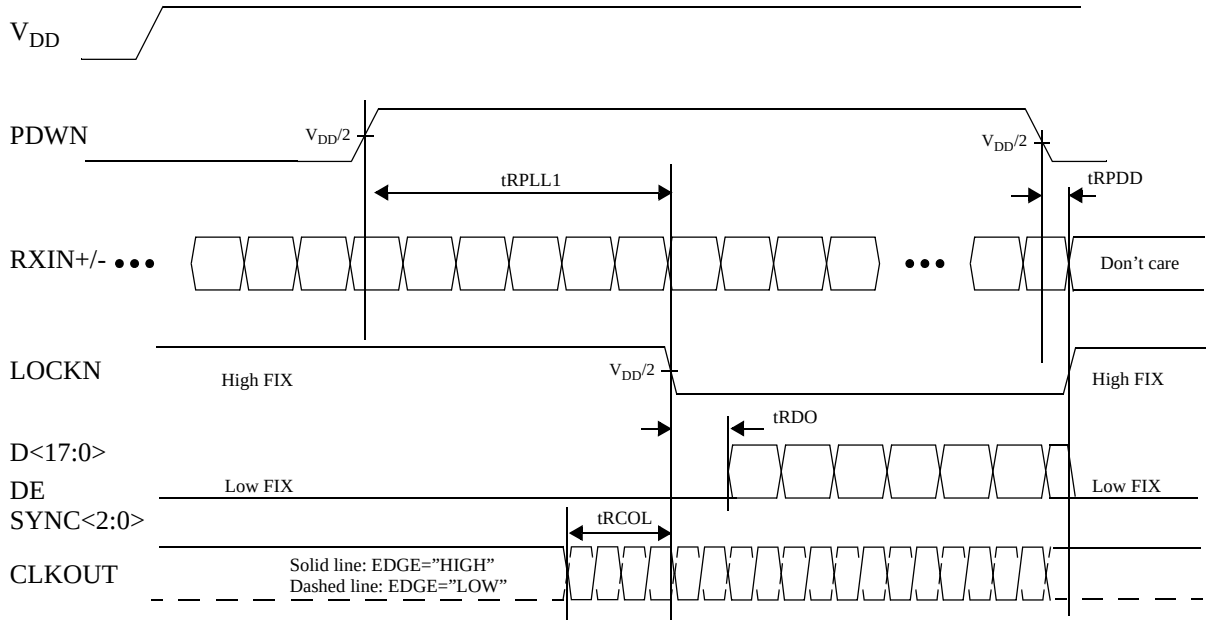


Fig. 9 Receiver Start-up and Power-down Sequence

Receiver Lock Recovery Sequence

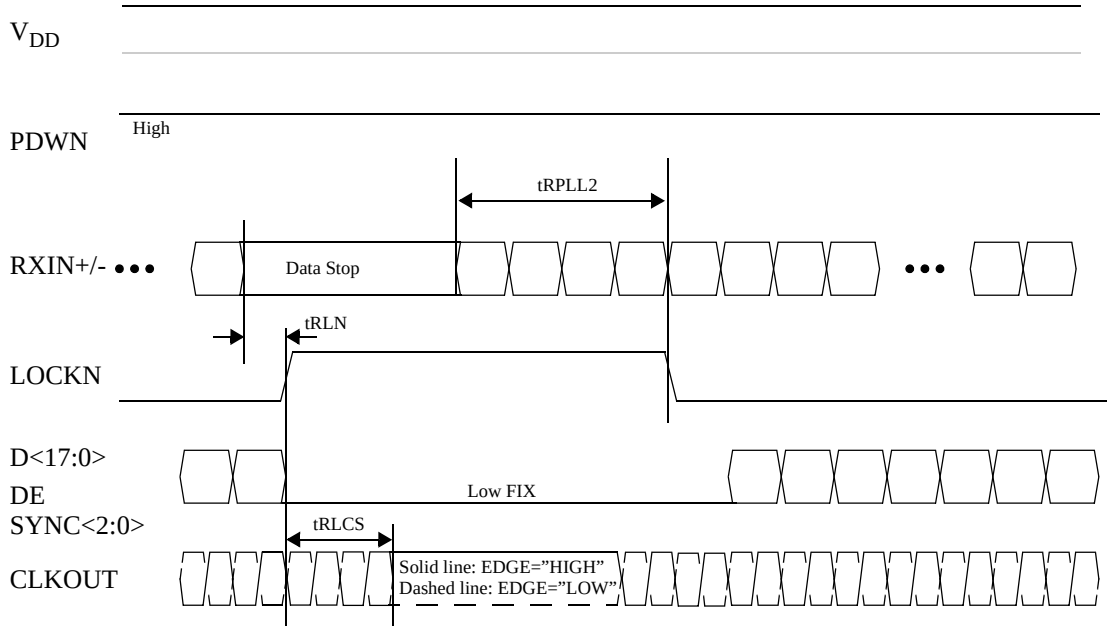


Fig. 10 Receiver Lock Recovery Sequence

Detailed Description

With V-by-One®'s proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, THCV213 and THCV214 enable transmission of 18bit video signals (D17 to D0) and 4 bit control signals (SYNC2 to SYNC0, and DE) by a single differential pair cable with minimal external components. THCV214, the receiver, can seamlessly operate for a wide range of a parallel clock frequency of 5MHz to 40MHz, detecting the frequency of an incoming data stream, and recovering both the clock and data by itself. It does not need any external frequency reference, such as a crystal oscillator.

THCV213 serializes video signals and control signals separately, depending on the polarity of Data Enable (DE) input. DE is a signal which indicates whether video or control signals are active. When DE input is high, it serializes D17 to D0 inputs into a single differential data stream. And it transmits serialized control signals (SYNC2 to SYNC0) when DE input is low.

THCV214 automatically extracts the clock from the incoming data stream and converts the serial data into 18 bit parallel data with DE being high or three control signals with DE being low, recognizing which type of serial data is being sent by the transmitter.

Operation Mode

In order to accommodate various types of data format or to expedite the link establishment between the transmitter and receiver, THCV214 has two modes of operation, namely Normal mode and Shake Hand mode.

Normal Mode

The Normal mode operation is the one described above in "Detailed Description." This mode fully utilizes the chipset's capability, enabling the transmission of 18 video and 4bit control signals. It is required to have DE signal which indicates whether video or control signals are active.

Shake Hand Mode

This mode requires an extra wire connecting THCV214's LOCKN and THCV213's INIT pin. This wire does not need to be impedance controlled one. While the link is not being established between the transmitter and receiver, the receiver's LOCKN is driven low, telling the transmitter to send a special set of data pattern which eases connection between the two. The chipset automatically enters the Shake Hand mode, once THCV214's LOCKN pin and THCV213's INIT pin are connected together.

If there is no DE signal, THCV213/214 can still work in the Shake Hand mode with the transmitter's DE input tied high. In this case, the amount of data transmission reduces to 18 bit digital signals (D17 to D0.)

DE Requirement

There are some requirements for DE signal if the chipset is to be used in the Normal mode as described in Table 2.

DE Requirements for Normal Mode

The length of DE being low is at least 50 clock cycle long. The maximum time of DE being high is 80us, the minimum of DE=L is 2 clock cycles.

THCV213 Power Down (PDWN)

Setting the PDWN pin low results in THCV213 in the Power Down mode. All the internal circuitry turns off and the TXOUT+/- outputs turn to Hi-Z. Refer to Fig. 7

THCV213 EDGE

The polarity of the EDGE pin selects which edge (rising or falling) of the input clock by which the input data are latched in. When EDGE is set high, the transmitter uses the rising edge of the input clock to take in the input data. When EDGE is low, it takes in the data at the falling edge of the clock. Select its polarity so that the transmitter latches in the data with better setup/hold time margin.

THCV213 Pre-Emphasis (PRE1,0)

Pre-emphasis can equalize severe signal degradation caused by long distance or high-speed transmission. Two pins, PRE1 and PRE0, select the strength of pre-emphasis.

PRE1	PRE0	Description
L	L	w/o Pre-Emphasis
L	H	w/ 25% Pre Emphasis
H	L	w/ 50% Pre Emphasis
H	H	w/ 100% Pre Emphasis

THCV213 INIT

Driving the INIT pin high forces the transmitter to send a special set of pattern called SYNC pattern, which makes it easier for the receiver to recover the clock and data. This function is normally used in the Shake Hand mode with a wire connecting the transmitter INIT pin and the receiver LOCKN pin.

It can also be used to expedite the link establishment in the Normal mode by driving the INIT pin high at power up, forcing the transmitter to output the SYNC pattern for a certain amount of time in order to train the receiver.

THCV213 Dual Display Mode (DUAL)

THCV213 has two high speed output buffers so that it can be used in an application where a video source wants to send the same data to two displays. The DUAL pin activates the Dual Display mode.

THCV213 PRBS

Setting the PRBS pin high enables the internal test pattern generator. It generates Pseudo-Random Bit Sequence of 2^{23}-1.

The generated PRBS is fed into input data latches, formatted as VGA video like data, encoded and serialized into TXOUT output.

This function is normally to be used for analyzing the signal integrity of the transmission channel including PCB traces, connectors, and cables.

THCV214 Lock/Input Detect (LOCKN)

When the PLL of THCV214 has locked to the incoming data stream, it drives LOCKN low. And then TTL/CMOS outputs become valid. This LOCKN signal can also be used as an indicator of whether the incoming data is valid or not.

This pin is to be connected to the transmitter INIT pin with a cable in the Shake Hand mode.

THCV214 Power Down (PDWN)

Setting the PDWN pin low results in THCV214 in the Power Down mode. All the internal circuitry and input buffers turn off, and all outputs except LOCKN and CLKOUT are held low. The LOCKN pin is driven high when in the Power Down mode. The CLKOUT is fixed one way or the other depending on the EDGE input. Refer to Fig. 9.

THCV214 EDGE

The polarity of the EDGE pin selects which edge (rising or falling) of the output clock by which the output data are latched out. When EDGE is set high, the receiver uses the falling edge of the output clock to put out the data so that the next-stage chip can use the rising edge of the clock to latch in the data with the maximum setup/hold time margin, and vice versa. Select its polarity according to the next-stage chip input characteristics.

THCV214 Output Enable (OE)

The OE pin can disable TTL/CMOS outputs and place them in Hi-Z. Thus THCV214's TTL/CMOS outputs can be bused so that the receiver can be used in an application where there are multiple video sources and one display.

THCV214 MOD1,0

Both MOD1 and MOD0 must be tied to GND. The receiver enters into an appropriate operation mode by itself.

Cables and Connectors

In a system with high speed digital signals, a special care must be taken to avoid loss and degradation of the signals due to limited bandwidth and impedance mismatch along the transmission line. Characteristic impedance of PCB traces, cables, and connectors must be tightly controlled.

Use cables that have a differential characteristic impedance of 100Ω. Shielded twisted pair cables are recommended for increasing noise immunity and lowering EMI.

Connectors are recommended that cause minimum discontinuities in terms of characteristic impedance and geometry of the transmission path.

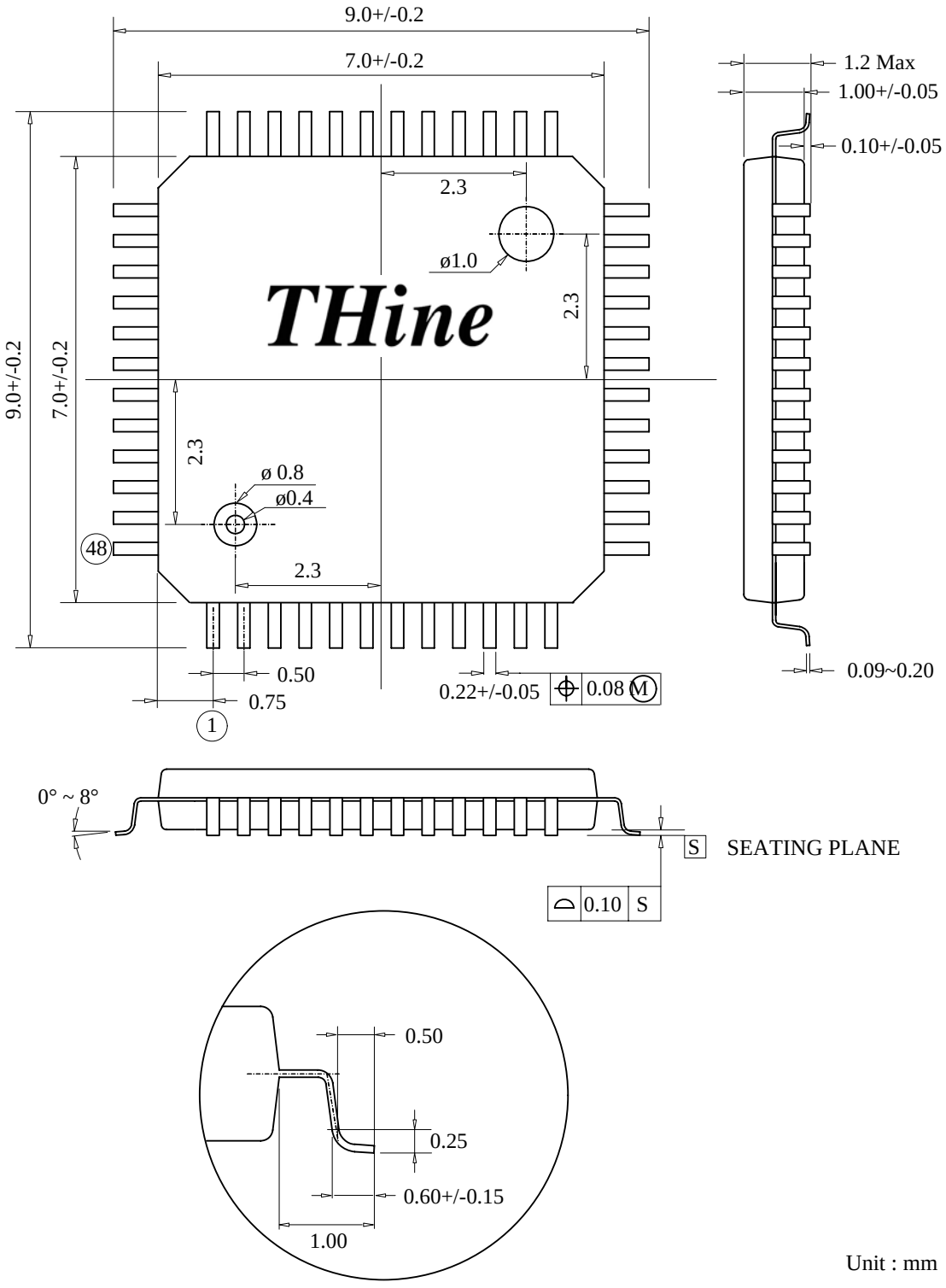
PCB Layout Considerations

Use a four-layer PCB with signal, ground, power, and signal assigned for each layer. PCB traces for high-speed signals (TXOUT, RXIN) must be microstrip lines with a differential impedance of 100Ω. Route differential signal traces symmetrically. Avoid right angle turns of the high speed traces because they usually cause impedance discontinuity.

Place a 100 Ω termination resistor between RXIN+ and RXIN- as close to the receiver as possible to reduce reflection.

Separate all the power domains in order to avoid unwanted noise coupling between noisy digital and sensitive analog domains. Use high frequency ceramic capacitors of 10nF or 0.1μF as bypass capacitors between power and ground pins. Place them as close to each power pin as possible. A 4.7μF capacitor in parallel with the smaller capacitor to PLLVDD is recommended for the receiver.

Package



Unit : mm

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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