S5933
32-Bit PCI MatchMaker

February 12, 1997 Revised October 1998

FEATURES

- **PCI 2.1 Compliant Master/Slave Device**
- **Full 132 Mbytes/sec Transfer Rate**
- **PCI Bus Operation DC to 33 Mhz**
- **8/16/32 Bit Add-On User Bus**
- **Four Definable Pass-Thru Regions**
- **Two 32 Byte FIFOs**
- **Sync/Async Add-On Bus Operation**
- **Mail Box Registers w/Byte Level Status**
- **Direct Mail Box Data Strobe/Interrupts**
- **Big/Little Endian Conversions**
- **Direct PCI & Add-On Interrupt Pins**
- **Boot Loading from nvRAM or Byte Wide**
- **Optional Expansion BIOS/POST Code**
- **160 Pin PQFP**

APPLICATIONS

- **High Speed Networking**
- **Digital Video Applications**
- **I/O Communications Ports**
- **High Speed Data Input/Output**
- **Multimedia Communications**
- **Memory Interfaces**
- **High Speed Data Acquisition**
- **Data Encryption/Decryption**
- **Intel i960 Interface**
- **General Purpose PCI Interfacing**

DESCRIPTION

The PCI Local bus concept was developed to break the PC data I/O bottleneck and clearly opens the door to increasing system speed and expansion capabilities. The PCI Local bus moves high speed peripherals from the I/O bus and places them closer to the system's processor bus, providing faster data transfer between the processor and peripherals. The PCI Local bus also addresses the industry's need for a standard that is not directly dependent on the speed, size and type of processor bus. It represents the first microprocessor independent bus offering performance more than adequate for the most demanding applications, such as full-motion video.

Applied Micro Circuits Corporation (AMCC), the premier supplier of single chip solutions, has developed and produced the S5933 to solve the problem of interfacing applications to the PCI Local bus. The S5933, or 'Matchmaker', is a powerful and flexible PCI controller supporting several levels of interface sophistication. At the lowest level, it can serve simply as a PCI bus Target with modest transfer requirements. For high-performance applications, the S5933 can become a Bus Master to attain the PCI Local bus peak transfer capability of 132 MBytes/sec.

The MatchMaker is an off-the-shelf, low-cost, standard product, which is PCI 2.1 compliant. And, since AMCC is a member of the PCI Special Interest Group, the S5933 has been tested in "compliance workshops" along with other manufacturer's PCI systems, chip sets and BIOSs. This removes the burden of compliance testing from the designer and thus significantly reduces development time. Utilizing the S5933 allows the designer to focus on the actual application, not debugging the PCI interface.

The MatchMaker allows special direct data accessing between the PCI bus and the user application through implementation of four definable Pass-Thru data channels. Each data channel is implemented by defining a Host memory segment size and 8/16/32-bit user bus width. The addition of two 32 byte FIFOs, also used in S5933 Bus Mastering applications, provides further versatility to data transfer capabilities. FIFO DMA transfers are supported using Address and Transfer Count Registers. Four 32-bit Mailbox Registers coupled with a Status Register and extensive interrupt capabilities provide flexible user command or message transfers between the two buses. In addition, the S5933 also allows use of an external serial, or byte-wide non-volatile memory to perform any pre-boot initialization requirements and to provide custom expansion BIOS or POST code capability.

AMCC
Applied Micro Circuits Corporation

6290 Sequence Drive, San Diego, California 92121-4358
800-755-2622 Fax: 619-450-9885
http://www.amcc.com

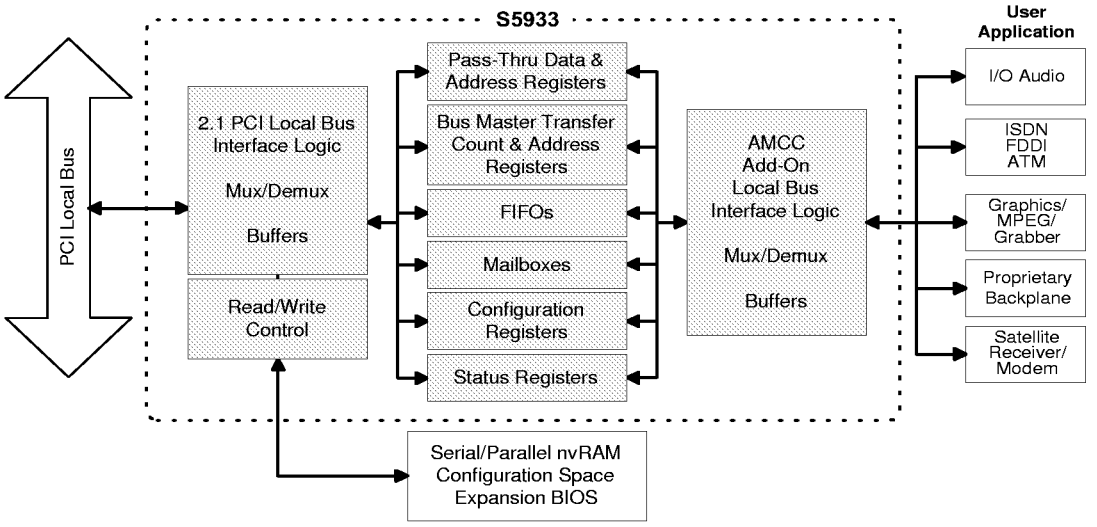


Figure 1

S5933 Architecture

The block diagram in figure 1 above shows the major functional elements within the S5933. The S5933 provides three physical bus interfaces: the PCI Local bus, the user local bus referred to as the Add-On Local bus and the optional serial and byte-wide non-volatile memory buses. Data movement between buses can take place through mailbox registers or the FIFO data channel, or a user can define and enable one or more of the four Pass-Thru data channels. S5933 Bus Master or DMA data transfers to and from the PCI Local bus are performed through the FIFO data channel under either Host or Add-On software control or Add-On hardware control using dedicated S5933 signal pins.

The S5933 signal pins are shown in Figure 2 right. The PCI Local Bus signals are detailed on the left side; Add-On Local Bus signal are detailed on the right side. All additional S5933 device control signals are shown on the lower right side.

The S5933 supports a two wire serial nvRAM bus and a byte-wide EPROM/FLASH bus. This allows the designer to customize the S5933 configuration by loading setup information on system power-up.

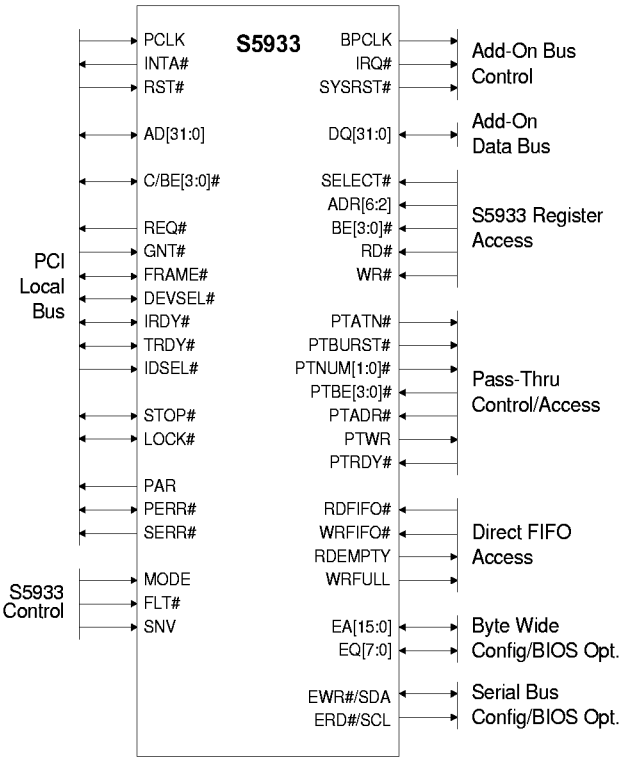


Figure 2

S5933 Register Architecture

Control and configuration of the Add-On Local bus, and the MatchMaker itself, is performed through three primary groups of registers. These groups consist of PCI Configuration Registers, PCI Operation Registers and Add-On Operation Registers. All these registers are user configurable through their associated bus or from an external non-volatile memory device. This section will provide a brief overview of each of these register groups and the optional non-volatile interface.

PCI Configuration Registers

All PCI compliant devices are required to provide a group of Configuration Registers for the host system. These registers are polled during power up initialization and contain specific device and add-in card product information including Vendor ID, Device ID, Revision and the amount of memory required for product operation. The S5933 can either load these registers with default values or initialize them from an external non-volatile memory area called 'Configuration Space'. The S5933 can accommodate a total of 256 bytes of external memory for this purpose. The first 64 bytes is reserved for user defined configuration data which is loaded into the PCI Configuration Registers during power-up initialization. The remaining 192 bytes may be used to implement an Expansion BIOS or contain add-in card POST code. Table 1 shows all the S5933 PCI Configuration Registers.

Byte 3	Byte 2	Byte 1	Byte 0	Address
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
Class Code			Revision ID	08h
Built-In Self Test	Header Type	Latency Timer	CacheLine Size	0Ch
Base Address Register 0				10h
Base Address Register 1				14h
Base Address Register 2				18h
Base Address Register 3				1Ch
Base Address Register 4				20h
Base Address Register 5				24h
Reserved Space				28h
Reserved Space				2Ch
Expansion ROM Base Address				30h
Reserved Space				34h
Reserved Space				38h
Max. Latency	Min. Grant	Interrupt Pin	Interrupt Line	3Ch

Table 1

PCI Operation Registers

The second group of registers are the PCI Operation Registers shown in Table 2. This group consists of sixteen 32-bit (DWORD) registers accessible to the Host processor from the PCI Local bus. These are the main registers through which the PCI Host configures S5933 operation and communicates with the Add-On Local bus. These registers encompass the PCI bus incoming and outgoing Mailboxes, FIFO data channel, Bus Master Address and Count registers, Pass-Thru data channel registers and S5933 device Status and Control registers.

PCI Operation Registers	Address Offset
Outgoing Mailbox Register 1 (OMB1)	00h
Outgoing Mailbox Register 2 (OMB2)	04h
Outgoing Mailbox Register 3 (OMB3)	08h
Outgoing Mailbox Register 4 (OMB4)	0Ch
Incoming Mailbox Register 1 (IMB1)	10h
Incoming Mailbox Register 2 (IMB2)	14h
Incoming Mailbox Register 3 (IMB3)	18h
Incoming Mailbox Register 4 (IMB4)	1Ch
FIFO Register Port (bidirectional) (FIFO)	20h
Master Write Address Register (MWAR)	24h
Master Write Transfer Count Register (MWTC	28h
Master Read Address Register (MRAR)	2Ch
Master Read Transfer Count Register (MRTC	30h
Mailbox Empty/Full Status Register (MBEF)	34h
Interrupt Control/Status Register (INTCSR)	38h
Bus Master Control/Status Register (MCSR)	3Ch

Table 2

Add-On Bus Operation Registers

The third and last register group consists of the Add-On Operation Registers, shown in Table 3. This group of eighteen 32-bit (DWORD) registers is accessible to the Add-On Local bus. These are the main registers through which the Add-On logic configures S5933 operation and communicates with the PCI Local bus. These registers encompass the Add-On bus Mailboxes, Add-On FIFO, DMA Address/Count Registers (when Add-On initiated Bus Mastering), Pass-Thru Registers and Status/Control registers.

Non-Volatile Memory Interface

The S5933 contains a set of PCI Configuration Registers. These registers can be initialized with default values or with designer specified values contained in an external nvRAM. The nvRAM can be either a serial (2 Kbytes, maximum) or a byte-wide device (64 Kbytes, maximum).

The optional nvRAM allows the Add-On card manufacturer to initialize the S5933 with his specific Vendor ID and Device ID numbers along with desired S5933 operation characteristics. The non-volatile memory feature also provides for the Expansion BIOS and POST code (power-on-self-test) options on the PCI bus.

Mailbox Operation

The Mailbox Registers are divided into two four DWORD sets. Each set is dedicated to one bus for transferring data to the other bus. Figure 3 below shows a block diagram of the mailbox section of the S5933. The provision of Mailbox Registers provides an easy path for the transfer of user information (command, status or parametric data) between the two buses. An empty/full indication for each Mailbox Register, at the byte level, is determined by polling a Status Register accessible to both the PCI and Add-On buses. Providing Mailbox byte level empty/full indications allows for greater flexibility in 8-, 16- or 32-bit system interfaces. i.e., transferring a single byte to an 8-bit Add-On bus without requiring the assembling or disassembling of 32-bit data.

The generation of interrupts from Mailbox Registers is equivalent with the commonly known 'DOORBELL' interrupt technique. Bit locations configured within the S5933's Operation Registers select a Mailbox and Mailbox byte which is to generate an interrupt when full or touched. A mailbox interrupt control register is then used to enable interrupt generation and to select if the interrupt is to be generated on the PCI or Add-On Local bus. PCI Local bus interrupts may also be generated from direct hardware interfacing due to a unique AMCC feature. A dedicated Mailbox byte of the S5933 is directly accessible via a set of hardware device signal pins. A single mailbox load signal pin latches Add-On bus data directly into the Mailbox initiating a PCI bus interrupt if enabled. The mailbox data may also be read in a similar manner. This option is shared with the byte wide non-volatile memory signal pins. The S5933 must use the serial nvRAM option for the direct mailbox option signals to be available or they will be assigned to the byte wide at power up.

Add-On Bus Operation Registers	Address
Incoming Mailbox Register 1 (AIMB1)	00h
Incoming Mailbox Register 2 (AIMB2)	04h
Incoming Mailbox Register 3 (AIMB3)	08h
Incoming Mailbox Register 4 (AIMB4)	0Ch
Outgoing Mailbox Register 1 (AOMB1)	10h
Outgoing Mailbox Register 2 (AOMB2)	14h
Outgoing Mailbox Register 3 (AOMB3)	18h
Outgoing Mailbox Register 4 (AOMB4)	1Ch
FIFO Port (AFIFO)	20h
Bus Master Write Address Register (MWAR)	24h
Pass-Thru Address Register (APTA)	28h
Pass-Thru Data Register (APTD)	2Ch
Bus Master Read Address Register (MRAR)	30h
Maibox Empty/Full Status Register (AMBEF)	34h
Interrupt Control/Status Register (AINT)	38h
General Control/Status Register (ARCR)	3Ch
Bus Master Write Transfer Count (MWTC)	58h
Bus Master Read Transfer Count (MRTC)	5Ch

Table 3

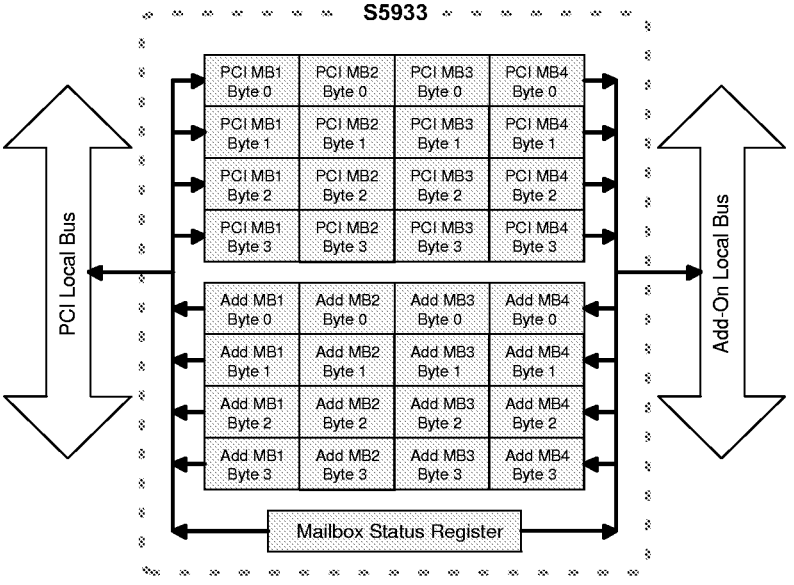


Figure 3

Pass-Thru Operation

Pass-Thru operation executes PCI bus cycles in real time with the Add-On bus. This allows the PCI bus to directly read or write to Add-On resources. The S5933 allows the designer to declare up to four individual Pass-Thru Regions. Each region may be defined as 8-, 16-, or 32-bits wide, mapped into host memory or I/O space and may be up to 512MB bytes in size. Figure 4 right shows a block diagram of the S5933 Pass-Thru architecture.

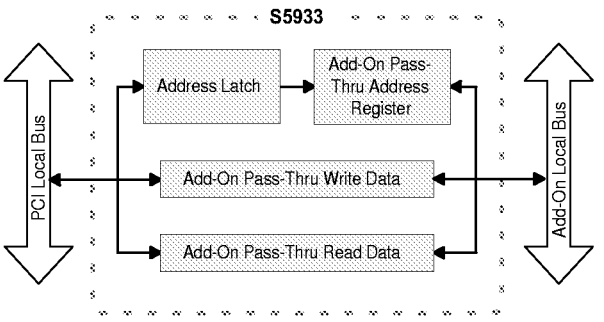


Figure 4

Pass-Thru operations are performed in PCI target only mode, making this data channel useful for converting existing ISA or EISA designs over to the fast PCI architecture. The Pass-Thru data channel utilizes separate Add-On bus signal pins to reflect a PCI bus read or write request. Add-On logic decodes these signals to determine if it must read or write data to the S5933 to satisfy the request. Information decoded includes PCI request occurring, the byte lanes involved, the specific Pass-Thru region accessed and if the request is a burst or single-cycle access. All requested Pass-Thru address and data information is passed via Add-On Operation Registers.

Pass-Thru operation supports single PCI data cycles and PCI data bursts. During PCI burst operations, the S5933 is capable of transferring data at the full PCI bandwidth. Should slower Add-On logic be implemented, the S5933 automatically issues PCI bus waits or a Host retry indication until the requested transfer is satisfied.

FIFO PCI Bus Mastering Operation

FIFO PCI Bus Master data transfers are processed by one of two 8-DWORD FIFOs. The FIFO block diagram is shown in Figure 5. The particular FIFO selected for a data transfer is dependent only on the direction of data flow and is completely transparent to the user. Internal S5933 decode logic selects the FIFO that is dedicated to transferring data to the other bus.

The way data is transferred by a FIFO, is determined by Operation and Configuration Registers contained within the S5933. A FIFO may be configured for either PCI or Add-On initiated Bus Mastering with programmable byte advance conditions, read vs. write priorities and Add-On bus widths. Advance conditions allow the FIFO to implement 8-, 16- or 32-bit bus widths. Configuring the S5933 for Bus Master operation enables separate address and data count registers, which are loaded with the PCI memory address location and number of bytes to be read or written. This is accomplished by either the Host CPU or Add-On logic. Data can be transferred between the two buses transparent to the PCI Host processor, however, the Add-On logic is required to service the S5933 Add-On Local bus. An indication of transfer completion can be seen by polling a status register done bit or S5933 signal pin or enabling a 'transfer count = 0' interrupt to either bus.

Further FIFO configuration bits select 16, 32, or 64 bit Endian conversion options for incoming and outgoing data. Endian conversion allows an Add-On processor and the host to transfer data in their native Endian format. Other configuration bits determine if the Add-On Local bus width is 8, 16 or 32 bits. 16-bit bus configurations internally steer FIFO data from the upper 16 bits of the DWORD and then to the lower 16-bits on alternate accesses. FIFO pointers are then updated when appropriate bytes are accessed. Other methods are available for 8-bit or 16-bit Add-Ons.

Efficient FIFO management configuration schemes unique to the AMCC S5933 specify how full or empty a FIFO must be before it requests the PCI Local bus. These criteria include bus requests when any of the 8 DWORDs are empty, or when four or more DWORDs are empty. This allows the designer to control how often the S5933 requests the bus. The S5933 always attempts to perform burst operations to empty or fill the FIFOs. Further FIFO capabilities over the standard register access methods allow for direct hardware FIFO access. This is provided through separate access pins on the S5933. Other status output pins allow for easily cascading external FIFOs to the Add-On design.

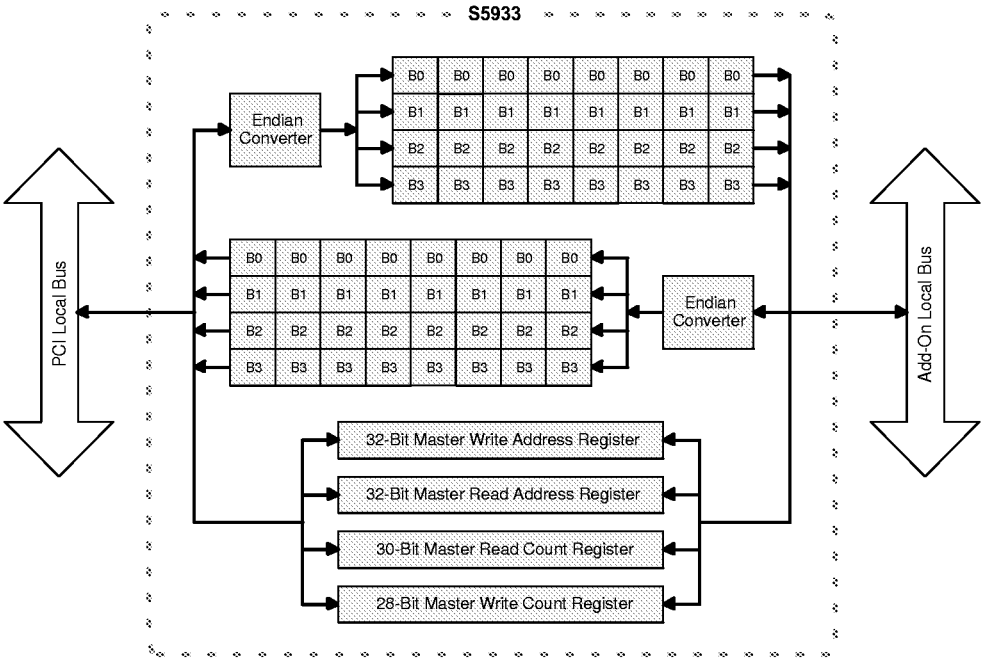


Figure 5

Summary

Because the PCI bus applies to numerous system architectures, it allows a single add-in card hardware design to be created for multiple platforms. The PCI standard also provides the bandwidth required for many new, high-performance applications.

The AMCC S5933 provides a flexible, low-cost, compliant interface to the PCI bus. The architecture of the S5933 makes it an excellent choice for cards being converted from the ISA/EISA standard, as well as newer applications requiring high data rates and bus mastering capabilities. These applications include frame grabbers, work station graphics, satellite receivers, modems, ISDN/FDDI/ATM communications and I/O interfaces. The S5933 allows the hardware developer to focus on the actual application development rather than debugging the PCI bus interface logic. This significantly shortens design cycles and decreases development costs.

S5933 PIN DESCRIPTIONS

AD[31:0] t/s *Address/Data.* Address and data are multiplexed on the same PCI bus pins. A PCI Bus transaction consists of an address phase followed by one or more data phases. An address phase occurs on the PCLK cycle in which FRAME# is asserted. A data phase occurs on the PCLK cycles in which IRDY# and TRDY# are both asserted.

C/BE[3:0]# t/s *Bus Command/Byte Enable.* Bus commands and byte enables are multiplexed on the same pins. These pins define the current bus command during an address phase. During a data phase, these pins are used as Byte Enables, with C/BE[0]# enabling byte 0 (LSB) and C/BE[3]# enabling byte 3 (MSB).

C/BE# [3	2	1	0]	Description
0	0	0	0	Interrupt Acknowledge
0	0	0	1	Special Cycle
0	0	1	0	I/O Read
0	0	1	1	I/O Write
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Memory Read
0	1	1	1	Memory Write
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Configuration Read
1	0	1	1	Configuration Write
1	1	0	0	Memory Read Multiple
1	1	0	1	Dual Address Cycle
1	1	1	0	Memory Read Line
1	1	1	1	Memory Write and Invalidate

PAR t/s *Parity.* Parity is always driven as even from all AD[31:0] and C/BE[3:0]# signals. The parity is valid during the clock following the address phase and is driven by the bus master. During a data phase for write transactions, the bus master sources this signal on the clock following IRDY# active; during a data phase for read transactions, this signal is driven by the target and is valid on the clock following TRDY# active. The PAR signal has the same timing as AD[31:0], delayed by one clock.

PCLK in *Clock.* The rising edge of this signal is the reference upon which all other signals are based except for RST# and INTA#. The maximum PCLK frequency for the S5933 is 33 MHz and the minimum is DC (0 Hz).

RST# in *Reset* is used to bring all other signals within the S5933 to a known, consistent state. All PCI bus interface output signals are not driven (tri-stated), and open drain signals such as SERR# are floated.

FRAME# s/t/s *Frame.* This signal is driven by the current bus master to indicate the beginning and duration of a bus transaction. When FRAME# is first asserted, it indicates a bus transaction is beginning with a valid addresses and bus command present on AD[31:0] and C/BE[3:0]. FRAME# remains asserted during a burst data transfer and is deasserted to signify the final data phase.

IRDY# s/t/s *Initiator Ready.* This signal is always driven by the bus master to indicate its ability to complete the current data phase. During write transactions, it indicates AD[31:0] contains valid data. Wait states occur until both TRDY# and IRDY# are asserted together.

TRDY#	s/t/s	*Target Ready.* This signal is sourced by the selected target and indicates the target is able to complete the current data phase of a bus transaction. For read operation, it indicates that the target is providing valid data on the AD[31:0] pins. Wait states occur until both TRDY# and IRDY# are asserted together.
STOP#	s/t/s	*Stop.* The Stop signal is driven by a selected target and conveys a request to the bus master to stop the current transaction.
LOCK#	in	*Lock.* The lock signal provides for the exclusive use of a resource. The S5933 may be locked by one master at a time. The S5933 cannot lock a target when it is a master.
IDSEL	in	*Initialization Device Select.* This pin is used as a chip select during configuration read or write transactions.
DEVSEL#	s/t/s	*Device Select.* This signal is driven by a target decoding and recognizing its bus address. This signal informs a bus master whether an agent has decoded a current bus cycle.
INTA#	o/d	*Interrupt A.* This signal is defined as optional and a level sensitive Host interrupt. The INTA# is used for any single function device requiring an interrupt capability.
REQ#	out	*Request.* This signal is sourced by an agent wishing to become the bus master. It is a point-to-point signal and each master has its own REQ#.
GNT#	in	*Grant.* The GNT# signal is a dedicated, point-to-point signal provided to each potential bus master and signifies that access to the bus has been granted.
PERR#	s/t/s	*Parity Error.* Is used for reporting data parity errors for all bus transactions except for Special Cycles. It is driven by the agent receiving data two clock cycles after the parity was detected as an error. This signal is driven inactive (high) for one clock cycle prior to returning to the tri-state condition.
SERR#	o/d	*System Error.* Used to report address and data parity errors on Special Cycle commands and any other error condition having a catastrophic system impact.
SCL	t/s	*Serial Clock.* This clock provides timing for transactions on the two-wire serial bus. This signal is intended to be directly connected to one serial non-volatile RAM. This pin is shared with the byte-wide interface signal, ERD#.
SDA	t/s	*Serial Data/Address.* This bidirectional pin is used to transfer addresses and data to or from a serial nvRAM. It is an open drain output requiring a 10K external pull-up resistor. This pin is shared with the byte-wide interface signal, EWR#.
EA[15:0]	t/s	*External nv Memory Address.* These signals connect directly to the external byte wide or EPROM address pins EA0 through EA15. The PCI interface controller assembles 32-bit wide accesses through multiple read cycles of the 8-bit device. The address space from 0040h through 007Fh is used to preload and initialize the PCI configuration registers. Should an external nv memory be used, the minimum size required is 128 bytes and the maximum is 64K bytes. When a serial memory is connected to the S5933, the pins EA[7:0] are reconfigured to become hardware Add-On to PCI mailbox register controls with the EA8 pin as the mailbox load clock. Also, the EA15 signal pin will provide an indication that the PCI to Add-On FIFO is full (FRF), and the EA14 signal pin will indicate whether the add-On to PCI FIFO is empty (FWE).
ERD#	out	*External nv Memory Read Control.* This pin is asserted during read operations involving the external non-volatile memory. Data is transferred into the S5933 during the low to high transition of ERD#. This pin is shared with the serial external memory interface signal, SCL.

EWR# t/s *External nv Memory Write Control.* This pin is asserted during write operations involving the external non-volatile memory. Data is presented on pins EQ[7:0] along with its address on pins EA[15:0] throughout the entire assertion of EWR#. This pin is shared with the serial external memory interface signal, SDA.

EQ[7:0] t/s *External Memory Data Bus.* These pins are used to directly connect with the data pins of an external non-volatile memory. When a serial memory is connected to the S5933, the pins EQ4, EQ5, EQ6, and EQ7 become reconfigured to provide signal pins for bus mastering control from the Add-On interface.

DQ[31:0] t/s *Address/Data Bus.* The 32 bit Add-On data bus. The DQMODE signal configures the bus width for either 32 or 16 bits. All DQ[31:0] signals have an internal pull-up.

ADR[6:2} in Address [6:2]. These inputs select which S5933 register is to be read from or written to. To be used in conjunction with SELECT#, BE[3:0]# and WR# or RD#. The following table shows the register addresses.

ADR [6	5	4	3	2]	Description
0	0	0	1	1	Add-On Incoming Mailbox Register
0	0	1	1	1	Add-On Outgoing Mailbox Register
0	1	0	1	0	Add-On Pass-Thru Address Register
0	1	0	1	1	Add-On Pass-Thru Data Register
0	1	1	0	1	Add-On Mailbox Status Register
0	1	1	1	0	Add-On Interrupt Control Register
0	1	1	1	1	Add-On Reset Control Register
1	0	0	0	0	Pass-Thru/FIFO Configuration Register

BE[2:0]# in *Byte Enable [2:0].* Provides individual read/write byte enabling during register read or write transactions. BE2# enables activity over DQ[23:16], BE1# enables DQ[15:8], and BE0# enables DQ[7:0]. During read transactions, enables the output driver for each byte lane; for write transactions, serves as an input enable to perform the write to each byte lane.

BE3#/ADR1 in *Byte Enable 3/Address 1.* BE3#, enables DQ[31:24] input drivers for writing data to registers identified by ADR[6:2] and enables DQ[31:24] output drivers to read registers identified by ADR[6:2]. To be used in conjunction with SELECT# and RD# or WR#. ADR1, selects the upper or lower WORD of a DWORD when a 16 bit wide bus is selected. 1 = lower, 0 = upper.

SELECT# in *Select.* Enables internal S5933 logic to decode WR#, RD# and ADR[6:2] when reading or writing to any Add-On register.

WR# in *Write Enable.* Asserting this signal writes DQ bus data byte(s) selected by BE[3:0]# into the S5933 register defined by SELECT# and ADR[6:2].

RD# in *Read Enable.* Asserting this signal drives data byte(s) selected by BE[3:0]# from the S5933 register defined by SELECT# and ADR[6:2] onto the DQ bus.

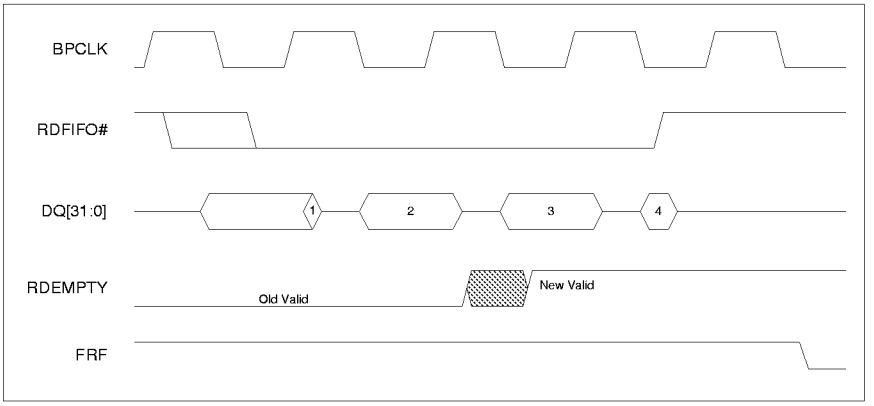
MODE in *DQ Mode.* Defines the DQ bus width when accessing data using WR#, RD#, SELECT# and ADR[6:2]#. Low = 32-bit wide DQ bus. High = 16-bit wide DQ bus. When high, the signal BE3# is re-assigned to the ADR1 signal and only DQ[15:0] is active.

PTATN# out *Pass-Thru Attention.* Signals a decoded PCI to Pass-Thru region bus cycle. PTATN# is generated to signal Add-On logic Pass-Thru data must be read from or written to the S5933.

PTBURST#	out	*Pass-Thru Burst.* Informs the Add-On bus the current Pass-Thru region decoded PCI bus cycle is a burst access.
PTRDY#	in	*Pass-Thru Ready.* This input indicates when Add-On logic has completed a Pass-Thru cycle and another may be initiated.
PTNUM[1:0]	out	*Pass-Thru Number.* Identifies which of the four Pass-Thru regions the Host read/write is requesting. Only valid for the duration of PTATN#. 00 = Base Address Register 1, 01 = Base Address Register 2, 10 = Base Address Register 3, 11 = Base Address Register 4.
PTBE[3:0]#	out	*Pass-Thru Byte Enables.* During a PCI to Pass-Thru read, Indicates which bytes of a DWORD is to be written into. During a PCI to Pass-Thru write, indicates which bytes of a DWORD are valid to read. PTBE[3:0]# are only valid while PTATN# is asserted.
PTADR#	in	*Pass-Thru Address.* When asserted, the 32-bit Pass-Thru address register contents is driven onto the DQ[31:0] bus. All other Add-On control signals must be inactive during the assertion of PTADR#.
PTWR	out	*Pass-Thru Write.* This signal indicates the current PCI to Pass-Thru bus transaction is a read or write cycle. Valid only when PTATN# is active.
SYSRST#	out	*System Reset.* An active-low buffered PCI bus RST# output signal. The signal is asynchronous and can be asserted through software from the PCI host interface.
BPCLK	out	*Buffered PCI Clock.* This output is a buffered form of the PCI bus clock and has all of the behavioral characteristics of the PCI clock (i.e., DC-to-33 MHz capability).
IRQ#	out	*Interrupt Request.* This output signals Add-On logic a significant event has occurred as a result of activity within the S5933.
FLT#	in	*Float.* Floats all S5933 output signals when asserted. This signal is connected to an internal pull-up resistor.
SNV	in	*Serial Non-Volatile Device.* This input, when high, indicates that a serial boot device or that no boot device in present. When this pin is low, a byte-wide boot device is present.
WRFIFO#	in	*Write FIFO.* This signal provides a method to directly write the FIFO without having to generate the SELECT# signal or the ADR[6:2] value of [01000b] to access the FIFO. Access width is either 32 bits or 16 bits depending on the data bus size available. This signal is intended for implementing PCI DMA transfers with the Add-On system. This pin has an internal pull-up resistor.
RDFIFO#	in	*Read FIFO.* This signal provides a method to directly read the FIFO without having to generate the SELECT# signal or the ADR[6:2] value of [01000b] to access the FIFO. Access width is either 32 bits or 16 bits depending on the data bus size defined by the MODE pin. This signal is intended for implementing PCI DMA transfers with the Add-On system. This pin has an internal pull-up resistor.
WRFULL	out	*Write FIFO Full.* This pin indicates whether the Add-On-to-PCI bus FIFO is able to accept more data. This pin is intended to be used to implement DMA hardware on the Add-On system bus. A logic low output from this pin can be used to represent a DMA write (Add-On-to-PCI FIFO) request.
RDEMTPY	out	*Read FIFO Empty.* This pin indicates whether the read FIFO (PCI-to-Add-On FIFO) contains data. This pin is intended to be used by the Add-On system to control DMA transfers from the PCI bus to the ADd-On system bus. A logic low from this pin can be used to represent a DMA (PCI-to-Add-On FIFO) request.

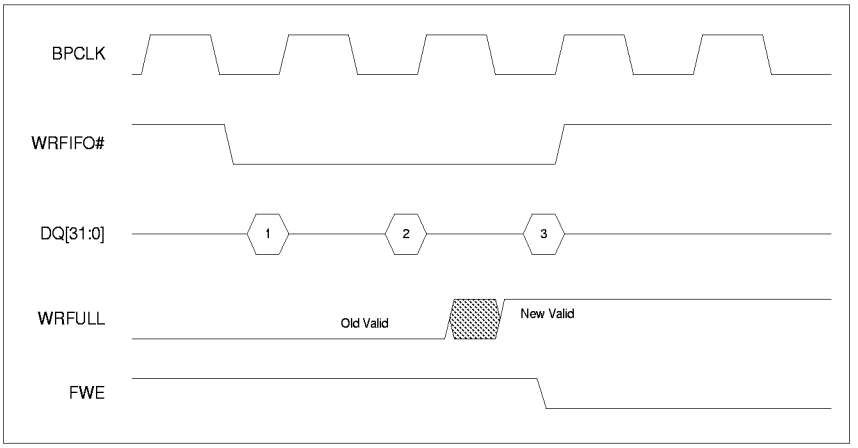
TIMING DIAGRAMS

Synchronous RDFIFO# Timing



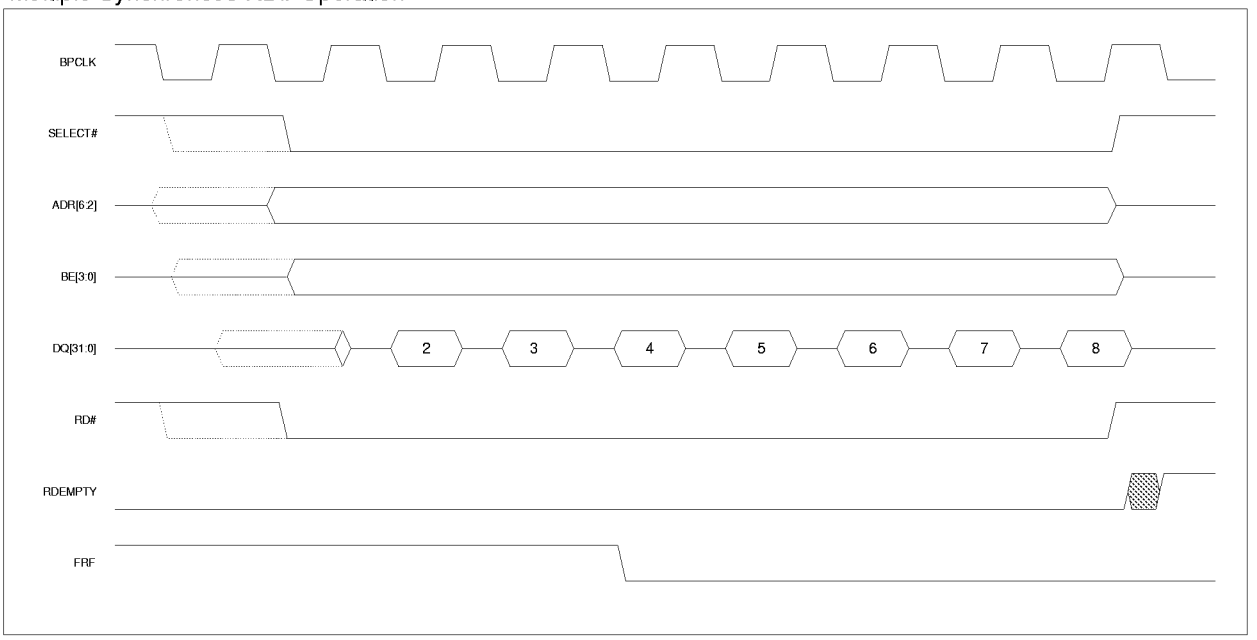
Notes:
1. The data 1 valid time is dependent on where RDFIFO# is asserted in it's window.
2. The data 4 signal is cut short due to the de-assertion of RDFIFO#.
3. The RDEMPTY is an example relative to data 2, if the FIFO went empty on data 2.

Synchronous WRFIFO# Timing

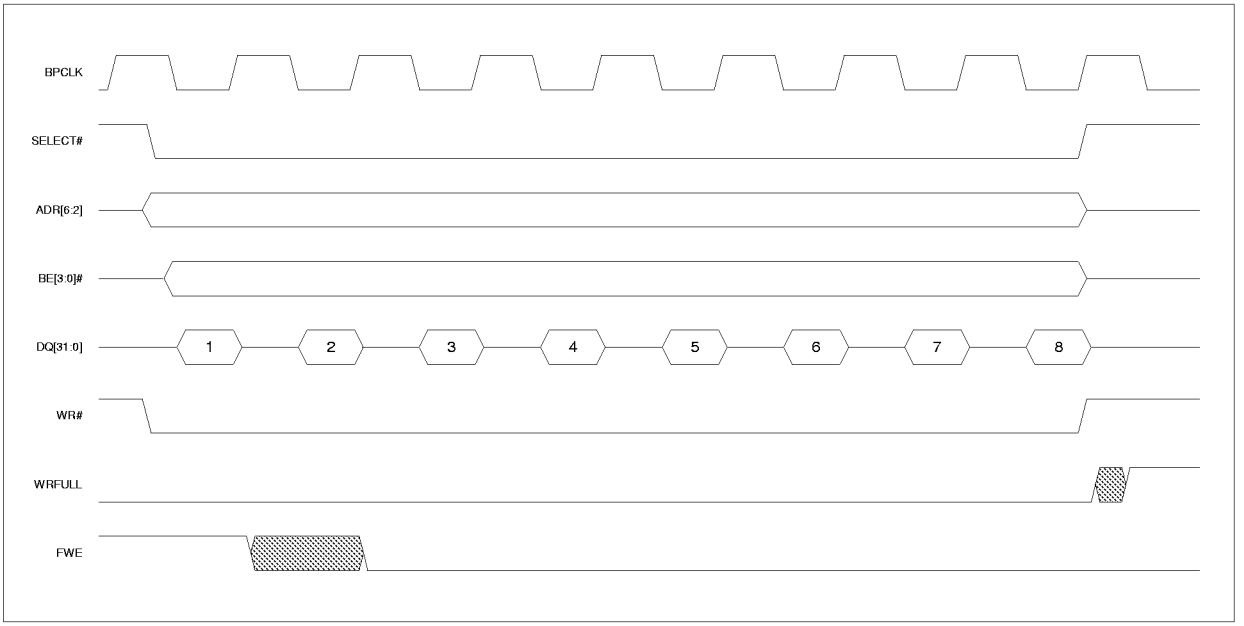


Notes:
1. The WRFULL is an example relative to data 2, if data 2 were to fill the FIFO.

Multiple Synchronous RD# Operation



Multiple Synchronous WR# Operation



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range (V_{DD} Core)-0.3 V to 7.0 V
Input Pin Voltage Range-0.5 V to VDD + 0.5 V
Storage Temperature Range-55 to 125 °C

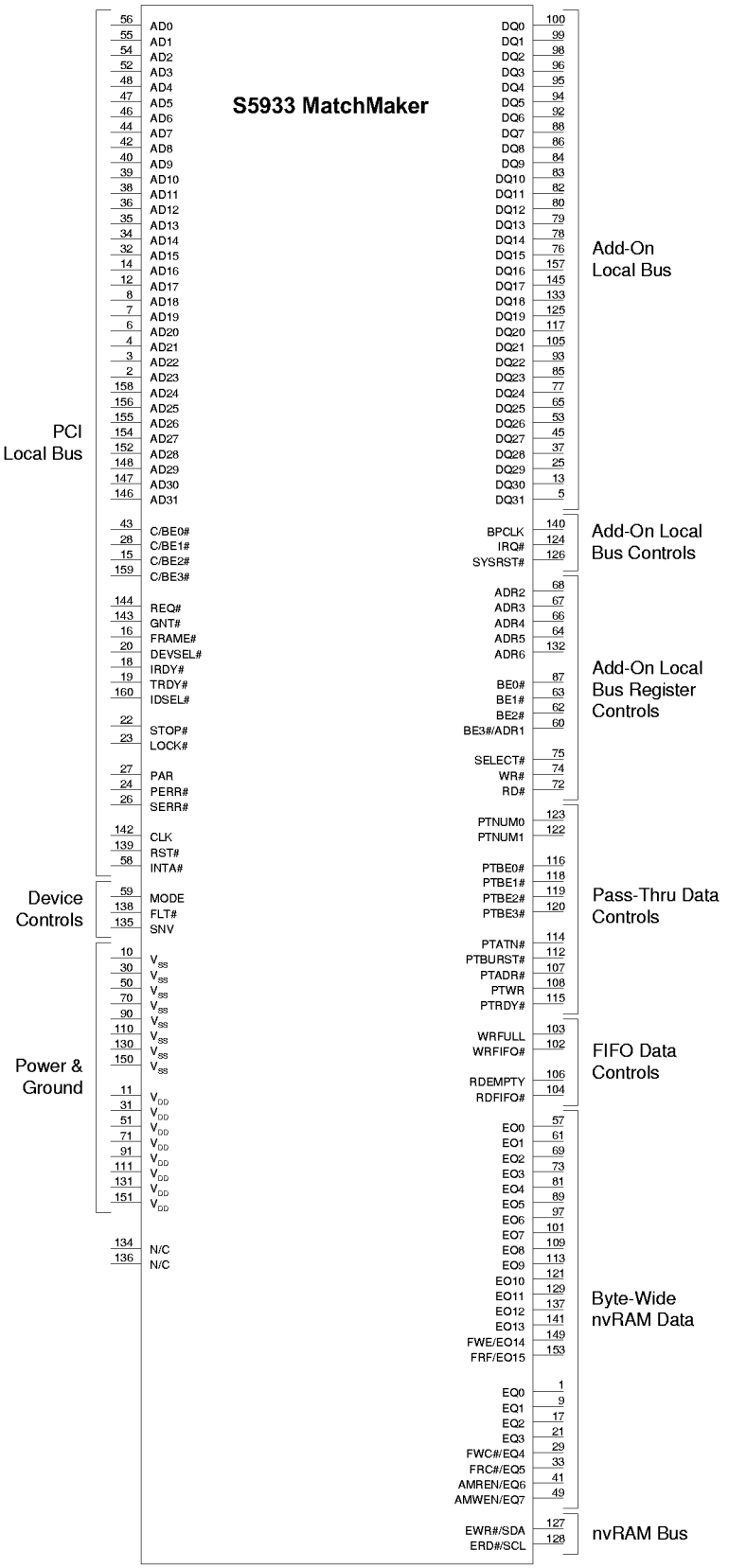
⊗ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to this device. These are stress ratings only.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units	Test Conditions	Notes
V_{DD}	Supply Voltage	4.75	5.25	Volts	To PCI Spec 2.2	
V_{ih}	High Level Input Voltage	2.0	-	Volts		
V_{il}	Low Level Input Voltage	-0.5	0.8	Volts		
V_{oh}	High Level Output Voltage	2.4	-	Volts	I_{out} = -2 ma	
V_{ol}	Low Level Output Voltage	-	0.55	Volts	I_{out} = 3 ma, 6 ma	1
I_{ih}	High Input Leakage Current	-	70	µA	V_{in} = 2.7 VDC	2
I_{il}	Low Input Leakage Current	-	-70	µA	V_{in} = 0.5 VDC	2
C_{in}	Input Pin Capacitance	-	10	pF		3
C_{CLK}	CLK Pin Capacitance	5	12	pF		
C_{IDSEL}	IDSEL Pin Capacitance	-	8	pF		

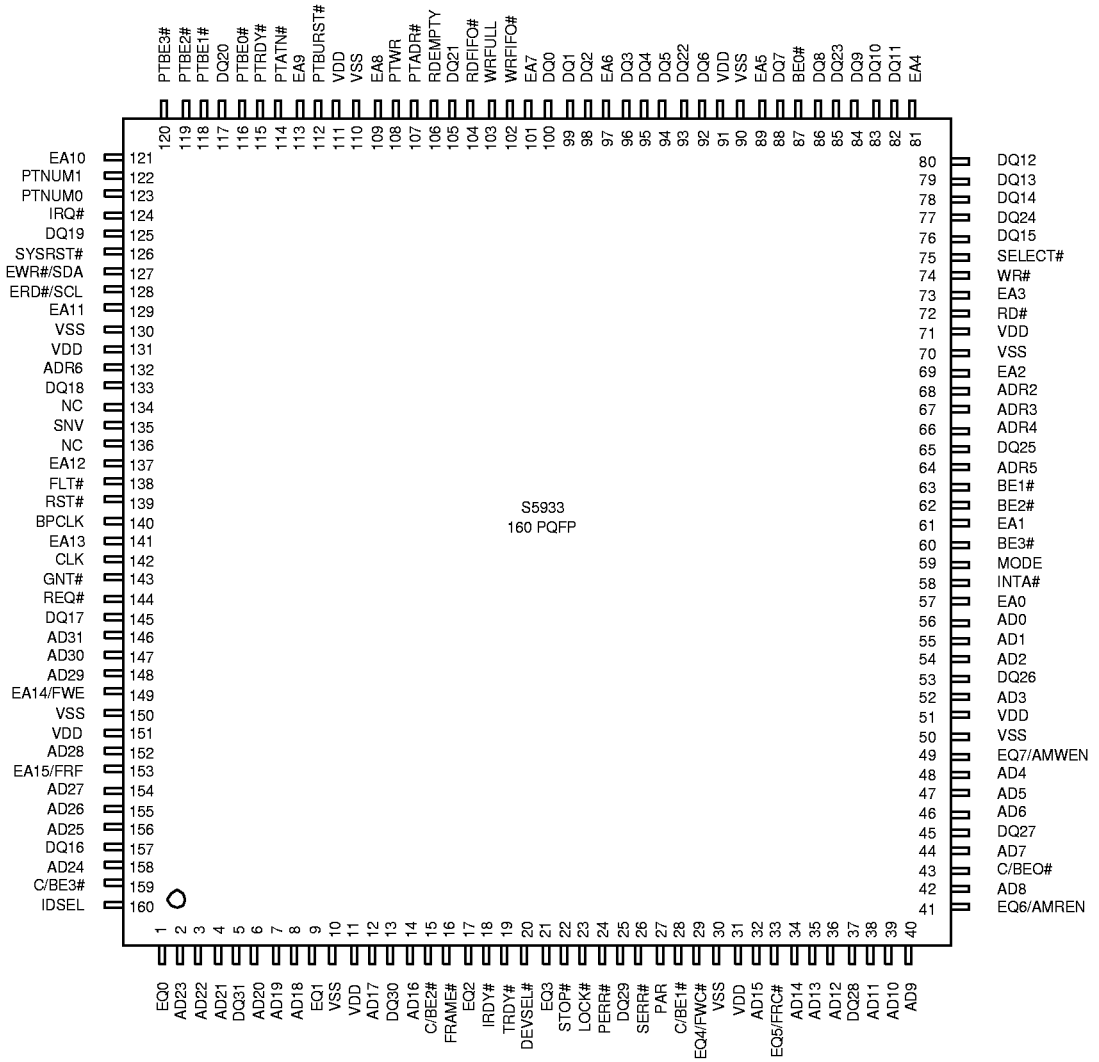
Notes:

1. PCI bus signals without pull-up resistors will provide the 3 ma output current. Signals which require a pull-up Resistor (FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR# and PERR#) will provide 6 ma output current.
2. Input leakage applies to all inputs and bidirectional buffers.
3. The PCI specification limits all PCI inputs not located on the motherboard to 10 pF (the PCI clock is allowed to be 12 pF).


S5933 MatchMaker
PCI Local Bus
56 AD0
55 AD1
54 AD2
52 AD3
48 AD4
47 AD5
46 AD6
44 AD7
42 AD8
40 AD9
39 AD10
38 AD11
36 AD12
35 AD13
34 AD14
32 AD15
14 AD16
12 AD17
8 AD18
7 AD19
6 AD20
4 AD21
3 AD22
2 AD23
158 AD24
156 AD25
155 AD26
154 AD27
152 AD28
148 AD29
147 AD30
146 AD31
43 C/BE0#
28 C/BE1#
15 C/BE2#
159 C/BE3#
144 REQ#
143 GNT#
16 FRAME#
20 DEVSEL#
18 IRDY#
19 TRDY#
160 IDSEL#
22 STOP#
23 LOCK#
27 PAR
24 PERR#
26 SERR#
142 CLK
139 RST#
58 INTA#
Device Controls
59 MODE
138 FLT#
135 SNV
Power & Ground
10 VSS
30 VSS
50 VSS
70 VSS
90 VSS
110 VSS
130 VSS
150 VSS
11 VDD
31 VDD
51 VDD
71 VDD
91 VDD
111 VDD
131 VDD
151 VDD
134 N/C
136 N/C
100 DQ0
99 DQ1
98 DQ2
96 DQ3
95 DQ4
94 DQ5
92 DQ6
88 DQ7
86 DQ8
84 DQ9
83 DQ10
82 DQ11
80 DQ12
79 DQ13
78 DQ14
76 DQ15
157 DQ16
145 DQ17
133 DQ18
125 DQ19
117 DQ20
105 DQ21
93 DQ22
85 DQ23
77 DQ24
65 DQ25
53 DQ26
45 DQ27
37 DQ28
25 DQ29
13 DQ30
5 DQ31
Add-On Local Bus
140 BPCLK
124 IRQ#
126 SYSRST#
Add-On Local Bus Controls
68 ADR2
67 ADR3
66 ADR4
64 ADR5
132 ADR6
87 BE0#
63 BE1#
62 BE2#
60 BE3#/ADR1
75 SELECT#
74 WR#
72 RD#
Add-On Local Bus Register Controls
123 PTNUM0
122 PTNUM1
116 PTBE0#
118 PTBE1#
119 PTBE2#
120 PTBE3#
114 PTATN#
112 PTBURST#
107 PTADR#
108 PTWR
115 PTRDY#
Pass-Thru Data Controls
103 WRFULL
102 WRFIFO#
106 RDEMPTY
104 RDFIFO#
FIFO Data Controls
57 EO0
61 EO1
69 EO2
73 EO3
81 EO4
89 EO5
97 EO6
101 EO7
109 EO8
113 EO9
121 EO10
129 EO11
137 EO12
141 EO13
149 FWE/EO14
153 FRF/EO15
Byte-Wide nvRAM Data
1 EQ0
9 EQ1
17 EQ2
21 EQ3
29 FWC#/EQ4
33 FRC#/EQ5
41 AMREN/EQ6
49 AMWEN/EQ7
127 EWR#/SDA
128 ERD#/SCL
nvRAM Bus

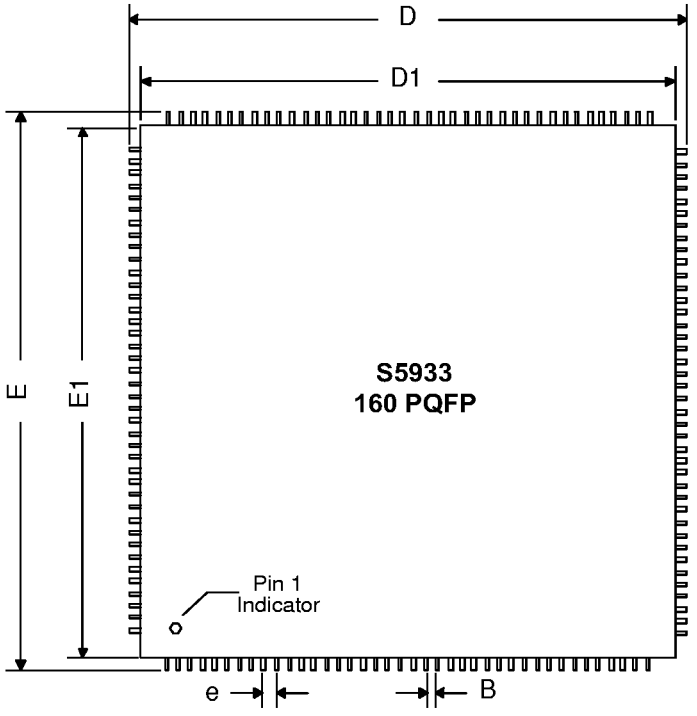
PACKAGE INFORMATION

160 PQFP

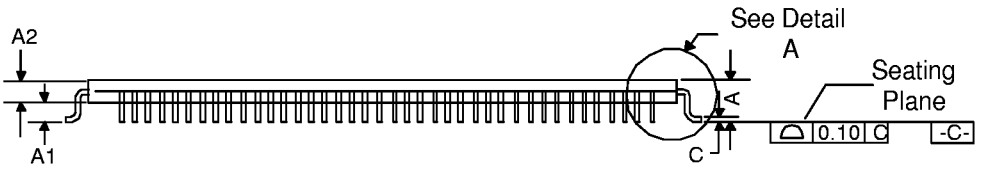


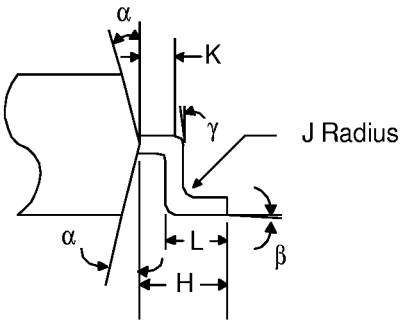
PACKAGE INFORMATION

160 PQFP



Symbol	MIN	NOM	MAX
A	-	-	4.07
A1	0.25	-	-
A2	3.17	-	-
D		31.90 BSC	
D1		28.00 BSC	
E		31.90 BSC	
E1		28.00 BSC	
L	0.65	0.80	1.03
e		0.65 BSC	
B	0.22	-	0.38
c	0.11	-	0.23
α	5	-	16
β	0	-	7
γ	0	-	-
G	0.13	-	-
H		1.95 BSC	
J	0.13	-	0.30
K	0.40	-	-
2H	-	3.9	-





Detail A

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