Synchronous Buck Converter Controller

FEATURES

- 6- to 16.5-V Input Range (Si9150CY)
- Voltage-Mode PWM Control
- Low-Current Standby Mode
- Enable Control
- Dual 100-mA Output Drivers
- 2% Band Gap Reference
- Multiple Converters Easily Synchronized
- Over-Current Protection

DESCRIPTION

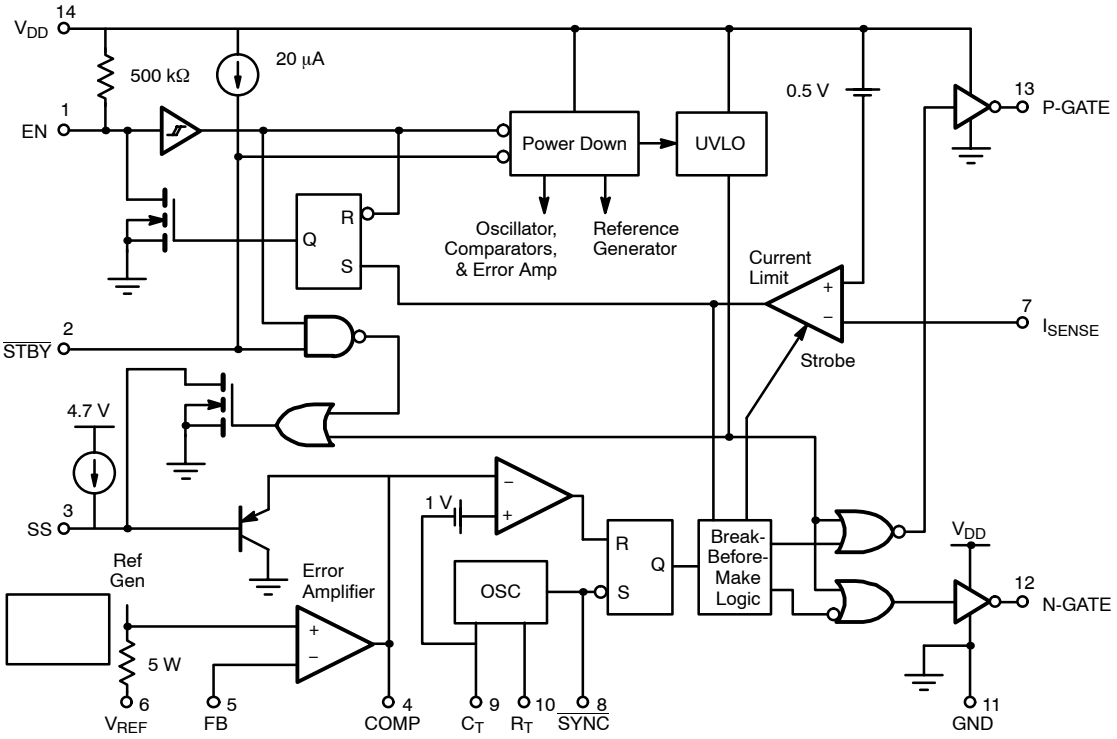
The Si9150 synchronous buck regulator controller is ideally suited for high-efficiency step down converters in battery-powered equipment. Combined with the Si9943DY MOSFET half-bridge, a 90% efficient, 7.5-W, 3.3-V or 5-V power supply can be implemented using standard surface-mount assembly techniques. The wide input range allows operation from NiCd or NiMH battery packs using six to ten cells.

Over-current protection is achieved by sensing the on-state voltage drop across the high side p-channel MOSFET, which eliminates the need for a current sense resistor.

Duty ratios of 0 to 100% and switching frequencies up to 300 kHz are possible. The IC can be disabled by pulling EN low (I_{DD} = 100 μA), or the 2.5-V reference can be maintained, with all other functions disabled, by pulling $\overline{\text{STBY}}$ low (I_{DD} = 500 μA).

The Si9150 is available in both standard and lead (Pb)-free 14-pin SOIC and rated for the commercial temperature range of 0 to 70°C (C suffix), and the industrial temperature range of –40 to +85°C (D suffix).

FUNCTIONAL BLOCK DIAGRAM



Synchronous Buck Regulator Controller

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND.
V_{DD} . . . . . 18 V
I_{SENSE} Input . . . . . −2 V to V_{DD} +2 V
All Other Inputs . . . . . −0.3 to V_{DD} + 0.3 V
P-Gate, N-Gate Continuous Source/Sink Current . . . . . 50 mA
Storage Temperature . . . . . −65 to 125°C
Operating Junction Temperature . . . . . 150°C

Power Dissipation (Package)a
14-Pin SOIC (Y Suffix)b . . . . . 900 mW
Thermal Impedance (Θ_{JA})
14-Pin SOIC . . . . . 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.2 mW/°C.

SPECIFICATIONS[a]

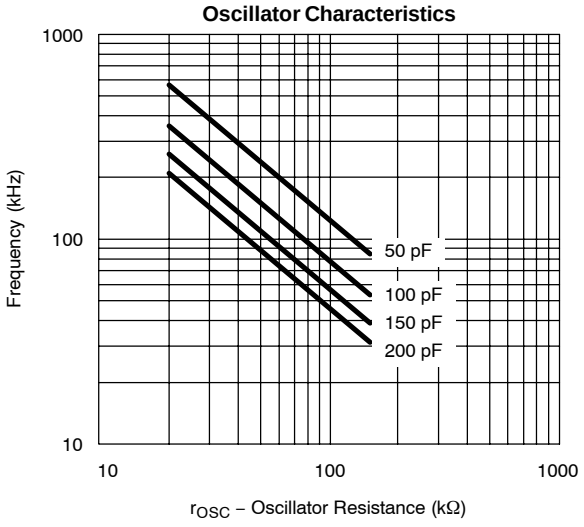
Parameter	Symbol	Test Conditions Unless Otherwise Specified $6.0 \le V_{DD} \le 16.5$ V	Limits C Suffix 0 to 70°C Min[b]	Typ[c]	Max[b]	Limits D Suffix −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Reference									
Output Voltage	V_{REF}	T_A = 25°C Measured at Feedback[e] Pin 5	2.45	2.50	2.55	2.45	2.50	2.55	V
		T_{MIN} to T_{MAX}[d]	2.425	2.500	2.575	2.40	2.500	2.60	
Oscillator									
Maximum Frequency	f_{MAX}	C_{OSC} =94.3 pF, R_{OSC} = 28.7 kΩ T_A = 25°C[f]	255	300	345	255	300	345	kHz
Initial Accuracy	f_{OSC}	C_{OSC} =212 pF, R_{OSC} = 41.2 kΩ T_A = 25°C[f]	85	100	115	85	100	115	
Oscillator Ramp Amplitude	V_{OSC}	T_A = 25°C, 100 kHz	2.05	2.65	2.85	2.05	2.65	2.85	V
Temperature Stability[d]	f_{TEMP}	V_{DD} = 10 V, T_{MIN} to T_{MAX}	−5	±3	+5	−6	±4	+6	%
Error Amplifier									
Input BIAS Current	I_B	$V_{FB} = V_{REF}$		25	500		25	750	nA
Open Loop Voltage Gain[d]	A_{VOL}		60	72		58	72		dB
Offset Voltage	V_{OS}			10	25		10	30	mV
Unity Gain Bandwidth[d]	BW		1	1.5		1	1.5		MHz
Output Current	I_{OUT}	Source, V_{COMP} = 2.50 V		−0.30	−0.20		−0.30	−0.15	mA
		Sink, V_{COMP} = 1.0 V	1	2.5		0.9	2.5		
Power Supply Rejection	PSRR		50	70		48	70		dB
Protection									
Current Limit Threshold Voltage	V_{CL}	T_A = 25°C, V_{DD} = 10 V	0.43	0.49	0.55	0.43	0.49	0.55	V
Current Limit Delay to Output[d]	t_d	T_A = 25°C		500	1000		500	1000	ns
Undervoltage Lockout Voltage	V_{UVLO}	Upper Threshold	5.4	5.7	6.0	5.38	5.7	6.01	V
Undervoltage Hysteresis	V_{HYS}		0.10	0.17	0.25	0.10	0.17	0.26	
Softstart Pull-Up Current	I_{SS}			20			20		µA
Supply									
Supply Current (Enable Low)	I_{OFF}			60	100		60	100	µA
Supply Current (Enable High)	I_{CC}	C_L = 0 pF, f_{OSC} = 100 kHz V_{DD} = 10 V		2.2	3.0		2.2	3.0	mA
Supply Current ($\overline{STBY}$ Low)	I_{SB}			300	500		300	550	µA

SPECIFICATIONS[a]

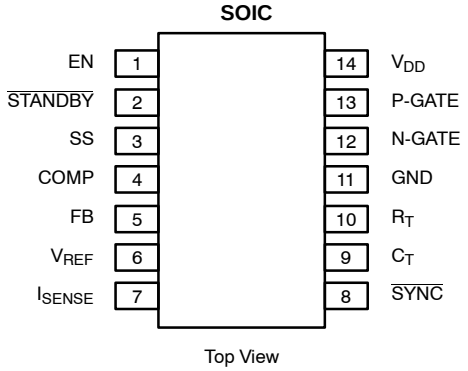
Parameter	Symbol	Test Conditions Unless Otherwise Specified $6.0 \le V_{DD} \le 16.5$ V	Limits C Suffix 0 to 70°C			Limits D Suffix −40 to 85°C			Unit
			Min[b]	Typ[c]	Max[b]	Min[b]	Typ[c]	Max[b]	
Output									
Output High Voltage	V_{OH}	I_{OUT} = 10 mA, V_{DD} = 10 V	9.75			9.7			V
Output Low Voltage	V_{OL}	I_{OUT} = −10 mA, V_{DD} = 10 V			0.25			0.3	
Output Resistance	R_{OUT}	I_{OUT} = 100 mA, V_{DD} = 10 V		10	20		10	25	Ω
Rise Time[d]	t_r	C_L = 800 pF, V_{DD} = 10 V		30	60		30	70	ns
Fall Time[d]	t_f			30	60		30	70	
Logic									
Delay to Output	$t_{d(EN)}$	Transition High to Low		0.25	1		0.25	1	µs
Enable Pull-Up Resistance	R_{EN}			500			500		kΩ
$\overline{STBY}$ Pull-Up Current	$I_{\overline{STBY}}$	T_A = 25°C, $V_{\overline{STBY}}$ = 0 V, V_{DD} = 10 V	−25	−20	−15	−28	−20	−12	µA
Turn-On Threshold	V_{ENH}	V_{DD} = 10 V, Rising Input Voltage	6	6.8	8	6	6.8	8	V
Turn-Off Threshold	V_{ENL}	V_{DD} = 10 V, Falling Input Voltage	2	3.75	5	2	3.75	5	

Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. The voltage reference is trimmed with the feedback (Pin 5) connected to compensation (Pin 4) so that the effect of the error amplifier's input offset voltage is eliminated.
f. C_{OSC} includes the PC board's parasitic capacitance.

TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)



PIN CONFIGURATION AND ORDERING INFORMATION



ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9150CY	0 to 70°C	SOIC-14
Si9150CY-T1		
Si9150CY-T1—E3		
Si9150DY	−40 to 85°C	
Si9150DY-T1		
Si9150DY-T1—E3		

PIN DESCRIPTION

Pin 1: EN

When this pin is low, the IC is shut down. After a low signal is applied to EN, then COMP, REF, R_T, and C_T settle toward ground; N-GATE, $\overline{\text{STBY}}$ and Soft-Start are grounded; and P-GATE is pulled high. The current consumption is no more than 100 μA in this state. This input's threshold has substantial hysteresis so that a capacitor to GND can be used to delay restart after the current limit is activated. After V_{ENH} is exceeded, one clock cycle elapses before N-GATE and P-GATE are enabled. EN is pulled up to V_{DD} through a 500-k resistor and is pulled down internally when the current limit is triggered.

Pin 2: $\overline{\text{STBY}}$

Has a function similar to EN. The differences are that the EN pin is unaffected, that the reference is still available, that bias currents are still present internally, and that this pin's pull up current is present. This pin should be used to disable an application if the reference voltage is still needed.

Pin 3: Soft-Start (SS)

This pin limits the maximum voltage that the error amplifier can output. A capacitor between this pin and ground will limit the rate at which the duty factor can increase during initial power up, during a restart when EN or $\overline{\text{STBY}}$ goes high, or after the current limit is triggered. A capacitor here can prevent an application from triggering the Si9150's current limit during startup. Soft-Start is pulled low if either EN or $\overline{\text{STBY}}$ is low.

Pin 4: Compensation (COMP)

This pin is tied directly to the output of the error amplifier. The feedback network which insures the stability of an application uses this pin. COMP settles low when either EN or $\overline{\text{STBY}}$ is pulled low.

Pin 5: Feedback (FB)

This pin is attached directly to the inverting input of the error amplifier. This pin is used to regulate the power supply's output voltage.

Pin 6: Reference (V_{REF})

The internal 2.5-V reference generator is attached to this pin through a 5-Ω resistor. A 0.1-μF bypass capacitor is needed to suppress noise. Also note that the generator has an open emitter; it will not pull down. The maximum current that the generator will source before it current limits is about 10 mA. Many parts of the IC use this voltage, so it is important not to overload the reference generator.

Pin 7: I_{SENSE}

This pin should be attached to the switched node (the drains of the application's p-channel and n-channel MOSFETs). If the voltage between V_{DD} and this pin is more then 0.46 V while the P-GATE is low, the current limit is activated. The current limit is relatively slow to prevent false triggering due to noise. Activating the current limit causes EN to be pulled to GND. I_{SENSE} may be operated from V_{DD} + 2 V to GND − 2 V. For operation above 13.5 V_{DD} a filter (1 kΩ, 33 pF) is needed between the MOSFET drains and the I_{SENSE} pin; refer to Figure 1.

Pin 8: $\overline{\text{SYNC}}$

This pin forces the clock to reset when low, and is also pulled low when the clock resets itself. Thus if several Si9150's have their sync pins shorted together, they will be synchronized; the shortest duration clock will control the other clocks.

Pin 9: C_T

A capacitor from this pin to ground is charged until it reaches 2.5 V, at which point the capacitor is rapidly discharged. The resulting sawtooth with about 1 V added is compared to the input voltage at COMP to determine whether P-GATE and N-GATE should be high or low. The maximum recommended value for C_{OSC} is 200 pF (See Typical Characteristics). The capacitor's charging current is controlled by Pin 10, R_T.

Pin 10: R_T

The IC applies 2.5 V to this pin, and the current is mirrored and applied to Pin 9 while charging the capacitor. The minimum recommended value of R_{OSC} is 20 kΩ (Figure 1).

Pin 11: GND

Since the Si9150 has a high-side current limit, it is important that V_{DD} track the voltage on the source of the p-channel power MOSFET. For noise immunity, it is best to separate the logic ground from the power ground. The logic ground should be decoupled to V_{DD} through at least a 1-μF capacitor. The two grounds may be connected by a path that is long compared to the the path from V_{DD} to the source of the application's p-channel MOSFET.

Pin 12: N-GATE

This pin is used to drive the application's n-channel MOSFET. When turning the n-channel MOSFET off, the p-channel MOSFET will not be turned on until N-GATE is within a few volts of ground. This pin is low while either EN or $\overline{\text{STBY}}$ is low.

Pin 13: P-GATE

This pin is used to drive the application's p-channel MOSFET. The break before make circuitry for the P-GATE is complimentary to that for the N-GATE. This pin is high while either EN or $\overline{\text{STBY}}$ is low.

Pin 14: V_{DD}

This pin powers the IC. The connection between this pin and the source of the p-channel FET should be as short as practical. Read Pin 11's description for bypassing suggestions.

APPLICATIONS

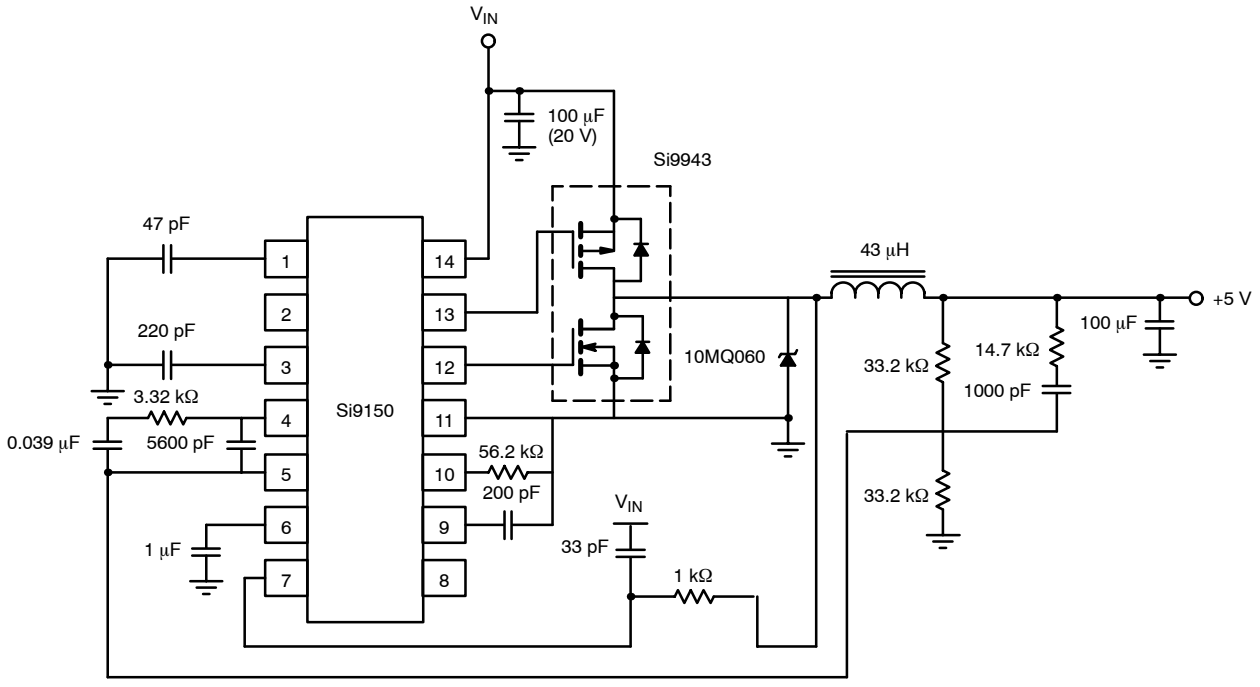


FIGURE 1. Typical Application Circuit

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