

## Low-Voltage Switchmode Controller

### FEATURES

- 2.7-V to 7-V Input Operating Range
- Voltage-Mode PWM Control
- High-Speed, Source-Sink Output Drive (200 mA)
- Internal Oscillator (up to 2 MHz)
- Standby Mode
- 0–100% Controllable Maximum Duty-Cycle

### DESCRIPTION

The Si9145 switchmode controller IC is ideally suited for high efficiency dc/dc converters in low input voltage systems. Operation is guaranteed down to 2.7 V, with a minimum start-up voltage of 3.0 V making the Si9145 ideal for use with NiCd, NMH, and lithium ion battery packs. A mode select pin allows the output driver polarity to be programmed allowing the device to function as a step-up or step-down converter.

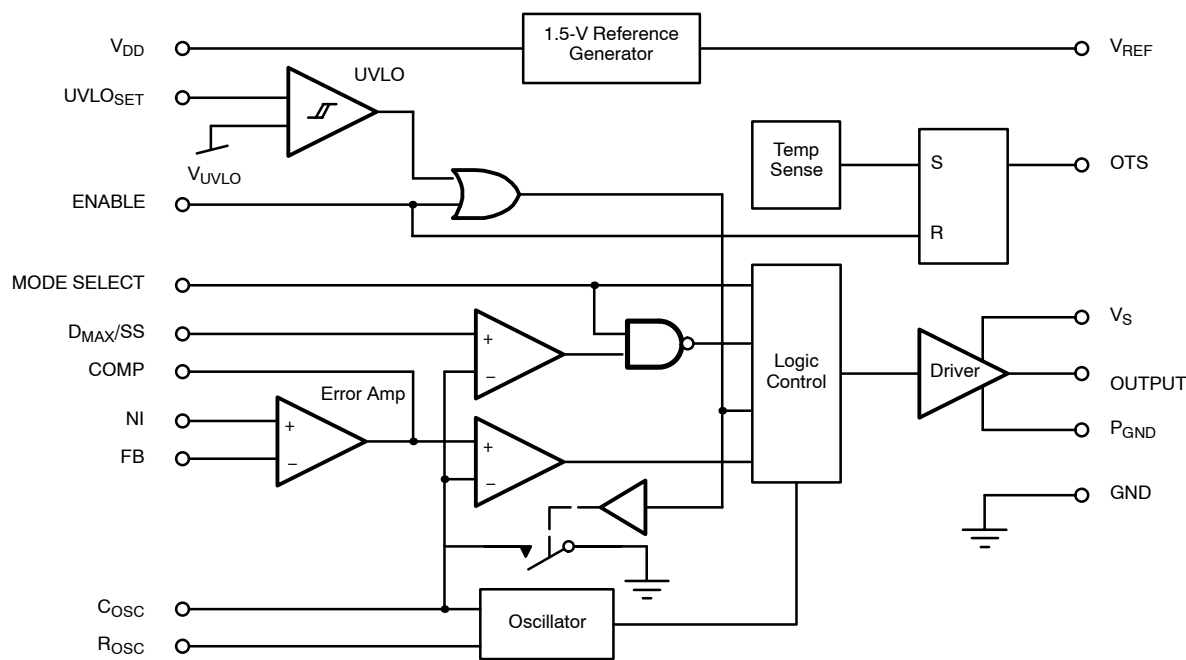
Features include a precision bandgap reference, a wide bandwidth error amplifier, a 2-MHz oscillator, an input voltage monitor with standby mode and a 200-mA output driver.

Supply current in normal operation is typically 1.1 mA and 250  $\mu$ A in standby mode.

The Si9145 implements conventional voltage mode control. The maximum duty cycle in boost mode can be limited by voltage on  $D_{MAX}/SS$  pin. Frequency can be externally programmed by selection of  $R_{OSC}$  and  $C_{OSC}$ .

The Si9145 is available in both standard and lead (Pb)-free 16-pin SOIC and TSSOP packages and is specified over the industrial temperature range ( $-25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ).

### FUNCTIONAL BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND.

$V_{DD}, V_S$	8 V
$P_{GND}$	$\pm 0.3$ V
$V_{DD}$ to $V_S$	-0.3 V
Linear Inputs	-0.3 V to $V_{DD}$ to +0.3 V
Logic Inputs	-0.3 V to $V_{DD}$ to +0.3 V
Continuous Output Current	100 mA
Storage Temperature	-65 to 125°C
Operating Junction Temperature	150°C

Power Dissipation (Package)<sup>a</sup>

16-Pin SOIC (Y Suffix) <sup>b</sup>	900 mW
16-Pin TSSOP (Q Suffix) <sup>c</sup>	925 mW

Thermal Impedance ( $\Theta_{JA}$ )

16-Pin SOIC	140°C/W
16-Pin TSSOP	135°C/W

Notes

- Device mounted with all leads soldered or welded to PC board.
- Derate 7.2 mW/°C above 25°C.
- Derate 7.4 mW/°C above 25°C.

## RECOMMENDED OPERATING RANGE

Voltages Referenced to GND.

$V_{DD}$	2.7 V to 7 V
$V_S$	2.7 V to 7 V
$f_{OSC}$	2 kHz to 2 MHz
$R_{OSC}$	5 k $\Omega$ to 250 k $\Omega$

$C_{OSC}$	47 pF to 200 pF
Linear Inputs	0 to $V_{DD}$
Digital Inputs	0 to $V_{DD}$
$V_{REF}$ Load Resistance	>150 k $\Omega$

SPECIFICATIONS							
Parameter	Symbol	Test Conditions Unless Otherwise Specified <sup>a</sup> $2.7\text{ V} \leq V_{DD} \leq 7\text{ V}, V_{DD} = V_S$ $GND = P_{GND}$		Limits B Suffix - 25 to 85°C			Unit
				Min <sup>b</sup>	Typ	Max <sup>b</sup>	
<b>Reference</b>							
Output Voltage	$V_{REF}$	$I_{REF} = -10\ \mu\text{A}$		1.455		1.545	V
			$T_A = 25^\circ\text{C}$	1.477	1.50	1.523	
<b>Oscillator</b>							
Maximum Frequency <sup>c</sup>	$f_{MAX}$	$V_{CC} = 3.0\text{ V}, C_{OSC} = 47\text{ pF}, R_{OSC} = 5.0\text{ k}\Omega$		2.0			MHz
Accuracy	$f_{OSC}$	$V_{CC} = 3.0\text{ V}$ $C_{OSC} = 100\text{ pF}, R_{OSC} = 6.98\text{ k}\Omega$	$T_A = 25^\circ\text{C}$	0.85	1.0	1.15	
$R_{OSC}$ Voltage	$V_{ROSC}$				1.0		V
Minimum Start-Up Voltage	$V_{DDOSC}$			3.0			
50% $D_{MAX}/SS$	$V_{D_{MAX} 50\%}$	MODE SELECT = $V_{DD}$			1.30		
100% $D_{MAX}/SS$	$V_{D_{MAX} 100\%}$				1.58		
$D_{MAX}/SS$ Input Current	$I_{D_{MAX}}$	$D_{MAX} = 0$ to $V_{DD}$		-100		100	nA
Voltage Stability <sup>c</sup>	$\Delta f/f$	$2.7\text{ V} \leq V_{DD} \leq 7\text{ V}, \text{Ref to } 4.8\text{ V}$		$T_A = 25^\circ\text{C}$	-16	16	%
		$2.7\text{ V} \leq V_{DD} \leq 4.2\text{ V}, \text{Ref to } 3.5\text{ V}$			-8	8	
		$3.8\text{ V} \leq V_{DD} \leq 5.6\text{ V}, \text{Ref to } 4.7\text{ V}$			-7	7	
Temperature Stability <sup>c</sup>		Referenced to 25°C			$\pm 5$		

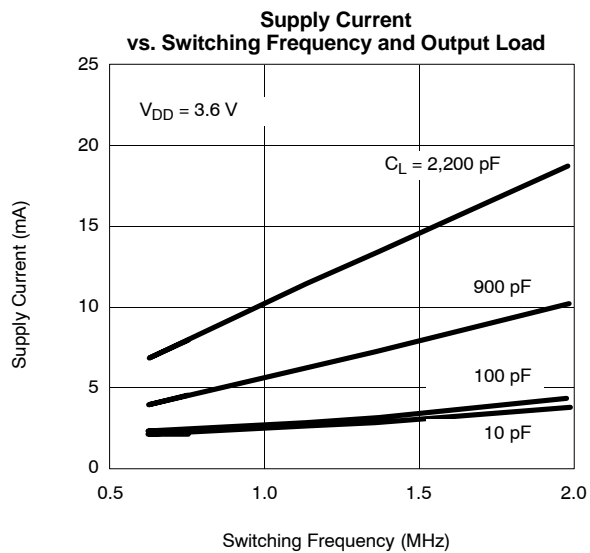
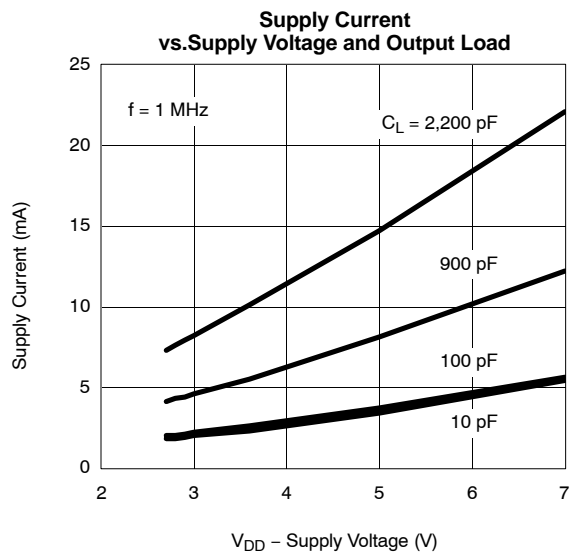
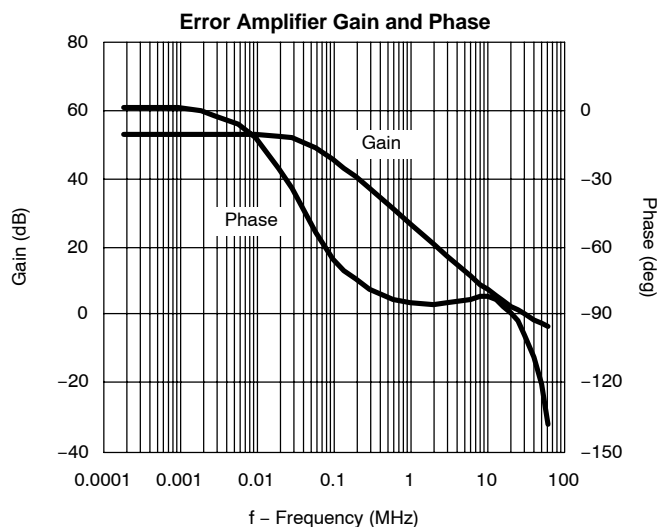
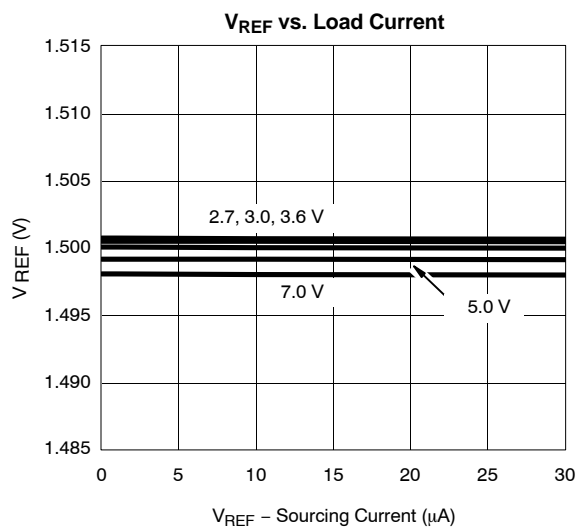
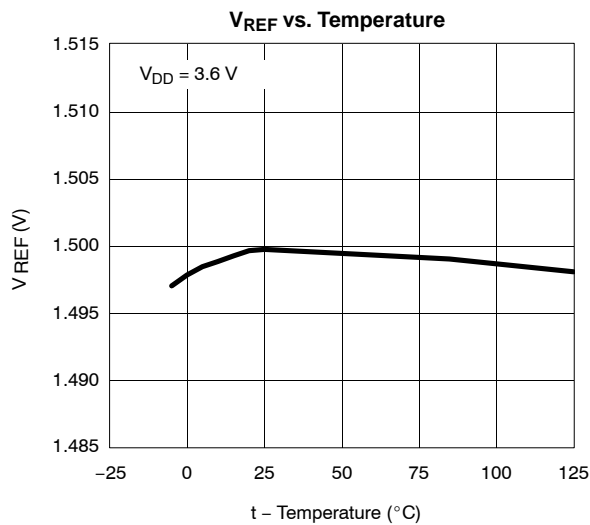
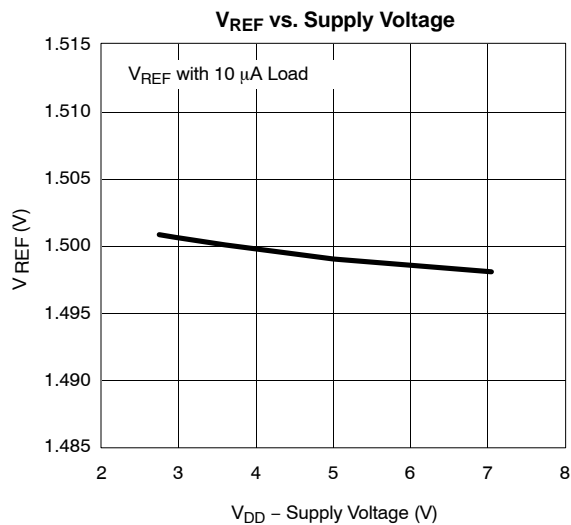


SPECIFICATIONS						
Parameter	Symbol	Test Conditions Unless Otherwise Specified <sup>a</sup> $2.7\text{ V} \leq V_{DD} \leq 7\text{ V}, V_{DD} = V_S$ $GND = P_{GND}$	Limits B Suffix – 25 to 85°C			Unit
			Min <sup>b</sup>	Typ	Max <sup>b</sup>	
<b>Error Amplifier (C<sub>OSC</sub> = GND, OSC DISABLED)</b>						
Input Bias Current	I <sub>FB</sub>	V <sub>NI</sub> = V <sub>REF</sub> , V <sub>FB</sub> = 1.0 V	-1.0		1.0	μA
Open Loop Voltage Gain	A <sub>VOL</sub>		47	55		dB
Offset Voltage	V <sub>OS</sub>	V <sub>NI</sub> = V <sub>REF</sub>	-15	0	15	mV
Unity Gain Bandwidth <sup>c</sup>	BW			10		MHz
Output Current	I <sub>EA</sub>	Source (V <sub>FB</sub> = 1 V, NI = V <sub>REF</sub> )		-2.0	-1.0	mA
		Sink (V <sub>FB</sub> = 2 V, NI = V <sub>REF</sub> )	0.4	0.8		
Power Supply Rejection <sup>c</sup>	P <sub>SRR</sub>	2.7 V < V <sub>DD</sub> < 7.0 V		60		dB
<b>UVLO<sub>SET</sub> Voltage Monitor</b>						
Under Voltage Lockout	V <sub>UVLOHL</sub>	UVLO <sub>SET</sub> High to Low	0.85	1.0	1.15	V
	V <sub>UVLOLH</sub>	UVLO <sub>SET</sub> Low to High		1.2		
Hysteresis	V <sub>HYS</sub>	V <sub>UVLOLH</sub> - V <sub>UVLOHL</sub>		200		mV
UVLO Input Current	I <sub>UVLO</sub>	V <sub>UVLO</sub> = 0 to V <sub>DD</sub>	-100		100	nA
<b>Output</b>						
Output High Voltage	V <sub>OH</sub>	V <sub>DD</sub> = 2.7 V, I <sub>OUT</sub> = -10 mA	2.55	2.60		V
Output Low Voltage	V <sub>OL</sub>	V <sub>DD</sub> = 2.7 V, I <sub>OUT</sub> = 10 mA		0.06	0.15	
Peak Output Current	I <sub>SOURCE</sub>	V <sub>DD</sub> = 2.7 V, V <sub>OUT</sub> = 0 V		-180	-130	mA
Peak Output Current	I <sub>SINK</sub>	V <sub>DD</sub> = 2.7 V, V <sub>OUT</sub> = 2.7 V	150	200		
<b>Logic</b>						
ENABLE Delay to Output	td <sub>EN</sub>	ENABLE Rising to OUTPUT		1.5		vs
ENABLE Logic Low	V <sub>ENL</sub>				0.2 V <sub>DD</sub>	V
ENABLE Logic High	V <sub>ENH</sub>		0.8 V <sub>DD</sub>			
ENABLE Input Current	I <sub>EN</sub>	ENABLE = 0 to V <sub>DD</sub>	-1.0		1.0	μA
MODE SELECT Logic Low	V <sub>MODEL</sub>				0.2 V <sub>DD</sub>	V
MODE SELECT Logic High	V <sub>MODEH</sub>		0.8 V <sub>DD</sub>			
MODE SELECT Input Current	I <sub>MODE</sub>	MODE SELECT = 0 to V <sub>DD</sub>	-1.0		1.0	μA
<b>Over Temperature Sense</b>						
Trip Point	T <sub>TRIP</sub>			150		°C
Output Low Voltage	V <sub>OTSL</sub>	V <sub>DD</sub> = 2.7 V, I <sub>OUT</sub> = 1 μA		0.06	0.15	V
Output High Voltage	V <sub>OTSH</sub>	V <sub>DD</sub> = 2.7 V, I <sub>OUT</sub> = -1 μA	2.55	2.6		
<b>Supply</b>						
Supply Current – Normal Mode	I <sub>DD</sub>	V <sub>DD</sub> = 2.7 V, f <sub>OSC</sub> = 1 MHz, R <sub>OSC</sub> = 6.98 kΩ		1.1	1.5	mA
		V <sub>DD</sub> = 7 V, f <sub>OSC</sub> = 1 MHz, R <sub>OSC</sub> = 6.98 kΩ		1.6	2.3	
Supply Current – Standby Mode		ENABLE = Low		250	330	μA

Notes

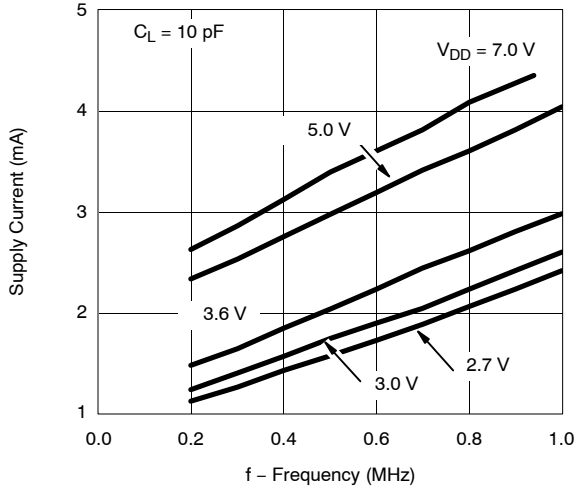
- a. C<sub>STRAY</sub> < 5 pF on C<sub>OSC</sub>. After Start-Up, V<sub>DD</sub> of ≥ 3 V.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production testing.

**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**

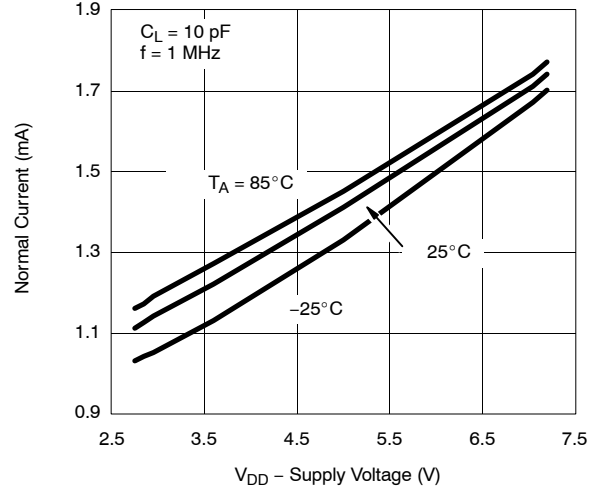


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

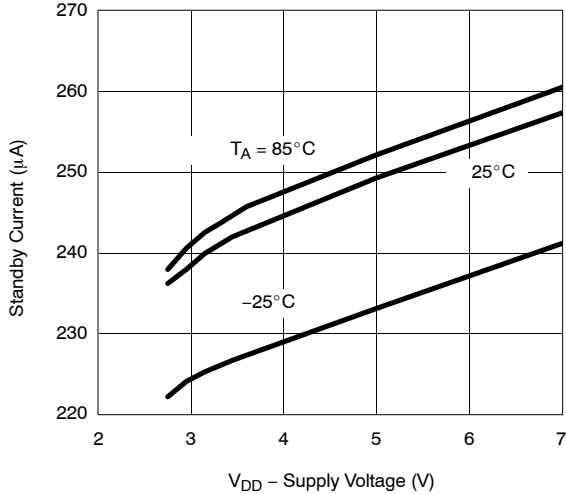
**Supply Current vs. Frequency and Supply Voltage**



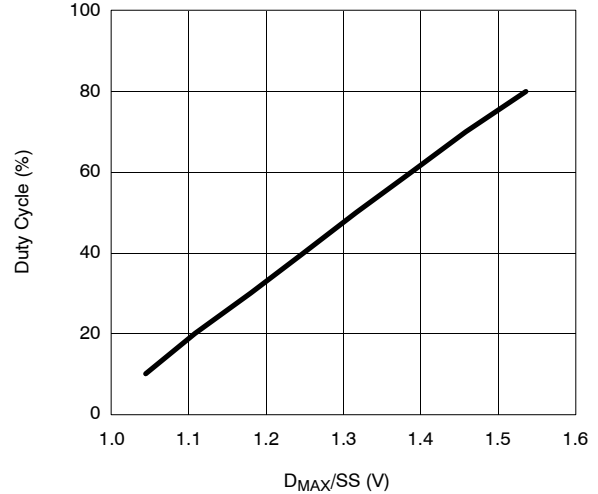
**Supply Current vs. Supply Voltage and Temperature**



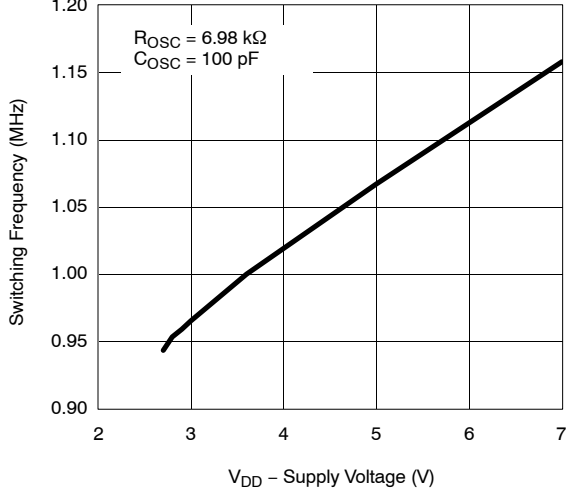
**Standby Current vs. Supply Voltage and Temperature**



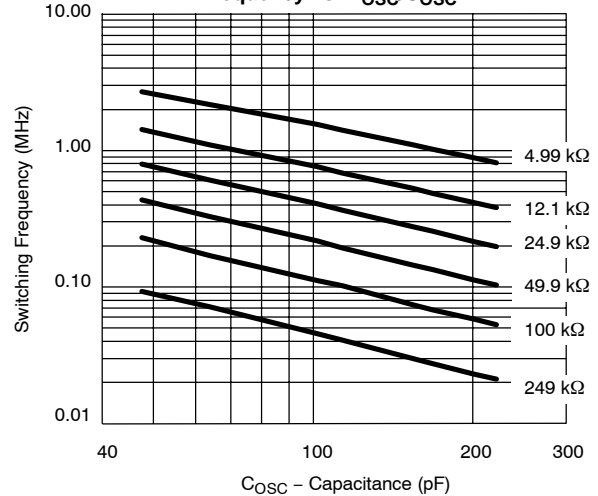
**Duty Cycle vs. DMAX/SS Voltage**



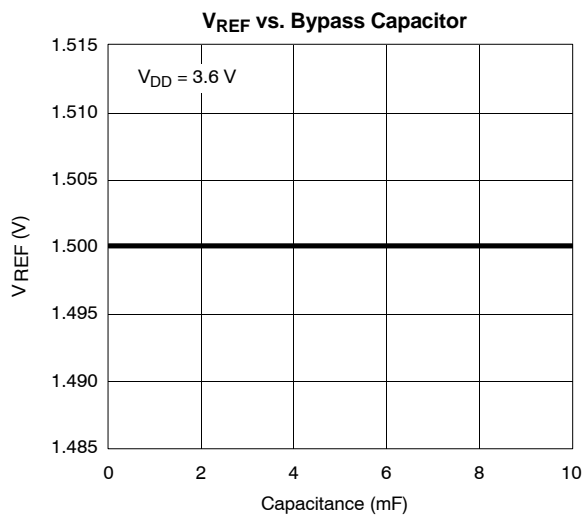
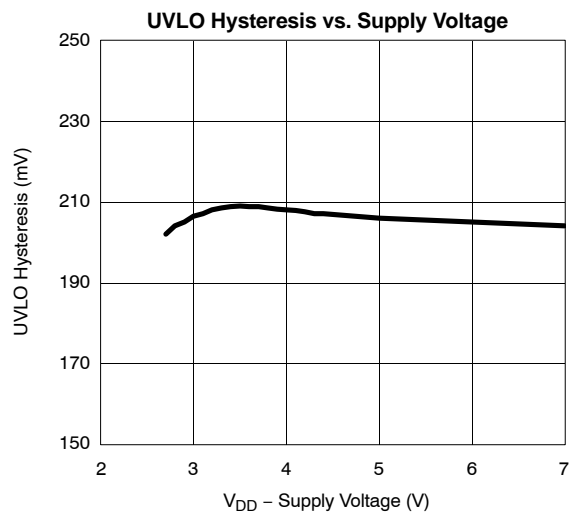
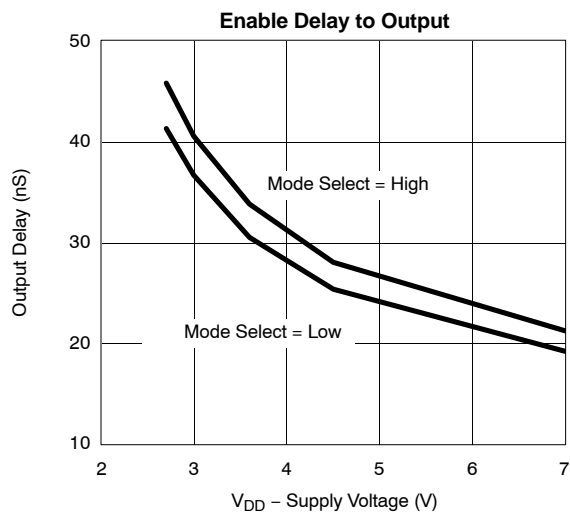
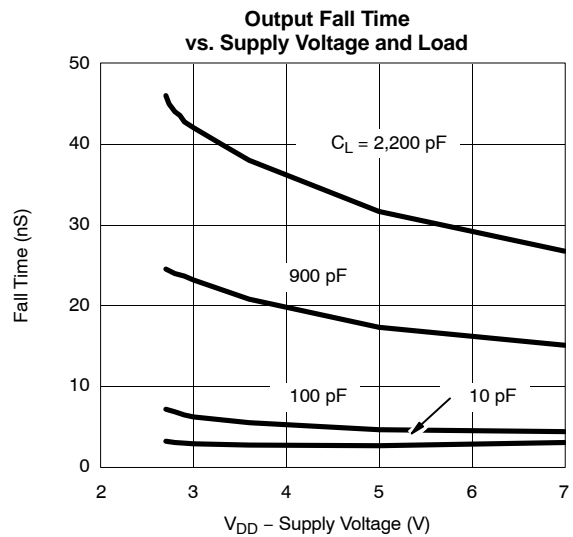
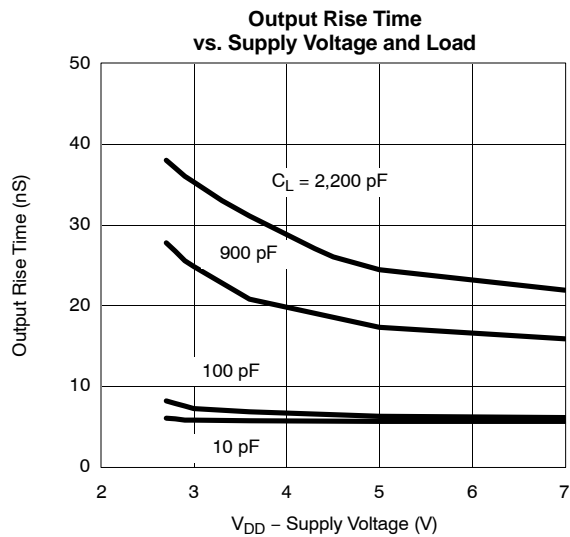
**Switching Frequency vs. Supply Voltage**



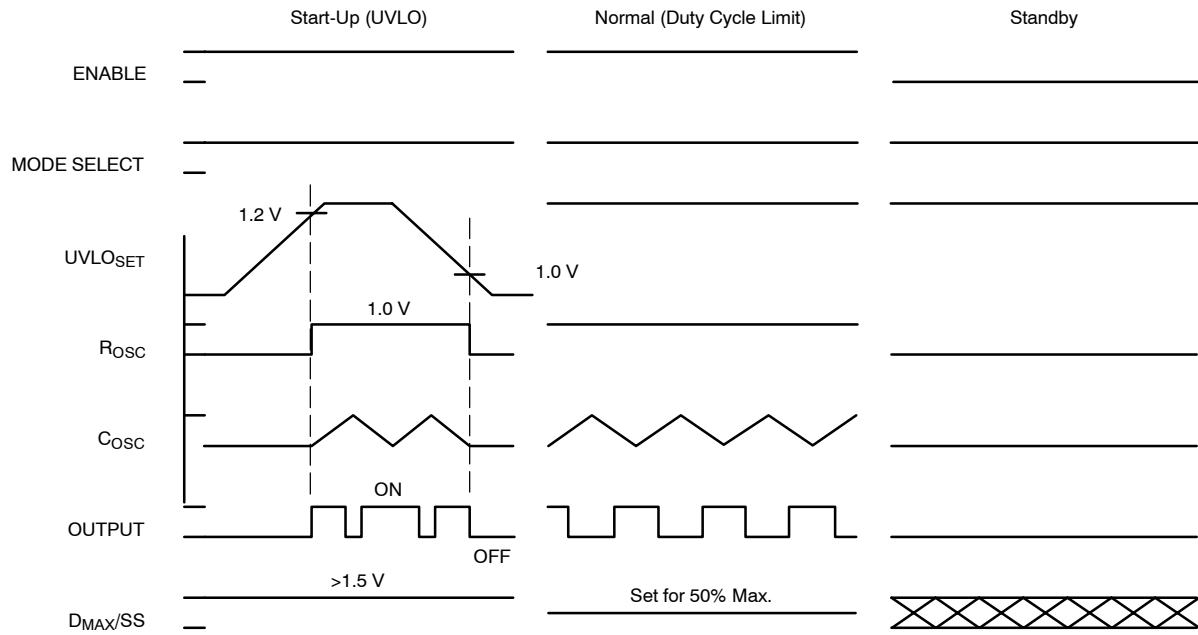
**Frequency vs. ROSC/COSC**



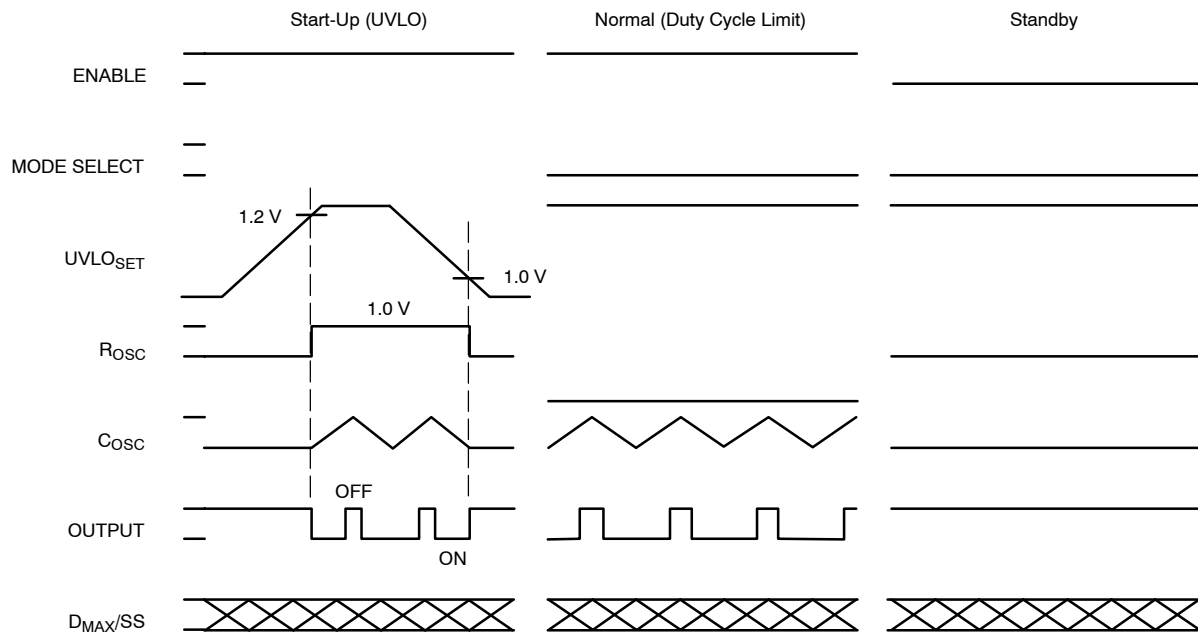
**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



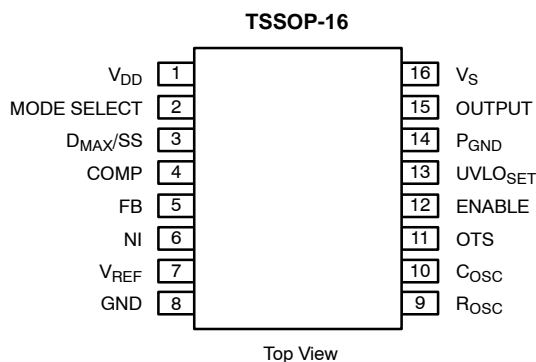
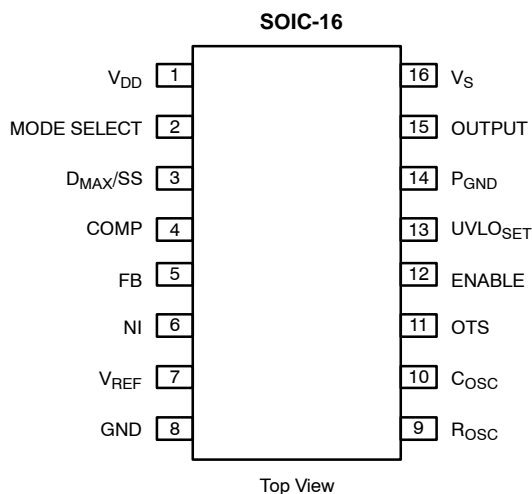
**TIMING WAVEFORMS**



**Figure 1.** Si9145 Timing Diagram (MODE SELECT = High)



**Figure 2.** Si9145 Timing Diagram (MODE SELECT = Low)

**PIN CONFIGURATIONS**

**ORDERING INFORMATION-SOIC-16**

Part Number	Temperature Range
Si9145BY-T1	-25° to 85°C
Si9145BY-T1—E3	

**ORDERING INFORMATION-TSSOP-16**

Part Number	Temperature Range
Si9145BQ-T1	-25° to 85°C
Si9145BQ-T1—E3	

**PIN DESCRIPTION**
**Pin 1: V<sub>DD</sub>**

The positive power supply for all functional blocks except output driver. A bypass capacitor of 0.1  $\mu$ F (minimum) is recommended.

**Pin 2: MODE SELECT**

This pin is used to enable maximum duty cycle limit and set output polarity of controller. When connected to V<sub>DD</sub>, the maximum duty cycle function is controlled by the D<sub>MAX</sub>/SS pin. The maximum duty cycle limit is usually used for forward, flyback, and boost converters. The output polarity is high when the PWM circuitry requires the external device to be turned on.

When connected to GND, the maximum duty cycle is not limited (usually for buck converters driving a p-channel MOS). The output polarity is low when the PWM circuitry requires the external PMOS to be turned on.

**Pin 3: D<sub>MAX</sub>/SS**

D<sub>MAX</sub>/SS pin controls the maximum duty cycle achievable by the PWM circuitry when the MODE SELECT = V<sub>DD</sub>.

When D<sub>MAX</sub>/SS is at less than 1.0 V (typical) the OUTPUT is held low (0% duty cycle). When D<sub>MAX</sub>/SS is at more than 1.5 V (typical), the PWM circuitry can achieve 100% duty cycle. With

voltage at D<sub>MAX</sub>/SS between 1.0 V and 1.5 V, the maximum duty cycle is proportionally limited to this voltage.

The addition of external components can implement a soft start function.

**Pin 4: COMP**

This pin is the output of the error amplifier. A compensation network is connected from this pin to the FB pin to stabilize the system. This pin drives one input of the internal pulse width modulation comparator.

**Pin 5: FB**

The inverting input of the error amplifier. External resistors are connected to this pin to set the regulated output voltage. The compensation network is also connected to this pin.

**Pin 6: NI**

The non-inverting input of the error amplifier. In normal operation it is externally connected to the V<sub>REF</sub> pin.

**Pin 7: V<sub>REF</sub>**

This pin supplies 1.5 V trimmed to  $\pm 1.5\%$ . The reference voltage is generated by a band-gap reference.

**Pin 8: GND**

Negative return for V<sub>DD</sub>.



**Pin 9: R<sub>osc</sub>**

This pin is the equivalent of a 1.0-V voltage source derived from the on-chip  $V_{REF}$ . When a low T.C. resistor is externally connected from this pin to GND, a temperature independent current is generated internally. This current is used as the charging current source connected to the  $C_{OSC}$  pin. The current is internally multiplied by 2 and is used as the discharging current source connected to the  $C_{OSC}$  pin. Therefore, the external resistor is one of the factors that determine the oscillator frequency.

**Pin 10: C<sub>osc</sub>**

An external capacitor is connected to this pin to set the oscillator frequency. Internal current sources alternately charge and discharge the external capacitor. The oscillator waveform is a symmetrical triangular type with a typical voltage swing between 1.0 V and 1.5 V.

$$f_{osc} \approx \frac{0.7}{R_{osc} * C_{osc}}$$

**Pin 11:  $\overline{OTS}$** 

This pin indicates an over-temperature condition on the device when the output is low. The output is latched low and is reset with the ENABLE pin going low then high, or by turning power off and on.

**Pin 12: ENABLE**

A logic high on this pin allows normal operation. A logic low places the chip in the standby mode. In standby mode normal operation is disabled, supply current is reduced, the oscillator stops and the output is held high for MODE SELECT = low, and low for MODE SELECT = high.

**Pin 13: UVLO<sub>SET</sub>**

This pin will place the chip in the standby mode if the UVLO<sub>SET</sub> voltage drops below 1.2 V. Once the UVLO<sub>SET</sub> voltage exceeds 1.2 V, the chip operates normally. There is a built-in hysteresis of 200 mV.

**Pin 14: P<sub>GND</sub>**

The negative return for the  $V_S$  supply.

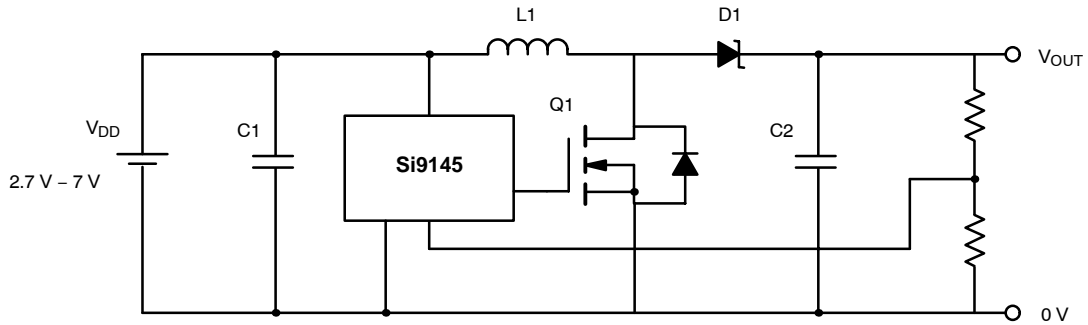
**Pin 15: OUTPUT**

This CMOS push-pull output pin drives the external MOSFET and is capable of sinking 150 mA or sourcing 130 mA with  $V_S$  equal to 2.7 V.

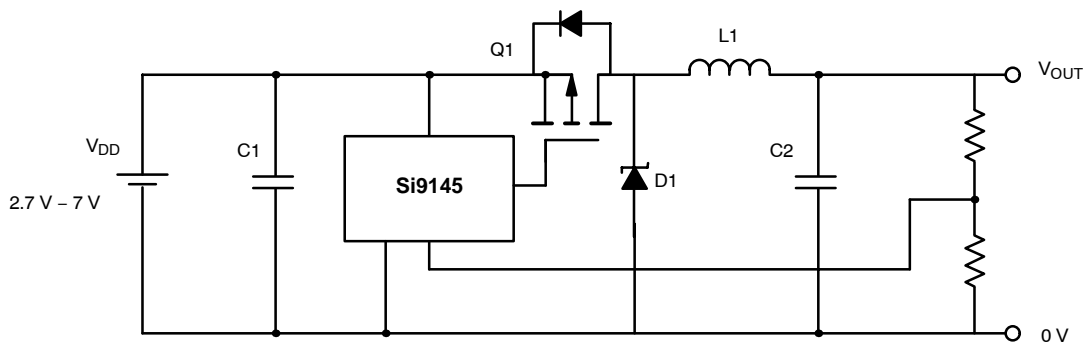
**Pin 16:  $V_S$** 

The positive terminal of the power supply which powers the CMOS output driver. A bypass capacitor is required.

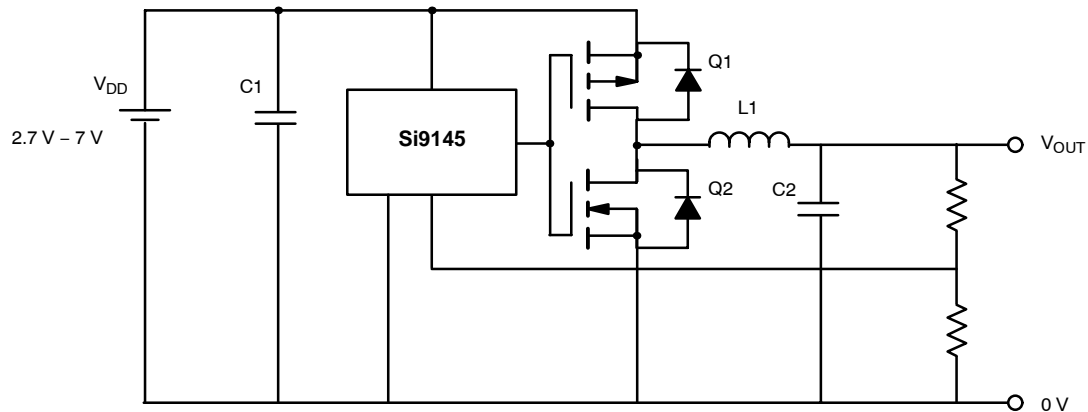
**APPLICATIONS**



**Figure 3.** Non-Isolated Step Up Boost Converter for  $V_{OUT} > V_{IN}$



**Figure 4.** Non-Isolated Step Down Buck Converter for  $V_{OUT} < V_{IN}$



**Figure 5.** Non-Isolated Synchronous Buck Converter for  $V_{OUT} < V_{IN}$



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