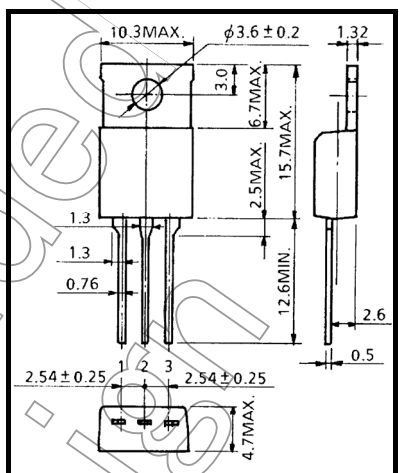
TOSHIBA BI−DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM12G45, SM12J45, SM12G45A, SM12J45A

AC POWER CONTROL APPLICATIONS

- Repetitive Peak Off−State Voltage : V_{DRM} = 400V, 600V
- R.M.S On−State Current : $I_{T\ (RMS)}$ = 12A
- High Commutating (dv / dt)

Unit: mm



1. T1
2. T2 (HEAT SINK)
3. GATE

JEDEC	TO-220AB
JEITA	—
TOSHIBA	13-10G1A

Weight: 2.0 g (typ.)

ABSOLUTE MAXIMUM RATINGS

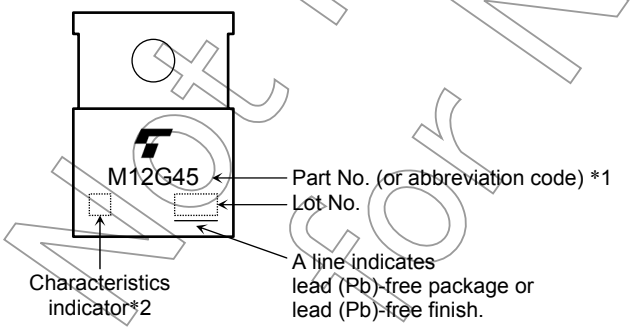
CHARACTERISTIC		SYMBOL	RATING	UNIT
Repetitive Peak Off−State Voltage	SM12G45 SM12G45A	V_{DRM}	400	V
	SM12J45 SM12J45A		600	
R.M.S On−State Current (Full Sine Waveform Tc = 98°C)		$I_{T\ (RMS)}$	12	A
Peak One Cycle Surge On−State Current (Non−Repetitive)		I_{TSM}	120 (50Hz)	A
			132 (60Hz)	
I^2t Limit Value (t = 1~10ms)		I^2t	72	A^2s
Critical Rate of Rise of On−State Current		di / dt	50	A / μs
Peak Gate Power Dissipation		P_{GM}	5	W
Average Gate Power Dissipation		$P_{G\ (AV)}$	0.5	W
Peak Gate Voltage		V_{GM}	10	V
Peak Gate Current		I_{GM}	2	A
Junction Temperature		T_j	−40~125	°C
Storage Temperature Range		T_{stg}	−40~125	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

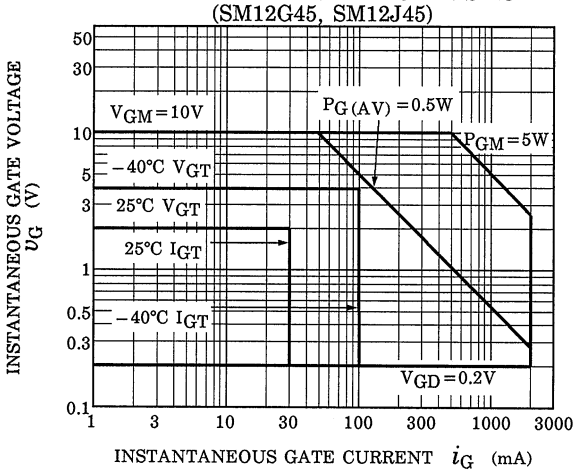
CHARACTERISTIC			SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Repetitive Peak Off−State Current			I_{DRM}	V_{DRM}=Rated, T_j = 125°C		—	—	2	mA
Gate Trigger Voltage	SM12G45 SM12J45	I	V_{GT}	V_D = 12V, R_L = 20Ω	T2 (+) , Gate (+)	—	—	2	V
		II			T2 (+) , Gate (−)	—	—	2	
		III			T2 (−) , Gate (−)	—	—	2	
		IV			T2 (−) , Gate (+)	—	—	—	
	SM12G45A SM12J45A	I			T2 (+) , Gate (+)	—	—	1.5	
		II			T2 (+) , Gate (−)	—	—	1.5	
		III			T2 (−) , Gate (−)	—	—	1.5	
		IV			T2 (−) , Gate (+)	—	—	—	
Gate Trigger Current	SM12G45 SM12J45	I	I_{GT}	V_D = 12V, R_L = 20Ω	T2 (+) , Gate (+)	—	—	30	mA
		II			T2 (+) , Gate (−)	—	—	30	
		III			T2 (−) , Gate (−)	—	—	30	
		IV			T2 (−) , Gate (+)	—	—	—	
	SM12G45A SM12J45A	I			T2 (+) , Gate (+)	—	—	20	
		II			T2 (+) , Gate (−)	—	—	20	
		III			T2 (−) , Gate (−)	—	—	20	
		IV			T2 (−) , Gate (+)	—	—	—	
Peak On−State Voltage			V_{TM}	I_{TM} = 17A		—	—	1.5	V
Gate Non−Trigger Voltage			V_{GD}	V_D = Rated, Tc = 125°C		0.2	—	—	V
Holding Current			I_H	V_D = 12V, I_{TM} = 1A		—	—	50	mA
Thermal Resistance			$R_{th\ (j-c)}$	Junction to Case, AC		—	—	1.8	°C / W
Critical Rate of Rise of Off−State Voltage at Commutation	SM12G45 SM12J45		(dv / dt) c	V_{DRM} = 400V (di / dt) c = − 6.5A / ms		10	—	—	V / μs
	SM12G45A SM12J45A					4	—	—	

MARKING

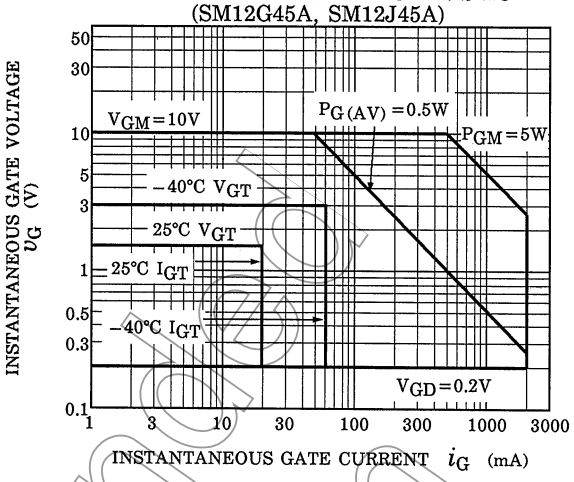


	Part No. (or abbreviation code)	Part No.
*1	M12G45	SM12G45, SM12G45A
	M12J45	SM12J45, SM12J45A
*2	A	SM12G45A,SM12J45A

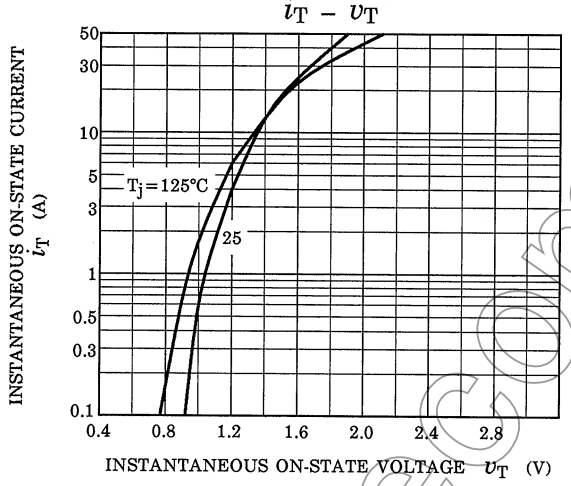
GATE TRIGGER CHARACTERISTIC
(SM12G45, SM12J45)



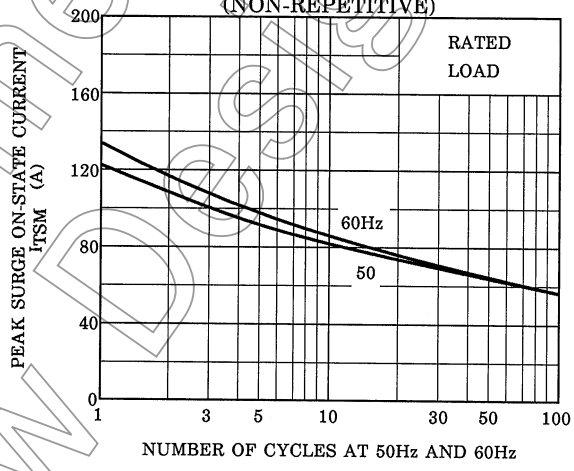
GATE TRIGGER CHARACTERISTIC
(SM12G45A, SM12J45A)



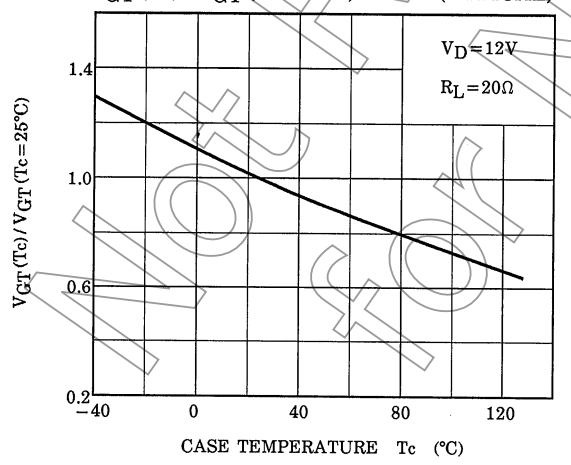
$i_T - v_T$



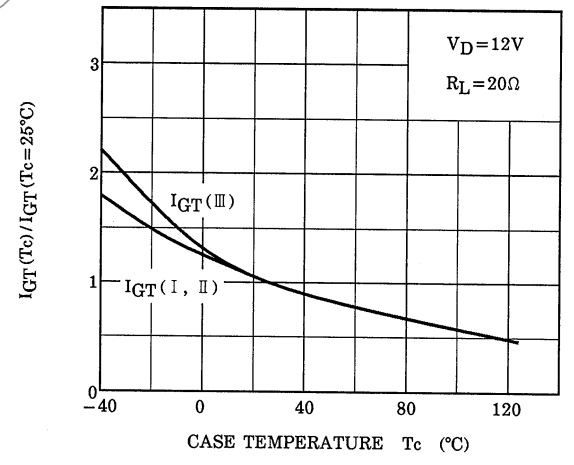
SURGE ON-STATE CURRENT
(NON-REPETITIVE)



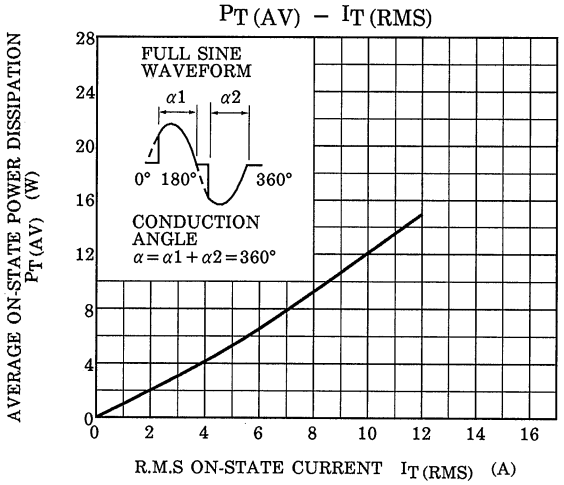
V_{GT} (Tc) / V_{GT} (Tc = 25°C) − Tc (TYPICAL)



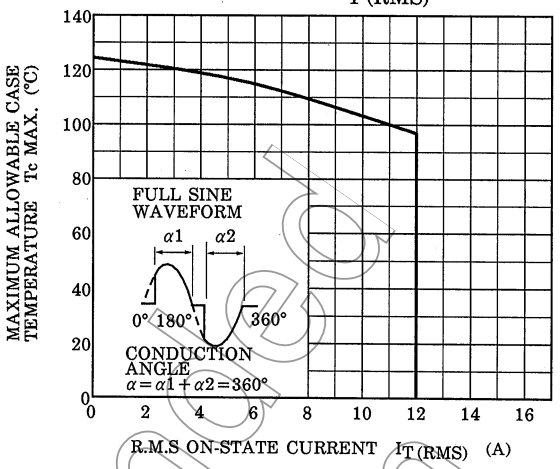
I_{GT} (Tc) / I_{GT} (Tc = 25°C) − Tc (TYPICAL)



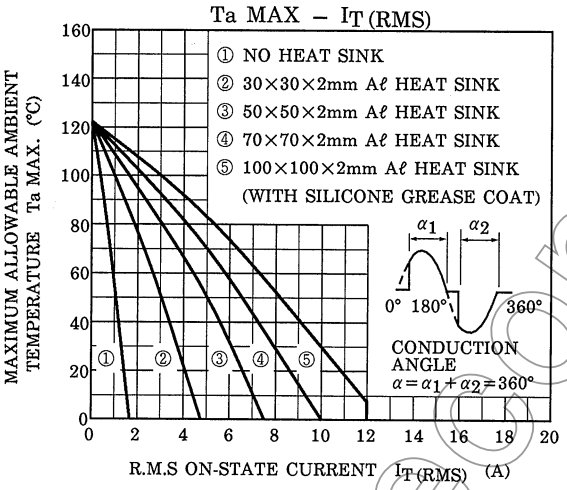
$P_{T(AV)}$ – $I_{T(RMS)}$



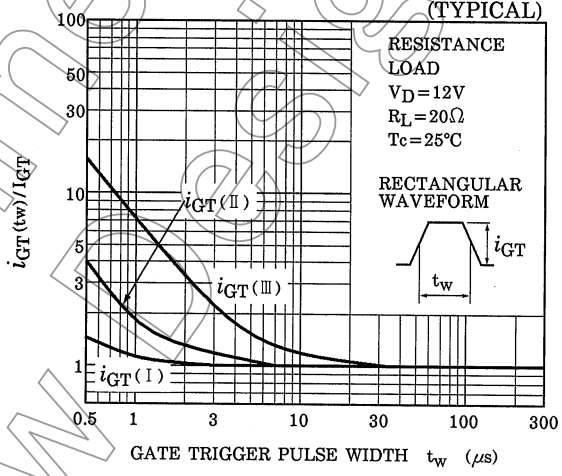
Tc MAX – $I_{T(RMS)}$



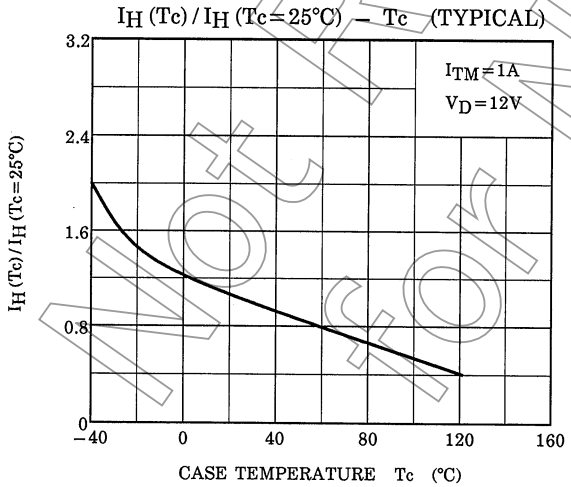
Ta MAX – $I_{T(RMS)}$



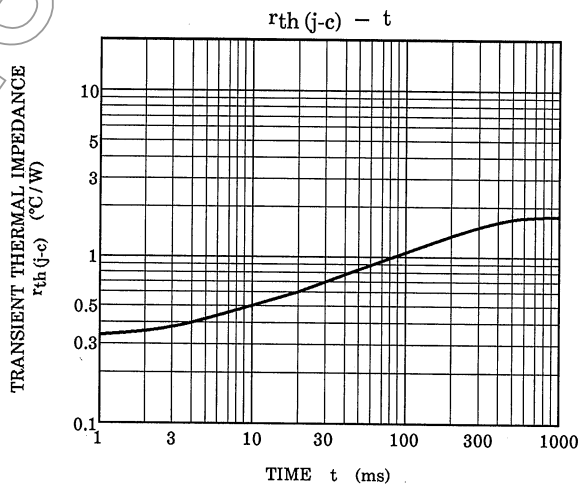
PULSE TRIGGER CHARACTERISTIC (TYPICAL)



I_H (Tc) / I_H (Tc=25°C) – Tc (TYPICAL)



$r_{th(j-c)}$ – t



RESTRICTIONS ON PRODUCT USE

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