ProASIC to SX-A PQ208 Prototyping Adapter Board

User Document for P/N SI-SXA-APAPQ208-KIT

December 2003

Introduction

The SI-SXA-APAPQ208 adapter board is a prototyping tool that maps the footprint of an Actel ProASIC device in a PQFP208 package on the top to the footprint of an Actel SX-A device on the bottom. Using this adapter board, designs targeted for production in an SX-A FPGA can be prototyped using the re-programmable ProASIC family.

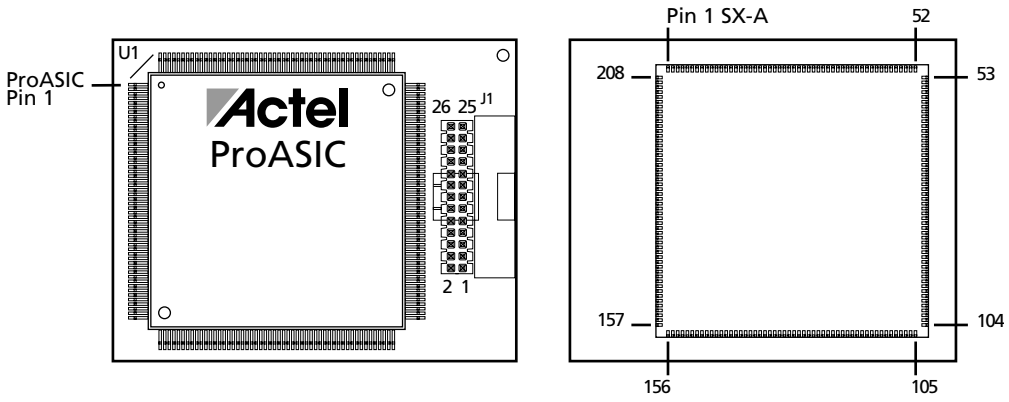


Figure 1: SI-SXA-APAPQ208 Top and Bottom View Drawings

The SI-SXA-APAPQ208 adapter board is manufactured by Ironwood. The complete SI-SXA-APAPQ208-KIT adapter board solution is a two-piece product consisting of a top “adapter board” and a bottom “foot”. The foot portion maps directly to the PQ208 footprint of an SX-A device and should be soldered directly to a system PCB. The top adapter board portion attaches to the foot through a PGA-like interconnecting grid. A ProASIC A500K130-PQ208I device is attached onto the top adapter board piece. A small ISP header is provided with the adapter, and the FlashPro programmer can be connected directly to the top adapter board for programming the ProASIC device. The pins of the ProASIC device are mapped down to the corresponding SX-A pin connections on the system board.

The SI-SXA-APAPQ208-KIT consists of:

Actel Part Number	Ironwood Part Number	Component
SI-SXA-APAPQ208-A	C4654	top adapter board
SI-SXA-APAPQ208-B	C4741	bottom foot
SMPA-ISP-HEADER-S	n/a	Small ISP header

This two-piece prototyping adapter board solution allows the top adapter board to be mobile and re-used as required during the prototyping stage of design development. The top adapter board can be used to prototype any SX-A design in the PQ208 package, as it can be easily attached and detached from multiple “feet” placed on a system board, and can be re-programmed as needed to verify multiple designs.

ProASIC to SX-A Pin Mapping Connections

Following are pin mapping connections for the SI-SXA-APAPQ208 adapter board.

Table 1 on page 4 lists the I/O pin mapping between the ProASIC device on top and the SX-A device on the bottom. When prototyping in ProASIC, the I/O connections for the target SX-A device should be mapped to the ProASIC PQ208 according to Table 1. By default, the adapter board comes with a ProASIC

A500K130-PQ208I device and is qualified to run at industrial temperature range. The bottom SX-A footprint can be targeted to any SX-A family member (e.g. SX08A, SX16A, SX32A, or SX72A). As some subtle differences in the pin assignments exist for the different SX-A family members, please refer to the table below to ensure the pin mapping is properly managed.

Table 2 on page 7 lists the pin-out for the programming header included with the top adapter board.

Table 3 on page 7 through Table 7 on page 8 list the connections for all power and ground connections between the SX-A and ProASIC device. This is shown for information only, and users do not have to make any modifications in the V_{CC}/GND connections on their board. As long as the system board provides normal power and ground connections to the pins of the bottom SX-A footprint, the signals are automatically mapped to the correct ProASIC pins through the adapter board.

Important I/O Considerations for Mapping Designs from SX-A to ProASIC

Key to Signal Mapping Notes in Table 1

(**NC:**	No Connect Pin)	**–:**	A54SX32A NC	**V:**	A54SX72A V_{CC}
+:	A54SX08A NC	**Q:**	A54SX72A QCLK	**A:**	SX-A Probe A
x:	A54SX16A NC	**G:**	A54SX72A GND	**B:**	SX-A Probe B

The following I/Os are *not* mapped in the adapter: **SX-A Pins 67, 106, 155, 156, 167, 170, and 173.**

Note: These I/Os can still be used in the transition from the adapter to SX-A device. These seven pins are NC for the A54SX08A, but are available as user I/Os for other SX-A devices.

SX-A Pins 25 and 132 are NC for all SX-A devices except A54SX72A. Pin 132 is NOT mapped in the adapter board, but Pin 25 is available for use with the adapter board.

SX-A Pin 189 is NC for A54SX08A and I/O for all other SX-A devices. Pin 189 is mapped in the adapter board and is available for use with the adapter board.

SX-A Pins 80 and 182 are NC for all SX-A devices.

Pin Mapping for A500K (Top) to SX-A (Bottom)

Table 1: Pin Mapping

Signal	A500K	SX-A
I/O_2	2	53
I/O_3	3	54
I/O_4	4	55
I/O_5	5	56
I/O_6	6	57
I/O_7	7	58
I/O_8	8	59
I/O_9	9	61^{+}
I/O_10	10	62
I/O_11	11	63
I/O_12	12	64^{+}
I/O_13	13	65^{-}
I/O_14	14	66
I/O_15	15	68
I/O_18	18	69
I/O_19	19	70^{+}
I/O_20	20	71
I/O_21	21	72
I/O_23	23	73^{+}
I/O_24	24	74^{Q}
GL_0	25	84^{Q}
GL_1	26	82
I/O_27	27	76^{B}
I/O_28	28	81
I/O_30	30	75^{+}
I/O_31	31	83^{V}
I/O_32	32	85^{+}
I/O_33	33	86
I/O_34	34	87
I/O_35	35	88^{+}
I/O_37	37	89
I/O_38	38	90
I/O_39	39	91^{+}
I/O_42	42	92
I/O_43	43	93
I/O_44	44	94^{+}

Table 1: Pin Mapping (Continued)

Signal	A500K	SX-A
I/O_45	45	95
I/O_46	46	96
I/O_47	47	97^{+}
I/O_48	48	99
I/O_49	49	100
I/O_50	50	101
I/O_51	51	102
I/O_54	54	104
I/O_55	55	107
I/O_56	56	108^{+}
I/O_57	57	109
I/O_58	58	110
I/O_59	59	111
I/O_60	60	112
I/O_61	61	113
I/O_62	62	116^{+G}
I/O_63	63	117^{V}
I/O_64	64	118
I/O_66	66	119^{+}
I/O_67	67	120
I/O_68	68	121
I/O_69	69	122^{+}
I/O_70	70	123
I/O_73	73	124
I/O_74	74	125^{+}
I/O_75	75	126
I/O_76	76	127
I/O_77	77	128
I/O_78	78	133
I/O_79	79	134
I/O_80	80	135^{+}
I/O_82	82	136
I/O_83	83	137
I/O_84	84	138^{+}
I/O_85	85	139
I/O_86	86	140

Table 1: Pin Mapping (Continued)

Signal	A500K	SX-A
I/O_87	87	141+
I/O_90	90	142
I/O_91	91	143+
I/O_92	92	144
I/O_93	93	147
I/O_94	94	149
I/O_95	95	150
I/O_96	96	151
I/O_98	98	152
I/O_99	99	153
I/O_100	100	154
TRST, I/O_109	109	30
I/O_111	111	158
I/O_112	112	159
I/O_113	113	161
I/O_114	114	162
I/O_115	115	163
I/O_116	116	165
I/O_117	117	166
I/O_118	118	168
I/O_119	119	169
I/O_120	120	171
I/O_121	121	172
I/O_124	124	174
I/O_125	125	175
I/O_127	127	176+
I/O_128	128	177
I/O_129	129	178Q
I/O_131	131	179
I/O_132	132	186A
GL_2	133	180
GL_3	134	181
I/O_135	135	187V
I/O_136	136	188
I/O_137	137	190Q
I/O_139	139	191
I/O_140	140	192+

Table 1: Pin Mapping (Continued)

Signal	A500K	SX-A
I/O_143	143	193
I/O_144	144	194
I/O_145	145	195+
I/O_146	146	196
I/O_147	147	197
I/O_148	148	198+
I/O_149	149	199
I/O_150	150	200
I/O_151	151	202+
I/O_152	152	203+
I/O_153	153	204
I/O_154	154	205+
I/O_155	155	206
I/O_158	158	189+
I/O_159	159	207
I/O_160	160	3
I/O_161	161	4+
I/O_163	163	5
I/O_164	164	6+
I/O_165	165	7
I/O_166	166	8
I/O_167	167	9
I/O_168	168	10
I/O_169	169	13
I/O_172	172	14+
I/O_173	173	15
I/O_174	174	16
I/O_175	175	17+
I/O_176	176	18G
I/O_177	177	19V
I/O_179	179	20+
I/O_180	180	21
I/O_181	181	22
I/O_182	182	23+
I/O_183	183	24
I/O_184	184	25+x-
I/O_185	185	29

Table 1: Pin Mapping (Continued)

Signal	A500K	SX-A
I/O_188	188	31+
I/O_189	189	32
I/O_190	190	33
I/O_191	191	34
I/O_192	192	35+
I/O_193	193	36
I/O_194	194	37
I/O_196	196	38
I/O_197	197	39+
I/O_198	198	42
I/O_199	199	43
I/O_200	200	44
I/O_201	201	45
I/O_202	202	46
I/O_203	203	47
I/O_204	204	48+
I/O_205	205	49
I/O_206	206	50+
I/O_207	207	51

Programming Header Connections

Table 2: Programming Header Connections

Signal Name	A500K	SX-A	Header
VDDL_PROG	–	–	J1.1
VDDL_NORMAL	–	–	J1.2
VDDL_PROG	–	–	J1.3
VDDL_NORMAL	–	–	J1.4
VDDL_PROG	–	–	J1.5
VDDL_NORMAL	–	–	J1.6
RCK	110	160	J1.7
TMS	103	11	J1.9
TDO	108	103	J1.11
TDI	102	2	J1.13
TCK	101	208	J1.15
Ground	–	–	J1.17
Ground	–	–	J1.18
VPN	107	–	J1.19
Ground	–	–	J1.20
VPP	106	–	J1.21
VDDP_NORMAL	–	–	J1.22
VDDP_PROG	–	–	J1.23
VDDP_NORMAL	–	–	J1.24
VDDP_PROG	–	–	J1.25
VDDP_NORMAL	–	–	J1.26

Voltage Connections

Table 3: V_{DDL} Connections

J1.1	ProASIC 16	ProASIC 88	ProASIC 171
J1.3	ProASIC 36	ProASIC 126	ProASIC 187
J1.5	ProASIC 71	ProASIC 142	

VDDL_PROG

The signals above are V_{DDL} (Logic Array Voltage) connections to the ProASIC device and the programming header. These signals are mapped to the appropriate SX-A V_{CCA} (SX-A Logic Array Voltage) pins through the adapter board. Note that the SX-A V_{CCA} and ProASIC V_{DDL} supplies are both 2.5V.

Table 4: V_{CCA} Connections

J1.2	SX-A 27	SX-A 114	SX-A 184
J1.4	SX-A 41	SX-A 130	
J1.6	SX-A 78	SX-A 145	

VDDL_NORMAL

The signals above are V_{CCA} connections to the SX-A device and the programming header. These signals are also mapped to the appropriate ProASIC V_{DDL} pins through the adapter board. Note that the SX-A V_{CCA} and ProASIC V_{DDL} supplies are both 2.5V.

Table 5: V_{CCI} Connections

J1.22	SX-A 12	SX-A 98	SX-A 164
J1.24	SX-A 40	SX-A 115	SX-A 201
J1.26	SX-A 60	SX-A 148	

VDDP_NORMAL

The signals above are the V_{CCI} connections to the SX-A device. Note that the SX-A V_{CCI} and ProASIC V_{DDP} both supply voltage to the I/O ring.

Table 6: V_{DDP} Connections

J1.23	ProASIC 53	ProASIC 123	ProASIC 186
J1.25	ProASIC 72	ProASIC 138	ProASIC 208
ProASIC 22	ProASIC 89	ProASIC 157	
ProASIC 40	ProASIC 104	ProASIC 170	

VDDP_PROG

The signals above are V_{DDP} connections to the ProASIC device. Note that the SX-A V_{CCI} and ProASIC V_{DDP} both supply voltage to the I/O ring.

Table 7: GROUND Connections

J1.17	ProASIC 65	ProASIC 162	SX-A 79
J1.18	ProASIC 81	ProASIC 178	SX-A 105
J1.20	ProASIC 97	ProASIC 195	SX-A 129
ProASIC 1	ProASIC 105	SX-A 1	SX-A 131
ProASIC 17	ProASIC 122	SX-A 26	SX-A 146
ProASIC 29	ProASIC 130	SX-A 28	SX-A 157
ProASIC 41	ProASIC 141	SX-A 52	SX-A 183
ProASIC 52	ProASIC 156	SX-A 77	SX-A 185

ProASIC Pin Descriptions

I/O User Input/Output (2.5V or 3.3V)

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with a pull-up resistor.

NC No Connect

It is recommended that this pin not be connected to the circuitry on the board.

GL Global Input Pin

Low skew input pin for clock or other global signals. Input only. This pin can be configured with a pull-up resistor.

GND Ground

Common ground supply voltage

V_{DDL} Logic Array Power Supply Pin

2.5V supply voltage.

V_{DDP} I/O Pad Power Supply Pin

2.5V or 3.3V supply voltage

V_{PP} Programming Supply Pin

This pin must be connected to V_{DDP} during normal operation, or it can remain at 16.5V in an ISP application. This pin must not float.

V_{PN} Programming Supply Pin

This pin must be connected to GND during normal operation, or it can remain at –12V in an ISP application. This pin must not float.

TMS Test Mode Select

The TMS pin controls the use of Boundary Scan circuitry.

TCK Test Clock

Clock input pin for Boundary Scan

TDI Test Data In

Serial input for Boundary Scan

TDO Test Data Out

Serial output for Boundary Scan

TRST Test Reset Input

An optimal Boundary Scan reset pin

RCK Running Clock

A free running clock is required during programming if the programmer cannot guarantee that TCK will be uninterrupted.

SX-A Pin Descriptions

I/O User Input/Output (2.5V, 3.3V, or 5.0V)

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL, LVCMOS, and PCI specifications. Unused I/O pins are configured as tristate outputs.

NC No Connect

It is recommended that this pin not to be connected to the circuitry on the board.

CLKA/B Clock A and B

These two pins are inputs for the clock distribution networks. Input levels are compatible with standard TTL, LVTTL, and PCI specifications. If not used, the pin(s) must be set LOW or HIGH; it must not be left floating.

GND Ground

Common ground supply voltage

V_{CCA} Logic Array Power Supply Pin

2.5V supply voltage

V_{CCI} I/O Pad Power Supply Pin

2.5V, 3.3V or 5.0V supply voltage

TMS Test Mode Select

The TMS pin controls the use of Boundary Scan circuitry.

TCK Test Clock

Clock input pin for Boundary Scan

TDI Test Data In

Serial input for Boundary Scan

TDO Test Data Out

Serial output for Boundary Scan

TRST Test Reset Input

An optional Boundary Scan reset pin

Pin Descriptions and Design Considerations

The ProASIC to SX-A Family prototyping adapter board is an engineering tool that provides the best of both aspects of Actel's devices. The SX-A device family is one of the fastest FPGAs on the market today. The ProASIC device offers a single-chip solution that is also re-programmable. For prototyping and debugging your design, this tool eliminates the need for a socket, and will allow design modifications due to changing requirements and/or design enhancements to be easily implemented. The adapter also allows users to stay in the same software design environment for development with the ProASIC flash technology and the SX-A antifuse technology.

Here are a few points to be considered for the design flow to ensure a smooth transition from the ProASIC flash technology to the SX-A antifuse technology:

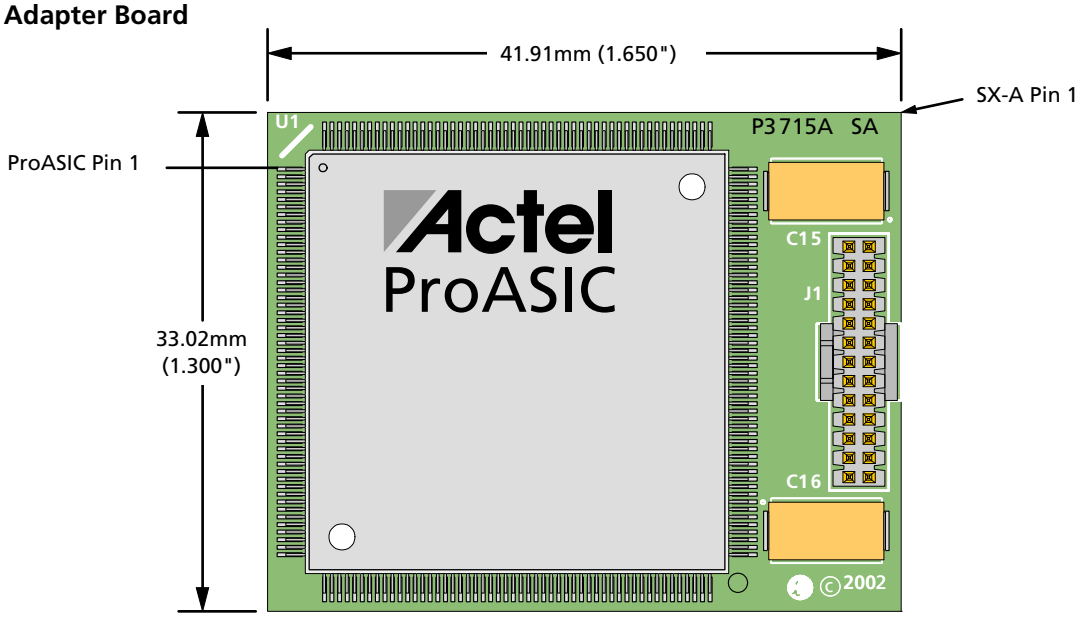
- The flash technology is based on a universal logic tile that will support a flip-flop or any 3-input / 1-output logic function. The SX-A antifuse technology is divided into two dedicated logic tiles: R-Cells (flip-flops) and C-Cells (5-input / 1-output logic). This key technology difference will affect your utilization numbers when synthesizing and running P&R for each family. This is not a point to be overly concerned about, just a point to understand as you develop your application.
- Synthesis tools will handle the EDIF netlist generation differently for each technology. This means that synthesis will have to be run through completely for both technologies.
- As the technologies are different from a logic standpoint, simulation results will have to be verified independently for each technology flow when appropriate.
- Instantiation of Actel macros should be reviewed closely. If you use ACTgen macros, these macros will have to be built separately for the ProASIC and the SX-A technologies. The implementation is the main difference. ProASIC ACTgen macros will only function properly in ProASIC devices, so you will have to build separate SX-A ACTgen macros for the SX-A.
- The ProASIC device on its own has a 3.3V input tolerance. The I/Os for ProASIC can be selected as 2.5V or 3.3V on a pin-by-pin basis. The SX-A devices are capable of 2.5V, 3.3V, or 5.0V. The SX-A pins are only selectable as one voltage. They do not have the pin-by-pin basis capability.
- The programming requirements for the ProASIC reduce the number of available I/Os that are mapped to the SX-A base. This means that there are additional I/Os available on the SX-A device if you run out with the ProASIC prototype. Refer to Table 1 on page 4 for details regarding SX-A I/Os that remain unused in the adapter board.

For specific technical material on either the ProASIC or SX-A device families, please refer to the latest ProASIC Datasheet or SX-A Family Datasheet. Other useful documents are:

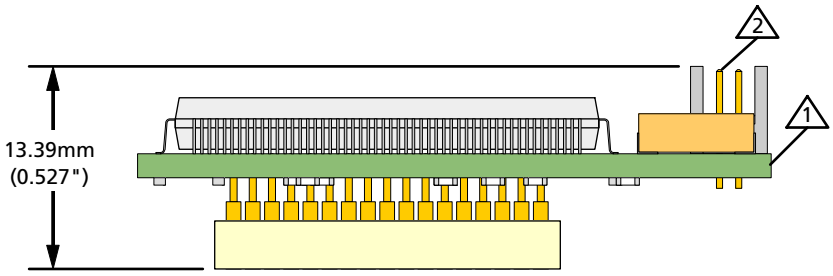
1. *Silicon Sculptor User's Guide*
2. *FlashPro User's Guide*
3. *I/O Cell Selection for ProASIC™ 500K Devices*
4. *Antifuse Macro Library Guide*
5. *Flash Macro Library Guide*
6. *ACTgen Macros Reference Guide*

For any other technical questions regarding the SI-SXA-APAPQ208 adapter board, please contact Actel Technical Support by calling 800-262-1060, or by email at *tech@actel.com*.

Top Adapter Board



Side View



1. Substrate: 1.59mm ± 0.18mm (0.0625" ± 0.007")
FR4/G10 or equivalent high temp material.
17 µm (1/2 oz.) Cu clad. SnPb plating.

2. Test points: material - Phosphor Bronze; plating -
Sn over 1.27µm (50µ") Ni. Gold flash on contact end.

Figure 2: QFP Adapter

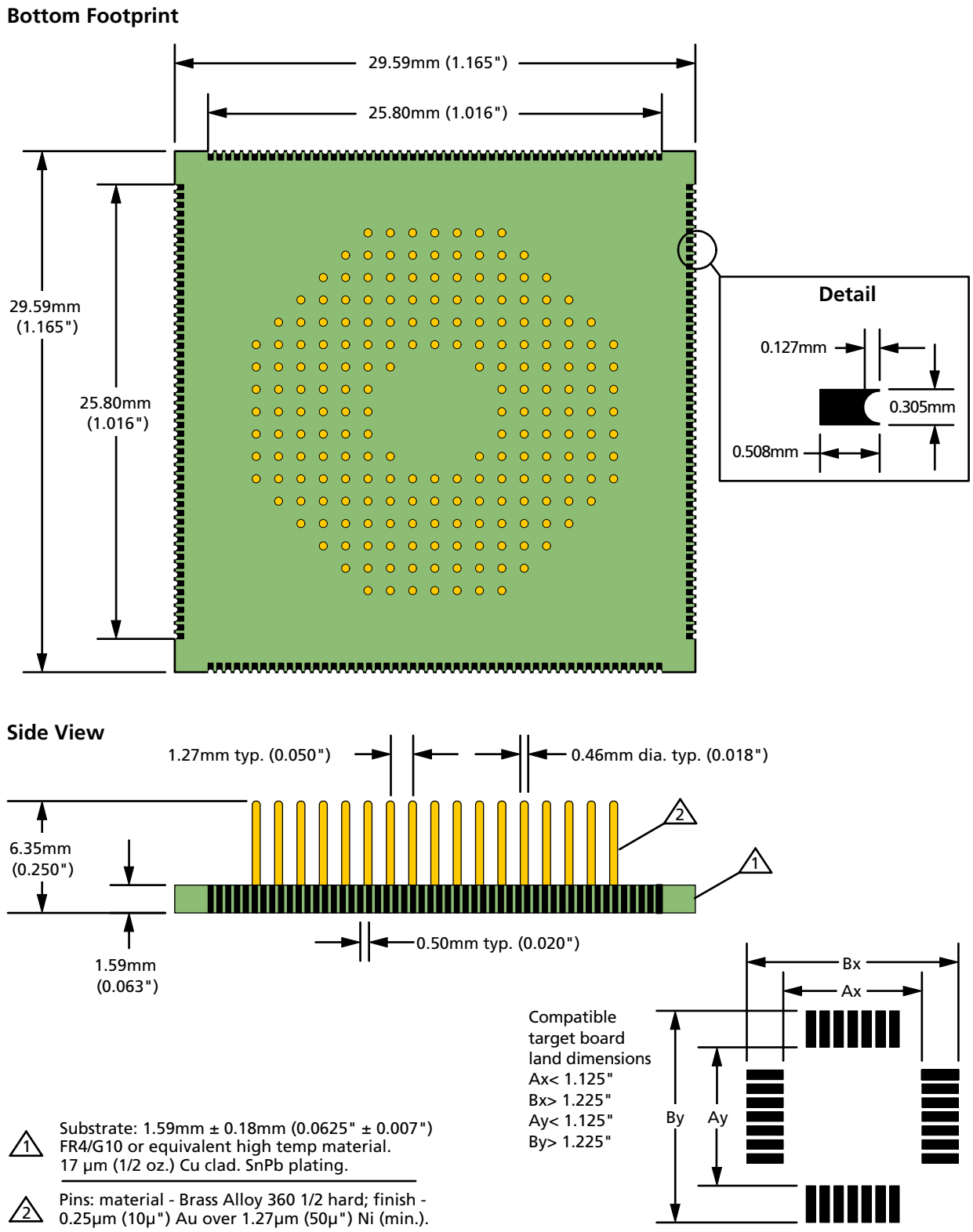


Figure 3: Surface-Mountable QFP Emulator Foot

For more information, visit our website at **http://www.actel.com**

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