13.0 ELECTRICAL CHARACTERISTICS

13.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Storage Temperature	–55	125	°C
Supply Voltage (V_{cc})	–0.3	7.0	Volts
Input Pin Voltage	–0.5	V_{cc}+ 5.0	Volts
Power Dissipation		1.05	Watts @ 33 MHz

13.2 DC CHARACTERISTICS

The Following table summarizes the required parameters defined by the PCI specification as they apply to the S5933 controller.

PCI Input/Output Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions	Notes
V_{CC}	Supply Voltage	4.75	5.25	V		
V_{ih}	Input High Voltage	2.0		V		
V_{il}	Input Low Voltage	–0.5	0.8	V		
I_{ih}	Input High Leakage Current		70	µA	V_{in} = 2.7	1
I_{il}	Input Low Leakage Current		–70	µA	V_{in} = 0.5	1
V_{oh}	Output High Voltage	2.4		V	I_{out} = –2mA	
V_{ol}	Output Low Voltage		0.55	V	I_{out} = 3mA, 6mA	2
C_{in}	Input Pin Capacitance		10	pF		3
C_{clk}	CLK Pin Capacitance	5	12	pF		
C_{IDSEL}	IDSEL Pin Capaticance		8	pF		

Notes:

1. Input leakage applies to all inputs and bi-directional buffers.
2. PCI Bus signals without pull-up resistors will provide the 3 mA output current. Signals which require a pull-up resistor will provide 6 mA output current.
3. The PCI specification limits all PCI inputs not located on the motherboard to 10 pf (the clock is allowed to be 12 pf).

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13.2.1 PCI Bus Signals

The following table summarizes the PCI Bus D.C. parameters defined by the PCI specification as they apply to the S5933 controller.

Signal	Type	Direction	Max	Units	Notes
CLK		Input			
RST#		Input			
INTA#	Open Drain	Output	4	mA	
AD[31:0]	t/s	Bi-directional		mA	
REQ#	t/s	Output	4	mA	
GNT#		Input			
C/BE[3:0]#	t/s	Bi-directional	4	mA	
DEVSEL#	s/t/s	Bi-directional		mA	
FRAME#	s/t/s	Bi-directional	4	mA	
IRDY#	s/t/s	Bi-directional	4	mA	
TRDY#	s/t/s	Bi-directional	4	mA	
PERR#	s/t/s	Bi-directional	4	mA	
PAR	t/s	Bi-directional	4	mA	
SERR#	Open Drain	Output	4	mA	
STOP#	s/t/s	Bi-directional	4	mA	
LOCK#		Input			
IDSEL		Input			

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13.2.2 Add-On Bus Signals

The following table summarizes the Add-On Bus D.C. parameters as they apply to the S5933 controller.

Signal	Type	Direction	Max	Units	Notes
PCLK		Output	8	mA	
IRQ#		Output	4	mA	
SYSRST#		Output	4	mA	
ADR[6:2]		Input			
SELECT		Input			
ADR[6:2]		Input			
BE[3:0]#		Input			
RD#		Input			
WR#		Input			
DQ[31:0]	t/s	Bi-directional	4	mA	
WRFULL		Output	4	mA	
RDEMPTY		Output	4	mA	
RDFIFO#		Input			
WRFIFO#		Input			
PTATN#		Output	4	mA	
PTBURST#		Output	4	mA	
PTADR#		Input			
PTRDY#		Input			
PTWR		Output	4	mA	
PTBE[3:0]#		Output	4	mA	
PTNUM[1:0]		Output	4	mA	
EQ[7:0]	t/s	Bi-directional	1	mA	
EA[8:0]	t/s	Output	1	mA	
EA[15:9]		Output	1	mA	
MODE		Input			
TEST		Output	4	mA	
FLT#		Input			
ERD#/SCL		Output	1	mA	
EWR#/SDA	t/s	Bi-directional	1	mA	

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13.3 AC CHARACTERISTICS

13.3.1 PCI Bus Timings

Functional Operation Range (V_{CC}=5.0V ±5%, 0°C to 70°C, 50 pF load on outputs)

Symbol	Parameter	Min	Max	Units	Notes
TCL	Cycle Time	30		ns	
t1	High Time	12		ns	
t2	Low Time	12		ns	
t3	Rise Time (0.8V to 2.0V)		3	ns	
t4	Fall Time (2.0V to 0.8V)		3	ns	
t5	Output Valid Delay (Bussed Signals) Output Valid Delay (Point-to-Point Signals)	2 2	11 12	ns	Note 1
t6	Float to Active Delay	2		ns	
t7	Active to Float Delay		28	ns	
t8	Rising Edge Setup (Bussed Signals) Rising Edge Setup (GNT#) Rising Edge Setup (REQ#)	7 10 12		ns	
t9	Hold from PCI Clock Rising Edge	0		ns	

Notes:

1. Minimum times are for unloaded outputs, maximum times are for 50 pF equivalent loads.

Figure 13-1. PCI Clock Timing

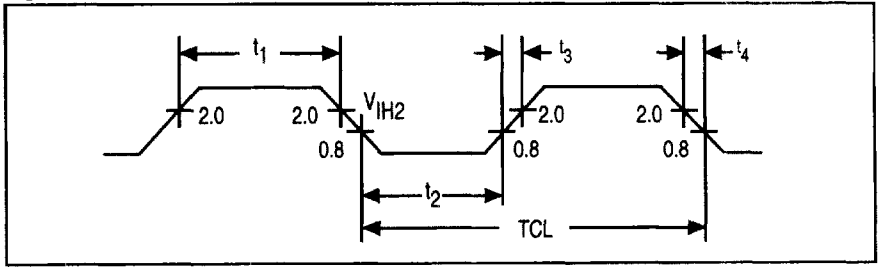

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Figure 13-2. PCI Output Timing

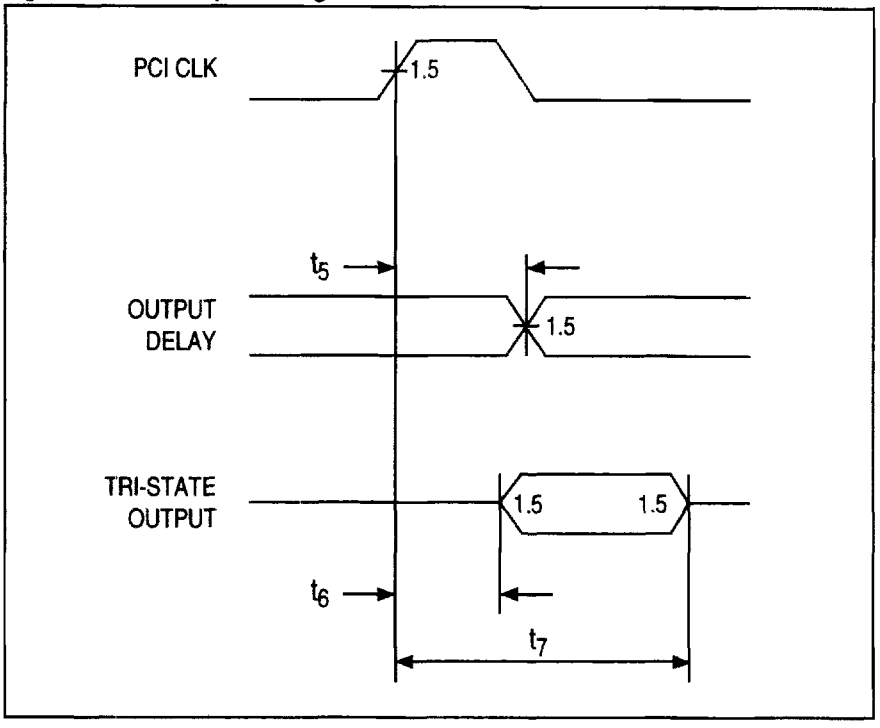
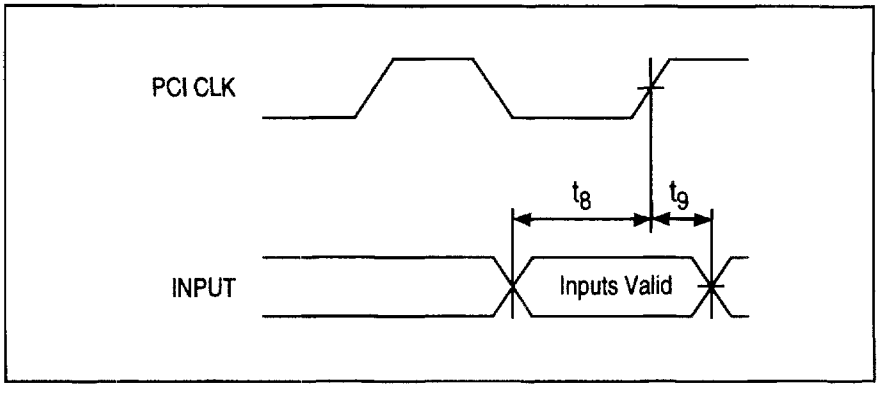


Figure 13-3. PCI Input Timing



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13.3.2 Add-On Bus Timings

Figure 13-4. Add-On Clock Timing

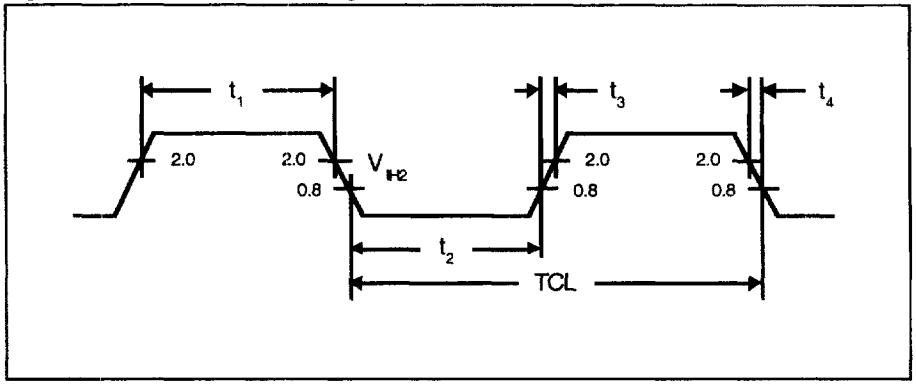
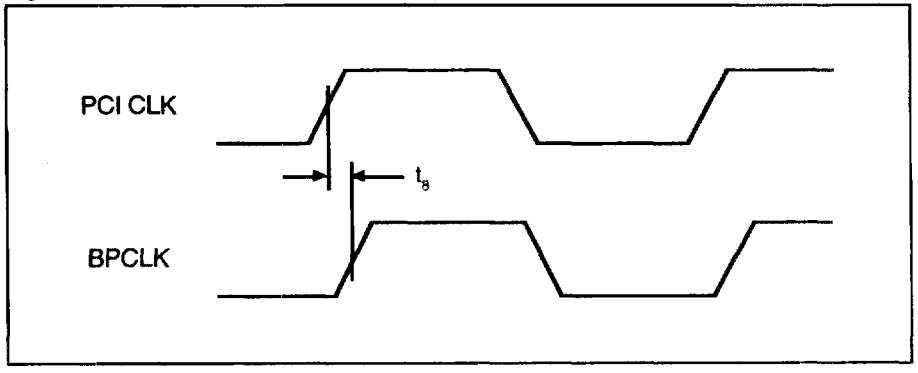


Figure 13-5. Pass-Thru Clock Relationship to PCI Clock



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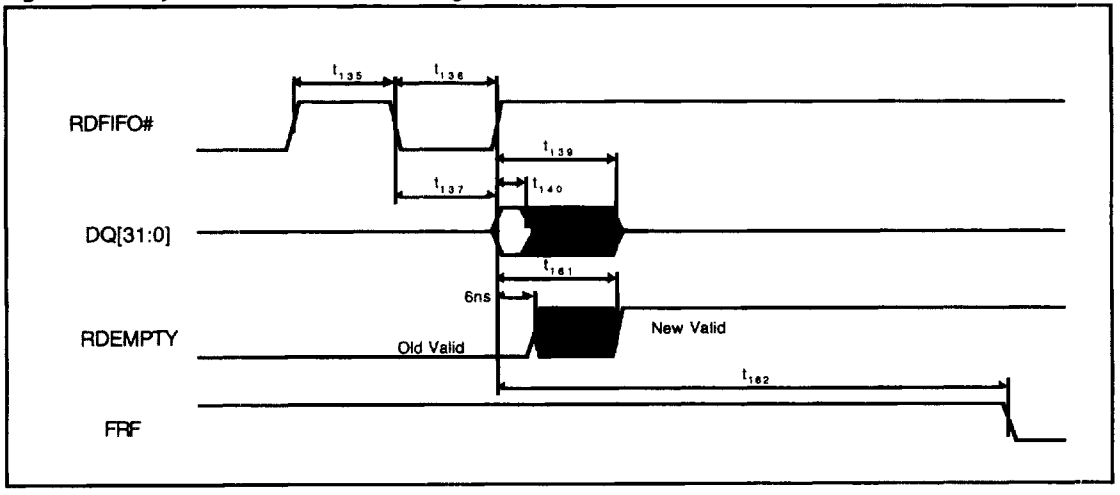
13.3.3 Asynchronous RDFIFO# Timing

Functional Operation Range (V_{CC}= 5.0V 5%, 0°C to 70°C T_a, 50 pf load on outputs).

Symbol	Parameter	Min	Max	Units	Notes
t_{135}	RDFIFO# High Time	17		ns	
t_{136}	RDFIFO# Low Time	17		ns	
t_{137}	RDFIFO# Low to DQ[31:0] Driven		21	ns	
t_{139}	RDFIFO# High to DQ[31:0] Float		20	ns	
t_{140}	DQ[31:0] Hold from RDFIFO# Rising Edge	5		ns	
t_{161}	PCI to ADD-ON FIFO RDEMPTY Valid from RDFIFO# Rising Edge		15	ns	
t_{162}	PCI to ADD-ON FIFO FRF Valid from RDFIFO# Rising Edge		85	ns	

Figure 13-6. Asynchronous RDFIFO# Timing



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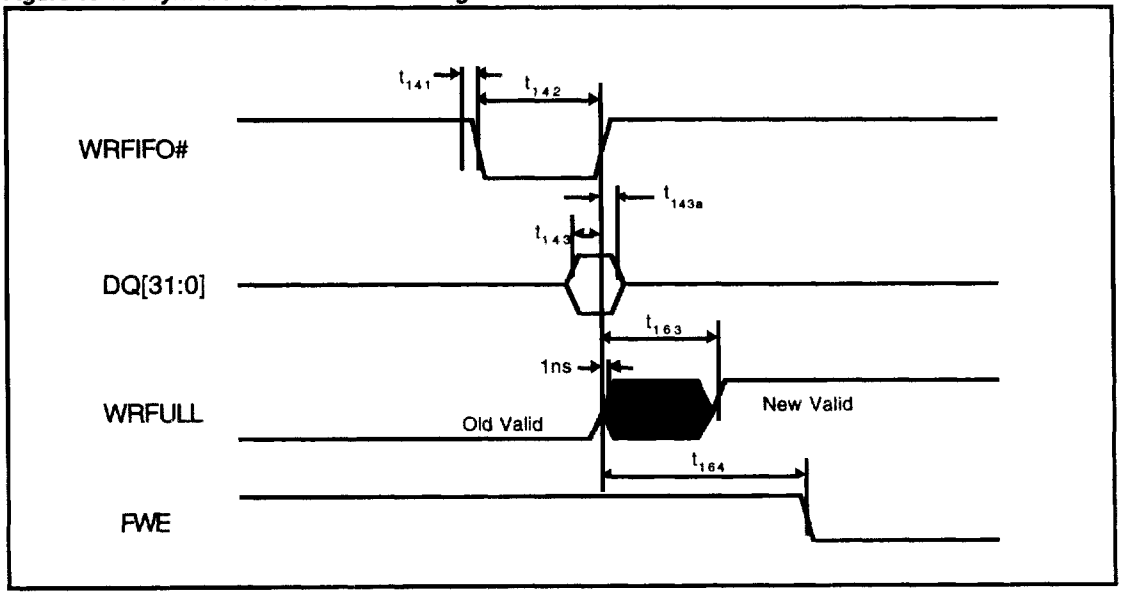
13.3.4 Asynchronous WRFIFO# Timing

Functional Operation Range (V_{CC}=5.0V 5%, 0°C to 70°C T_a, 50 pf load on outputs).

Symbol	Parameter	Min	Max	Units	Notes
t_{141}	WRFIFO# High Time	2		ns	
t_{142}	WRFIFO# Low Time	17		ns	
t_{143}	DQ[31:0] Setup to WRFIFO# Rising Edge	4		ns	
t_{143a}	DQ[31:0] Hold from WRFIFO# Rising Edge	2		ns	
t_{163}	ADD-ON to PCI FIFO WRFULL Valid from WRFIFO# Rising Edge		16	ns	
t_{164}	ADD-ON to PCI FIFO FWE Valid from WRFIFO# Rising Edge		28	ns	

Figure 13-7. Asynchronous WRFIFO# Timing



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13.3.5 Synchronous RDFIFO# Timing

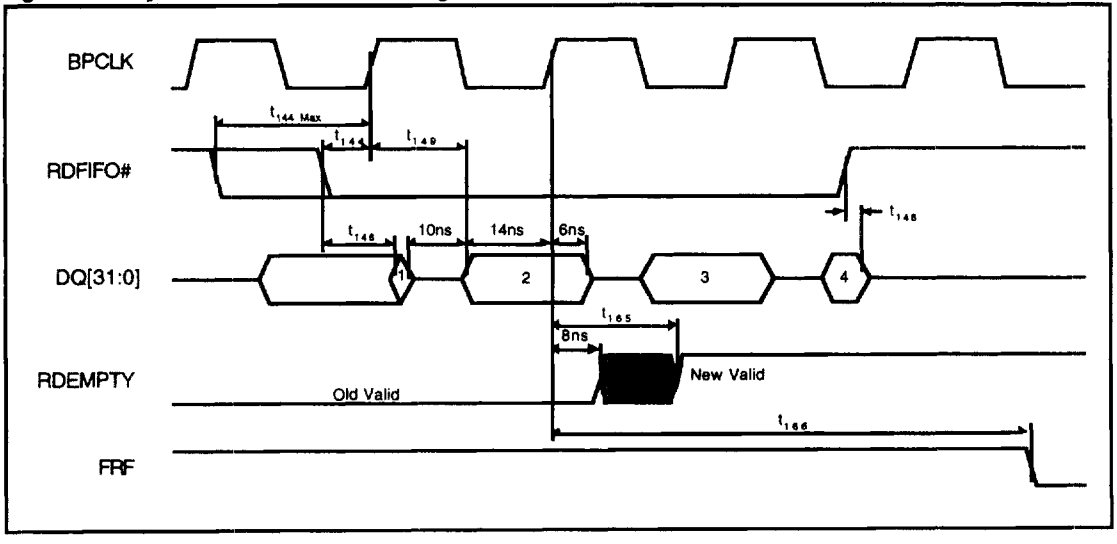
Functional Operation Range (V_{CC}=5.0V 5%, 0°C to 70°C T_a, 50 pf loaf on outputs).

Symbol	Parameter	Min	Max	Units	Notes
t_{144}	RDFIFO# Setup tp BPCLK Rising Edge	8	26	ns	1
t_{145}	RDFIFO# Low Time	8		ns	
t_{146}	RDFIFO# Low to DQ[31:0] Driven		12	ns	
t_{148}	RDFIFO# High to DQ[31:0] Float		3	ns	
t_{149}	DQ[31:0] Valid from BPCLK Rising Edge		16	ns	3
t_{165}	PCI to ADD-ON FIFO RDEMPTY Valid from BPCLK Rising Edge		15	ns	2
t_{166}	PCI to ADD-ON FIFO FRF Valid from BPCLK Rising Edge		80	ns	

Notes:

1. Min and Max times are indicated to allow increased valid data time as shown by dashed lines.
2. State change of RDEMPTY shown below is reference only. Actual change would indicate no Data 3 available.
3. Valid applies after first access. First access is async with following as sync accesses.

Figure 13-8. Synchronous RDFIFO# Timing



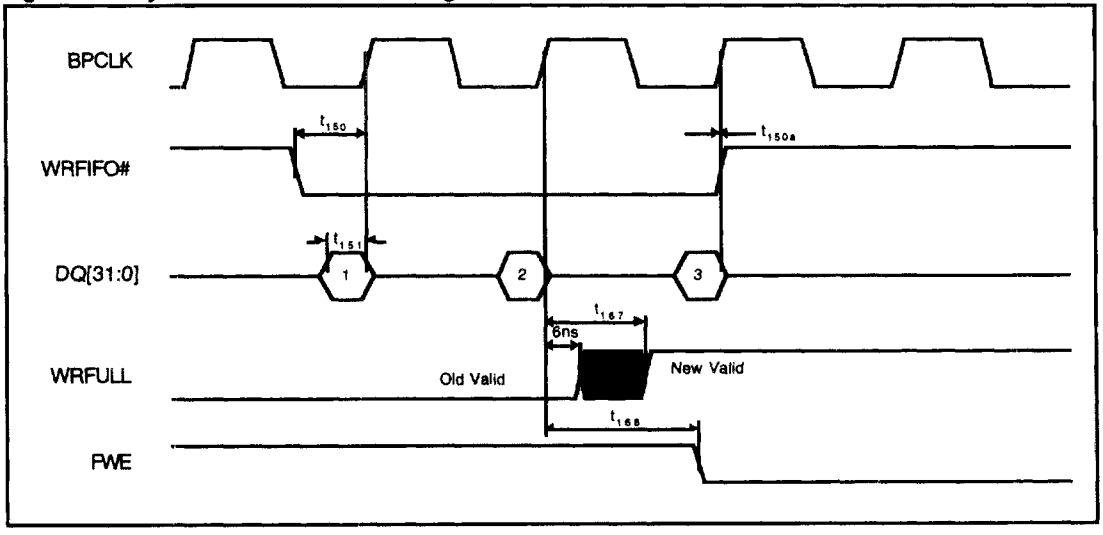
13.3.6 Synchronous WRFIFO# Timing

Functional Operation Range (V_{CC}= 5.0V 5%, 0°C to 70°C T_a, 50 pf load on outputs).

Symbol	Parameter	Min	Max	Units	Notes
t_{1350}	WRFIFO# Setup to BPCLK Rising Edge	12		ns	
t_{150a}	WRFIFO# Hold Time to BPCLK Rising Edge		0	ns	
t_{151}	DQ[31:0] Setup to BPCLK Rising Edge	7			
t_{151a}	DQ[31:0] Hold from BPCLK Rising Edge		0		
t_{167}	ADD-ON to PCI WRFULL Valid from BPCLK Rising Edge		17	ns	1
t_{168}	ADD-ON to PCI FIFO FWE Valid from BPCLK Rising Edge		26	ns	

Notes:
1. State change of WRFULL shown below is reference only. Actual change would indicate no Data 3 written.

Figure 13-9. Synchronous WRFIFO# Timing



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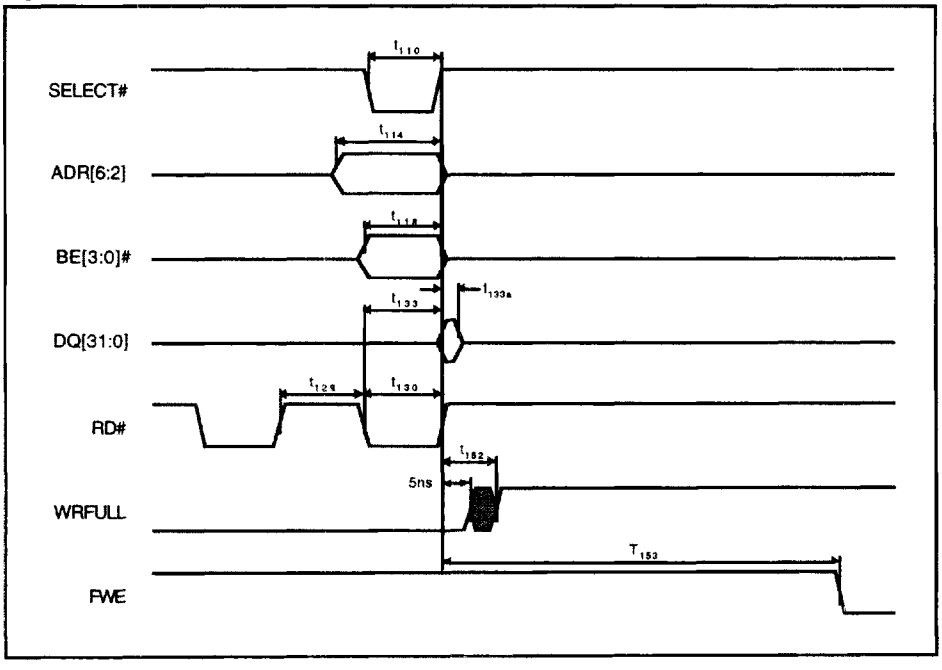
13.3.7 Asynchronous RD# FIFO Timing

Functional Operation Range (V_{CC}=5.0V 5%, 0°C to 70°C T_a, 50 pf load on outputs).

Symbol	Parameter	Min	Max	Units	Notes
t_{110}	SELECT# Setup to RD# Rising Edge	10		ns	
t_{114a}	SELECT# Hold from RD# Rising Edge	-1		ns	
t_{114}	ADR[6:2] Setup to RD# Rising Edge	18		ns	
t_{114a}	ADR[6:2] Hold from RD# Rising Edge	0			
t_{118}	BE[3:0]# Setup to RD# Rising Edge	12		ns	
t_{118a}	BE[3:0]# Hold from RD# Rising Edge	0		ns	
t_{129}	RD# High Time	16		ns	
t_{130}	RD# Low Time	15		ns	
t_{133}	DQ[31:0] Valid from RD# Falling Edge	15		ns	
t_{133a}	DQ[31:0] Hold from RD# Rising Edge	3		ns	
t_{152}	RDEMPTY Status Valid from RD# Rising Edge		10	ns	
t_{153}	FWE Status Valid from RD# Rising Edge		75	ns	

Figure 13-10. Asynchronous RD# FIFO Timing



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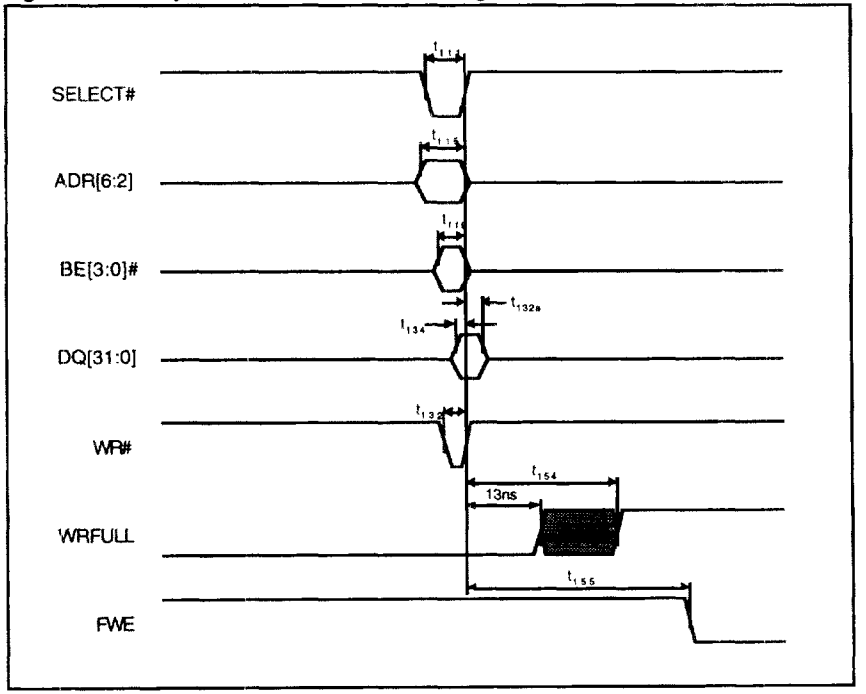
13.3.8 Asynchronous WR# FIFO Timing

Functional Operation Range (V_{CC}=5.0V 5%, 0°C to 70°C T 50 pf load on outputs).

Symbol	Parameter	Min	Max	Units	Notes
t_{111}	SELECT# Setup to WR# Rising Edge	7		ns	
t_{111a}	SELECT# Hold from WR# Rising Edge	0		ns	
t_{115}	ADR[6:2] Setup to WR# Rising Edge	8		ns	
t_{115a}	ADR[6:2] Hold from WR# Rising Edge	0		ns	
t_{119}	BE[3:0]# Setup to WR# Rising Edge	5		ns	
t_{119a}	BE[3:0]# Hold from WR# Rising Edge	0		ns	
t_{131}	WR# High Time	TBD		ns	
t_{132}	WR# Low Time	4		ns	
t_{134}	DQ[31:0] Setup to WR# Rising Edge	2		ns	
t_{134a}	DQ[31:0] Hold from WR# Rising Edge	3		ns	
t_{154}	WRFULL Status Valid from WR# Rising Edge		27	ns	
t_{155}	FWE Status Valid from WR# Rising Edge		40	ns	

Figure 13-11. Asynchronous WR# FIFO Timing



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13.3.9 Synchronous RD# FIFO Timing

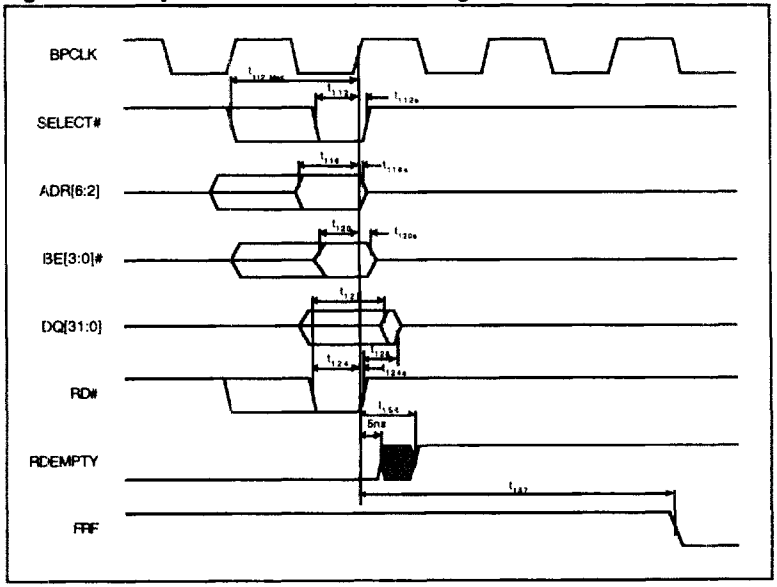
Functional Operation Range (V_{CC}=5.0V 5%, 0°C to 70°C T 50 pf load on outputs).

Symbol	Parameter	Min	Max	Units	Notes
t_{112}	SELECT# Setup to BPCLK Rising Edge	10	30	ns	4
t_{112a}	SELECT# Hold from BPCLK Rising Edge	2		ns	
t_{116}	ADR[6:2] Setup to BPCLK Rising Edge	14	34	ns	4
t_{116a}	ADR[6:2] Hold from BPCLK Rising Edge	1		ns	
t_{120}	BE[3:0]# Setup to BPCLK Rising Edge	9	29	ns	4
t_{120a}	BE[3:0]# Hold from BPCLK Rising Edge	3		ns	
t_{125}	RD# Low to DQ[31:0] Driven		17	ns	1
t_{128}	RD# High to DQ[31:0] Float		8	ns	
t_{156}	RDEMPTY Status Valid to BPCLK Rising Edge		13	ns	
t_{157}	FRF Status Valid to BPCLK Rising Edge		74	ns	
t_{124}	RD# Setup to BPCLK Rising Edge	11	31	ns	4
t_{124a}	RD# Hold from BPCLK Rising Edge	1		ns	
t_{127}	DQ[31:0] Valid from BPCLK Rising Edge		6	ns	

Notes:

1. Data is valid for 22ns for a 31ns t_{124} RD# Setup.
2. RD# and SELECT# must both be asserted to dric=ve DQ[31:0] - delay is from the last one asserted.
3. When increasing Setup times, ADR[6:2], BE[3:0]#, SELECT#, and RD# timing relations remain relative to each other as shown.
4. Min and Max are indicated to allow increased valid data time as shown by dashed lines. First accesses are async.

Figure 13-12. Synchronous RD# FIFO Timing



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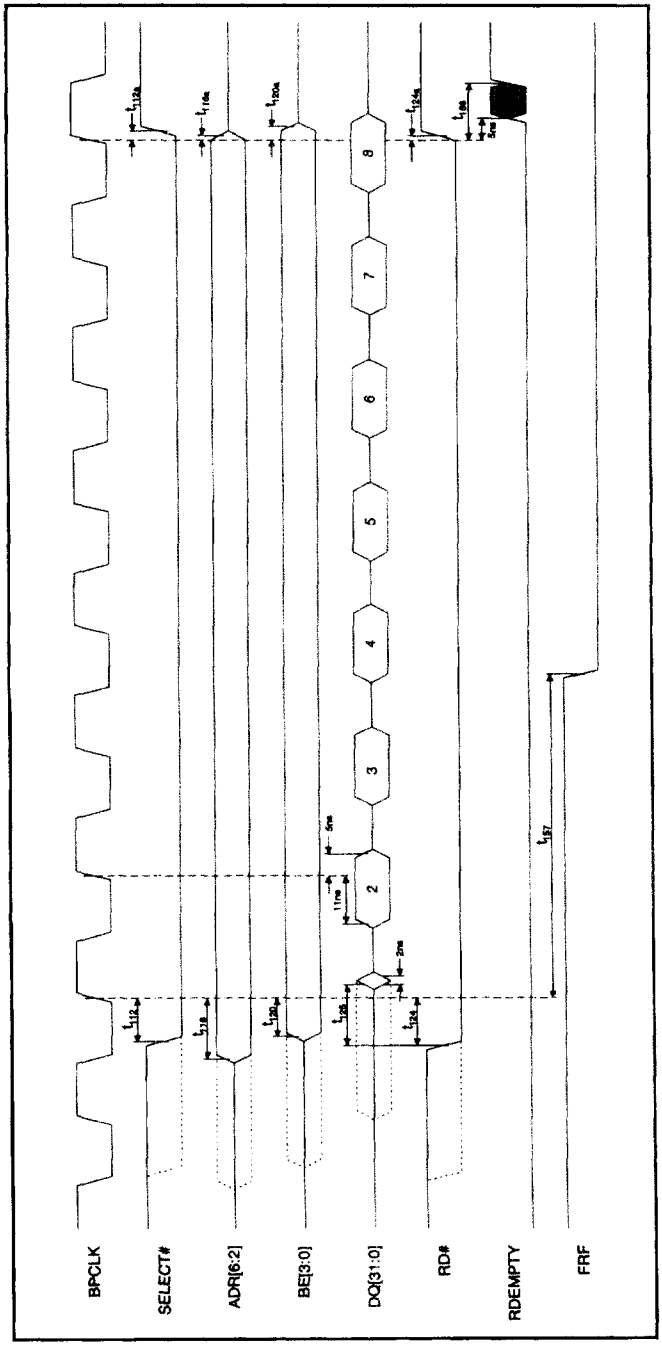
13.3.10 Synchronous Multiple RD# FIFO Timing

Figure 13-13. Synchronous RD# FIFO Timing

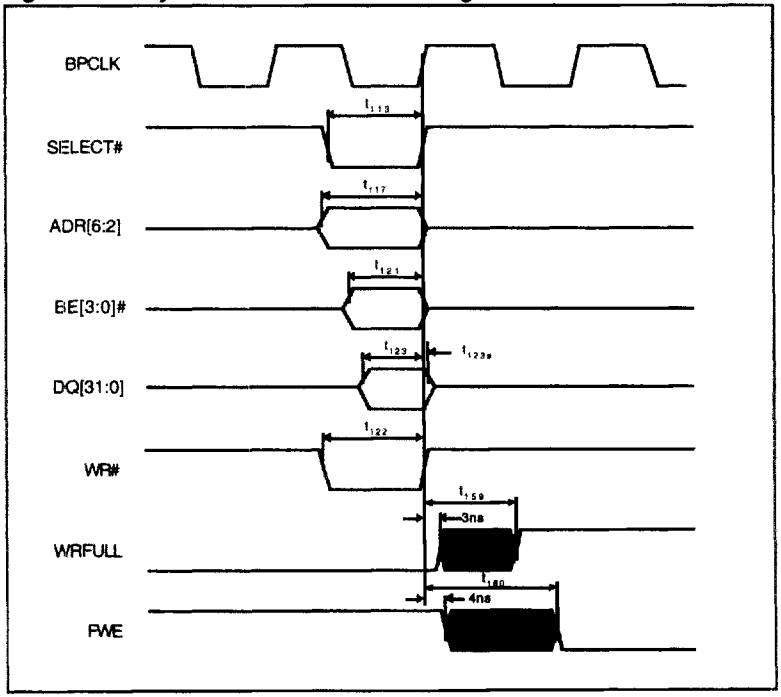


13.3.11 Synchronous WR# FIFO Timing

Functional Operation Range (V_{CC}=5.0V 5%, 0°C to 70°C T_a, 50 pf load on outputs).

Symbol	Parameter	Min	Max	Units	Notes
t_{113}	SELECT# Setup to BPCLK Rising Edge	19		ns	
t_{113a}	SELECT# Hold from BPCLK Rising Edge	0		ns	
t_{117}	ADR[6:2] Setup to BPCLK Rising Edge	20		ns	
t_{117a}	ADR[6:2] Hold from BPCLK Rising Edge	0		ns	
t_{121}	BE[3:0]# Setup to BPCLK Rising Edge	15		ns	
t_{121a}	BE[3:0]# Hold from BPCLK Rising Edge	0		ns	
t_{123}	DQ[31:0] Setup to BPCLK Rising Edge	12		ns	
t_{123a}	DQ[31:0] Hold from BPCLK Rising Edge	1		ns	
t_{122}	WR# Setup to BPCLK Rising Edge	20		ns	
t_{122a}	WR# Hold from BPCLK Rising Edge	0		ns	
t_{159}	WRFULL Status Valid to BPCLK Rising Edge		18	ns	
t_{160}	FWE Status Valid to BPCLK Rising Edge		26	ns	

Figure 13-14. Synchronous WR# FIFO Timing



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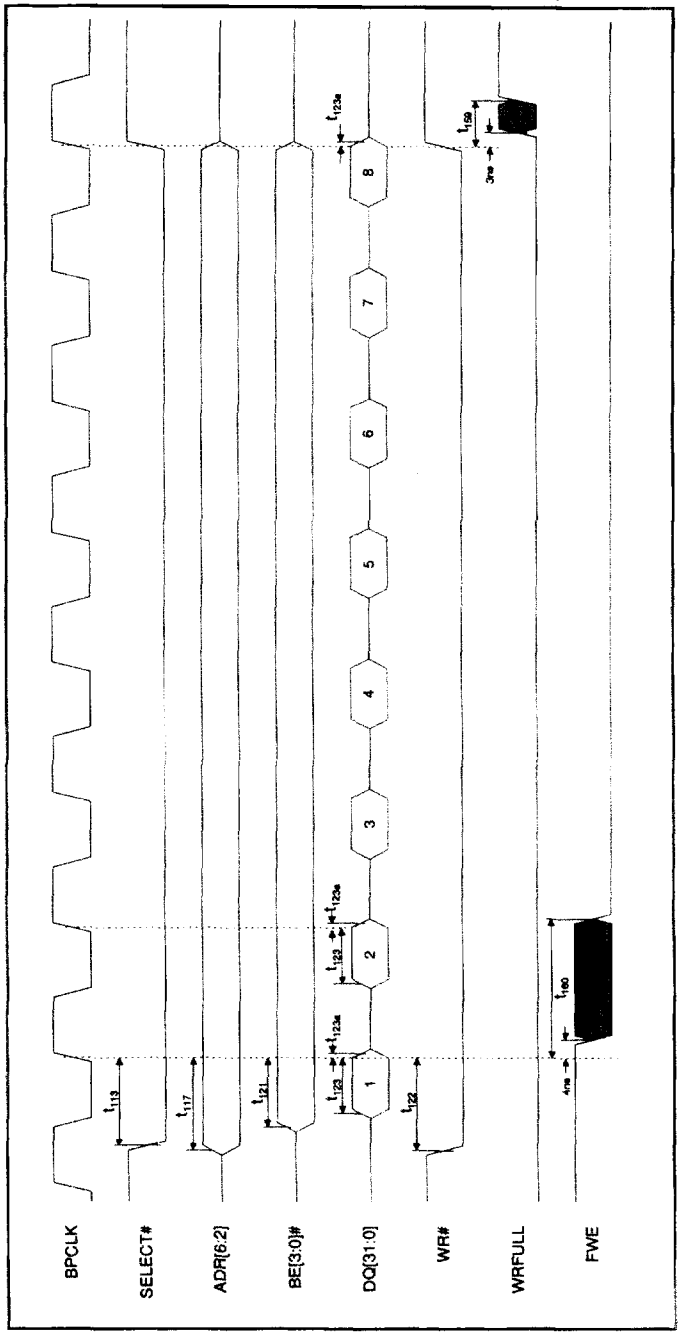
13.3.12 Synchronous Multiple WR# FIFO Timing

Figure 13-15. Synchronous Multiple WR# FIFO Timing



13.3.13 Target S5933 Pass-Thru Interface Timings

Functional Operation Range (V_{CC}=5.0V ±5%, 0°C to 70°C, 50 pF load on outputs)

Symbol	Parameter	Min	Max	Units	Notes
t_{10a}	SELECT# Setup to BPCLK Rising Edge	3		ns	
t_{11a}	SELECT# Hold from BPCLK Rising Edge	2		ns	
t_{13}	ADR[6:2], BE[3:0]# Setup to BPCLK Rising Edge	5		ns	
t_{14}	ADR[6:2], BE[3:0]# Hold from BPCLK Rising Edge	2		ns	
t_{17}	RD# Low to DQ{31:0} Driven		13	ns	1
t_{24}	Pass-Thru Status Valid from BPCLK Rising Edge		5	ns	
t_{25}	Pass-Thru Status Hold from BPCLK Rising Edge	0		ns	
t_{26}	PTRDY# Setup to BPCLK Rising Edge	5		ns	
t_{27}	PTRDY# Hold from BPCLK Rising Edge	3		ns	
t_{28}	PCICLK to BPCLK delay	2	6.5	ns	
t_{29}	RD#, WR# Setup to BPCLK Rising Edge	5		ns	
t_{30}	RD#, WR# Hold from BPCLK Rising Edge	2		ns	
t_{31}	DQ[31:0] Setup to BPCLK Rising Edge	5		ns	
t_{32}	DQ[31:0] Hold from BPCLK Rising Edge	2		ns	
t_{33}	DQ[31:0] Valid from BPCLK Rising Edge		15	ns	
t_{34}	DQ[31:0] Float from RD# Rising Edge		12	ns	

Notes:

1. This timing also applies to the use of BE[3:0]# to control DQ[31:0] drive.

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Figure 13-17. Pass-Thru Data Register Read Timing

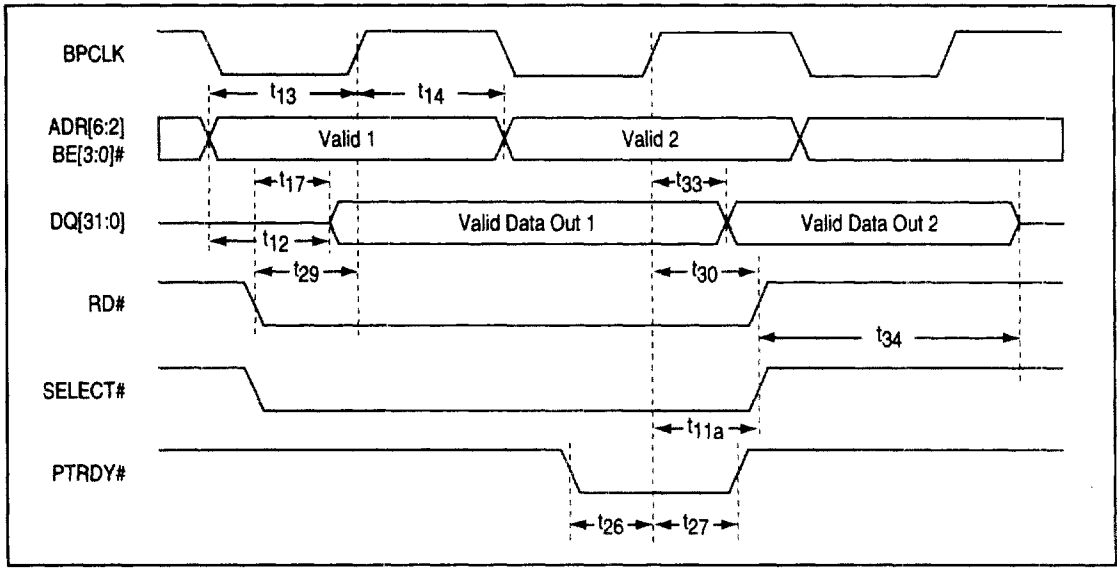

Figure 13-18. Pass-Thru Data Register Write Timing

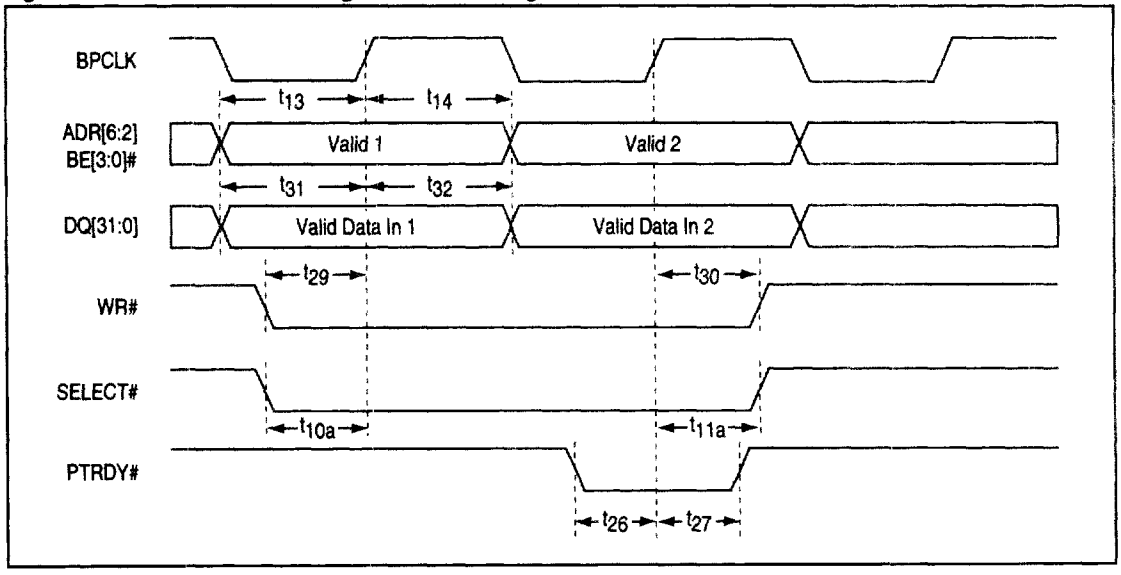

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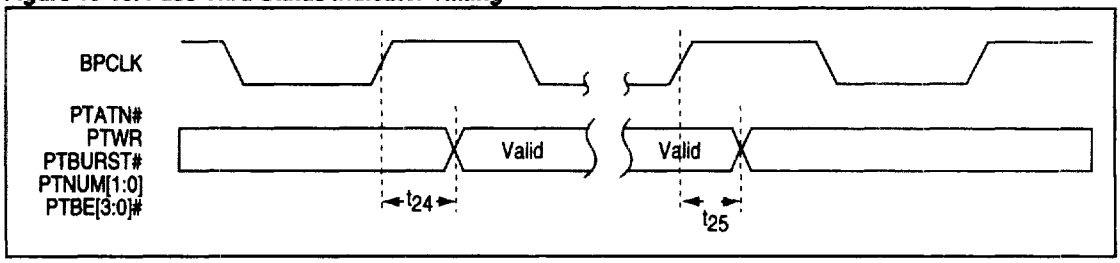
Figure 13-19. Pass-Thru Status Indicator Timing



13.3.14 Target Byte-Wide nv Memory Interface Timings

Functional Operation Range (V_{CC}=5.0V ±5%, 0°C to 70°C, 50 pF load on outputs)

Symbol	Parameter	Min	Max	Units	Notes
t35	ERD# Cycle Time	8T		ns	Note 1
t36	ERD# Low Time	6T		ns	Note 1
t37	ERD# High Time	2T		ns	Note 1
t38	EA[15:0] Setup to ERD# or EWR# Low	T		ns	Note 1
t39	EA[15:0] Hold from ERD# or EWR# High	T		ns	Note 1
t40	EQ[7:0] Setup to ERD# Rising Edge	10		ns	Note 1
t41	EQ[7:0] Hold from ERD# Rising Edge	2		ns	Note 1
t42	EWR# Cycle Time			ns	Note 1,2
t43	EWR# Low Time	6T		ns	Note 1
t44	EWR# High Time	2T		ns	Note 1
t45	EQ[7:0] Setup to EWR# Low	-10	0	ns	Note 1
t46	EQ[7:0] Hold from EWR# High	T		ns	Note 1

Notes:

1. T represents the clock period for the PCI bus clock (30ns @ 33 MHz).
2. The write cycle time is controlled by both the PCI bus clock and software operations to initiate the write operation of nv memory. This parameter is the result of several software operations to the Bus Master Control/Status Register (MCSR) — Section 4.10.

Figure 13-20. nv Memory Read Timing

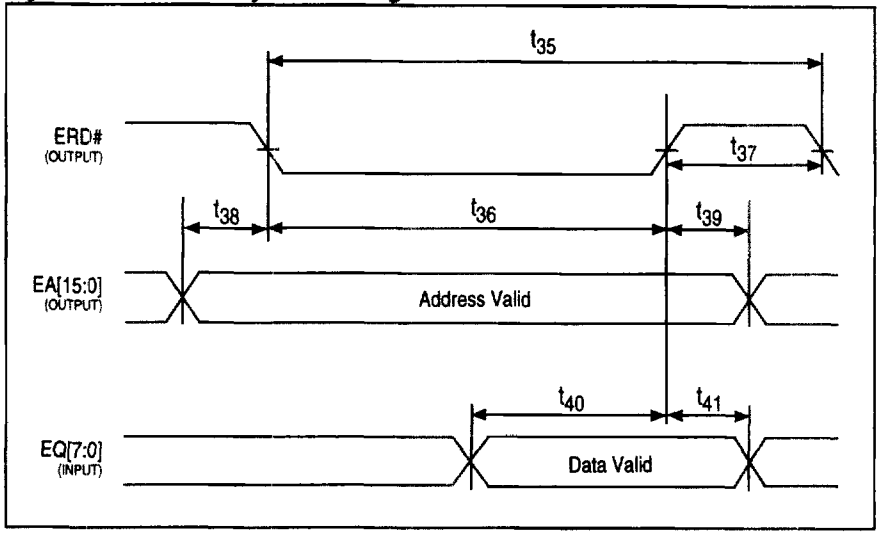
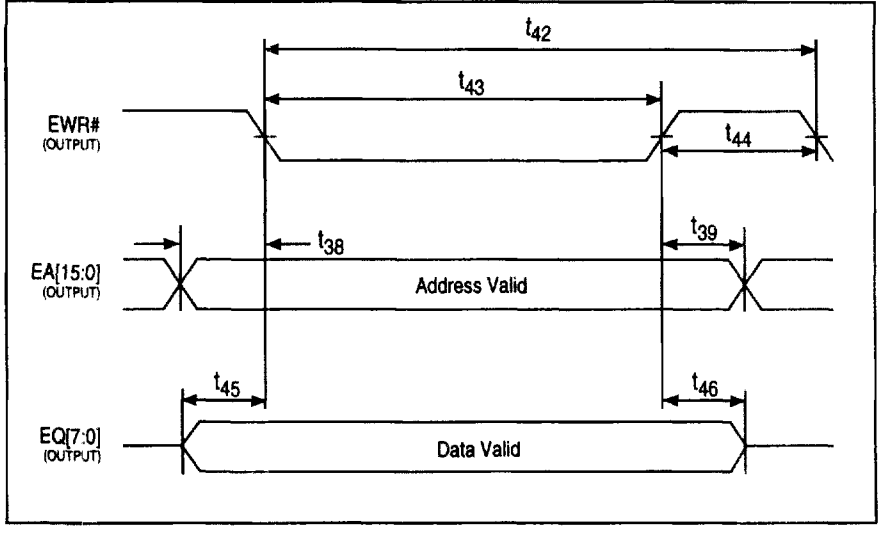


Figure 13-21. nv Memory Write Timing



13.3.15 Target Interrupt Timings

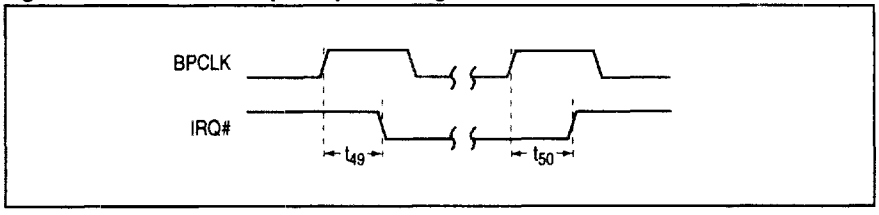
Functional Operation Range (V_{CC}=5.0V ±5%, 0°C to 70°C, 50 pF load on outputs)

Symbol	Parameter	Min	Max	Units	Notes
t49	IRQ# Low from BPCLK Rising Edge		15	ns	Note 1
t50	IRQ# High from BPCLK Rising Edge		15	ns	Note 1

Notes:

1. This timing applies to interrupts generated and cleared from the PCI interface.

Figure 13-22. IRQ# Interrupt Output Timing



Functional Operation Range (V_{CC}=5.0V ±5%, 0°C to 70°C, 50 pF load on outputs)

Symbol	Parameter	Min	Max	Units	Notes
t51	EMBCLK Low Time	12		ns	
t52	EMBLK High Time	12		ns	
t53	EMB[7:0] Setup to EMBCLK Rising Edge	5		ns	
t54	EMB[7:0] Hold from EMBCLK Rising Edge	2		ns	

Figure 13-23. Mailbox 4, Byte 3 Direct Input Timing