



T-46-13-47  
**CMOS E<sup>2</sup>PLD**  
**Electrically Erasable Programmable Logic**

**PEEL™ 18CV8**

**Features**

**Advanced CMOS E<sup>2</sup>PROM Technology**

**Low Power Consumption**

- CMOS: 15mA Standby + 1mA/MHz Max
- TTL: 25mA Standby + 1mA/MHz Max

**High Performance**

- T<sub>PD</sub> 25nS Max, T<sub>CO</sub> 18nS Max, T<sub>SC</sub> 15nS Min

**Reprogrammability**

- 100% factory tested
- Cost effective "window-less" package
- Erase/Program time in seconds
- Adds convenience, reduces field retrofit and development cost

**Design Security**

- Prevents unauthorized reading or copying of design

**Architectural Flexibility**

- 74 Product Term x 36 Input array
- Up to 18 Inputs and 8 I/O pins
- Independently configurable I/O macro cells: polarity, register, combinatorial, bi-directional

- Synchronous preset, asynchronous clear
- Independent output enables

**Application Versatility**

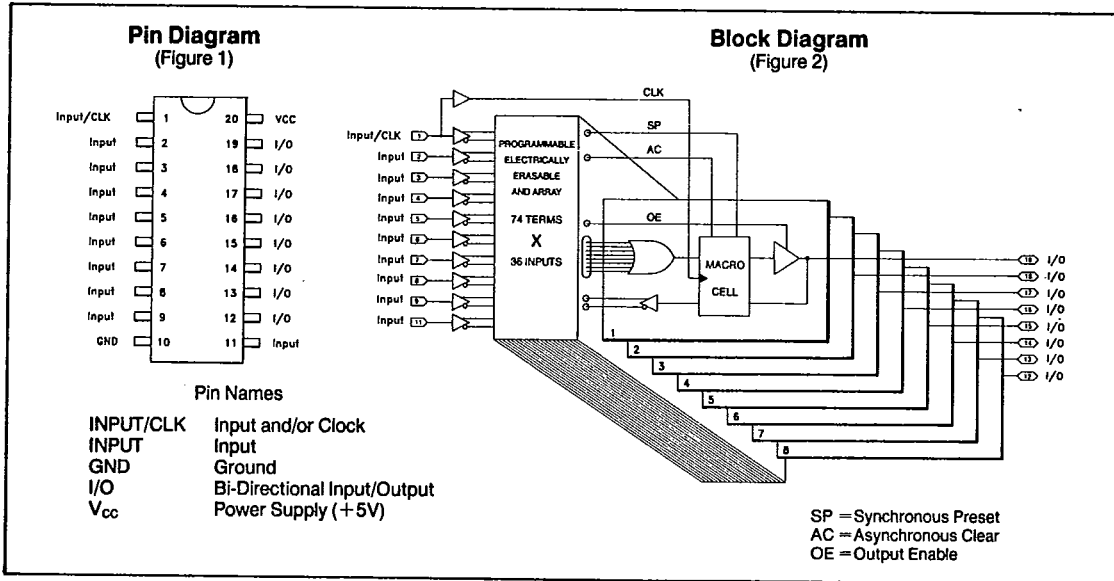
- Replace SSI/MSI logic
- Emulates bipolar PAL™ devices and the EP300/310
- Simplifies inventory control
- Allows new design possibilities

**Development/Programmer Support**

- Popular PC-based development tools and programmers

**General Description**

The Gould PEEL™ 18CV8 is a CMOS Programmable Electrically Erasable Logic device that provides a high performance, low power, reprogrammable, and architecturally flexible alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS E<sup>2</sup>PROM technology, the performance of the PEEL 18CV8 rivals speed parameters of standard bipolar PLDs with a dramatic improvement in power consumption. The electrically erasable reprogrammable technology of the PEEL

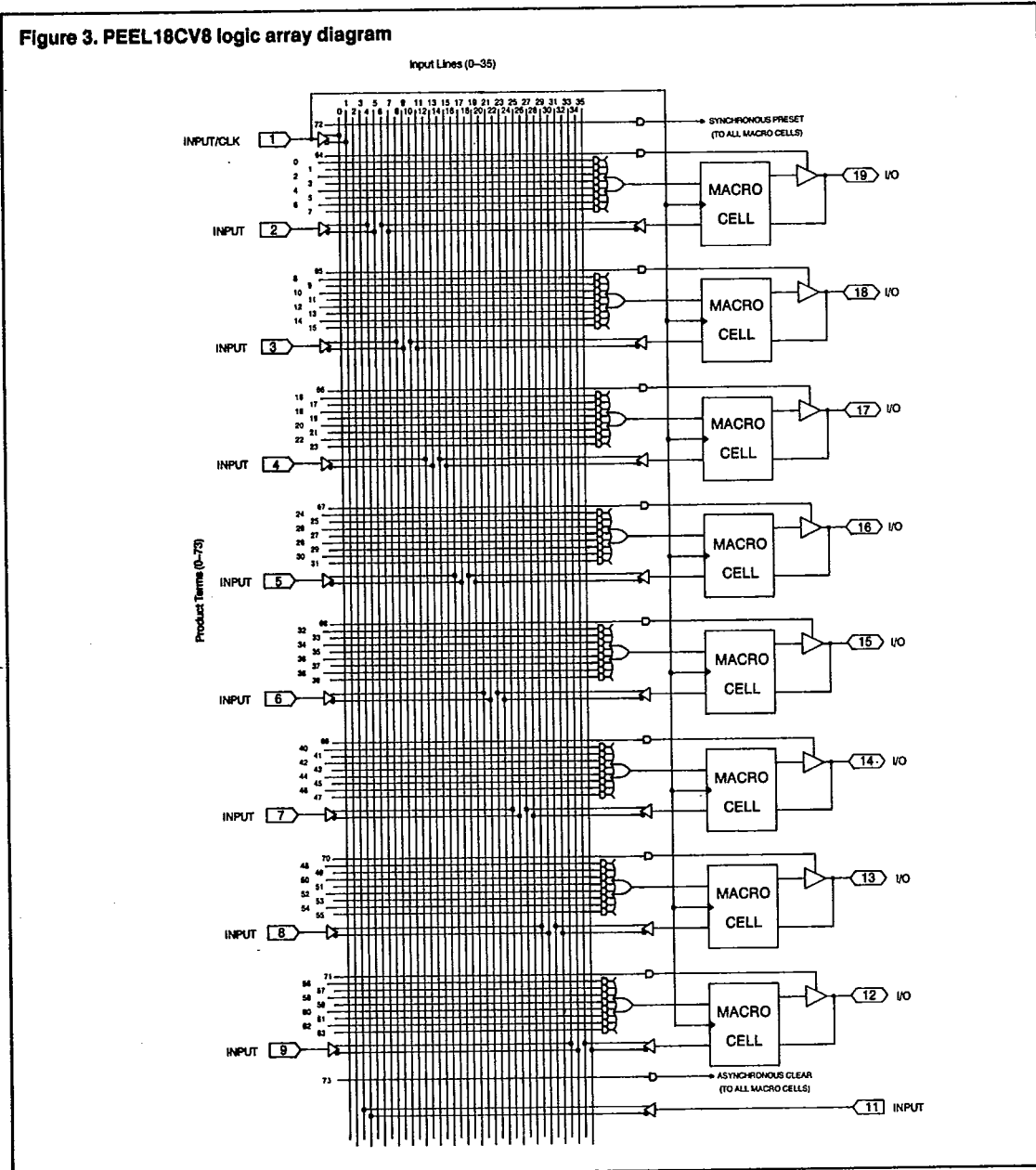


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Figure 3. PEEL18CV8 logic array diagram





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18CV8 not only reduces development and field retrofit costs but enhances testability enabling Gould to ensure 100% field programmability and function.

Packaged in a cost-effective "window-less" 20 pin DIP, the flexible architecture of the PEEL 18CV8 allows for replacement of standard SSI/MSI logic circuitry or pin-out compatible emulation of 20-pin bipolar PAL devices and the Altera EP300/310. In addition, over a hundred new logic configurations, not possible with earlier generation PLDs, can be implemented. Primary development and programming support of the PEEL 18CV8 is provided by popular third-party PC based development tools and stand-alone programmers. Gould also offers a Development System specifically for the PEEL 18CV8 and other PEEL devices.

**Architectural Overview**

The basic architecture of the PEEL 18CV8 is similar to that of earlier generation PLDs to the extent that it utilizes a sum-of-products logic array in a programmable AND fixed OR structure. This familiar logic arrangement allows user defined output functions to be created by programming the connection of input signals into the array. What makes the architecture of the PEEL 18CV8 different, however, is the increased capability and flexibility it provides resulting in a higher level of equivalent gate integration and a simplification of design.

The block diagram in figure 2 illustrates the key elements of the PEEL 18CV8 architecture. Externally, the PEEL 18CV8 provides up to 18 inputs and 8 outputs for use. At the core is a programmable electrically erasable "AND array" of 36 input lines by 74 product terms. The 36 input lines are derived from the true and complements of the 18 possible input pins. The 74 product terms are made up of: 1 synchronous preset term, 1 asynchronous clear term, 8 output enable terms and 64 terms divided into groups of 8 each feeding into an OR function.

Each OR function is directly associated with one of eight macro cells and I/O pins. An individual macro cell can be programmed into one of twelve different configurations. Depending on the configuration, the output of the macro cell can be fed back into the array or output via its associated I/O pin. The configurations include various arrangements for bi-directional I/O, registered or combinatorial

feedback, registered or combinatorial output and output polarity control. The output enable term of each I/O pin can be used to force a high impedance state for bi-directional I/O operations or for dedicated input usage. The synchronous preset term, asynchronous clear term and clock (pin 1, I/CLK) are globally routed to all macro cells.

**Logic Array Operation**

A more detailed view of the overall architecture, specifically the logic array, is illustrated by the PEEL 18CV8 Logic Array diagram in figure 3. As referred to previously, the logic array of the PEEL 18CV8 consists of:

- 36 Input Lines:
  - 10 true and complement inputs
  - 8 true and complement inputs/feedbacks
- 74 Product Terms:
  - 64 product terms (8x8 Sum-of-Products form)
  - 8 output enable product terms
  - 1 synchronous preset term
  - 1 asynchronous clear term

Looking at the logic array diagram, the 36 input lines (0-35) run vertically and the 74 product terms (0-73) run horizontally. Each input line and product term intersection in the array has an associated programmable E<sup>2</sup>PROM memory cell that determines whether the intersection is connected or open. A connection allows an input line to become a logical input of the intersected product term (AND gate). Thus, each product term, although unlikely in a real application, truly equals a 36 input AND gate.

In figure 3, the logic array has 64 product terms that are divided into groups of 8 each feeding into a sum (OR gate). By connecting specific inputs or I/O macro cell feedbacks to the product terms, complex sum-of-products logic functions can be created. Each sum feeds into its associated I/O macro cell where the logic function can be further controlled for output to an I/O pin or feedback into the array.

In addition to the 64 product terms of the 8 sum-of-product groups, there are 8 output enable product terms, 1 synchronous preset product term and 1 asynchronous clear product term. These additional terms are used to directly control specific I/O functions which are covered in the following section.

PLDs

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**I/O Macro Cell and Output Enable Operation**

A great amount of architectural flexibility is provided by the PEEL 18CV8's reconfigurable I/O macro cells and independently controlled output enables. A closer look at the I/O macro cell, figure 4, shows that it consists of a D-type flip-flop and two signal select multiplexers.

The D-type flip-flop operates similarly to standard TTL D flip-flops to the extent that the D input is latched on the rising edge (LOW to HIGH transition) of the CLK input and Q or Q output signals can be used. Two additional inputs are controlled by the asynchronous clear and synchronous preset terms.

When the asynchronous clear product term is asserted (HIGH) the Q output will immediately be set to a LOW regardless of the clock state. When the synchronous preset term is asserted (HIGH) the Q output will be set to a HIGH on the following rising edge (LOW to HIGH transition) of the CLK input. Priority is given to the asynchronous clear signal if both asynchronous clear and synchronous preset have been asserted. Upon power-up, the asynchronous clear function is automatically performed setting the Q outputs of all macro cell flip-flops to a LOW.

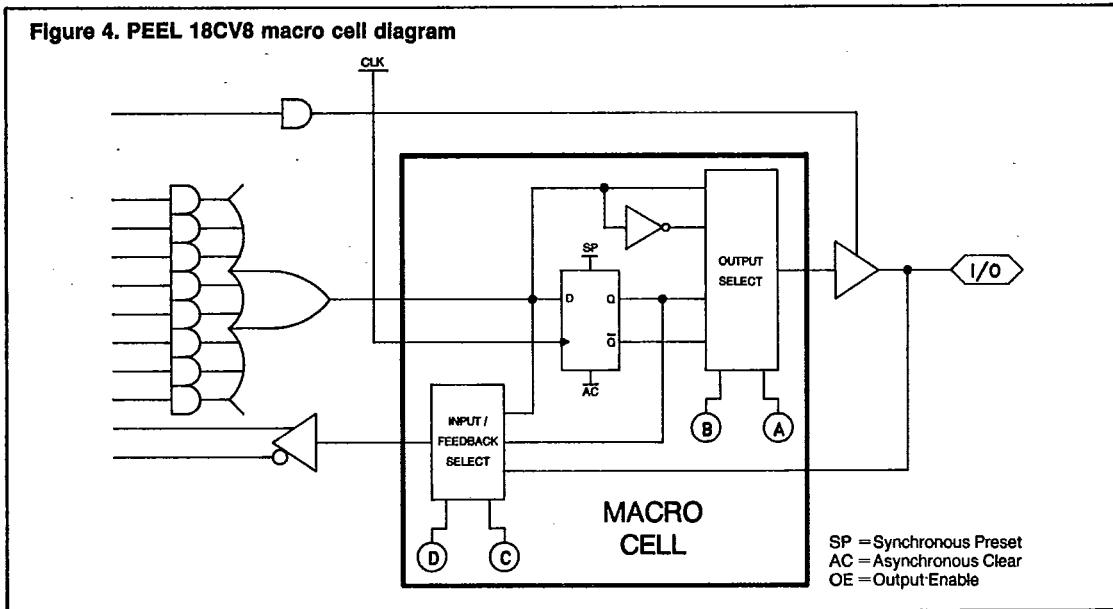
The two signal select multiplexers of each macro cell are controlled by four E<sup>2</sup>PROM programmable bits (A, B, C and D) that determine which of the twelve possible configurations the macro cell will assume. This independent flexibil-

ity allows a single PEEL 18CV8 to implement a combination of configurations among its eight macro cells. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output and output polarity control. The twelve possible I/O macro cell configurations are listed in table 1. Their equivalent circuits are illustrated in figure 5.

Table 1. PEEL 18CV8 macro cell configurations

Configuration				Input/Feedback Select	Output Select		
#	A	B	C		D		
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1			Active High
3	1	0	1	1		Combinatorial	Active Low
4	0	0	1	1			Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0			Active High
7	1	0	1	0		Combinatorial	Active Low
8	0	0	1	0			Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0			Active High
11	1	0	0	0		Combinatorial	Active Low
12	0	0	0	0			Active High

Figure 4. PEEL 18CV8 macro cell diagram





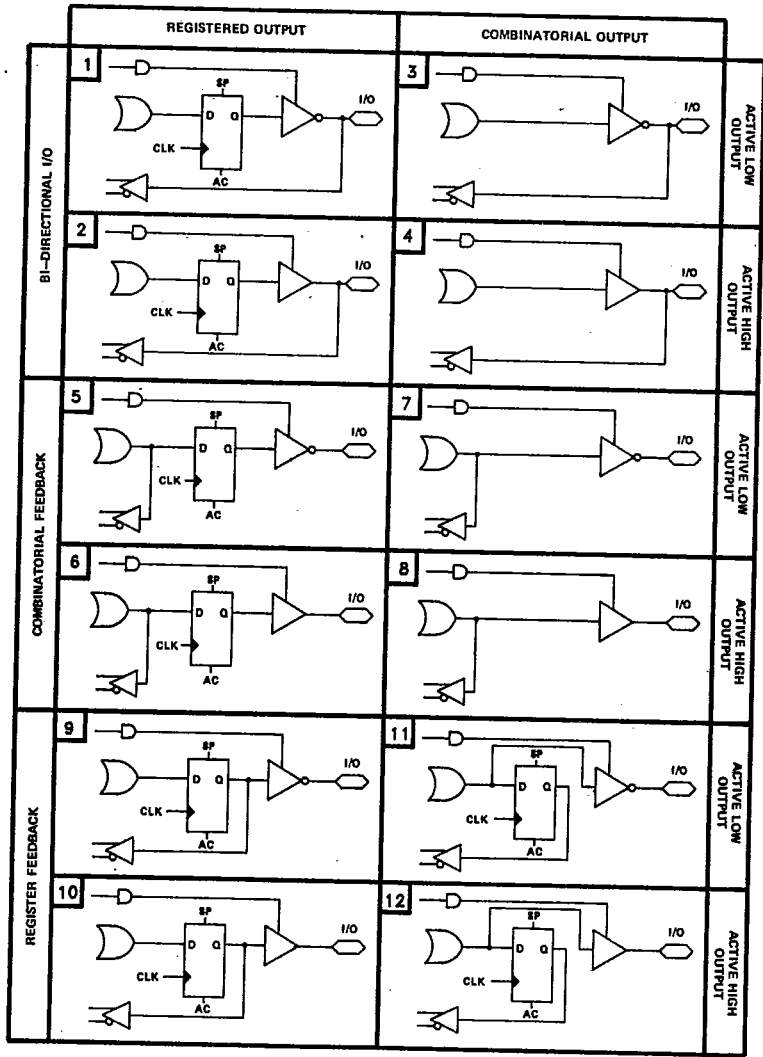
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Each of the 8 output enable terms can enable or disable the output of its associated I/O macro cell. When the output enable product term is a logical true (HIGH) the output signal is enabled to the I/O pin. When it is a logical false

(LOW) the I/O pin is in a high impedance state. The output enable product terms allow individual I/O pins to be input only or bi-direction I/O.

Figure 5. PEEL 18CV8 macro cell configuration equivalent circuits



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**Applications of the PEEL 18CV8**

The versatility of the PEEL makes it an effective alternative to conventional methods of logic design over a broad range of applications.

As an SSI/MSI logic replacement, the PEEL enhances the design process with increased flexibility, higher performance, faster development time and design security. Manufacturing benefits are also realized by requiring fewer components and interconnects resulting in more efficient use of space, simplified inventory control and higher reliability.

As a bipolar PAL replacement, the PEEL has comparable speed yet offers several advantages including: enhanced design flexibility, simplified inventory control, reduced power consumption, reprogrammability, and 100% factory testability for function and programming.

Design flexibility is of particular importance since the PEEL 18CV8 not only emulates the majority of the 20 pin PAL devices (see table 2) but also allows functions found among several PAL device types to be combined. In addition, completely new functions, not supported by the standard PAL devices, can be implemented. This flexibility means a designer can focus on the design rather than on the restrictions of a fixed architecture. Reprogrammability is also a key benefit over one time programmable PALs. This feature adds convenience and cost savings in development prototyping and field retrofitting of systems. Converting existing PAL designs to the PEEL 18CV8 for plug-in replacement is easily accomplished using the PEEL evaluation or development tools described later in this data sheet.

As a design alternative to low-density gate arrays, one or more PEEL 18CV8s offer a cost-effective and low-risk option. With its architectural flexibility and equivalent gate density of approximately 300 gates, designs traditionally employing low-density gate arrays can be implemented quickly at no factory development (NRE) cost. Unlike the lead times encountered with gate arrays, the PEEL 18CV8 is off-the-shelf available. Furthermore, if a design error is

made or an upgrade is necessary, the changes can simply be reprogrammed.

Similar to SSI/MSI logic, PALs and low density gate arrays, applications of the PEEL 18CV8 cover all the primary areas of system design including, data processing, communications, industrial, consumer, military and transportation. Specific functions implemented using the PEEL 18CV8 range from basic logic and system support circuitry to stand-alone controllers. Some of these applications possibilities include:

- **SSI/MSI Logic Replacement/Customization**
  - Random logic
  - Decoders/encoders
  - Comparators
  - Multiplexers
  - Counters
  - Shift registers
- **Processor System Support**
  - Address decoding
  - Wait-state generation
  - Memory protection
  - Memory refresh
  - DMA control
  - Interrupt control
  - Timer/Counter functions
  - Bus arbitration and interface
  - Error detection and correction
- **I/O Interface and Support**
  - Intelligent I/O port
  - Data Comm interface
  - Display interface
  - Keyboard scanning
  - Disk and tape drive control
  - Front panel interface
- **Stand-Alone Non  $\mu$ P Based Controllers**
  - Motor control
  - Sensor monitoring
  - Security access control
  - Display Control

**Table 2. PLD devices that can be emulated by the PEEL 18CV8**

**20-pin PAL**

Output Type	Part Number and I/O Capacity							
Combinatorial-High	10H8	12H6	14H4	16H2	16H8	16HD8		
Combinatorial-Low	10L8	12L6	14L4	16L2	16L8	16LD8		
Combinatorial-Polarity					16P8		18P8	
Registered-Low				16R4	16R6	16R8		
Registered-Polarity				16RP4	16RP6	16RP8		

**ALTERA**

EP 300/310
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**Absolute Maximum Ratings<sup>8</sup>**

Symbol	Parameter	Conditions	MIN	MAX	UNIT
V <sub>CC</sub>	Supply Voltage	relative to GND	-5	7.0	V
V <sub>I</sub>	Voltage applied to Input <sup>10</sup>	relative to GND <sup>12</sup>	-5	7.0	V
V <sub>O</sub>	Voltage applied to Output	relative to GND <sup>12</sup>	-5	7.0	V
I <sub>O</sub>	Output Current	per pin (I <sub>OL</sub> , I <sub>OH</sub> )		±25	mA
T <sub>ST</sub>	Storage Temperature		-65	+125	°C
T <sub>LT</sub>	Lead Temperature	(soldering 10 seconds)		+300	°C

**Operating Ranges**

Symbol	Parameter	Conditions	MIN	MAX	UNIT
V <sub>CC</sub>	Supply Voltage	Commercial	4.75	5.25	V
T <sub>A</sub>	Operating Temperature	Commercial	0	+70	°C
T <sub>R</sub>	Clock Rise Time	<sup>5</sup>		500	nS
T <sub>F</sub>	Clock Fall Time	<sup>5</sup>		500	nS
T <sub>RVCC</sub>	V <sub>CC</sub> Rise Time	<sup>5</sup>		10	mS

**D.C. Characteristics** (Over Operating Range Specifications)

Symbol	Parameter	Conditions	MIN	TYP <sup>7</sup>	MAX	UNIT
I <sub>CCS</sub>	V <sub>CC</sub> Current Standby	V <sub>N</sub> =V <sub>L</sub> or V <sub>H</sub> <sup>9</sup>		12	25	mA
I <sub>CCA</sub>	V <sub>CC</sub> Current Active	V <sub>N</sub> =V <sub>L</sub> or V <sub>H</sub> . All inputs, feedback and I/O switching. <sup>9</sup>			I <sub>CCS</sub> + .7 mA/MHz	mA
I <sub>L</sub>	Input Leakage	V <sub>N</sub> =GND to V <sub>CC</sub>			±10	µA
I <sub>OZ</sub>	Output Leakage	I/O = High Impedance, V <sub>O</sub> =GND to V <sub>CC</sub>			±10	µA
V <sub>IL</sub>	Input Low Voltage		-0.3		.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V <sub>CC</sub> +0.3	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +8.0mA <sup>12</sup>			.45	V
V <sub>OLC</sub>	Output Low Voltage CMOS	I <sub>OL</sub> = 10µA			0.1V	V
V <sub>OH</sub>	Output High Voltage TTL	I <sub>OH</sub> = -4.0mA	2.4			V
V <sub>OHc</sub>	Output High Voltage CMOS	I <sub>OH</sub> = -10µA	V <sub>CC</sub> -0.1V			V

**Capacitance<sup>3</sup>**

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
C <sub>N</sub>	Input Capacitance	f=1MHz		4	6	pf
C <sub>OUT</sub>	Output Capacitance	f=1MHz		8	12	pf
C <sub>CLK</sub>	Clock Pin Capacitance	f=1MHz		8	13	pf



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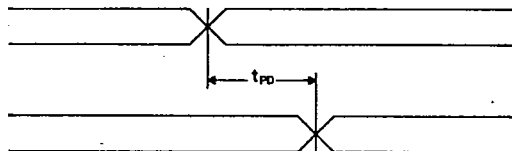


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**A.C. Switching Waveforms**

**Combinatorial**

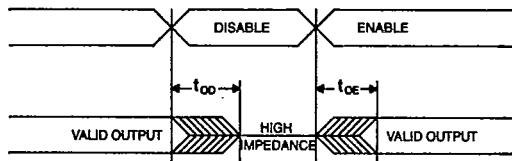
Input, I/O or Feedback



Combinatorial Output

**Output Enable**

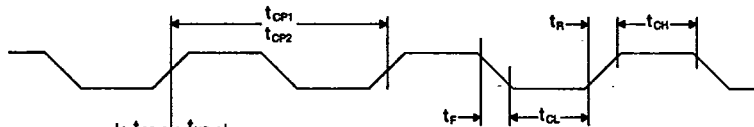
Input to Output Enable Term



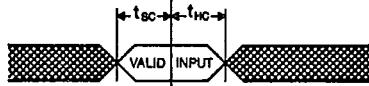
Registered or Combinatorial Output

**Registered**

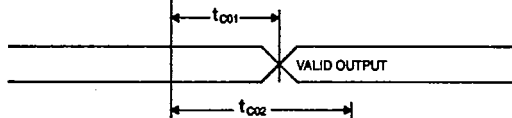
Clock



Input to Product or Sync. Preset Term



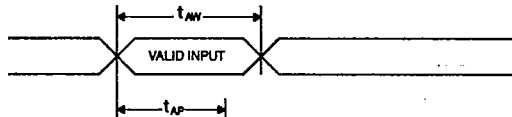
Registered Output



Combinatorial Output (From Registered Feedback)



Input to Async. Clear Term

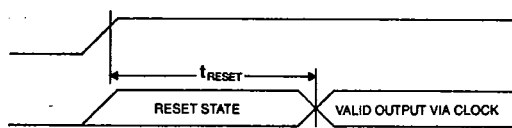


Registered Outputs



**Power-Up Reset**

V<sub>CC</sub>



Registered Output





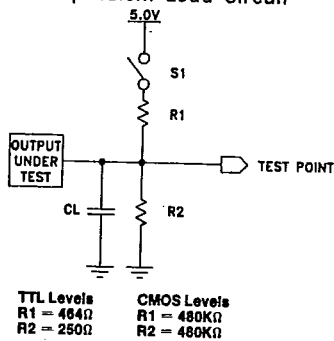
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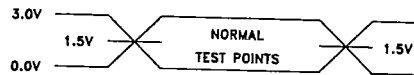
**A.C. Characteristics** (Over Operating Range Specifications)

Symbol	Parameter	Conditions	18CV8-25		18CV8-35		18CV8-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PD}$	Input <sup>4</sup> to combinatorial output			25		35		50	nS
$t_{OD}$	Input <sup>4</sup> to output disable	<sup>6</sup>		25		35		50	nS
$t_{OE}$	Input <sup>4</sup> output enable	<sup>6</sup>		25		35		50	nS
$t_{SC}$	Input <sup>4</sup> set-up to clock		20		30		32		nS
$t_{HC}$	Input <sup>4</sup> hold after clock		0		0		0		nS
$t_{CL}$	Clock low time	<sup>5</sup>	15		15		20		nS
$t_{CH}$	Clock high time	<sup>5</sup>	15		15		20		nS
$t_{CO1}$	Clock to output			15		20		28	nS
$t_{CO2}$	Clock to combinatorial output delay via registered feedback			35		50		70	nS
$t_{CP1}$	Minimum clock period (register feedback to register output via internal path)			30		45		42	nS
$f_{MAX1}$	Max. frequency ( $1/t_{CP1}$ )		35.3		22.2		23.8		MHz
$t_{CP2}$	Minimum clock period ( $t_{SC} + t_{CO1}$ )			35		50		60	nS
$f_{MAX2}$	Max. frequency ( $1/t_{CP2}$ )		28.5		20		16.6		MHz
$t_{AV}$	Async. clear pulse width	<sup>11</sup>	25		35		50		nS
$t_{AP}$	Input <sup>4</sup> to async. clear			30		40		55	nS
$t_{RESET}$	Power-on reset time for registers in clear state	<sup>5</sup>		5		5		5	uS

A.C. Equivalent Load Circuit



A.C. Testing Input/Output Waveform



A.C. Test Point/Load Circuit Table

AC TEST	TEST POINT	CL	S1
NORMAL	1.5V	30pf	closed
IOE(Z=1)	VOH	30pf	open
IOE(Z=0)	VOL	30pf	closed
IOD(1=Z)	VOH-.5V	5pf	open
IOD(0=Z)	VOL+.5V	5pf	closed

Z=High Impedance

**Notes**

- <sup>1</sup> Minimum DC input is  $-0.5V$ , however, inputs may undershoot to  $-2.0V$  for periods less than 20ns.
- <sup>2</sup> Voltage applied to input or output must not exceed  $V_{CC} + 1.0V$ .
- <sup>3</sup> These measurements are periodically sample tested.
- <sup>4</sup> "Input" refers to an Input signal.
- <sup>5</sup> Test points for Clock and  $V_{CC}$  in  $t_{r1}$ ,  $t_{f1}$ ,  $t_{CL}$ ,  $t_{CH}$ , and  $t_{RESET}$  are referenced at 10% and 90% levels.
- <sup>6</sup> See A.C. test point / load circuit table for  $t_{OE}$ , and  $t_{OD}$  testing.
- <sup>7</sup> Typical values and capacitance are measured at  $V_{CC} = 5.0V$  and  $T_A = 25^\circ C$ .
- <sup>8</sup> Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.
- <sup>9</sup> I/O pins are open (no load).
- <sup>10</sup>  $V_{AV}$  specified is not for program/verify operation. Contact Gould for information regarding PEEL 18CV8 program/verify specifications.
- <sup>11</sup> Minimum width required to ensure proper asynchronous clear operation and does not imply rejection of signal less than this value.
- <sup>12</sup> Contact factory for increased IOL requirements.





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Packaging

20-Pin Plastic

