Protection of Lithium Ion/Lithium Polymer Battery(one cell)
Monolithic IC MM3077

Outline

This protection IC was developed for use with lithium-ion/lithium polymer secondary 1-cell serial batteries. It detects overcharge, overdischarge, discharge overcurrent and other abnormalities, and functions to protect the battery by turning off the external FET-SW.
The IC also has a built-in timer circuit (for detection delay times), so fewer external parts can be used in protection circuit configuration.

Features

(1) High withstand voltage CMOS process used	Charger connection absolute maximum rating 28V
(2) High electrostatic tolerance	20kV (150pF, 330Ω aerial, contact discharge)
(3) Detection voltage precision	Overcharge detection precision ±25mV (0 ~ 50°C)
	Discharge overcurrent detection precision ±10mV
	Overdischarge detection precision ±58mV
(4) Built-in detection delay time (timer circuit)	Overcharge detection delay time 0.25 ~ 7.0s (mask option)
	Overdischarge detection delay time 4.0 ~ 32.0ms (mask option)
	Discharge overcurrent detection delay time 4.0 ~ 32.0ms (mask option)
	Short detection delay time 400µs
(5) Includes detection function for too large charger	Detection voltage for too large charger 8.0V
(6) Setting DS pin	At V_{DD} level allows shortening of overcharge, excess discharge, discharge overcurrent detection and reset delay time.

(7) OV charging prohibition function (mask option)

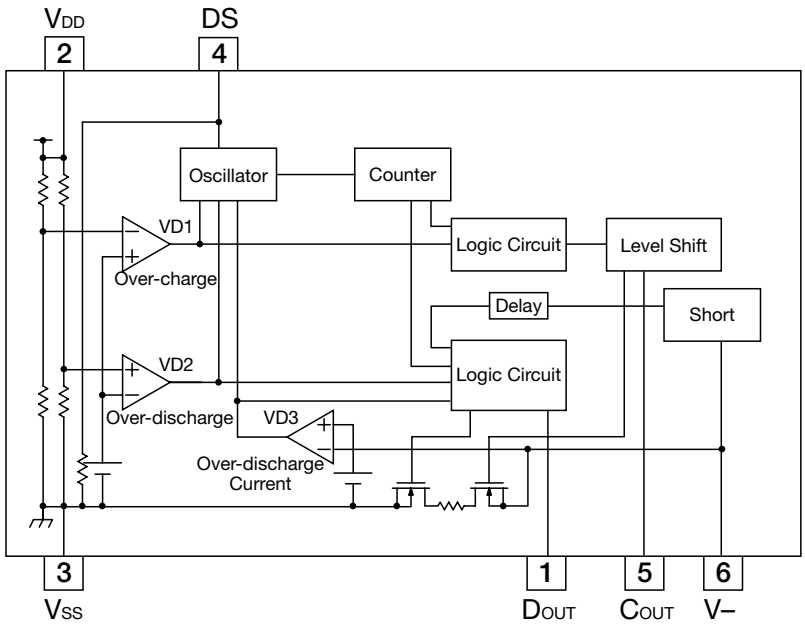
Package

SOT-26
SON-6

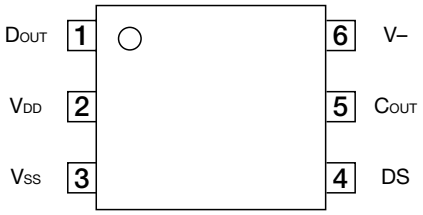
Applications

Lithium-ion/lithium polymer battery protection circuits

Block diagram



Pin Assignment



1	DOUT
2	VDD
3	VSS
4	DS
5	COUT
6	V–

Pin Description

Pin No.	Pin Name	Function
1	DOUT	Over discharge detection Output. Output type is CMOS.
2	VDD	VDD terminal. Connected to IC substrait.
3	VSS	VSS terminal. Connected to IC ground.
4	DS	Delay shorten terminal.
5	COUT	Over charge detection Output. Output type is CMOS.
6	V–	Charger negative voltage input.

Absolute maximum ratings (T_{OPR}=25°C, V_{SS}=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.3 ~ 12	V
Charger minus pin input voltage	V–	V_{DD}–28 ~ V_{DD}+0.3	V
DS pin input voltage	V_{DS}	V_{SS}–0.3 ~ V_{DD}+0.3	V
C_{OUT} pin output voltage	VC_{OUT}	V_{DD}–28 ~ V_{DD}+0.3	V
D_{OUT} pin output voltage	VD_{OUT}	V_{SS}–0.3 ~ V_{DD}+0.3	V
Operating temperature	T_{OPR}	–40 ~ +85	°C
Storage temperature	T_{STG}	–55 ~ +125	°C

Electrical characteristics (T_{OPR}=25°C)

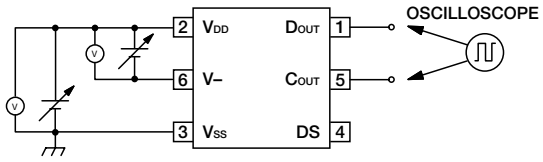
Parameter	Symbol	Conditions	min.	typ.	max.	Unit	*2
Operating input voltage	$V_{DD}1$	V_{DD}–V_{SS}	1.5		10.0	V	A
Minimum operating voltage for 0V charging	V_{ST}	V_{DD}–V–, V_{DD}–V_{SS}=0V			1.2	V	A
Over-charge detection voltage	$V_{DET}1$	R1=330Ω T_{OPR}=0 ~ 50°C, *1	4.275	4.300	4.325	V	B
Over-charge detection delay time	$tV_{DET}1$	V_{DD}=3.6V→4.4V	0.7	1.0	1.3	s	B
Over-charge release voltage	$V_{REL}1$	R1=330Ω	4.050	4.100	4.150	V	B
Over-charge release delay time	$tV_{REL}1$	V_{DD}=4.4V→3.6V	5.6	8.0	10.4	ms	B
Over-discharge detection voltage	$V_{DET}2$	Detect falling edge of supply voltage	2.242	2.300	2.358	V	D
Over-discharge detection delay time	$tV_{DET}2$	V_{DD}=3.6V→2.2V	16.8	24.0	31.2	ms	D
Over-discharge release delay time	$tV_{REL}2$	V_{DD}=3V, V–=3V→0V	2.8	4.0	5.2	ms	E
Over-discharge current detection voltage	$V_{DET}3$	Detect falling edge of supply voltage	0.140	0.150	0.160	V	F
Over-discharge curent detection delay time	$tV_{DET}3$	V_{DD}=3V, V–=0V→1V	8.4	12.0	15.6	ms	F
Over-discharge current release delay time	$tV_{REL}3$	V_{DD}=3V, V–=3V→0V	2.8	4.0	5.2	ms	F
Short detection voltage	V_{SHORT}	V_{DD}=3V	V_{DD}–1.2	V_{DD}–0.9	V_{DD}–0.6	V	F
Short detection delay time	t_{SHORT}	V_{DD}=3V, V–=0V→3V	250	400	600	µs	F
Over-discharge current release resistance	R_{SHORT}	V_{DD}=3.6V, V–=1V	30	50	100	kΩ	F
DS pin "H"input voltage	V_{IH}		V_{DD}–0.5		V_{DD}+0.3	V	H
DS pin pull-down resistance	R_{DS}	V_{DD}=3.6V	6.5	13.0	26.0	kΩ	H
C_{OUT} pin Nch ON voltage	$V_{OL}1$	I_{OL}=50µA, V_{DD}=4.5V		0.4	0.5	V	I
C_{OUT} pin Pch ON voltage	$V_{OH}1$	I_{OH}=50µA, V_{DD}=3.9V	3.4	3.7		V	J
D_{OUT} pin Nch ON voltage	$V_{OL}2$	I_{OL}=50µA, V_{DD}=2.0V		0.2	0.5	V	K
D_{OUT} pin Pch ON voltage	$V_{DD}2$	I_{DD}=50µA, V_{DD}=3.9V	3.4	3.7		V	L
Current consumption	I_{DD}	V_{DD}=3.9V, V–=0V		3.0	6.0	µA	M
Current consumption at stand-by	I_S	V_{DD}=2.0V			0.1	µA	M
Over voltage charger detection voltage	$V_{CHG}1$	V_{DD}=3.6V	6.0	8.0	10.0	V	G
Over voltage charger release voltage	$V_{CHG}2$	V_{DD}=3.6V	5.3	7.3	9.3	V	G

*1 The parameter is guaranteed by desing.

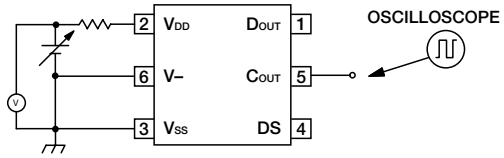
*2 The test circuit symbols on next page.

Test circuit

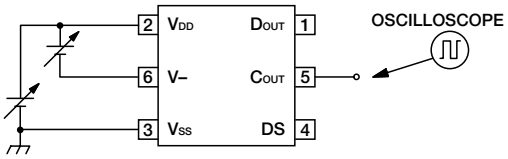
A



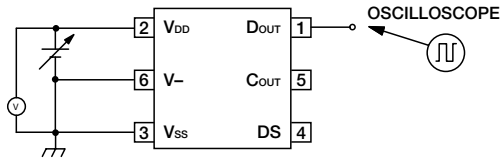
B



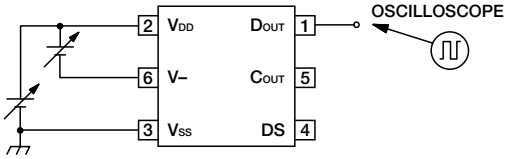
C



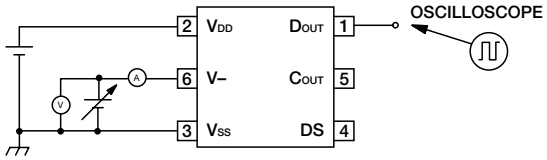
D



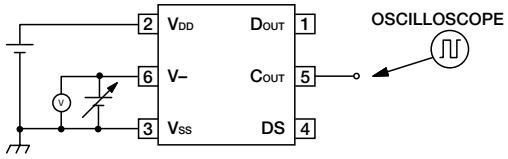
E



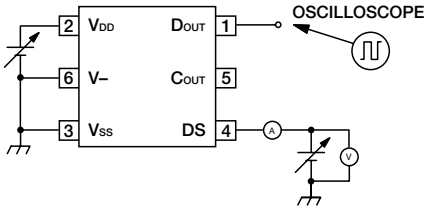
F



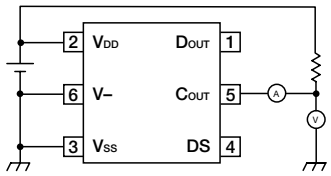
G



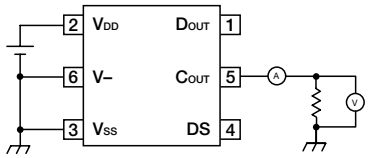
H



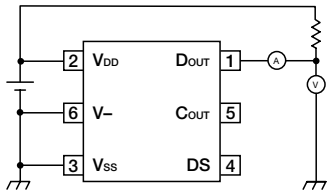
I



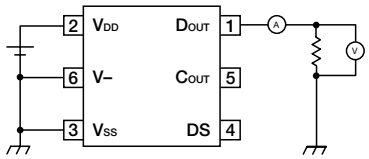
J



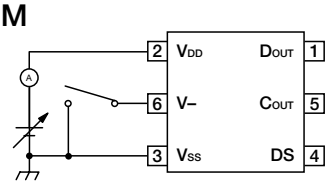
K



L



M



Description

1. Over charge detection circuit (VD1)

This IC monitor V_{DD} pin voltage, when the voltage of V_{DD} pin cross overcharge detection voltage (4.30V typ.) from a low value higher than the overcharge detection voltage, the IC sense a overcharging and external charging control Nch MOS FET turns to OFF with C_{OUT} pin being low level.

After detecting overcharge when the V_{DD} pin voltage is coming down to a level lower than overcharge release voltage (4.10V typ.) external charging control Nch MOS FET turns to ON with C_{OUT} pin being high level.

After detecting overcharge in the V_{DD} pin voltage, connecting system load to the battery charger makes load current allowable supplied to parasitic diode of charging control FET. The C_{OUT} pin level would be high when the V_{DD} pin level is coming down to a level below the overcharge detection voltage by continuous sending a load current.

There are delay time set in IC when the overcharge and the overcharge release are detected. When the V_{DD} level is going up to a higher level than overcharge detection voltage if the V_{DD} voltage would be back to a level lower than the overcharge detection voltage within a time period of the over charge release delay time (1.0s typ.). The overcharge detection does not release when returning to former state in the overcharge release dead time (8ms typ.) even if the load is connected after the charger is removed when the V_{DD} pin voltage is lower than the overcharge release voltage with the overcharge detected.

A level shifter incorporated in a buffer drive for the C_{OUT} to the V-pin voltage and the high level of C_{OUT} is set to V_{DD} voltage with CMOS buffer.

2. Over discharge detection circuit (VD2)

This IC monitors V_{DD} pin voltage, and when the voltage crosses the overdischarge detection voltage (2.30V typ.) from high value to a value lower than the overdischarge detection voltage, this IC sense an overdischarge and an external discharging control Nch MOS FET turns to OFF with D_{OUT} pin being at low level.

The release from the overdischarge is done only by connecting the charger. Charging current is supplied through a parasitic diode of Nch MOS FET when the V_{DD} pin voltage is below the overdischarge detection voltage to the connection of the charger, and the D_{OUT} pin enters the state which can be discharged by becoming high level,and turning on Nch MOS FET when the V_{DD} pin voltage rises more than the overdischarge detection voltage.

The C_{OUT} pin becomes high level and charging current is supplied if the voltage of the charger is more than the maximum value of 0V charging lowest operating voltage when the voltage of the battery is 0V.

An output delay time for the overdischarge detection is fixed internally (8ms typ.). When V_{DD} pin voltage becomes lower the over discharge detection voltage if V_{DD} pin higher more than the over discharge detection voltage in delay time even does not enter the over discharge detection mode.
Moreover, when the over discharge release,delay time is set (4ms typ.).

All the circuits are stopped, and after the overdischarge is detected, it is assumed the state of the standby, and decreases the current (standby current) which IC consumes as much as possible (The V_{DD} =2V 0.1μA max.).

The output type of D_{OUT} pin is CMOS having high level of V_{DD} and low level of V_{SS} .

3. Discharging over current detector,Short detector (VD3, Short Detector)

When the V-pin voltage is going up to a value during the short detection voltage (V_{DD}-0.9V typ.) and overdischarge current detection voltage (0.150V typ.) is overdischarge current detection mode, when the V-pin voltage higher than short detection voltage makes the short detection mode. This leads the external discharge control Nch MOS FET turns to OFF with the D_{OUT} pin being at low level.

An output delay time for the overdischarge current detection is fixed internally (12ms typ.).
When V-pin voltage becomes during the over discharge current detection voltage and the short circuit detection if V-pin lowers more than the over discharge current detection voltage in delay time even does not enter the over discharge current detection mode. Moreover,when the over discharge current release, delay time is set (4ms typ.).

The delay time set in IC exists when the short circuit is detected (400μs typ.).

The over discharge current release resistance (100kΩ typ.) is built into between V-pin and V_{SS} pin. When the load opened after detecting the over discharge current or the short circuit, V-pin is pulled down to the V_{SS} through the over discharge current release resistance, And IC returns automatically from the over discharge current or the short circuit detection mode when V-pin voltage becomes below the over discharge current detection voltage. When the over discharge current or the short circuit is detected, the over discharge current release resistance is turned on. The over discharge current release resistance is usually turned off.

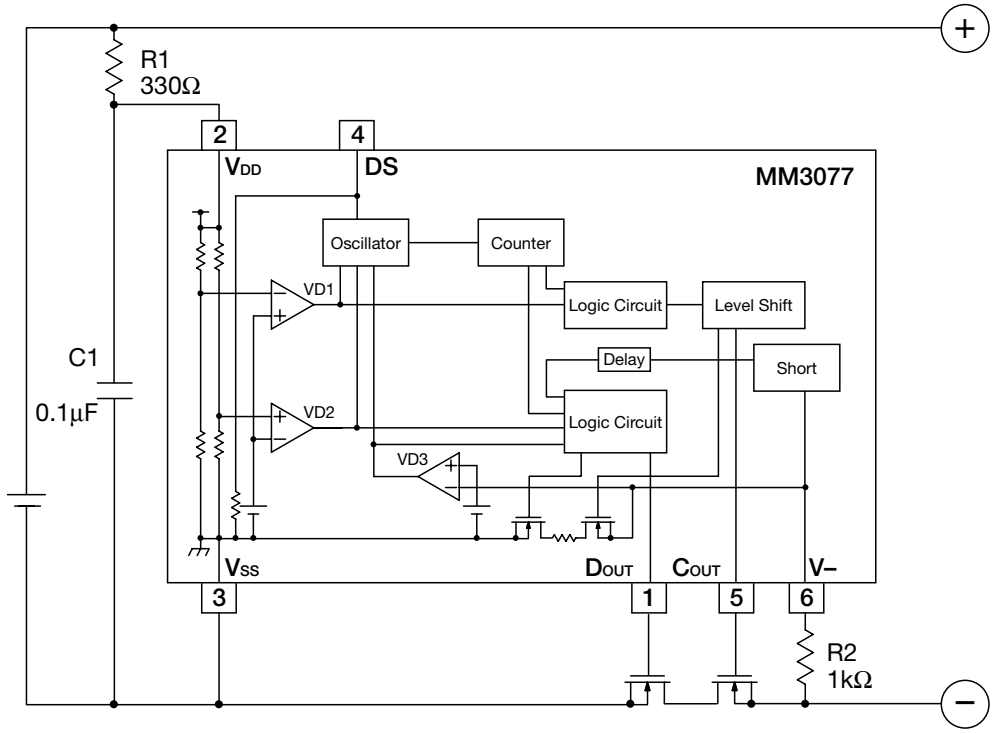
4. DS (Delay Shortening)function

The overcharge, the over discharge, the over discharge current detection, and the delay time when returning can be shortened by impressing the V_{DD} voltage level to the terminal DS.

In the DS pin, the pull-down resistance of 13kΩ is connected between V_{SS}.

Please connect V_{SS} or open the DS pin when using usually.

Application Circuit



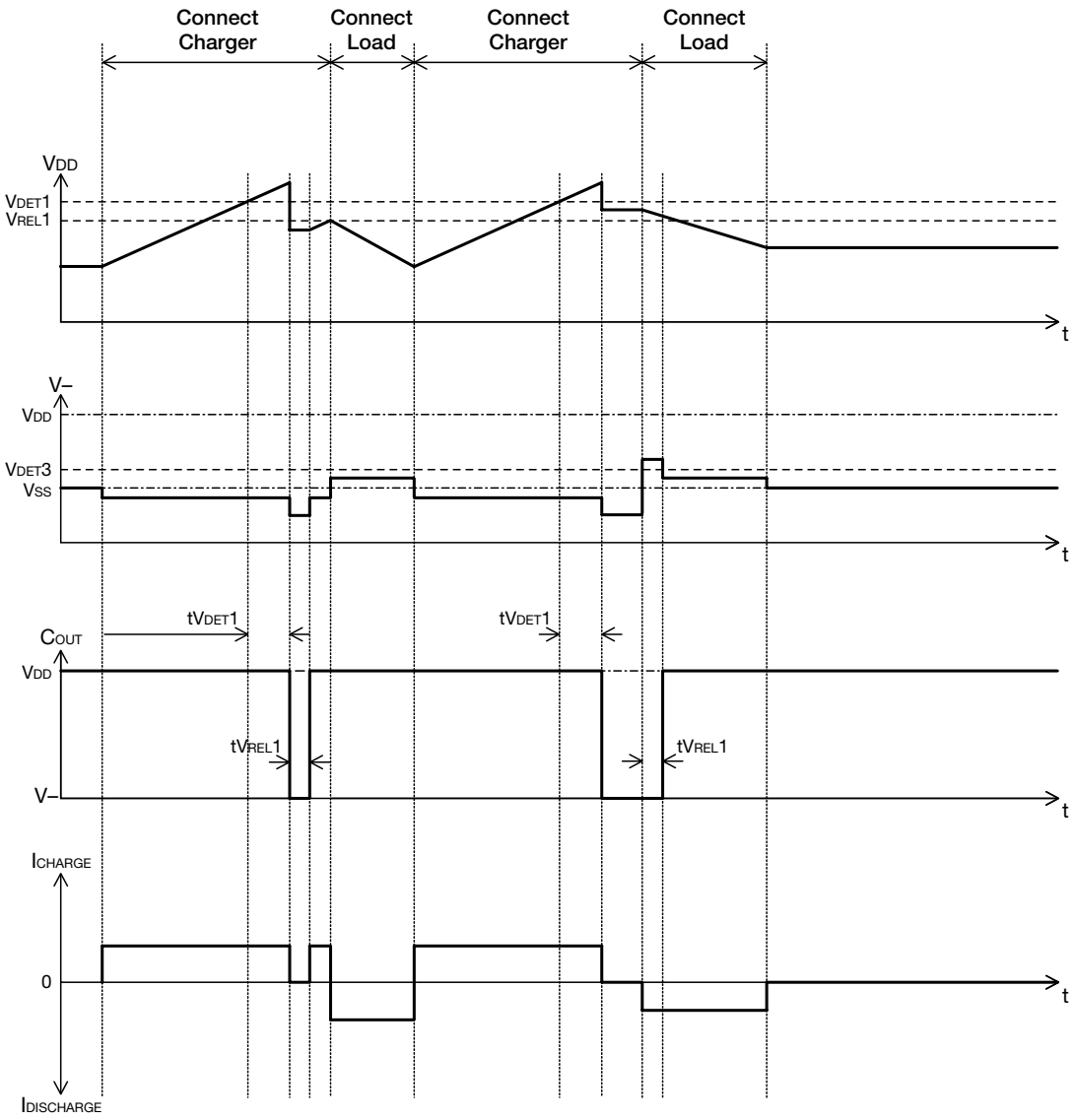
Application hints

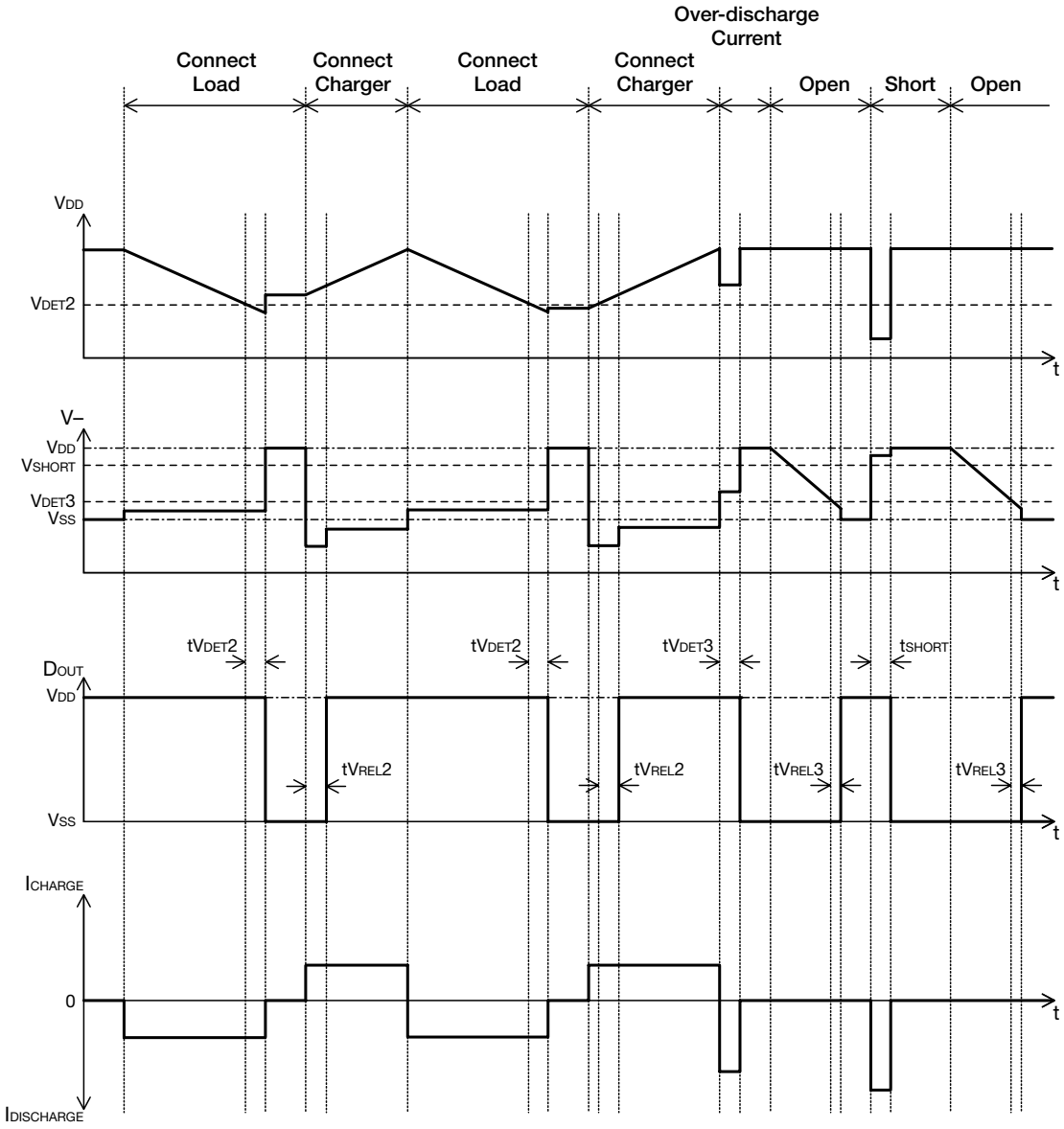
R1 and C1 stabilize a supply voltage to the MM3077. However, the detection voltage rises by the current of penetration in IC of the voltage detection when R1 is enlarged, and the value of R1 is adjusted to 1kΩ or less. Moreover, please adjust the value of C1 to 0.01µF or more to do the stability operation.

R1 and R2 are current limit resistance if a charger is connected reversibly or a high-voltage charger that exceed the absolute maximum rating is connected. R1 and R2 may cause a power consumption will be over rating of power dissipation therefore the `R1+R2` should be more than 1kΩ. Moreover, the charger connection release after the overedischarge is detected cannot be occasionally done when R2 is enlarged, and adjust the value of R2 to 10kΩ or less, please.

Timing chart

1 Over-charge operations



Timing chart

Over-discharge, over-discharge current, short operations