FINAL

COM'L: -10/12/15/20 IND: -14/18/24

MACH220-10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 68 Pins
- 96 Macrocells
- 10 ns t_{PD}
- 100 MHz f_{CNT}
- 56 Inputs with pull-up resistors
- 48 Outputs
- 96 Flip-flops; 4 clock choices
- 8 "PAL26V12" blocks with buried macrocells
- Pin-compatible with MACH120 and MACH221

GENERAL DESCRIPTION

The MACH220 is a member of AMD's high-performance EE CMOS MACH 2 device family. This device has approximately nine times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH220 consists of eight PAL blocks interconnected by a programmable switch matrix. The eight PAL blocks are essentially "PAL26V12" structures complete with product-term arrays, and programmable macrocells, including buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH220 has two kinds of macrocell: output and buried. The output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH220 has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers for use in synchronizing signals and reducing setup time requirements.

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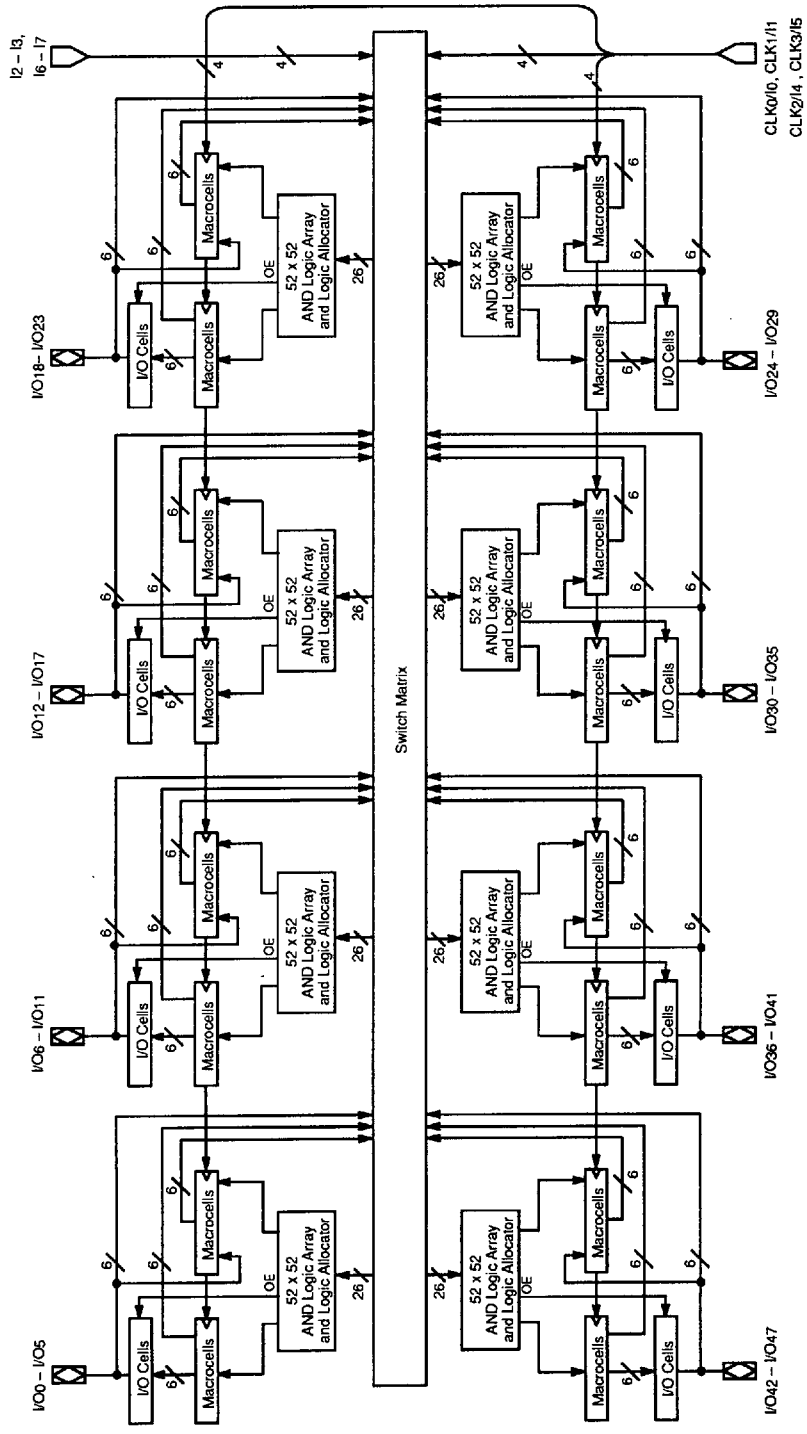
BLOCK DIAGRAM



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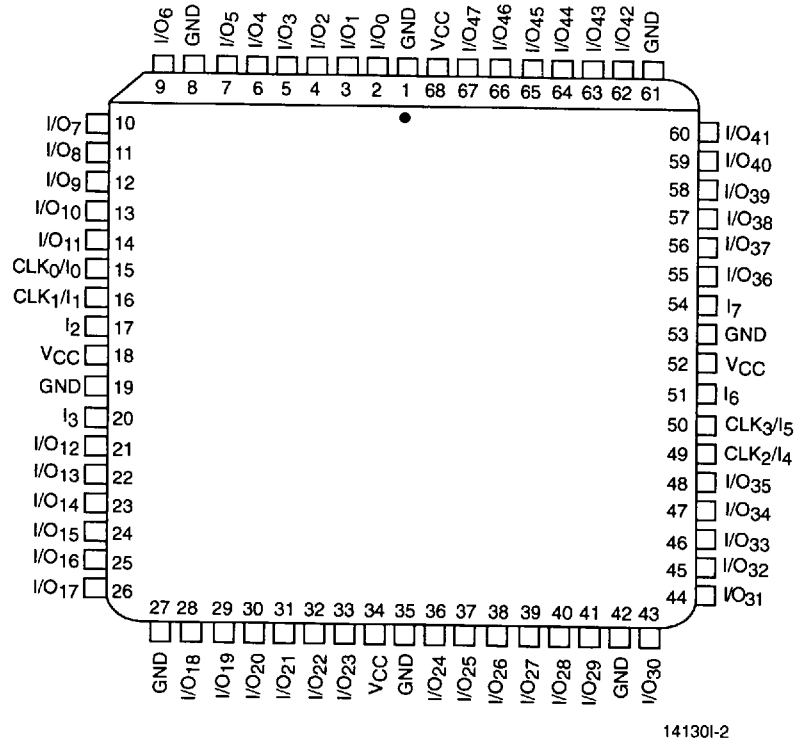
CONNECTION DIAGRAMS

Top View

PLCC



Note:
Pin-compatible with MACH120 and MACH221.

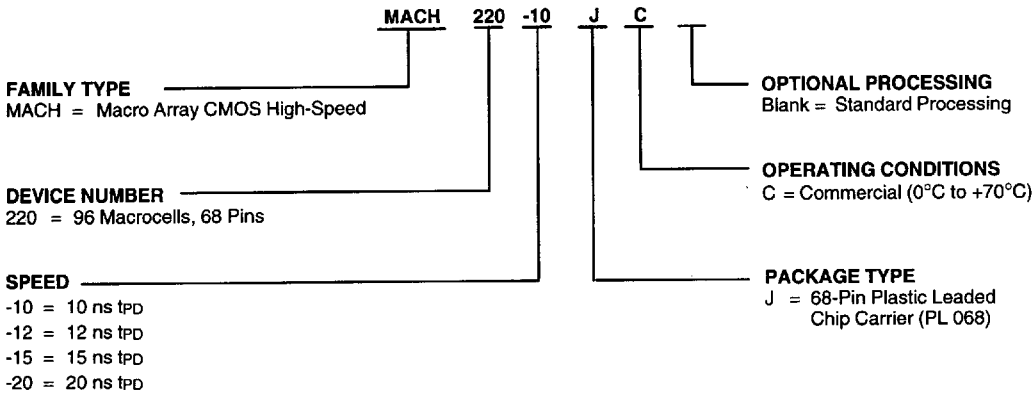
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH220-10	JC
MACH220-12	
MACH220-15	
MACH220-20	

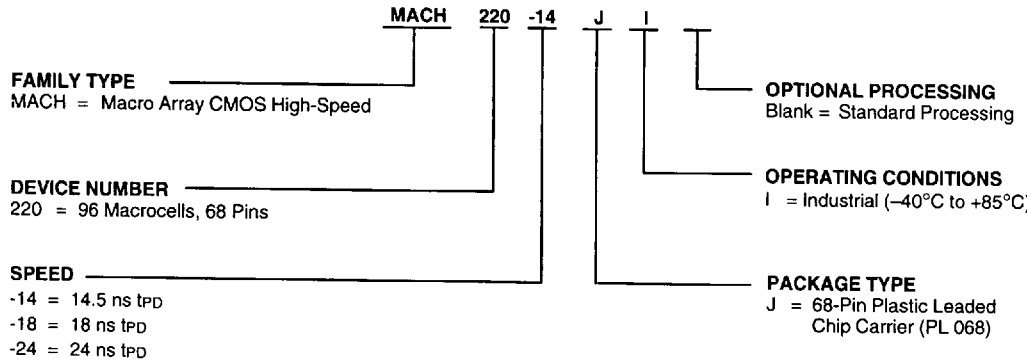
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH220-14	JI
MACH220-18	
MACH220-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH220 consists of eight PAL blocks connected by a switch matrix. There are 48 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high or low, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH220 (Figure 1) contains a 48-product-term logic array, a logic allocator, 6 output macrocells, 6 buried macrocells, and 6 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V12" with 6 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH220 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 12 internal feedback signals and 6 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH220 product-term array consists of 48 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH220 takes the 48 logic product terms and allocates them to the 12 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters
Output	Buried	
M_0		C_0, C_1, C_2
	M_1	C_0, C_1, C_2, C_3
M_2		C_1, C_2, C_3, C_4
	M_3	C_2, C_3, C_4, C_5
M_4		C_3, C_4, C_5, C_6
	M_5	C_4, C_5, C_6, C_7
M_6		C_5, C_6, C_7, C_8
	M_7	C_6, C_7, C_8, C_9
M_8		C_7, C_8, C_9, C_{10}
	M_9	C_8, C_9, C_{10}, C_{11}
M_{10}		C_9, C_{10}, C_{11}
	M_{11}	C_{10}, C_{11}

The Macrocell

The MACH220 has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH220 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

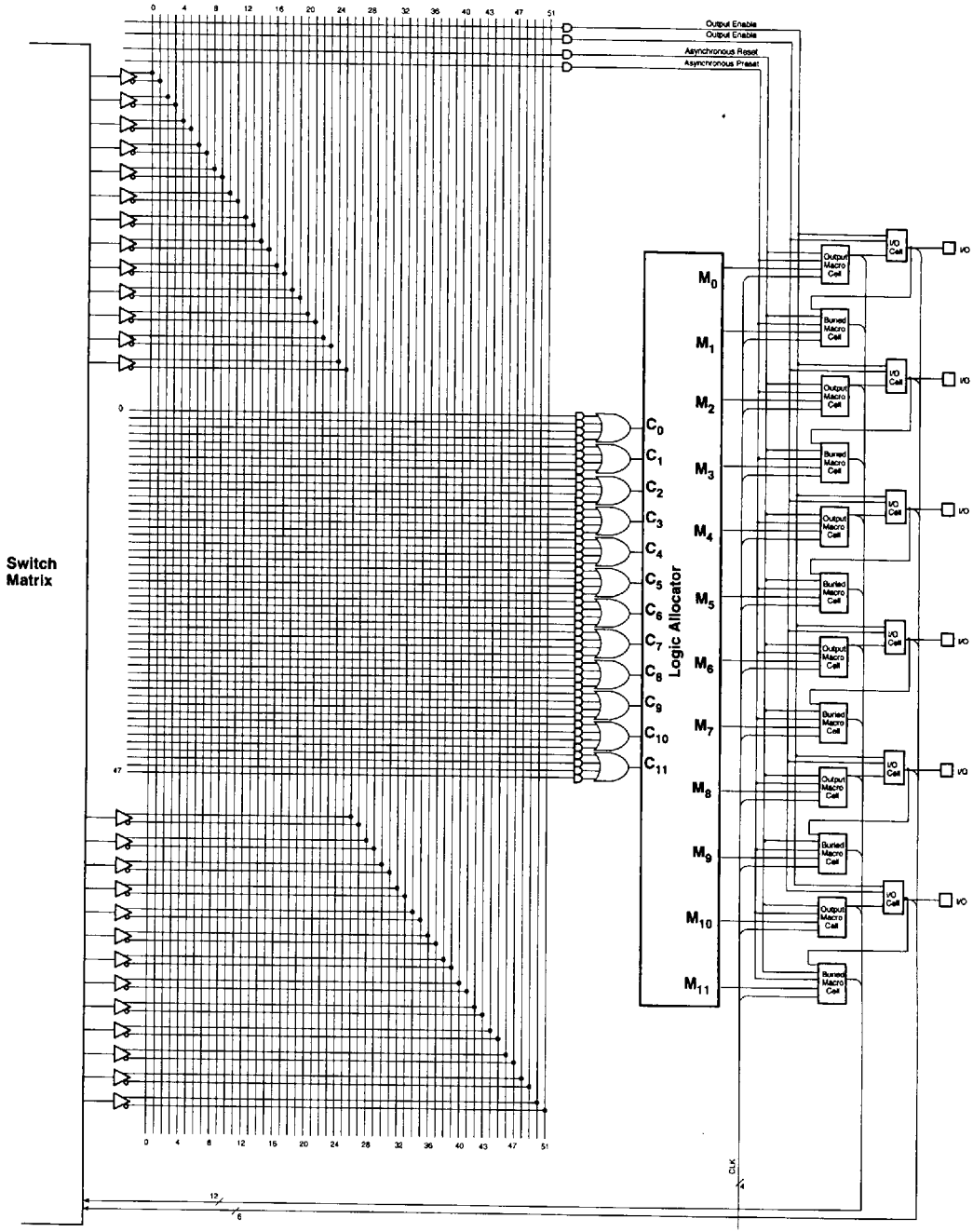


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Figure 1. MACH220 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		205		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10 Min	-10 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock		D-type	6.5		ns
			T-type	7.5		ns
t_H	Register Data Hold Time			0		ns
t_{CO}	Clock to Output				6.0	ns
t_{WL}	Clock Width		LOW	4		ns
t_{WH}			HIGH	4		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	D-type	80		MHz
			T-type	74		MHz
		Internal Feedback (f_{CNT})	D-type	100		MHz
			T-type	91		MHz
		No Feedback		125		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate			7		ns
t_{HL}	Latch Data Hold Time			0		ns
t_{GO}	Gate to Output				7.5	ns
t_{GWL}	Gate Width LOW			4		ns
t_{POL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch				14	ns
t_{SIR}	Input Register Setup Time			2		ns
t_{HIR}	Input Register Hold Time			2		ns
t_{ICO}	Input Register Clock to Combinatorial Output				15	ns
t_{ICS}	Input Register Clock to Output Register Setup		D-type	11		ns
			T-type	12		ns
t_{WICL}	Input Register Clock Width		LOW	4		ns
t_{WICH}			HIGH	4		ns
f_{MAXIR}	Maximum Input Register Frequency			125		MHz
t_{SIL}	Input Latch Setup Time			2		ns
t_{HIL}	Input Latch Hold Time			2		ns
t_{IGO}	Input Latch Gate to Combinatorial Output				17	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch				18	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate			10		ns
t_{IGS}	Input Latch Gate to Output Latch Setup			11		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-10 Min	-10 Max	Unit
t_{WIGL}	Input Latch Gate Width LOW	4		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		15	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	10		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	8		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		15	ns
t_{APW}	Asynchronous Preset Width (Note 1)	10		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	8		ns
t_{EA}	Input, I/O, or Feedback to Output Enable		10	ns
t_{ER}	Input, I/O, or Feedback to Output Disable		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit, for test conditions.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... 65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +70°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–30	–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		205		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					12		15		20	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					8		10		12	ns
t_{WL}	Clock Width			LOW	6		6		8		ns
t_{WH}				HIGH	6		6		8		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNT})		D-type	83.3		66.6		50		MHz
				T-type	76.9		62.5		47.6		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		83.3		83.3		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				7		10		13		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					10		11		12	ns
t_{GWL}	Gate Width LOW				6		6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					14		17		22	ns
t_{SIR}	Input Register Setup Time				2		2		2		ns
t_{HIR}	Input Register Hold Time				2		2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output					15		18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	12		15		20		ns
				T-type	13		16		21		ns
t_{WICL}	Input Register Clock Width			LOW	6		6		8		ns
t_{WICH}				HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		ns
t_{HIL}	Input Latch Hold Time				2		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					17		20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					19		22		27	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				9		12		15		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				13		16		21		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description	-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	
t_{WIGL}	Input Latch Gate Width LOW	6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)	12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		12		15		20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		12		15		20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *Parameters measured with 24 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... 65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = –40°C to +85°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air ..... –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–130	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 4)		205		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *Measured with a 12-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-14 Min	-14 Max	-18 Min	-18 Max	-24 Min	-24 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					14.5		18		24	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	8.5		12		16		ns
				T-type	10		13.5		17		ns
t_H	Register Data Hold Time				0		0		0		ns
t_{CO}	Clock to Output (Note 3)					10		12		14.5	ns
t_{WL}	Clock Width			LOW	7.5		7.5		10		ns
t_{WH}				HIGH	7.5		7.5		10		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	53		40		32		MHz
				T-type	50		38		30.5		MHz
		Internal Feedback (f_{CNT})		D-type	61.5		53		38		MHz
				T-type	57		44		34.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		66.5		66.5		50		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				8.5		12		16		ns
t_{HL}	Latch Data Hold Time				0		0		0		ns
t_{GO}	Gate to Output (Note 3)					12		13.5		14.5	ns
t_{GWL}	Gate Width LOW				7.5		7.5		10		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		20.5		26.5	ns
t_{SIR}	Input Register Setup Time				2.5		2.5		2.5		ns
t_{HIR}	Input Register Hold Time				3		3.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output					18		22		28	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	14.5		18		24		ns
				T-type	16		19.5		25.5		ns
t_{WICL}	Input Register Clock Width			LOW	7.5		7.5		10		ns
t_{WICH}				HIGH	7.5		7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$			66.5		66.5		50		MHz
t_{SIL}	Input Latch Setup Time				2.5		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time				3		3.5		4		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					20.5		24		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch					23		26.5		32.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate				11		14.5		18		ns
t_{IGS}	Input Latch Gate to Output Latch Setup				16		19.5		25.5		ns
t_{WIGL}	Input Latch Gate Width LOW				7.5		7.5		10		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches					19.5		23		29	ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

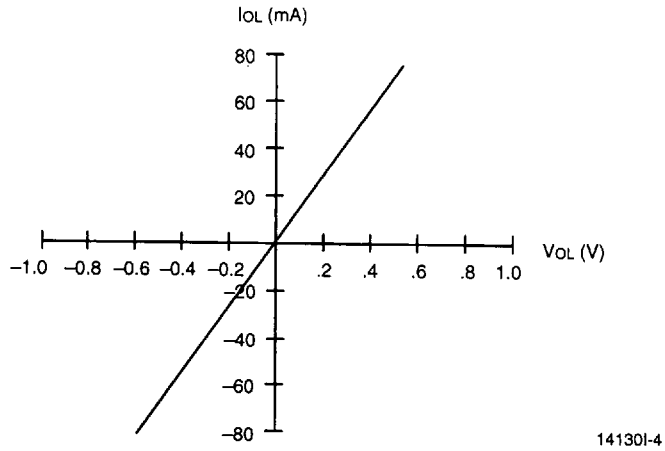
Parameter Symbol	Parameter Description	-14		-18		-24		Unit
		Min	Max	Min	Max	Min	Max	
t_{AR}	Asynchronous Reset to Registered or Latched Output		19.5		24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	14.5		18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		12		18		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		19.5		24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)	14.5		18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		14.5		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		14.5		18		24	ns

Notes:

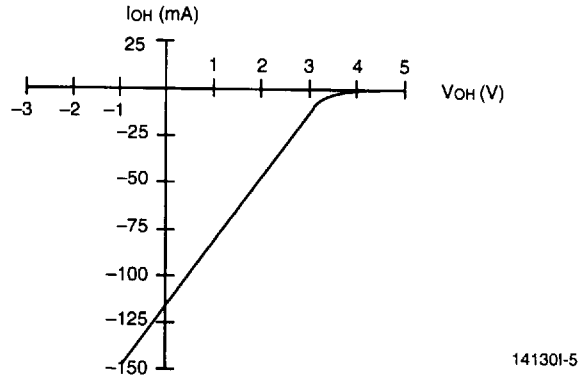
1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *Parameters measured with 24 outputs switching.*

TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

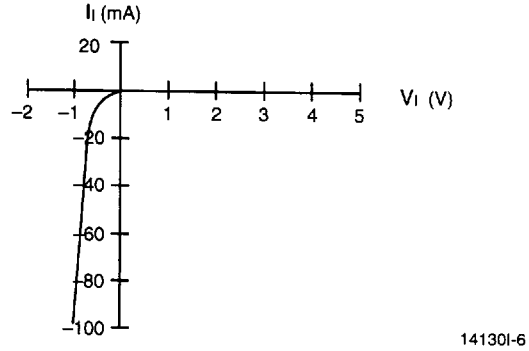
V_{CC} = 5.0 V, T_A = 25°C



Output, LOW



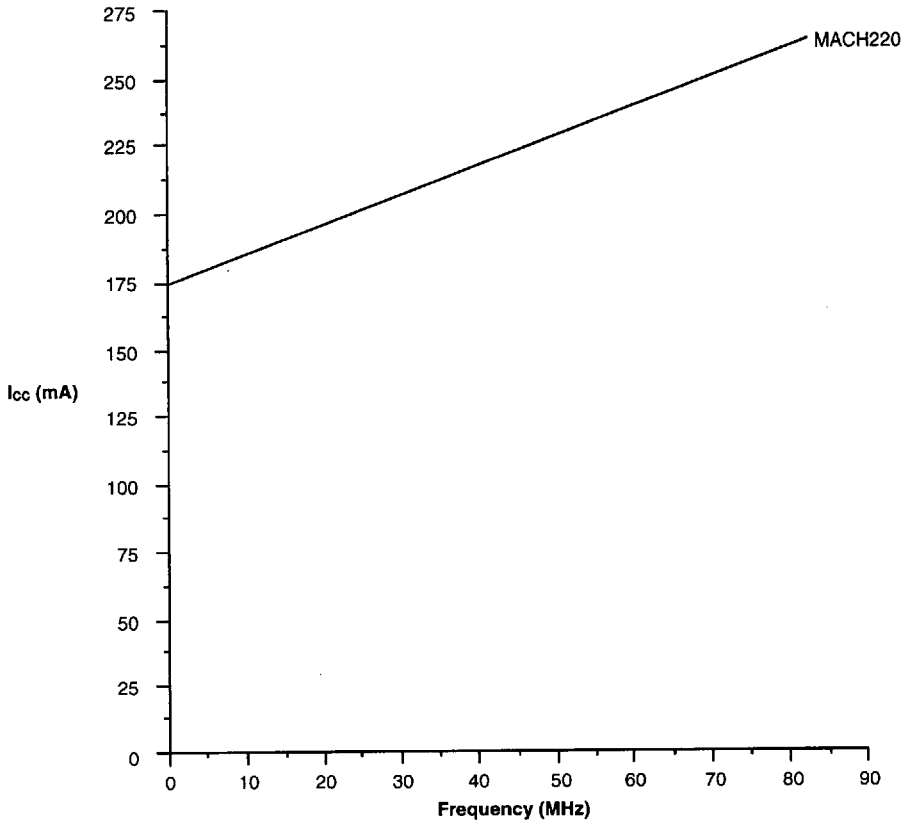
Output, HIGH



Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



14130I-7

The selected "typical" pattern is a 12-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		10	°C/W
θ_{ja}	Thermal impedance, junction to ambient		33	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	29	°C/W
		400 lfpm air	27	°C/W
		600 lfpm air	24	°C/W
		800 lfpm air	23	°C/W

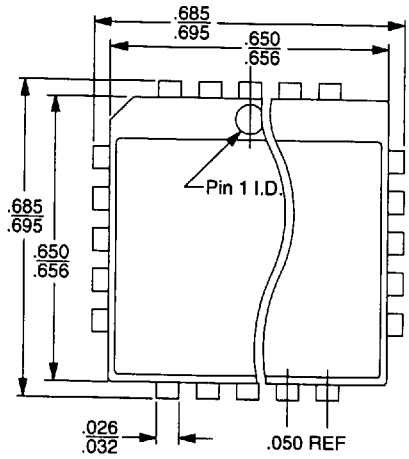
Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

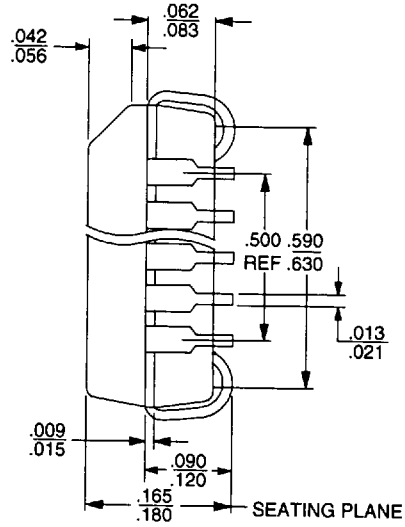
PHYSICAL DIMENSIONS*

PL 044

44-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW

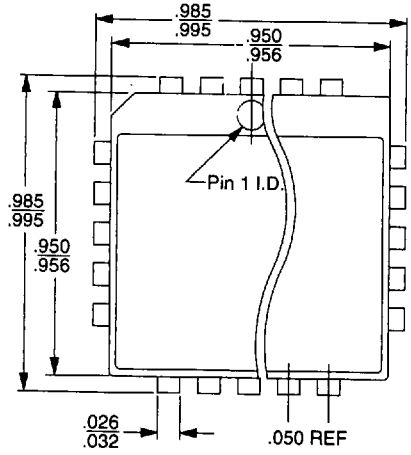


SIDE VIEW

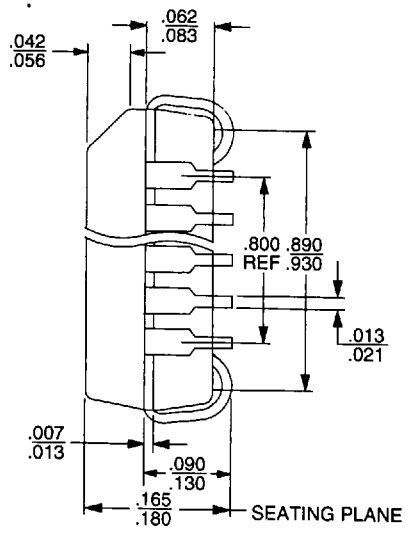
16-038-SQ
PL 044
DA78
6-28-94 ae

PL 068

68-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW

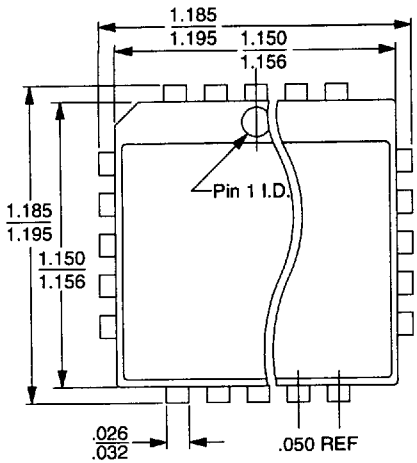


SIDE VIEW

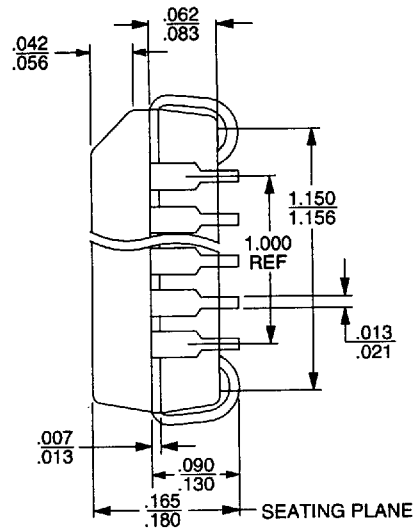
16-038-SQ
PL 068
DA78
6-28-94 ae

For reference only. BSC is an ANSI standard for Basic Space Centering.

PL 084
84-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW



SIDE VIEW

16-038-SQ
PL 068
DA78
6-28-94 ae

For reference only. BSC is an ANSI standard for Basic Space Centering.

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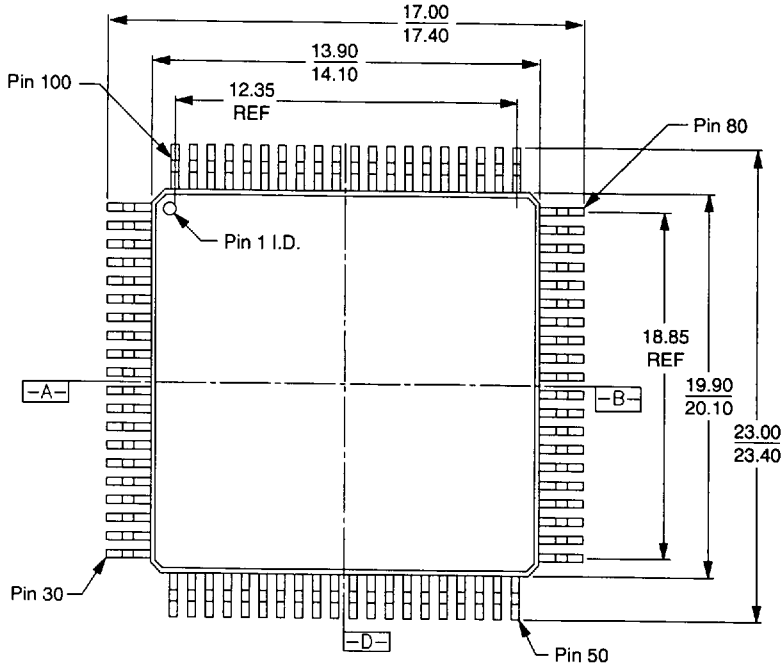
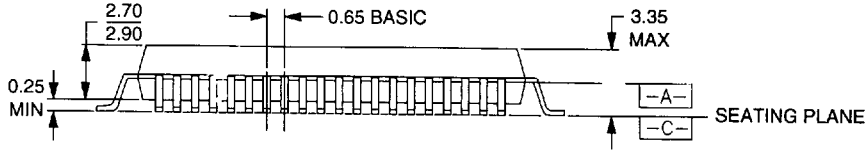
PHYSICAL DIMENSIONS*

PQR100

100-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)





16-038-PQR-2
PQR100
DA92
8-2-94 ae

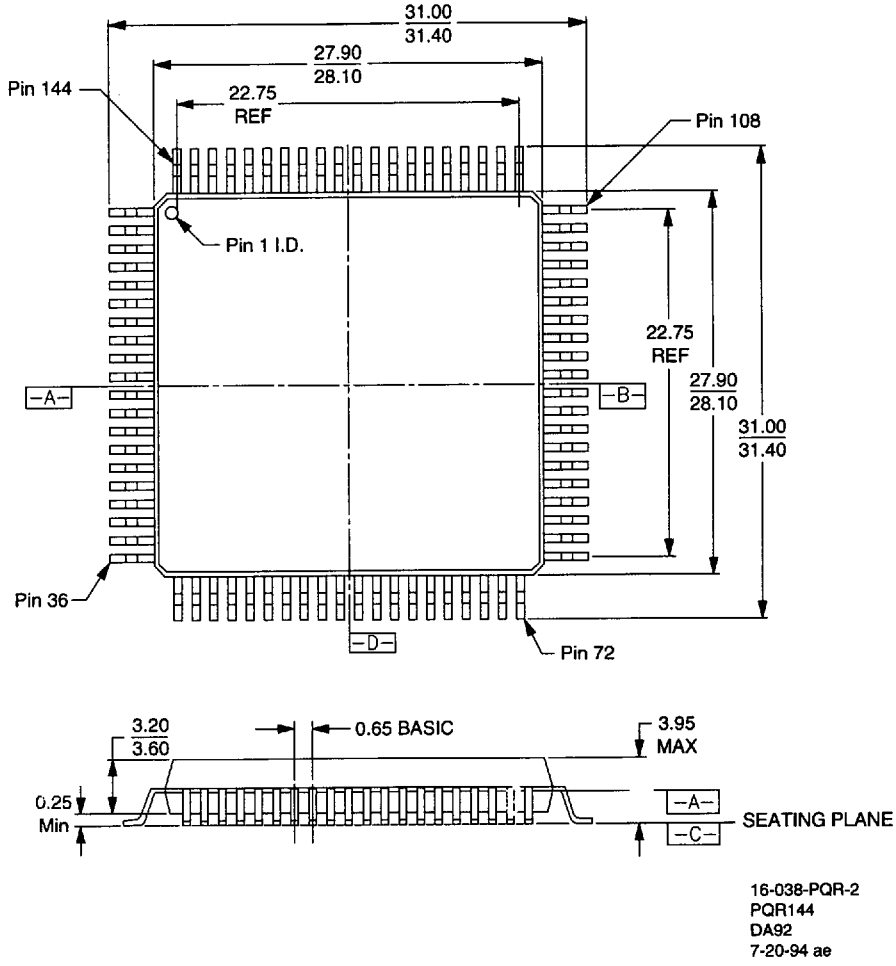
Note:
Although the PQR100 package is drawn as a square package, the actual package is rectangular as the dimensions suggest.

**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*

PQR144

144-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

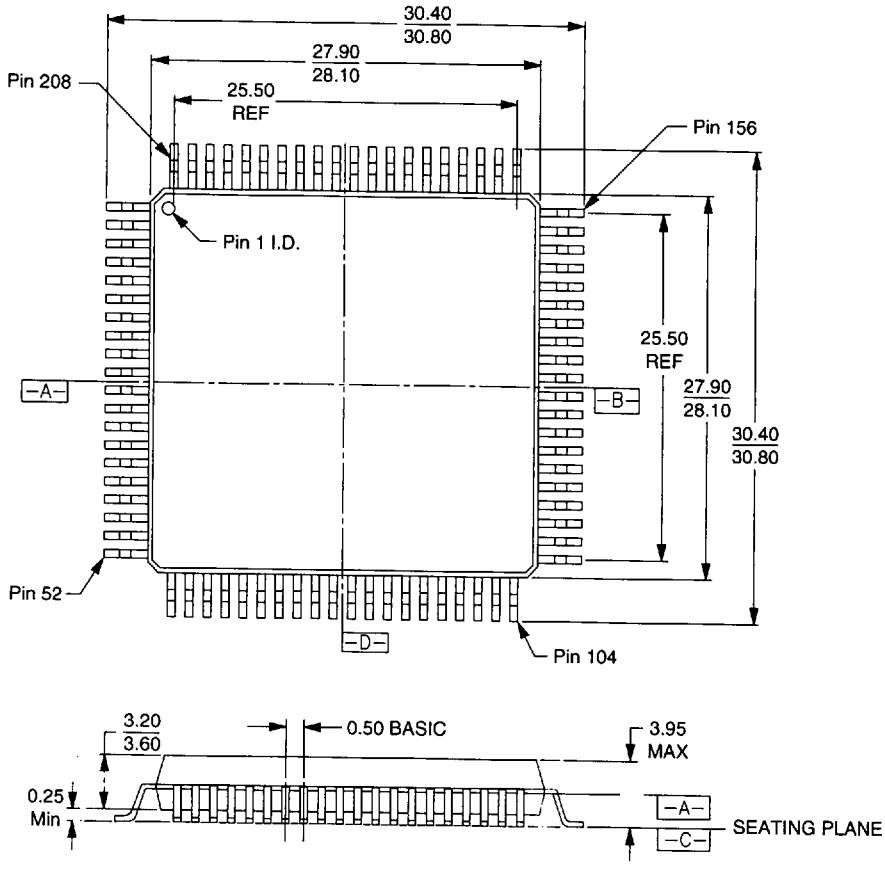


For reference only. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS*

PQR208

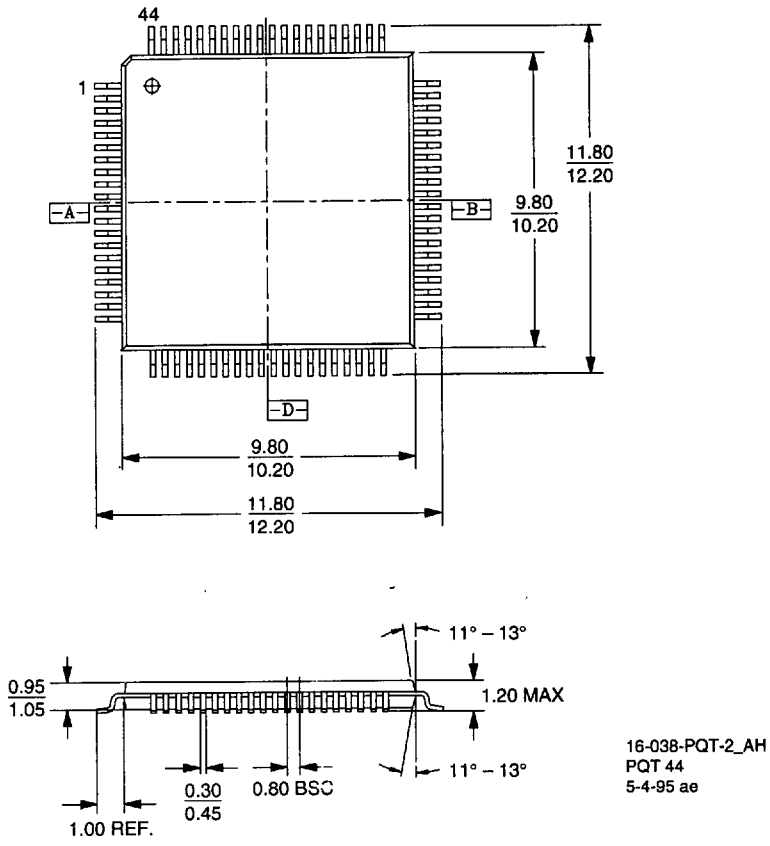
208-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)



*For reference only. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS*

PQT044
44-Pin Thin Quad Flat Pack (measured in millimeters)



For reference only. BSC is an ANSI standard for Basic Space Centering.