

# Military ProASIC3/EL Low Power Flash FPGAs with Flash\*Freeze Technology



## Features and Benefits

### Military Temperature Tested and Qualified

- Each Device Tested from –55°C to 125°C

### Firm-Error Immune

- Not Susceptible to Neutron-Induced Configuration Loss

### Low Power

- Dramatic Reduction in Dynamic and Static Power
- 1.2 V to 1.5 V Core and I/O Voltage Support for Low Power<sup>†</sup>
- Low Power Consumption in Flash\*Freeze Mode Allows for Instantaneous Entry To / Exit From Low-Power Flash\*Freeze Mode<sup>f</sup>
- Supports Single-Voltage System Operation
- Low-Impedance Switches

### High Capacity

- 600 k to 3 M System Gates
- Up to 504 kbits of True Dual-Port SRAM
- Up to 620 User I/Os

### Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

### High Performance

- 350 MHz (1.5 V systems) and 250 MHz (1.2 V systems) System Performance
- 3.3 V, 66 MHz, 66-Bit PCI (1.5 V systems) and 66 MHz, 32-Bit PCI (1.2 V systems)

### In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532–compliant)
- FlashLock<sup>®</sup> to Secure FPGA Contents

### High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network

- Architecture Supports Ultra-High Utilization

### Advanced and Pro (Professional) I/Os<sup>††</sup>

- 700 Mbps DDR, LVDS-Capable I/Os
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation<sup>†</sup>
- Bank-Selectable I/O Voltages—up to 8 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input<sup>†</sup>
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS
- Voltage-Referenced I/O Standards: GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II (A3PE3000L only)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Programmable Input Delay (A3PE3000L only)
- Schmitt Trigger Option on Single-Ended Inputs (A3PE3000L)
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the Military ProASIC<sup>®</sup>3EL Family

### Clock Conditioning Circuit (CCC) and PLL

- Six CCC Blocks, One with Integrated PLL (ProASIC3) and All with Integrated PLL (ProASIC3EL)
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range 1.5 MHz to 250 MHz (1.2 V systems) and 350 MHz (1.5 V systems)

### SRAMs and FIFOs

- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (x1, x2, x4, x9, and x18 organizations available)
- True Dual-Port SRAM (except x18)
- 24 SRAM and FIFO Configurations with Synchronous Operation:
  - 250 MHz: For 1.2 V Systems
  - 350 MHz: For 1.5 V Systems

### ARM<sup>®</sup> Processor Support in ProASIC3/EL FPGAs

- ARM Cortex<sup>™</sup>-M1 Soft Processor Available with or without Debug

Table I-1 • Military ProASIC3/EL Low-Power Devices

ProASIC3/EL Devices	A3PE600L	A3P1000	A3PE3000L
ARM Cortex-M1 Devices <sup>1</sup>		M1A3P1000	M1A3PE3000L
System Gates	600 k	1 M	3 M
VersaTiles (D-flip-flops)	13,824	24,576	75,264
RAM kbits (1,024 bits)	108	144	504
4,608-Bit Blocks	24	32	112
FlashROM Bits	1 k	1 k	1 k
Secure (AES) ISP2	Yes	Yes	Yes
Integrated PLL in CCCs	6	1	6
VersaNet Globals	18	18	18
I/O Banks	8	4	8
Maximum User I/Os	270	154	620
Package Pins PQFP FBGA	FG484	PQ208 FG144	FG484, FG896

**Notes:**

1. Refer to the Cortex-M1 product brief for more information.
2. AES is not available for ARM-enabled ProASIC3/EL devices.

<sup>†</sup> A3P1000 only supports 1.5 V core operation.

<sup>f</sup> Flash\*Freeze technology is not available for A3P1000.

<sup>††</sup>Pro I/Os are not available on A3P1000.

## I/Os Per Package <sup>1</sup>

ProASIC3/EL Low Power Devices	A3PE600L		A3P1000		A3PE3000L	
ARM Cortex-M1 Devices			M1A3P1000		M1A3PE3000L	
Package	Single- Ended I/O <sup>2</sup>	Differential I/O Pairs	Single- Ended I/O <sup>2</sup>	Differential I/O Pairs	Single- Ended I/O <sup>2</sup>	Differential I/O Pairs
PQ208	–	–	154	35	–	–
FG144	–	–	97	25	–	–
FG484	270	135	–	–	341	168
FG896	–	–	–	–	620	300

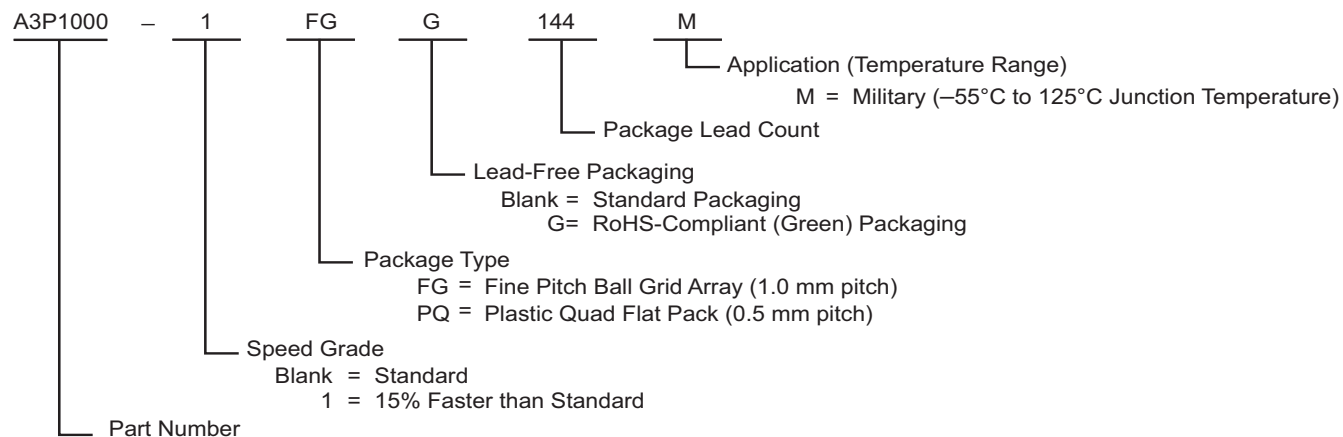
### Notes:

1. When considering migrating your design to a lower- or higher-density device, refer to the packaging section of the datasheet to ensure you are complying with design and board migration requirements.
2. Each used differential I/O pair reduces the number of single-ended I/Os available by two.
3. "G" indicates RoHS-compliant packages. Refer to "Military ProASIC3/EL Ordering Information" on page III for the location of the "G" in the part number.
4. For A3PE3000L devices, the usage of certain I/O standards is limited as follows:
  - SSTL3(I) and (II): up to 40 I/Os per north or south bank
  - LVPECL / GTL+ 3.3 V / GTL 3.3 V: up to 48 I/Os per north or south bank
  - SSTL2(I) and (II) / GTL+ 2.5 V / GTL 2.5 V: up to 72 I/Os per north or south bank
5. When the Flash\*Freeze pin is used to directly enable Flash\*Freeze mode and not as a regular I/O, the number of single-ended user I/Os available is reduced by one.

## Military ProASIC3/EL Device Status

Military ProASIC3/EL Devices	Status	M1 Military ProASIC3/EL Devices	Status
A3PE600L	Production		
A3P1000	Production	M1A3P1000	Production
A3PE3000L	Production	M1A3PE3000L	Production

## Military ProASIC3/EL Ordering Information



### Military ProASIC3/EL Devices

- A3PE600L = 600,000 System Gates
- A3P1000 = 1,000,000 System Gates
- A3PE3000L = 3,000,000 System Gates

### Military ProASIC3/EL Devices with ARM Cortex-M1

- M1A3P1000 = 1,000,000 System Gates
- M1A3PE3000L = 3,000,000 System Gates

## Temperature Grade Offerings

Package	A3PE600L	A3P1000	A3PE3000L
<b>ARM Cortex-M1 Devices</b>		<b>M1A3P1000</b>	<b>M1A3PE3000L</b>
PQ208	–	M	–
FG144	–	M	–
FG484	M	–	M
FG896	–	–	M

*Note:* M = Military temperature range: –55°C to 125°C junction temperature

## Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
M	✓	✓

*Note:* M = Military temperature range: –55°C to 125°C junction temperature

Contact your local Actel representative for device availability: <http://www.actel.com/contact/default.aspx>.

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# 1 – Military ProASIC3/EL Device Family Overview

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## General Description

The military ProASIC3/EL family of Actel flash FPGAs dramatically reduces dynamic power consumption by 40% and static power by 50%. These power savings are coupled with performance, density, true single chip, 1.2 V to 1.5 V core and I/O operation, reprogrammability, and advanced features.

Actel's proven Flash\*Freeze technology enables military ProASIC3EL device users to shut off dynamic power instantaneously and switch the device to static mode without the need to switch off clocks or power supplies, and retaining internal states of the device. This greatly simplifies power management. In addition, optimized software tools using power-driven layout provide instant push-button power reduction.

Nonvolatile flash technology gives military ProASIC3/EL devices the advantage of being a secure, low-power, single-chip solution that is live at power-up (LAPU). Military ProASIC3/EL devices offer dramatic dynamic power savings, giving FPGA users flexibility to combine low power with high performance.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Military ProASIC3/EL devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry (CCC) based on an integrated phase-locked loop (PLL). Military ProASIC3/EL devices support devices from 600 k system gates to 3 million system gates with up to 504 kbits of true dual-port SRAM and 620 user I/Os.

M1 military ProASIC3/EL devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. ARM Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low-power consumption and speed when implemented in an M1 military ProASIC3/EL device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. ARM Cortex-M1 is available at no cost from Actel for use in M1 military ProASIC3/ELFPGAs.

The ARM-enabled devices have Actel ordering numbers that begin with M1 and do not support AES decryption.

## Flash\*Freeze Technology<sup>†</sup>

Military ProASIC3EL devices offer Actel's proven Flash\*Freeze technology, which allows instantaneous switching from an active state to a static state. When Flash\*Freeze mode is activated, military ProASIC3EL devices enter a static state while retaining the contents of registers and SRAM. Power is conserved without the need for additional external components to turn off I/Os or clocks. Flash\*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of military ProASIC3EL devices to support a 1.2 V core voltage allows for an even greater reduction in power consumption, which enables low total system power.

When the military ProASIC3EL device enters Flash\*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash\*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with a reprogrammable, single-chip, single-voltage solution, make military ProASIC3EL devices suitable for low-power data transfer and manipulation in military-temperature applications where available power may be limited (e.g., in battery-powered equipment); or where heat dissipation may be limited (e.g., in enclosures with no forced cooling).

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<sup>†</sup> Flash\*Freeze technology is not supported on A3P1000.

## Flash Advantages

### **Low Power<sup>f</sup>**

The military ProASIC3EL family of Actel flash-based FPGAs provides a low-power advantage, and when coupled with high performance, enables designers to make power-smart choices using a single-chip, reprogrammable, and live-at-power-up device.

Military ProASIC3EL devices offer 40% dynamic power and 50% static power savings by reducing the core operating voltage to 1.2 V. In addition, the power-driven layout (PDL) feature in Libero® Integrated Design Environment (IDE) offers up to 30% additional power reduction. With Flash\*Freeze technology, military ProASIC3EL device is able to retain device SRAM and logic while dynamic power is reduced to a minimum, without the need to stop clock or power supplies. Combining these features provides a low-power, feature-rich, and high-performance solution.

### **Security**

Nonvolatile, flash-based military ProASIC3/EL devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. Military ProASIC3/EL devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Military ProASIC3/EL devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in military ProASIC3/EL devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. Military ProASIC3/EL devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. Military ProASIC3/EL devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the military ProASIC3/EL family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The military ProASIC3/EL family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. A military ProASIC3/EL device provides the most impenetrable security for programmable logic designs.

### **Single Chip**

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based military ProASIC3/EL FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

### **Live at Power-Up**

Actel flash-based military ProASIC3/EL devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based military ProASIC3/EL devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the military ProASIC3/EL device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based military ProASIC3/EL devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

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<sup>f</sup> A3P1000 only supports 1.5 V core operation.



## **Reduced Cost of Ownership**

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based military ProASIC3/EL devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The military ProASIC3/EL family device architecture mitigates the need for ASIC migration at higher volumes. This makes the military ProASIC3/EL family a cost-effective ASIC replacement.

## **Firm-Error Immunity**

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of military ProASIC3/EL flash-based FPGAs. Once it is programmed, the flash cell configuration element of military ProASIC3/EL FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

## **Advanced Flash Technology**

The military ProASIC3/EL family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with 7 layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

## **Advanced Architecture**

The proprietary military ProASIC3/EL architecture provides granularity comparable to standard-cell ASICs. The military ProASIC3/EL device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory
- Extensive CCCs and PLLs
- I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the military ProASIC3/EL core tile, as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable, allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of military ProASIC3/EL devices via an IEEE 1532 JTAG interface.

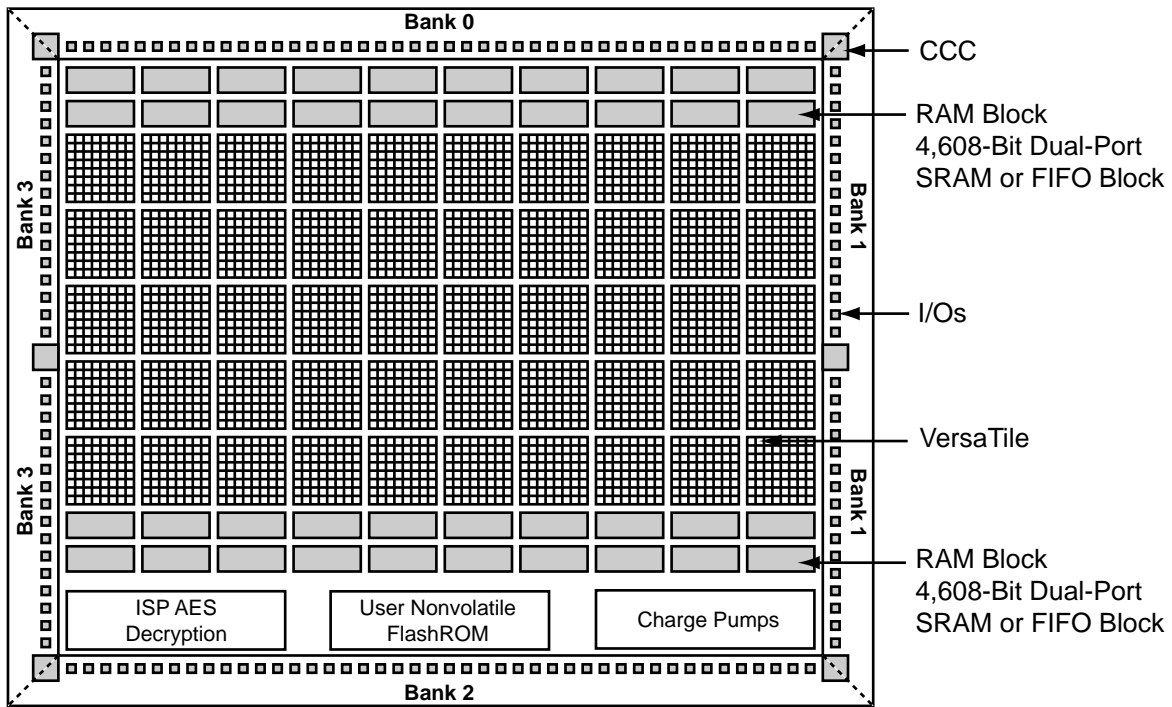


Figure 1-1 • Military ProASIC3 Device Architecture Overview with Four I/O Banks (A3P1000)

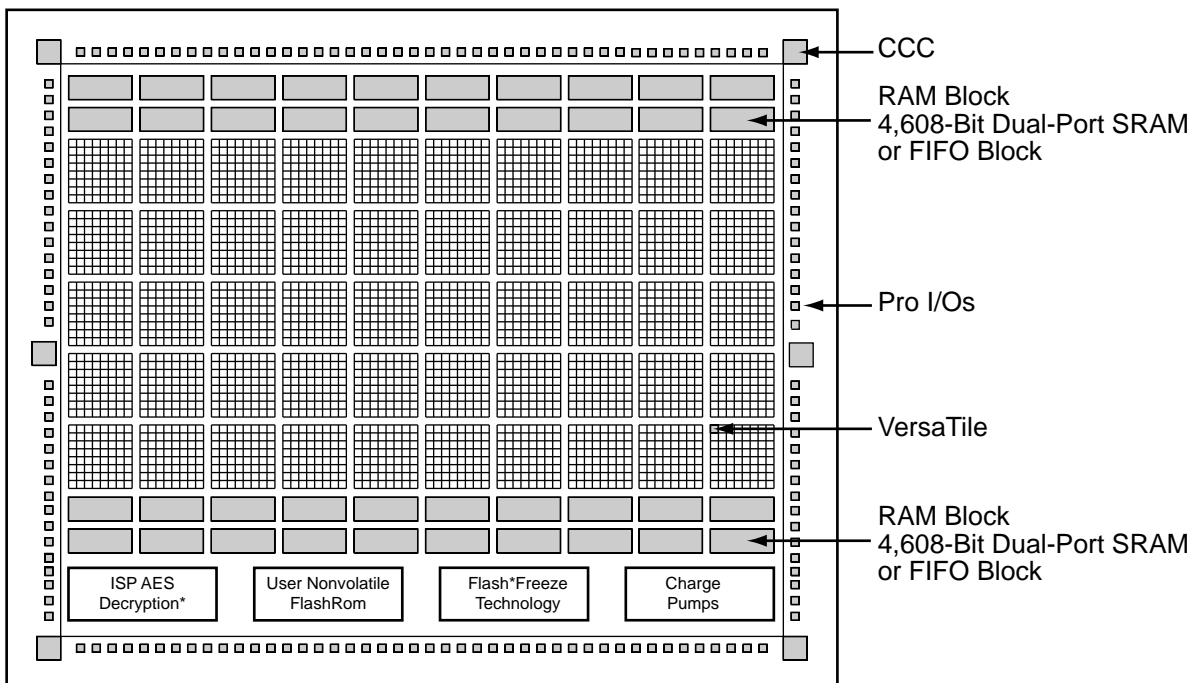
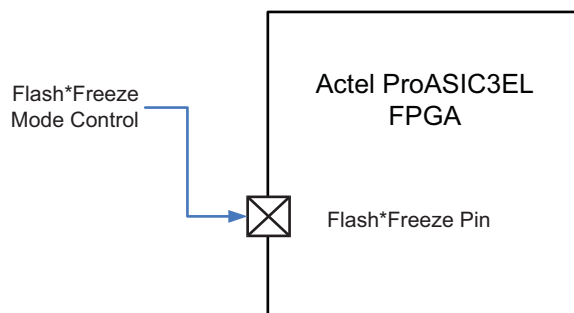


Figure 1-2 • Military ProASIC3EL Device Architecture Overview (A3PE600L and A3PE3000L)

## Flash\*Freeze Technology<sup>††</sup>

Military ProASIC3EL devices offer Actel's proven Flash\*Freeze technology, which enables designers to instantaneously shut off dynamic power consumption while retaining all SRAM and register information. Flash\*Freeze technology enables the user to quickly (within 1  $\mu$ s) enter and exit Flash\*Freeze mode by activating the Flash\*Freeze (FF) pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption; clocks can still be driven or can be toggling without impact on power consumption; all core registers and SRAM cells retain their states. I/Os are tristated during Flash\*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLLs. Flash\*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The FF pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the FF pin as a regular I/O if Flash\*Freeze mode usage is not planned, which is advantageous because of the inherent low-power static and dynamic capabilities of the military ProASIC3EL device. Refer to [Figure 1-3](#) for an illustration of entering/exiting Flash\*Freeze mode.



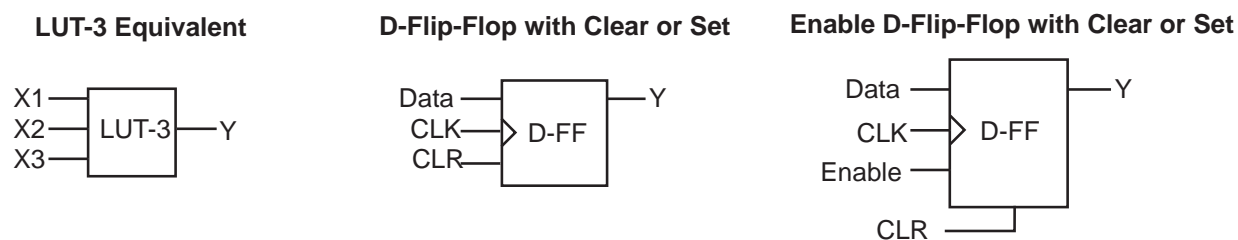
**Figure 1-3 • Military ProASIC3EL Flash\*Freeze Mode**

### VersaTiles

The military ProASIC3/EL core consists of VersaTiles, which have been enhanced beyond the ProASIC<sup>PLUS</sup>® core tiles. The military ProASIC3/EL VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-4](#) for VersaTile configurations.



**Figure 1-4 • VersaTile Configurations**

<sup>††</sup>Flash\*Freeze technology is not supported for A3P1000.

## **User Nonvolatile FlashROM**

Actel military ProASIC3/EL devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

FlashROM is written using the standard military ProASIC3/EL IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks, as in security keys stored in the FlashROM for a user design.

FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel military ProASIC3/EL development software solutions, Libero IDE and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## **SRAM and FIFO**

Military ProASIC3/EL devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256x18, 512x9, 1kx4, 2kx2, and 4kx1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## **PLL and CCC**

Military ProASIC3 devices provide designers with flexible clock conditioning circuit (CCC) capabilities. Each member of the military ProASIC3 family contains six CCCs, located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL. All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

Military ProASIC3EL devices also contain six CCCs; however, all six are equipped with a PLL.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range ( $f_{IN\_CCC}$ ) = 1.5 MHz up to 250 MHz
- Output frequency range ( $f_{OUT\_CCC}$ ) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration.
- Output duty cycle = 50% ± 1.5% or better
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used
- Maximum acquisition time is 300 μs
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns
- Four precise phases; maximum misalignment between adjacent phases of  $40 \text{ ps} \times 250 \text{ MHz} / f_{OUT\_CCC}$

### **Global Clocking**

Military ProASIC3/EL devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

### **I/Os with Advanced I/O Standards**

The military ProASIC3/EL family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). In addition, 1.2 V I/O operation is supported for military ProASIC3EL devices. Military ProASIC3/EL FPGAs support different I/O standards, including single-ended, differential, and voltage-referenced (military ProASIC3EL). The I/Os are organized into banks, with two, four, or eight (military ProASIC3EL only) banks per device. The configuration of these banks determines the I/O standards supported. For military ProASIC3EL, each I/O bank is subdivided into  $V_{REF}$  minibanks, which are used by voltage-referenced I/Os.  $V_{REF}$  minibanks contain 8 to 18 I/Os. All the I/Os in a given minibank share a common  $V_{REF}$  line. Therefore, if any I/O in a given  $V_{REF}$  minibank is configured as a  $V_{REF}$  pin, the remaining I/Os in that minibank will be able to use that reference voltage.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-data-rate applications (e.g., PCI 66 MHz, bidirectional SSTL 2 and 3, Class I and II)
- Double-data-Rate applications (e.g., DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications, and DDR 200 MHz SRAM using bidirectional HSTL Class II).

Military ProASIC3EL banks support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.



## 2 – Military ProASIC3/EL DC and Switching Characteristics

### General Specifications

#### Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2](#) on [page 2-2](#) is not implied.

**Table 2-1 • Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage for A3PE600L and A3PE3000L. DC Output buffer supply voltage for A3P1000.	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VMV	DC input buffer supply voltage for A3P1000	–0.3 to 3.75	V
T <sub>STG</sub> <sup>2</sup>	Storage temperature	–65 to +150	°C
T <sub>J</sub> <sup>2</sup>	Junction temperature	+150	°C

**Notes:**

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4](#) on [page 2-7](#).
2. For flash programming and retention maximum limits, refer to [Table 2-3](#) on [page 2-3](#), and for recommended operating limits, refer to [Table 2-2](#) on [page 2-2](#).

**Table 2-2 • Recommended Operating Conditions<sup>2</sup>**

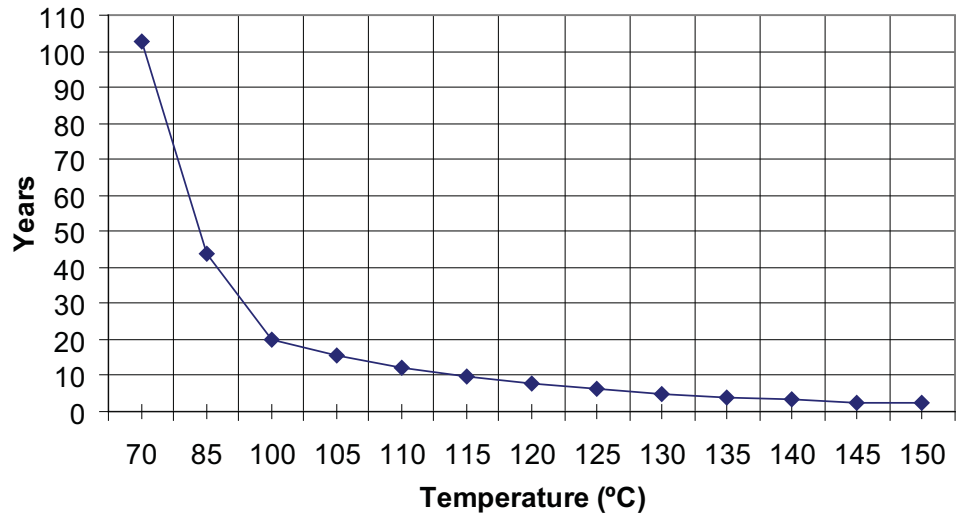
Symbol	Parameter		Military	Units
T <sub>A</sub>	Ambient temperature		-55 to 125	°C
T <sub>J</sub>	Junction temperature		-55 to 125	°C
VCC	DC core supply voltage for A3PE600L/A3PE3000L		1.14 to 1.575	V
	DC core supply voltage for A3P1000 <sup>1</sup>		1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	V
VPUMP <sup>3</sup>	Programming voltage	Programming mode	3.15 to 3.45	V
		Operation <sup>3</sup>	0 to 3.6	V
VCCPLL	Analog power supply (PLL) for A3PE600L/A3PE3000L	DC core supply voltage	1.14 to 1.575	V
	Analog power supply (PLL) for A3P1000	DC core supply voltage	1.425 to 1.575	
VCCI and VMV	1.2 V DC supply voltage <sup>4</sup>		1.14 to 1.26	V
	1.5 V DC supply voltage		1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	V

**Notes:**

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in [Table 2-23 on page 2-24](#). VMV and V<sub>CCL</sub> should be at the same voltage within a given I/O bank.
2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
3. V<sub>PUMP</sub> can be left floating during normal operation (not programming mode).
4. For A3PE600L and A3PE3000L devices only.



T <sub>J</sub> (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2



*Note:* HTR time is the period during which you would not expect a verify failure due to flash cell leakage.

**Figure 2-1 • High-Temperature Data Retention (HTR)**

**Table 2-3 • Overshoot and Undershoot Limits**

V <sub>CCI</sub> and VMV	Average V <sub>CCI</sub> -GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle	Maximum Overshoot/Undershoot (125°C)
2.7 V or less	10%	0.72 V
	5%	0.82 V
3 V	10%	0.72 V
	5%	0.81 V
3.3 V	10%	0.69 V
	5%	0.79 V
3.6 V	10%	N/A
	5%	N/A

**Notes:**

1. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
2. This table does not provide PCI overshoot/undershoot limits.

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Military)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-2 on page 2-5](#) and [Figure 2-3 on page 2-6](#).

There are five regions to consider during power-up.

Military ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-2 on page 2-5](#) and [Figure 2-3 on page 2-6](#)).
2.  $VCCI > VCC - 0.75 \text{ V}$  (typical)
3. Chip is in the operating mode.

### VCCI Trip Point:

Ramping up:  $0.6 \text{ V} < \text{trip\_point\_up} < 1.2 \text{ V}$

Ramping down:  $0.5 \text{ V} < \text{trip\_point\_down} < 1.1 \text{ V}$

### VCC Trip Point:

Ramping up:  $0.6 \text{ V} < \text{trip\_point\_up} < 1.1 \text{ V}$

Ramping down:  $0.5 \text{ V} < \text{trip\_point\_down} < 1 \text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

### PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic, at least until VCC and VCCPLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-2 and Figure 2-3 on page 2-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ( $0.75\text{ V} \pm 0.25\text{ V}$ ), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/Down Behavior of Low-Power Flash Devices" chapter of the *Military ProASIC3/EL FPGA Fabric User's Guide* for information on clock and lock recovery.

### Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

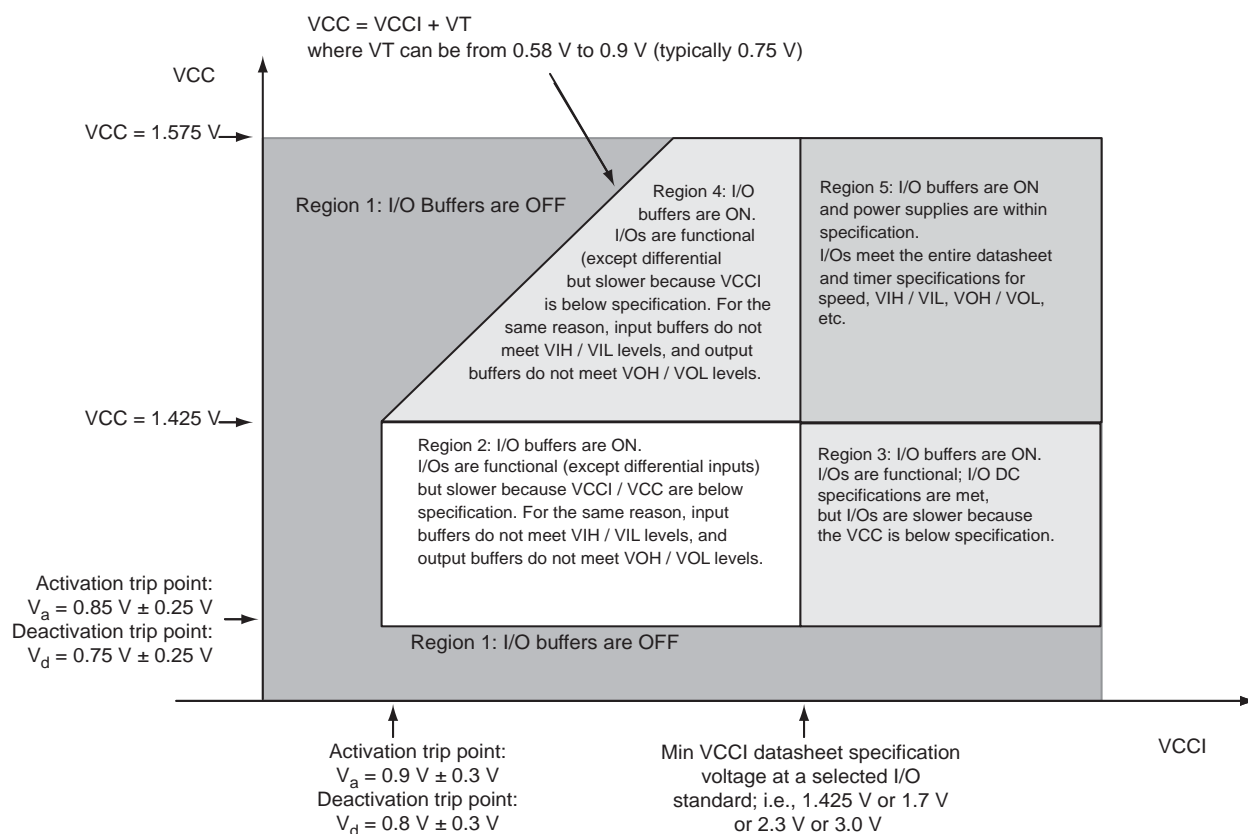
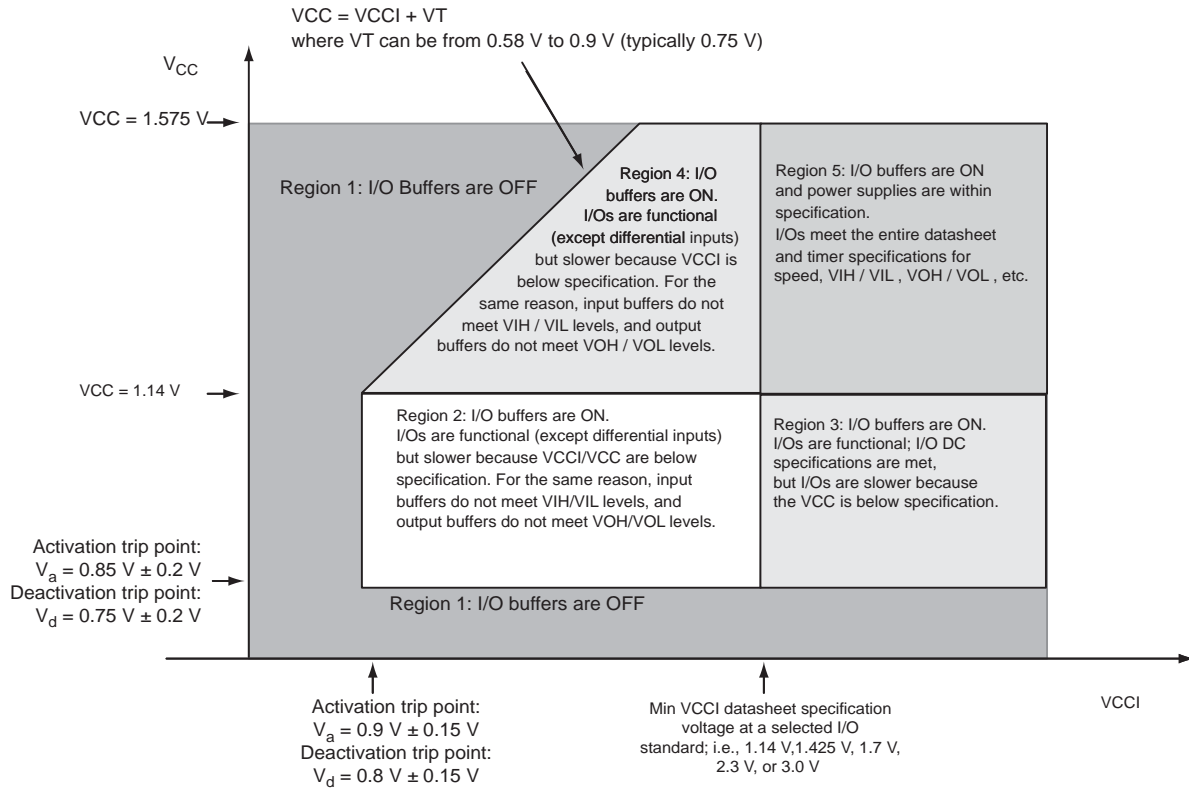


Figure 2-2 • Devices Operating at 1.5 V Core – I/O State as a Function of VCCI and VCC Voltage Levels



**Figure 2-3 • Device Operating at 1.2 V Core Voltage – I/O State as a Function of  $V_{CCI}$  and  $V_{CC}$  Voltage Levels; Only A3PE600L and A3PE3000L Devices Operate at 1.2 V Core Voltage**

## Thermal Characteristics

### Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction temperature to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

$T_A$  = Ambient Temperature

$\Delta T$  = Temperature gradient between junction (silicon) and ambient  $\Delta T = \theta_{ja} * P$

$\theta_{ja}$  = Junction-to-ambient of the package.  $\theta_{ja}$  numbers are located in [Table 2-4](#).

P = Power dissipation

### Package Thermal Characteristics

The device junction-to-case thermal resistivity is  $\theta_{jc}$  and the junction-to-ambient air thermal resistivity is  $\theta_{ja}$ . The thermal characteristics for  $\theta_{ja}$  are shown for two air flow rates. The recommended maximum junction temperature is 125°C. EQ 2 shows a sample calculation of the recommended maximum power dissipation allowed for a 484-pin FBGA package at military temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (\text{}^\circ\text{C/W)}} = \frac{125^\circ\text{C} - 70^\circ\text{C}}{20.6^\circ\text{C/W}} = 2.670$$

EQ 2

**Table 2-4 • Package Thermal Resistivities**

Package Type	Device	Pin Count	$\theta_{jc}$	$\theta_{ja}$			Units
				Still Air	200 ft./min.	500 ft./min.	
Plastic Quad Flat Pack (PQ208)*	A3P1000	208	3.8	16.2	13.3	11.9	C/W
Fine Pitch Ball Grid Array (FBGA)	A3P1000	144	6.3	31.6	26.2	24.2	C/W
	A3PE600L	484	9.5	27.5	21.9	20.2	C/W
	A3PE3000L	484	4.7	20.6	15.7	14.0	C/W
	A3PE3000L	896	2.4	13.6	10.4	9.4	C/W

\* Embedded heatspreader

### Temperature and Voltage Derating Factors

**Table 2-5 • Temperature and Voltage Derating Factors for Timing Delays**  
 (normalized to  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$ )  
 Applicable to A3PE600L and A3PE3000L Only

Array Voltage $V_{CC}$ (V)	Junction Temperature						
	$-55^\circ\text{C}$	$-40^\circ\text{C}$	$0^\circ\text{C}$	$25^\circ\text{C}$	$70^\circ\text{C}$	$85^\circ\text{C}$	$125^\circ\text{C}$
1.14	0.86	0.87	0.90	0.92	0.96	0.98	1.00
1.2	0.83	0.84	0.87	0.89	0.93	0.94	0.96
1.26	0.79	0.80	0.83	0.85	0.89	0.90	0.92
1.3	0.77	0.78	0.81	0.83	0.86	0.88	0.90
1.35	0.75	0.75	0.78	0.80	0.83	0.85	0.87
1.4	0.72	0.73	0.75	0.77	0.80	0.81	0.83
1.425	0.70	0.71	0.74	0.76	0.79	0.80	0.82
1.5	0.67	0.67	0.70	0.71	0.75	0.76	0.78
1.575	0.64	0.65	0.67	0.69	0.72	0.73	0.75

**Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays**  
 (normalized to  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ )  
 Applicable to A3P1000 Devices Only

Array Voltage $V_{CC}$ (V)	Junction Temperature						
	$-55^\circ\text{C}$	$-40^\circ\text{C}$	$0^\circ\text{C}$	$25^\circ\text{C}$	$70^\circ\text{C}$	$85^\circ\text{C}$	$125^\circ\text{C}$
1.425	0.81	0.83	0.88	0.90	0.95	0.97	1.00
1.5	0.77	0.79	0.83	0.85	0.90	0.92	0.95
1.575	0.74	0.76	0.80	0.82	0.87	0.88	0.92

## Calculating Power Dissipation

### Quiescent Supply Current

**Table 2-7 • Quiescent Supply Current ( $I_{DD}$ ) Characteristics When Using Flash\*Freeze Mode in Military ProASIC3/EL\***

	Core Voltage	A3PE600L	A3PE3000L	Units
Typical (25°C)	1.2 V		2.75	mA
	1.5 V			mA

\*  $I_{DD}$  includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents. Values do not include I/O static contribution ( $P_{DC6}$  and  $P_{DC7}$ ).

**Table 2-8 • Quiescent Supply Current ( $I_{DD}$ ) Characteristics, Military ProASIC3/EL Sleep Mode (VCC = 0 V)\***

	Core Voltage	A3PE600L	A3PE3000L	Units
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.7	1.7	$\mu$ A
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	$\mu$ A
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	$\mu$ A
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	$\mu$ A
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	$\mu$ A

\*  $I_{DD}$  includes VCC, VPUMP, and VCCPLL currents. Values do not include I/O static contribution ( $P_{DC6}$  and  $P_{DC7}$ ).

**Table 2-9 • Quiescent Supply Current ( $I_{DD}$ ) Characteristics for A3PE600L and A3PE3000L Devices Only Shutdown Mode, (VCC and VCCI = 0 V)\***

	Core Voltage	A3PE600L	A3PE3000L
Typical (25°C)	1.2 V		0 $\mu$ A

\*  $I_{DD}$  includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents. Values do not include I/O static contribution ( $P_{DC6}$  and  $P_{DC7}$ ).

**Table 2-10 • Quiescent Supply Current ( $I_{DD}$ ), No Military ProASIC3/EL Flash\*Freeze Mode <sup>1</sup>**

	Core Voltage	A3PE600L	A3PE3000L	Units
<b><math>I_{CCA}</math> Current<sup>2</sup></b>				
Typical (25°C)	1.2 V		2.75	mA
	1.5 V			mA
<b><math>I_{CCI}</math> or <math>I_{JTAG}</math> Current<sup>3, 4</sup></b>				
VCCI / VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.7	1.7	μA
VCCI / VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	μA
VCCI / VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	μA
VCCI / VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	μA
VCCI / VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	μA

**Notes:**

1. To calculate total device  $I_{DD}$ , multiply the number of banks used by  $I_{CCI}$  and add  $I_{CCA}$  contribution.
2. Includes VCC, VCCPLL, and VPUMP currents.
3. Per VCCI or VJTAG bank.
4. Values do not include I/O static contribution ( $P_{DC6}$  and  $P_{DC7}$ ).

**Table 2-11 • Quiescent Supply Current ( $I_{DD}$ ) Characteristics**

	A3P1000
Typical (25°C)	8 mA
Maximum Military (125°C)	200 mA

\*  $I_{DD}$  includes VCC, VPUMP, VCCI, VJTAG, and VCCPLL currents. Values do not include I/O static contribution ( $P_{DC6}$  and  $P_{DC7}$ ).



## Power per I/O Pin

**Table 2-12 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings**  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	VCCI (V)	Static Power P <sub>DC6</sub> (mW) <sup>1</sup>	Dynamic Power P <sub>AC9</sub> (μW/MHz) <sup>2</sup>
<b>Single-Ended</b>			
3.3 V LVTTTL/LVCMOS	3.3	–	16.34
3.3 V LVTTTL/LVCMOS – Schmitt trigger	3.3	–	24.49
2.5 V LVCMOS	2.5	–	4.71
2.5 V LVCMOS – Schmitt trigger	2.5	–	6.13
1.8 V LVCMOS	1.8	–	1.66
1.8 V LVCMOS – Schmitt trigger	1.8	–	1.78
1.5 V LVCMOS (JESD8-11)	1.5	–	1.01
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	0.97
1.2 V LVCMOS <sup>3</sup>	1.2	–	0.60
1.2 V LVCMOS (JESD8-11) – Schmitt trigger <sup>3</sup>	1.2	–	0.53
3.3 V PCI	3.3	–	17.76
3.3 V PCI – Schmitt trigger	3.3	–	19.10
3.3 V PCI-X	3.3	–	17.76
3.3 V PCI-X – Schmitt trigger	3.3	–	19.10
<b>Voltage-Referenced</b>			
3.3 V GTL	3.3	2.90	7.07
2.5 V GTL	2.5	2.13	3.62
3.3 V GTL+	3.3	2.81	2.97
2.5 V GTL+	2.5	2.57	2.55
HSTL (I)	1.5	0.17	0.85
HSTL (II)	1.5	0.17	0.85
SSTL2 (I)	2.5	1.38	3.30
SSTL2 (II)	2.5	1.38	3.30
SSTL3 (I)	3.3	3.21	8.08
SSTL3 (II)	3.3	3.21	8.08
<b>Differential</b>			
LVDS	2.5	2.26	0.95
LVPECL	3.3	5.71	1.62

**Notes:**

1. P<sub>DC6</sub> is the static power (where applicable) measured on VCCI.
2. P<sub>AC9</sub> is the total dynamic power measured on VCCI.

**Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings <sup>1</sup>**  
**Applicable to Advanced I/O Banks for A3P1000 Only**

	VMV (V)	Static Power $P_{DC6}$ (mW) <sup>2</sup>	Dynamic Power $P_{AC9}$ ( $\mu$ W/MHz) <sup>3</sup>
<b>Single-Ended</b>			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
<b>Differential</b>			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

*Notes:*

1.  $P_{DC6}$  is the static power (where applicable) measured on VMV.
2.  $P_{AC9}$  is the total dynamic power measured on VMV.

**Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings**  
**Applicable to Standard Plus I/O Banks for A3P1000 Only**

	VMV (V)	Static Power $P_{DC6}$ (mW) <sup>1</sup>	Dynamic Power $P_{AC9}$ ( $\mu$ W/MHz) <sup>2</sup>
<b>Single-Ended</b>			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.72
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
1.2 V LVCMOS	3.3	–	18.13
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	16.72

*Notes:*

1.  $P_{DC6}$  is the static power (where applicable) measured on VMV.
2.  $P_{AC9}$  is the total dynamic power measured on VMV.

**Table 2-15 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings <sup>1</sup>**  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

	$C_{LOAD}$ (pF)	$V_{CCI}$ (V)	Static Power $P_{DC7}$ (mW) <sup>2</sup>	Dynamic Power $P_{AC10}$ (μW/MHz) <sup>3</sup>
<b>Single-Ended</b>				
3.3 V LVTTTL/LVCMOS	5	3.3	–	148.00
2.5 V LVCMOS	5	2.5	–	83.23
1.8 V LVCMOS	5	1.8	–	54.58
1.5 V LVCMOS (JESD8-11)	5	1.5	–	37.05
1.2 V LVCMOS <sup>4</sup>	5	1.2	–	17.94
3.3 V PCI	10	3.3	–	204.61
3.3 V PCI-X	10	3.3	–	204.61
<b>Voltage-Referenced</b>				
3.3 V GTL	10	3.3	–	24.08
2.5 V GTL	10	2.5	–	13.52
3.3 V GTL+	10	3.3	–	24.10
2.5 V GTL+	10	2.5	–	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
<b>Differential</b>				
LVDS	–	2.5	7.70	89.62
LVPECL	–	3.3	19.42	168.02

**Notes:**

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2.  $P_{DC7}$  is the static power (where applicable) measured on  $V_{CCI}$ .
3.  $P_{AC10}$  is the total dynamic power measured on  $V_{CCI}$ .

**Table 2-16 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings <sup>1</sup>**  
**Applicable to Advanced I/O Banks for A3P1000 Only**

	$C_{LOAD}$ (pF)	VCCI (V)	Static Power $P_{DC7}$ (mW) <sup>2</sup>	Dynamic Power $P_{AC10}$ ( $\mu$ W/MHz) <sup>3</sup>
<b>Single-Ended</b>				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	141.97
2.5 V LVCMOS	5	2.5	–	79.98
1.8 V LVCMOS	5	1.8	–	52.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	35.62
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
<b>Differential</b>				
LVDS	–	2.5	7.74	89.71
LVPECL	–	3.3	19.54	167.54

*Notes:*

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2.  $P_{DC7}$  is the static power (where applicable) measured on VCCI.
3.  $P_{AC10}$  is the total dynamic power measured on VCCI.

**Table 2-17 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings**  
**Applicable to Standard Plus I/O Banks for A3P1000 Only**

	$C_{LOAD}$ (pF)	VCCI (V)	Static Power $P_{DC7}$ (mW) <sup>2</sup>	Dynamic Power $P_{AC10}$ ( $\mu$ W/MHz) <sup>3</sup>
<b>Single-Ended</b>				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	125.97
2.5 V LVCMOS	5	2.5	–	70.82
1.8 V LVCMOS	5	1.8	–	36.39
1.5 V LVCMOS (JESD8-11)	5	1.5	–	25.34
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

*Notes:*

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2.  $P_{DC7}$  is the static power (where applicable) measured on VCCI.
3.  $P_{AC10}$  is the total dynamic power measured on VCCI.

## Power Consumption of Various Internal Resources

**Table 2-18 • Different Components Contributing to Dynamic Power Consumption in Devices Operating at 1.2 V VCC**

Parameter	Definition	Device-Specific Dynamic Power (μW/MHz)	
		A3PE3000L	A3PE600L
P <sub>AC1</sub>	Clock contribution of a Global Rib	12.61	
P <sub>AC2</sub>	Clock contribution of a Global Spine	2.66	
P <sub>AC3</sub>	Clock contribution of a VersaTile row	0.56	
P <sub>AC4</sub>	Clock contribution of a VersaTile used as a sequential module	0.07	
P <sub>AC5</sub>	First contribution of a VersaTile used as a sequential module	0.05	
P <sub>AC6</sub>	Second contribution of a VersaTile used as a sequential module	0.19	
P <sub>AC7</sub>	Contribution of a VersaTile used as a combinatorial module	0.11	
P <sub>AC8</sub>	Average contribution of a routing net	0.45	
P <sub>AC9</sub>	Contribution of an I/O input pin (standard-dependent)	See Table 2-12 on page 2-11 through Table 2-14 on page 2-12.	
P <sub>AC10</sub>	Contribution of an I/O output pin (standard-dependent)	See Table 2-15 on page 2-13 through Table 2-17 on page 2-14.	
P <sub>AC11</sub>	Average contribution of a RAM block during a read operation	25.00	
P <sub>AC12</sub>	Average contribution of a RAM block during a write operation	30.00	
P <sub>AC13</sub>	Dynamic contribution for PLL	1.74	

**Table 2-19 • Different Components Contributing to Dynamic Power Consumption in Military ProASIC3/EL Devices at 1.5 V V<sub>CC</sub>**

Parameter	Definition	Device-Specific Dynamic Power (μW/MHz)		
		A3PE3000L	A3PE600L	A3P1000
P <sub>AC1</sub>	Clock contribution of a Global Rib	19.7		14.50
P <sub>AC2</sub>	Clock contribution of a Global Spine	4.16		2.48
P <sub>AC3</sub>	Clock contribution of a VersaTile row	0.88		0.81
P <sub>AC4</sub>	Clock contribution of a VersaTile used as a sequential module	0.12		
P <sub>AC5</sub>	First contribution of a VersaTile used as a sequential module	0.07		
P <sub>AC6</sub>	Second contribution of a VersaTile used as a sequential module	0.29		
P <sub>AC7</sub>	Contribution of a VersaTile used as a combinatorial Module	0.29		
P <sub>AC8</sub>	Average contribution of a routing net	0.70		
P <sub>AC9</sub>	Contribution of an I/O input pin (standard-dependent)	See Table 2-12 on page 2-11 through Table 2-14 on page 2-12.		
P <sub>AC10</sub>	Contribution of an I/O output pin (standard-dependent)	See Table 2-15 on page 2-13 through Table 2-17 on page 2-14.		
P <sub>AC11</sub>	Average contribution of a RAM block during a read operation	25.00		
P <sub>AC12</sub>	Average contribution of a RAM block during a write operation	30.00		
P <sub>AC13</sub>	Dynamic contribution for PLL	2.60		

**Table 2-20 • Different Components Contributing to the Static Power Consumption in Military ProASIC3/EL Devices**

Parameter	Definition	Device-Specific Dynamic Power (μW)		
		A3PE3000L	A3PE600L	A3P1000
P <sub>DC1</sub>	Array static power in Active mode	See Table 2-10 on page 2-10.		
P <sub>DC2</sub>	Array static power in Static (Idle) mode	See Table 2-10 on page 2-10.		
P <sub>DC3</sub>	Array static power in Flash*Freeze mode	See Table 2-7 on page 2-9.		
P <sub>DC4</sub>	Static PLL contribution at 1.2 V operating core voltage (for A3PE600L and A3PE3000L only)	1.42 mW		N/A
	Static PLL contribution 1.5 V operating core voltage	2.55 mW		
P <sub>DC5</sub>	Bank quiescent power (V <sub>CC1</sub> -dependent)	See Table 2-7 on page 2-9, Table 2-8 on page 2-9, Table 2-10 on page 2-10.		
P <sub>DC6</sub>	I/O input pin static power (standard-dependent)	See Table 2-12 on page 2-11. through Table 2-14 on page 2-12.		
P <sub>DC7</sub>	I/O output pin static power (standard-dependent)	See Table 2-15 on page 2-13 through Table 2-17 on page 2-14.		

\* For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Libero® Integrated Design Environment (IDE).

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-21 on page 2-19](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-22 on page 2-19](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-22 on page 2-19](#). The calculation should be repeated for each clock domain defined in the design.

### Methodology

#### Total Power Consumption— $P_{TOTAL}$

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

$P_{STAT}$  is the total static power consumption.

$P_{DYN}$  is the total dynamic power consumption.

#### Total Static Power Consumption— $P_{STAT}$

$$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$$

$N_{INPUTS}$  is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$  is the number of I/O output buffers used in the design.

$N_{BANKS}$  is the number of I/O banks powered in the design.

#### Total Dynamic Power Consumption— $P_{DYN}$

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

#### Global Clock Contribution— $P_{CLOCK}$

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

$N_{SPINE}$  is the number of global spines used in the user design—guidelines are provided in [Table 2-21 on page 2-19](#).

$N_{ROW}$  is the number of VersaTile rows used in the design—guidelines are provided in [Table 2-21 on page 2-19](#).

$F_{CLK}$  is the global clock signal frequency.

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design.

$P_{AC1}$ ,  $P_{AC2}$ ,  $P_{AC3}$ , and  $P_{AC4}$  are device-dependent.

#### Sequential Cells Contribution— $P_{S-CELL}$

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-21 on page 2-19](#).

$F_{CLK}$  is the global clock signal frequency.

### Combinatorial Cells Contribution— $P_{C-CELL}$

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

$N_{C-CELL}$  is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-21 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

### Routing Net Contribution— $P_{NET}$

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design.

$N_{C-CELL}$  is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-21 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

### I/O Input Buffer Contribution— $P_{INPUTS}$

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

$N_{INPUTS}$  is the number of I/O input buffers used in the design.

$\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in Table 2-21 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

### I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$  is the number of I/O output buffers used in the design.

$\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in Table 2-21 on page 2-19.

$\beta_1$  is the I/O buffer enable rate—guidelines are provided in Table 2-22 on page 2-19.

$F_{CLK}$  is the global clock signal frequency.

### RAM Contribution— $P_{MEMORY}$

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

$N_{BLOCKS}$  is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$  is the memory read clock frequency.

$\beta_2$  is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$  is the memory write clock frequency.

$\beta_3$  is the RAM enable rate for write operations—guidelines are provided in Table 2-22 on page 2-19.

### PLL Contribution— $P_{PLL}$

$$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$$

$F_{CLKOUT}$  is the output clock frequency.<sup>1</sup>

1. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ( $P_{AC13} * F_{CLKOUT}$  product) to the total PLL contribution.



## Guidelines

### Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - ...
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate =  $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

### Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

**Table 2-21 • Toggle Rate Guidelines Recommended for Power Calculation**

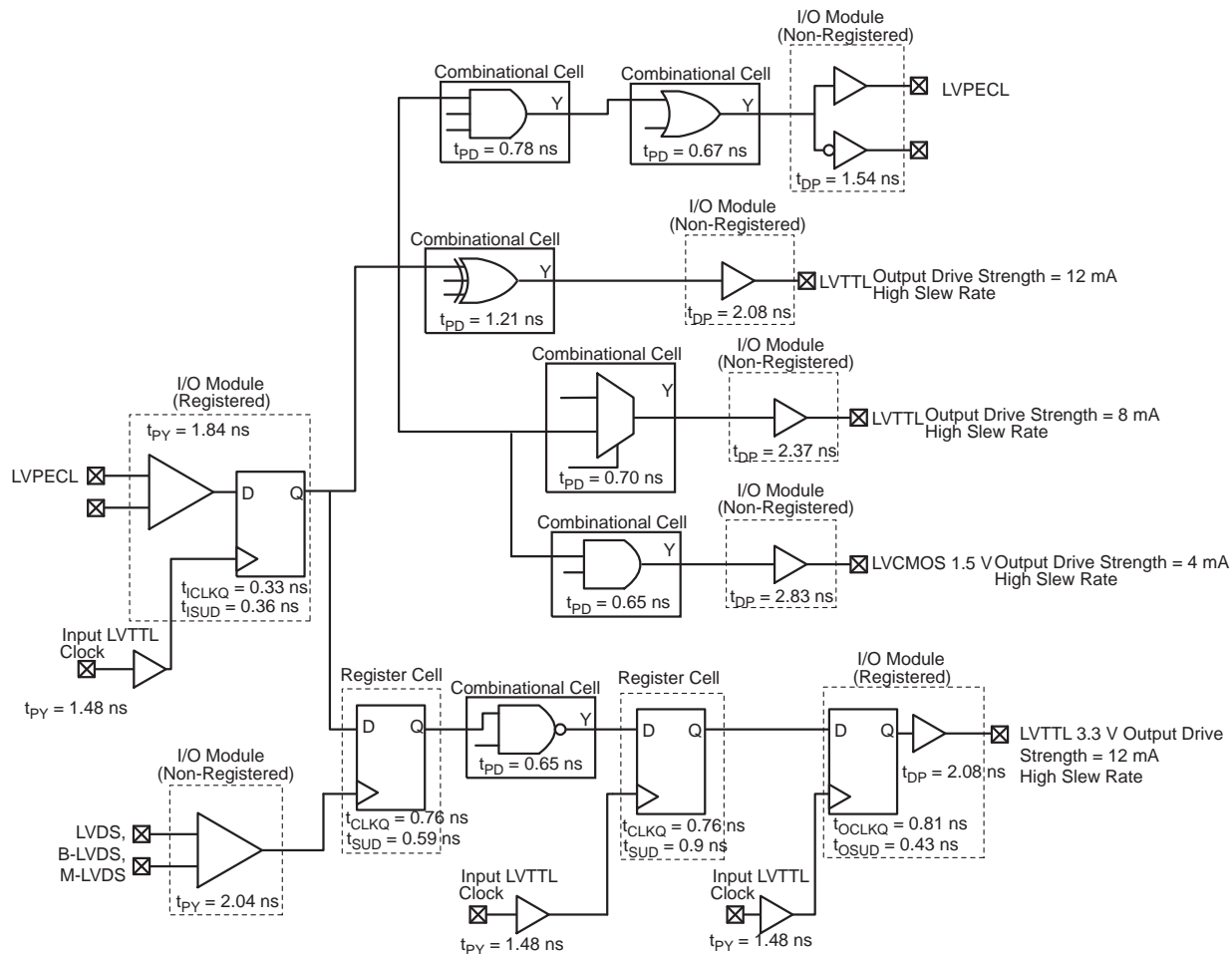
Component	Definition	Guideline
$\alpha_1$	Toggle rate of VersaTile outputs	10%
$\alpha_2$	I/O buffer toggle rate	10%

**Table 2-22 • Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
$\beta_1$	I/O output buffer enable rate	100%
$\beta_2$	RAM enable rate for read operations	12.5%
$\beta_3$	RAM enable rate for write operations	12.5%

# User I/O Characteristics

## Timing Model



**Figure 2-4 • Timing Model**

**Operating Conditions: -1 Speed, Military Temperature Range ( $T_J = 125^\circ\text{C}$ ), Worst-Case VCC = 1.14 V (example for A3PE3000L and A3PE600L)**

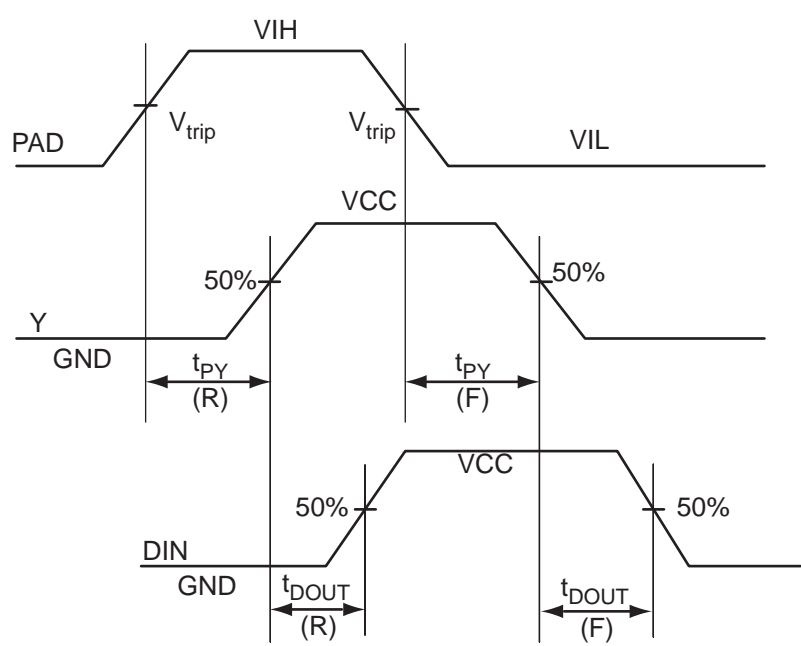
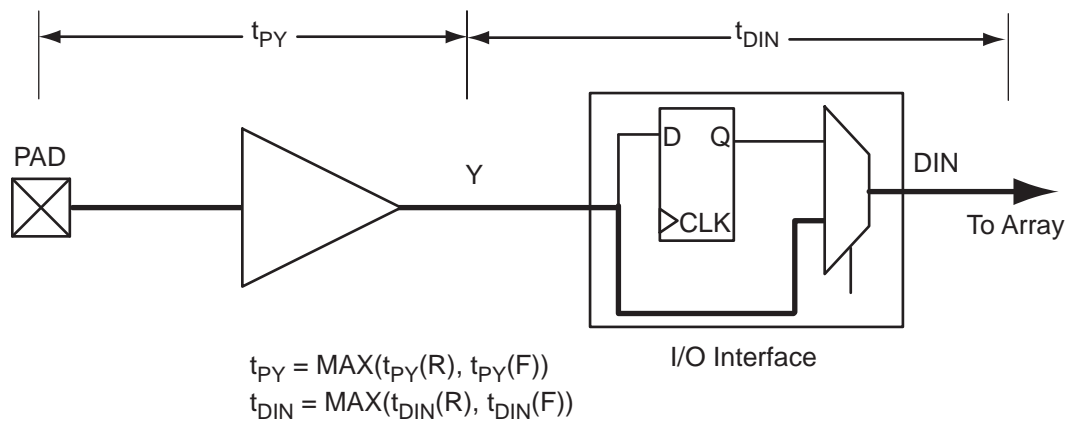


Figure 2-5 • Input Buffer Timing Model and Delays (example)

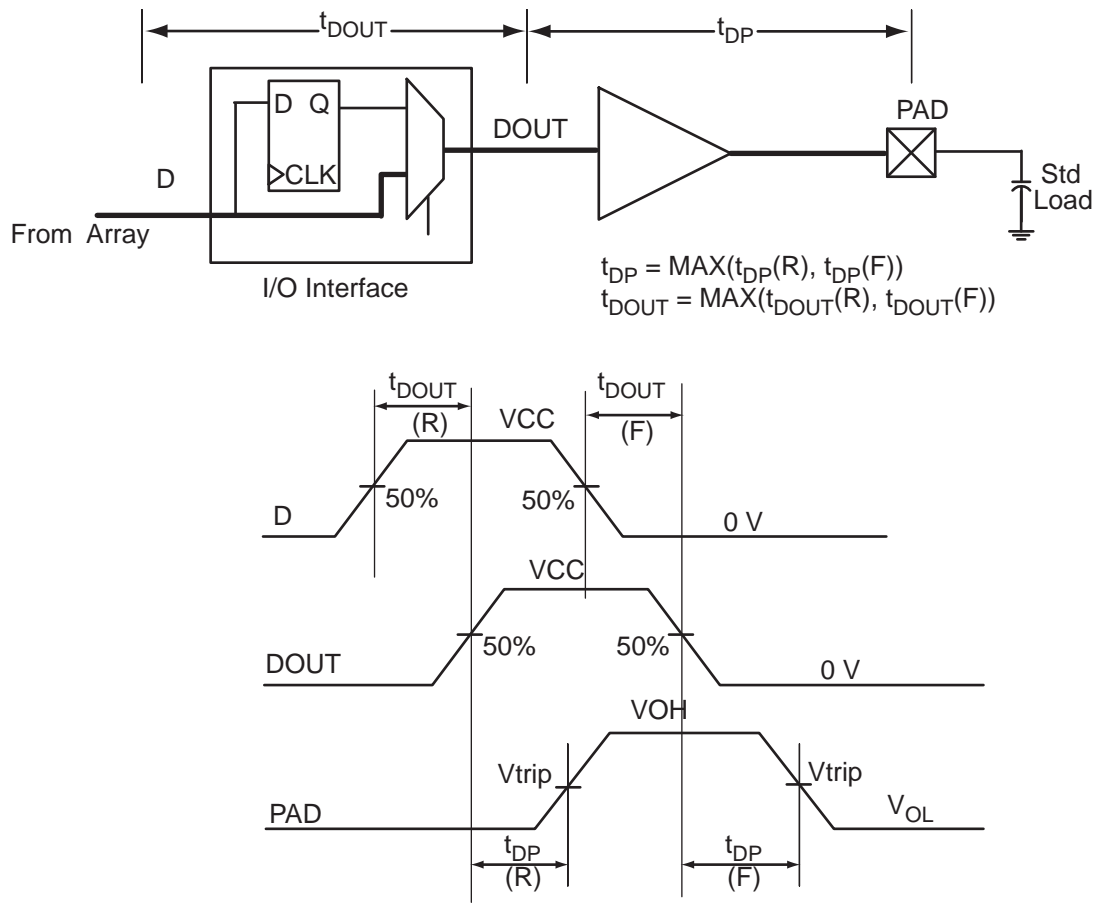


Figure 2-6 • Output Buffer Model and Delays (example)

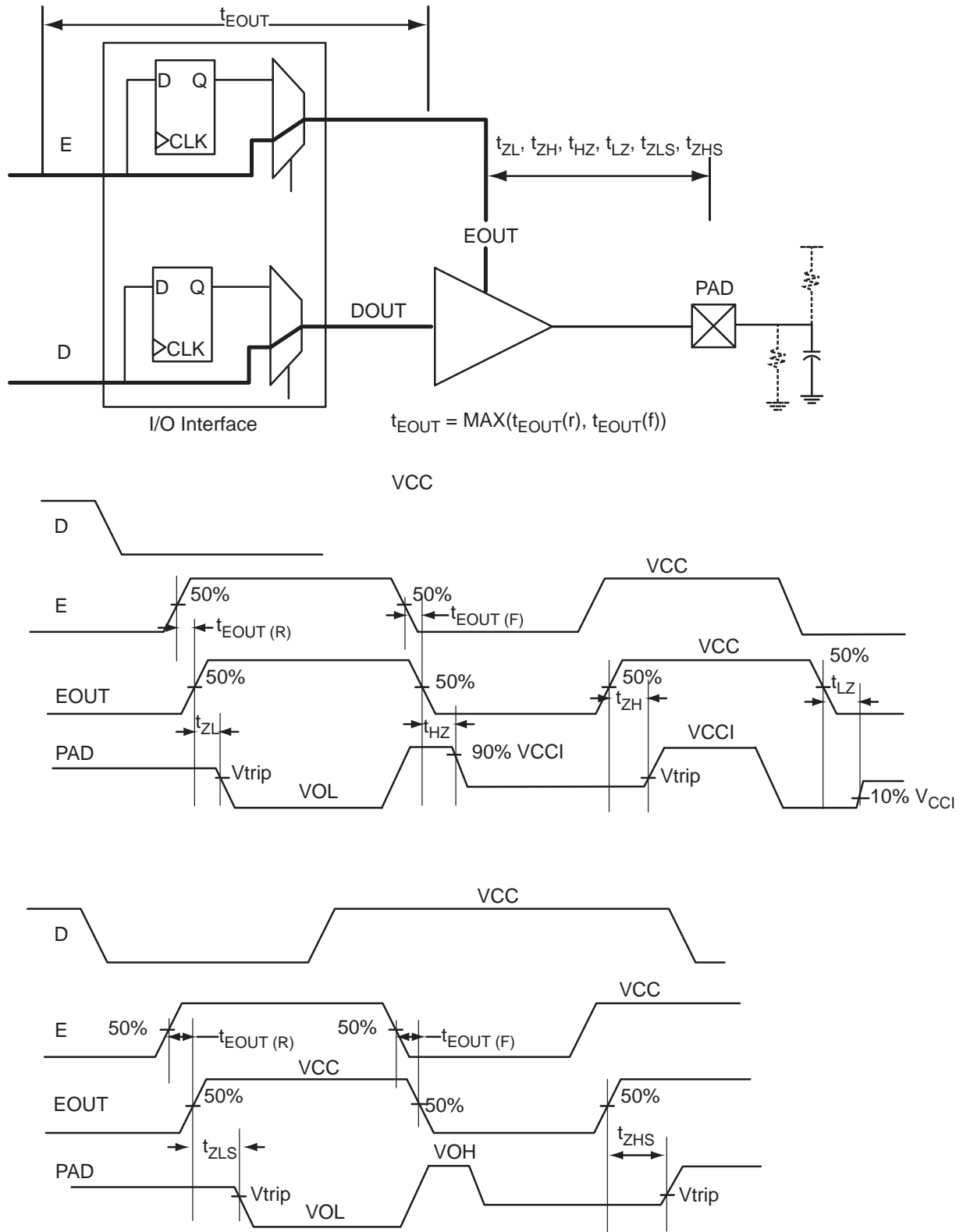


Figure 2-7 • Tristate Output Buffer Timing Model and Delays (example)

## Overview of I/O Performance

### Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-23 • Summary of Maximum and Minimum DC Input and Output Levels**  
 Applicable to Military Conditions—Software Default Settings  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL <sup>1</sup>	IOH <sup>1</sup>
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	-0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	12	12
1.5 V LVCMOS	12 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
3.3 V PCI	Per PCI Specification									
3.3 V PCI-X	Per PCI-X Specification									
3.3 V GTL	25 mA <sup>2</sup>	High	-0.3	VREF - 0.05	VREF + 0.05	3.6	0.4	-	25	25
2.5 V GTL	25 mA <sup>2</sup>	High	-0.3	VREF - 0.05	VREF + 0.05	2.7	0.4	-	25	25
3.3 V GTL+	35 mA	High	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.6	-	51	51
2.5 V GTL+	33 mA	High	-0.3	VREF - 0.1	VREF + 0.1	2.7	0.6	-	40	40
HSTL (I)	8 mA	High	-0.3	VREF - 0.1	VREF + 0.1	1.575	0.4	VCCI - 0.4	8	8
HSTL (II)	15 mA <sup>2</sup>	High	-0.3	VREF - 0.1	VREF + 0.1	1.575	0.4	VCCI - 0.4	15	15
SSTL2 (I)	15 mA	High	-0.3	VREF - 0.2	VREF + 0.2	2.7	0.54	VCCI - 0.62	15	15
SSTL2 (II)	18 mA	High	-0.3	VREF - 0.2	VREF + 0.2	2.7	0.35	VCCI - 0.43	18	18
SSTL3 (I)	14 mA	High	-0.3	VREF - 0.2	VREF + 0.2	3.6	0.7	VCCI - 1.1	14	14
SSTL3 (II)	21 mA	High	-0.3	VREF - 0.2	VREF + 0.2	3.6	0.5	VCCI - 0.9	21	21

**Notes:**

1. Currents are measured at 125°C junction temperature.
2. Output drive strength is below JEDEC specification.
3. Output slew rate can be extracted using the IBIS Models.

**Table 2-24 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Military Conditions—Software Default Settings  
Applicable to Advanced I/O Banks for A3P1000 Only**

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	I <sub>OL</sub> <sup>1</sup>	I <sub>OH</sub> <sup>1</sup>
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	-0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	12	12
1.5 V LVCMOS	12 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

**Notes:**

1. Currents are measured at 125°C junction temperature.
2. Output slew rate can be extracted using the IBIS Models

**Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Military Conditions—Software Default Settings  
Applicable to Standard Plus I/O Banks for A3P1000 Only**

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	I <sub>OL</sub> <sup>1</sup>	I <sub>OH</sub> <sup>1</sup>
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	-0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8
1.5 V LVCMOS	4 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4
1.2 V LVCMOS	2 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

**Notes:**

1. Currents are measured at 125°C junction temperature.
2. Output slew rate can be extracted using the IBIS Models.

**Table 2-26 • Summary of Maximum and Minimum DC Input Levels  
Applicable to Military Conditions**

DC I/O Standard	Military	
	$I_{IL}$	$I_{IH}$
	$\mu A$	$\mu A$
3.3 V LVTTTL / 3.3 V LVCMOS	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
1.2 V LVCMOS	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15
3.3 V GTL	15	15
2.5 V GTL	15	15
3.3 V GTL+	15	15
2.5 V GTL+	15	15
HSTL (I)	15	15
HSTL (II)	15	15
SSTL2 (I)	15	15
SSTL2 (II)	15	15
SSTL3 (I)	15	15
SSTL3 (II)	15	15

*Note:* Military temperature range:  $-55^{\circ}C$  to  $125^{\circ}C$



## Summary of I/O Timing Characteristics – Default I/O Software Settings

**Table 2-27 • Summary of AC Memory Points \***

Standard	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_REF)	Measuring Trip Point (Vtrip)
3.3 V LVTTTL / 3.3 V LVCMOS	–	–	1.4 V
2.5 V LVCMOS	–	–	1.2 V
1.8 V LVCMOS	–	–	0.90 V
1.5 V LVCMOS	–	–	0.75 V
1.2 V LVCMOS*	–	–	0.6V
3.3 V PCI	–	–	0.285 * VCCI (RR)
			0.615 * VCCI (FF))
3.3 V PCI-X	–	–	0.285 * VCCI (RR)
			0.615 * VCCI (FF)
3.3 V GTL	0.8 V	1.2 V	VREF
2.5 V GTL	0.8 V	1.2 V	VREF
3.3 V GTL+	1.0 V	1.5 V	VREF
2.5 V GTL+	1.0 V	1.5 V	VREF
HSTL (I)	0.75 V	0.75 V	VREF
HSTL (II)	0.75 V	0.75 V	VREF
SSTL2 (I)	1.25 V	1.25 V	VREF
SSTL2 (II)	1.25 V	1.25 V	VREF
SSTL3 (I)	1.5 V	1.485 V	VREF
SSTL3 (II)	1.5 V	1.485 V	VREF
LVDS	–	–	Cross point
LVPECL	–	–	Cross point

\* Applicable to A3PE600L and A3PE3000L devices operating at 1.2 V core regions only.

**Table 2-28 • I/O AC Parameter Definitions**

Parameter	Parameter Definition
t <sub>DP</sub>	Data to Pad delay through the Output Buffer
t <sub>PY</sub>	Pad to Data delay through the Input Buffer
t <sub>DOUT</sub>	Data to Output Buffer delay through the I/O interface
t <sub>EOUT</sub>	Enable to Output Buffer Tristate Control delay through the I/O interface
t <sub>DIN</sub>	Input Buffer to Data delay through the I/O interface
t <sub>HZ</sub>	Enable to Pad delay through the Output Buffer—HIGH to Z
t <sub>ZH</sub>	Enable to Pad delay through the Output Buffer—Z to HIGH
t <sub>LZ</sub>	Enable to Pad delay through the Output Buffer—LOW to Z
t <sub>ZL</sub>	Enable to Pad delay through the Output Buffer—Z to LOW
t <sub>ZHS</sub>	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t <sub>ZLS</sub>	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

## 1.2 V Core Operating Voltage

**Table 2-29 • Summary of I/O Timing Characteristics—Software Default Settings**  
 –1 Speed Grade, Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst Case VCC = 1.14 V, Worst Case VCCI  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{DOUT}$ (ns)	$t_{DP}$ (ns)	$t_{DIN}$ (ns)	$t_{PY}$ (ns)	$t_{PYS}$ (ns)	$t_{EOUT}$ (ns)	$t_{ZL}$ (ns)	$t_{ZH}$ (ns)	$t_{LZ}$ (ns)	$t_{HZ}$ (ns)	$t_{ZLS}$ (ns)	$t_{ZHS}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	5	–	0.68	2.08	0.05	1.48	2.03	0.44	2.12	1.56	2.76	3.04	4.00	3.44	ns
2.5 V LVCMOS	12 mA	High	5	–	0.68	2.12	0.05	1.74	2.16	0.44	2.16	1.74	2.84	2.94	4.04	3.63	ns
1.8 V LVCMOS	12 mA	High	5	–	0.68	2.36	0.05	1.69	2.38	0.44	2.40	1.94	3.14	3.57	4.28	3.82	ns
1.5 V LVCMOS	12 mA	High	5	–	0.68	2.71	0.05	1.86	2.59	0.44	2.76	2.24	3.34	3.68	4.64	4.12	ns
1.2 V LVCMOS	2mA	High	5	–	0.68	4.40	0.05	2.23	3.20	0.44	4.21	3.71	4.35	4.11	6.02	5.52	ns
3.3 V PCI	Per PCI spec	High	10	25	0.68	2.36	0.05	2.31	3.12	0.44	2.41	1.68	2.76	3.04	4.29	3.56	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25	0.68	2.36	0.05	2.31	3.12	0.44	2.41	1.68	2.76	3.04	4.29	3.56	ns
3.3 V GTL	25 mA	High	10	25	0.68	1.75	0.05	1.98	–	0.44	1.72	1.75	–	–	3.60	3.63	ns
2.5 V GTL	25 mA	High	10	25	0.68	1.79	0.05	1.92	–	0.44	1.82	1.79	–	–	3.70	3.68	ns
3.3 V GTL+	35 mA	High	10	25	0.68	1.73	0.05	1.98	–	0.44	1.76	1.73	–	–	3.65	3.61	ns
2.5 V GTL+	33 mA	High	10	25	0.68	1.86	0.05	1.92	–	0.44	1.89	1.77	–	–	3.78	3.65	ns
HSTL (I)	8 mA	High	20	25	0.68	2.68	0.05	2.34	–	0.44	2.73	2.65	–	–	4.61	4.53	ns
HSTL (II)	15 mA	High	20	50	0.68	2.55	0.05	2.34	–	0.44	2.59	2.29	–	–	4.48	4.17	ns
SSTL2 (I)	15 mA	High	30	25	0.68	1.79	0.05	1.77	–	0.44	1.82	1.56	–	–	1.82	1.56	ns
SSTL2 (II)	18 mA	High	30	50	0.68	1.83	0.05	1.77	–	0.44	1.86	1.49	–	–	1.86	1.49	ns
SSTL3 (I)	14 mA	High	30	25	0.68	1.94	0.05	1.69	–	0.44	1.98	1.55	–	–	1.98	1.55	ns
SSTL3 (II)	21 mA	High	30	50	0.68	1.74	0.05	1.69	–	0.44	1.77	1.41	–	–	1.77	1.41	ns
LVDS	24 mA	High	–	–	0.68	1.57	0.05	2.04	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.68	1.54	0.05	1.84	–	–	–	–	–	–	–	–	ns

**Notes:**

1. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-13 on page 2-65](#) for connectivity. This resistor is not required during normal operation.

### 1.5 V Core Voltage

**Table 2-30 • Summary of I/O Timing Characteristics—Software Default Settings**  
 –1 Speed Grade, Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst Case  $V_{CCI}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{DOUT}$ (ns)	$t_{DP}$ (ns)	$t_{DIN}$ (ns)	$t_{PY}$ (ns)	$t_{PYS}$ (ns)	$t_{EOUT}$ (ns)	$t_{ZL}$ (ns)	$t_{ZH}$ (ns)	$t_{LZ}$ (ns)	$t_{HZ}$ (ns)	$t_{ZLS}$ (ns)	$t_{ZHS}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	5	–	0.52	2.08	0.03	1.48	2.03	0.34	2.12	1.56	2.76	3.04	4.00	3.44	ns
2.5 V LVCMOS	12 mA	High	5	–	0.52	2.12	0.03	1.74	2.16	0.34	2.16	1.74	2.84	2.94	4.04	3.63	ns
1.8 V LVCMOS	12 mA	High	5	–	0.52	2.36	0.03	1.69	2.38	0.34	2.40	1.94	3.14	3.57	4.28	3.82	ns
1.5 V LVCMOS	12 mA	High	5	–	0.52	2.71	0.03	1.86	2.59	0.34	2.76	2.24	3.34	3.68	4.64	4.12	ns
3.3 V PCI	Per PCI spec	High	10	25	0.52	2.36	0.03	2.31	3.12	0.34	2.41	1.68	2.76	3.04	4.29	3.56	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25	0.52	2.36	0.03	2.31	3.12	0.34	2.41	1.68	2.76	3.04	4.29	3.56	ns
3.3 V GTL	25 mA	High	10	25	0.52	1.75	0.03	1.98	–	0.34	1.72	1.75	–	–	3.60	3.63	ns
2.5 V GTL	25 mA	High	10	25	0.52	1.79	0.03	1.92	–	0.34	1.82	1.79	–	–	3.70	3.68	ns
3.3 V GTL+	35 mA	High	10	25	0.52	1.73	0.03	1.98	–	0.34	1.76	1.73	–	–	3.65	3.61	ns
2.5 V GTL+	33 mA	High	10	25	0.52	1.86	0.03	1.92	–	0.34	1.89	1.77	–	–	3.78	3.65	ns
HSTL (I)	8 mA	High	20	25	0.52	2.68	0.03	2.34	–	0.34	2.73	2.65	–	–	4.61	4.53	ns
HSTL (II)	15 mA	High	20	50	0.52	2.55	0.03	2.34	–	0.34	2.59	2.29	–	–	4.48	4.17	ns
SSTL2 (I)	15 mA	High	30	25	0.52	1.79	0.03	1.77	–	0.34	1.82	1.56	–	–	1.82	1.56	ns
SSTL2 (II)	18 mA	High	30	50	0.52	1.83	0.03	1.77	–	0.34	1.86	1.49	–	–	1.86	1.49	ns
SSTL3 (I)	14 mA	High	30	25	0.52	1.94	0.03	1.69	–	0.34	1.98	1.55	–	–	1.98	1.55	ns
SSTL3 (II)	21 mA	High	30	50	0.52	1.74	0.03	1.69	–	0.34	1.77	1.41	–	–	1.77	1.41	ns
LVDS	24 mA	High	–	–	0.52	1.57	0.03	2.04	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.52	1.54	0.03	1.84	–	–	–	–	–	–	–	–	ns

**Notes:**

1. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-13 on page 2-65](#) for connectivity. This resistor is not required during normal operation.

**Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings**  
 –1 Speed Grade, Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst Case  $V_{CC} = 1.425\text{ V}$ , Worst Case  $V_{CCI}$   
 Applicable to Advanced I/O Banks for A3P1000 Only

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{DOUT}$ (ns)	$t_{DP}$ (ns)	$t_{DIN}$ (ns)	$t_{PY}$ (ns)	$t_{EOUT}$ (ns)	$t_{ZL}$ (ns)	$t_{ZH}$ (ns)	$t_{LZ}$ (ns)	$t_{HZ}$ (ns)	$t_{ZLS}$ (ns)	$t_{ZHS}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	5 pF	–	0.54	2.24	0.04	0.95	0.39	2.28	1.70	3.00	3.35	4.38	3.79	ns
2.5 V LVCMOS	12 mA	High	5 pF	–	0.54	2.26	0.04	1.23	0.39	2.30	1.89	3.09	3.22	4.39	3.99	ns
1.8 V LVCMOS	12 mA	High	5 pF	–	0.54	2.49	0.04	1.14	0.39	2.54	2.12	3.46	3.82	4.63	4.21	ns
1.5 V LVCMOS	12 mA	High	5 pF	–	0.54	2.85	0.04	1.35	0.39	2.90	2.45	3.69	3.93	4.99	4.55	ns
3.3 V PCI	Per PCI spec.	High	5 pF	$25^2$	0.54	2.51	0.04	0.81	0.39	2.39	1.68	3.00	3.35	4.65	3.92	ns
3.3 V PCI-X	Per PCI-X spec.	High	10 pF	$25^2$	0.54	2.51	0.04	0.78	0.39	2.39	1.68	3.00	3.35	4.65	3.92	ns
LVDS	24 mA	High	–	–	0.54	1.71	0.04	1.50	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVPECL	24 mA	High	–	–	0.54	1.68	0.04	1.31	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

**Notes:**

1. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-13 on page 2-65](#) for connectivity. This resistor is not required during normal operation.

**Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings**  
 –1 Speed Grade, Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst Case  $V_{CC} = 1.425\text{ V}$ , Worst Case  $V_{CCI} = 3.0\text{ V}$   
 Applicable to Standard Plus I/O Banks for A3P1000 Only

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	$t_{DOUT}$ (ns)	$t_{DP}$ (ns)	$t_{DIN}$ (ns)	$t_{PY}$ (ns)	$t_{EOUT}$ (ns)	$t_{ZL}$ (ns)	$t_{ZH}$ (ns)	$t_{LZ}$ (ns)	$t_{HZ}$ (ns)	$t_{ZLS}$ (ns)	$t_{ZHS}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	5pF	–	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56	ns
2.5 V LVCMOS	12 mA	High	5pF	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71	ns
1.8 V LVCMOS	8 mA	High	5pF	–	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71	ns
1.5 V LVCMOS	4 mA	High	5pF	–	0.54	2.62	0.04	1.33	0.39	2.67	2.23	2.84	2.93	4.77	4.32	ns
3.3 V PCI	Per PCI spec.	High	10 pF	$25^2$	0.54	2.16	0.04	0.80	0.39	2.03	1.45	2.61	3.01	4.29	3.69	ns
3.3 V PCI-X	Per PCI-X spec.	High	10 pF	$25^2$	0.54	2.16	0.04	0.78	0.39	2.03	1.45	2.61	3.01	4.29	3.69	ns

**Notes:**

1. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-13 on page 2-65](#) for connectivity. This resistor is not required during normal operation.

## Detailed I/O DC Characteristics

**Table 2-33 • Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
$C_{IN}$	Input capacitance	$V_{IN} = 0, f = 1.0\text{ MHz}$		8	pF
$C_{INCLK}$	Input capacitance on the clock pin	$V_{IN} = 0, f = 1.0\text{ MHz}$		8	pF

**Table 2-34 • I/O Output Buffer Maximum Resistances<sup>1</sup>**  
**Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Standard	Drive Strength	R <sub>PULL-DOWN</sub> (Ω) <sup>2</sup>	R <sub>PULL-UP</sub> (Ω) <sup>3</sup>
3.3 V LVTTTL / 3.3 V LVCMOS	4 mA	100	300
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	4 mA	100	200
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75
3.3 V GTL	25 mA	11	–
2.5 V GTL	25 mA	14	–
3.3 V GTL+	35 mA	12	–
2.5 V GTL+	33 mA	15	–
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	15 mA	27	31
SSTL2 (II)	18 mA	13	15
SSTL3 (I)	14 mA	44	69
SSTL3 (II)	21 mA	18	32

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V<sub>CCi</sub>, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2.  $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3.  $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{OH_{spec}}$

**Table 2-35 • I/O Output Buffer Maximum Resistances<sup>1</sup>**  
**Applicable to Advanced I/O Banks for A3P1000 Only**

Standard	Drive Strength	R <sub>PULL-DOWN</sub> (Ω) <sup>2</sup>	R <sub>PULL-UP</sub> (Ω) <sup>3</sup>
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
1.8 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V<sub>CCi</sub>, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2.  $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3.  $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

**Table 2-36 • I/O Output Buffer Maximum Resistances<sup>1</sup>**  
**Applicable to Standard Plus I/O Banks for A3P1000 Only**

Standard	Drive Strength	R <sub>PULL-DOWN</sub> (Ω) <sup>2</sup>	R <sub>PULL-UP</sub> (Ω) <sup>3</sup>
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on  $V_{CCi}$ , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2.  $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / IOL_{spec}$
3.  $R_{(PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / IOH_{spec}$



**Table 2-37 • I/O Weak Pull-Up/Pull-Down Resistances**  
**Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

V <sub>CCI</sub>	R <sub>(WEAK PULL-UP)</sub> <sup>1</sup> (Ω)		R <sub>(WEAK PULL-DOWN)</sub> <sup>2</sup> (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k
1.2 V	TBD	TBD	TBD	TBD

**Notes:**

1.  $R_{(WEAK PULL-UP-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2.  $R_{(WEAK PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$

**Table 2-38 • I/O Short Currents  $I_{OSH}/I_{OSL}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

	Drive Strength	$I_{OSL}$ (mA)*	$I_{OSH}$ (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	4 mA	25	27
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	4 mA	16	18
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2mA	TBD	TBD
3.3 V PCI/PCIX	Per PCI/PCI-X Specification	Per PCI Curves	
3.3 V GTL	25 mA	268	181
2.5 V GTL	25 mA	169	124
3.3 V GTL+	35 mA	268	181
2.5 V GTL+	33 mA	169	124
HSTL (I)	8 mA	32	39
HSTL (II)	15 mA	66	55
SSTL2 (I)	15 mA	83	87
SSTL2 (II)	18 mA	169	124
SSTL3 (I)	14 mA	51	54
SSTL3 (II)	21 mA	103	109

 \*  $T_J = 100^\circ\text{C}$

**Table 2-39 • I/O Short Currents  $I_{OSH}/I_{OSL}$**   
**Applicable to Advanced I/O Banks for A3P1000 Only**

	Drive Strength	$I_{OSL}$ (mA)*	$I_{OSH}$ (mA)*
3.3 V LVTTTL / 3.3V LVCMOS	2mA	25	27
	4mA	25	27
	6mA	51	54
	8mA	51	54
	12mA	103	109
	16mA	132	127
	24mA	268	181
3.3 V LVCMOS	2mA	25	27
	4mA	25	27
	6mA	51	54
	8mA	51	54
	12mA	103	109
	16mA	132	127
	24mA	268	181
2.5 V LVCMOS	2mA	16	18
	4mA	16	18
	6mA	32	37
	8mA	32	37
	12mA	65	74
	16mA	83	87
	24mA	169	124
1.8 V LVCMOS	2mA	9	11
	4mA	17	22
	6mA	35	44
	8mA	45	51
	12mA	91	74
	16mA	91	74
1.5 V LVCMOS	2mA	13	16
	4mA	25	33
	6mA	32	39
	8mA	66	55
	12mA	66	55
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

\*  $T_J = 100^\circ\text{C}$

**Table 2-40 • I/O Short Currents  $I_{OSH}/I_{OSL}$   
Applicable to Standard Plus I/O Banks for A3P1000 Only**

	Drive Strength	$I_{OSL}$ (mA)*	$I_{OSH}$ (mA)*
3.3 V LVTTTL / 3.3V LVCMOS	2mA	25	27
	4mA	25	27
	6mA	51	54
	8mA	51	54
	12mA	103	109
	16mA	103	109
2.5 V LVCMOS	2mA	16	18
	4mA	16	18
	6mA	32	37
	8mA	32	37
	12mA	65	74
1.8 V LVCMOS	2mA	9	11
	4mA	17	22
	6mA	35	44
	8mA	35	44
1.5V LVCMOS	2mA	13	16
	4mA	25	33
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

\*  $T_J = 100^\circ\text{C}$

**Table 2-41 • Schmitt Trigger Input Hysteresis, Hysteresis Voltage Value (typical) for Schmitt Mode Input Buffers Applicable to A3PE600L and A3PE3000L Only**

Input Buffer Configuration	Hysteresis Value (typical)
3.3 V LVTTTL/LVCMOS/PCI/PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV
1.2 V LVCMOS (Schmitt trigger mode)	40 mV

The length of time an I/O can withstand  $I_{OSH}/I_{OSL}$  events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

**Table 2-42 • Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
-40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months
125°C	1 month

**Table 2-43 • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

\* The maximum input rise/fall time is related to the noise induced in the input buffer trace. If the noise is low, the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

## Single-Ended I/O Characteristics

### 3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

**Table 2-44 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

3.3 V LVTTTL / 3.3 V LVCMOS	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	15	15
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-45 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks for A3P1000 Only

3.3 V LVTTTL / 3.3 V LVCMOS	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	15	15
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	15	15
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	15	15
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	15	15

**Notes:**

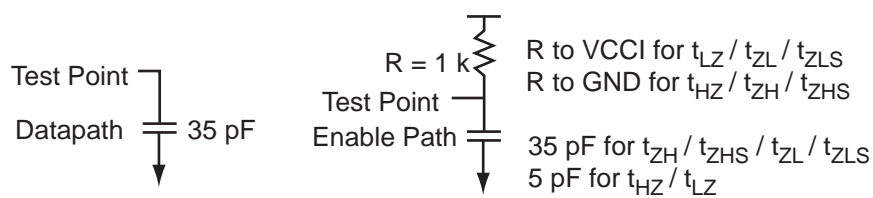
1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-46 • Minimum and Maximum DC Input and Output Levels**  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	15	15
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	15	15
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	15	15
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	15	15
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	15	15
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.



**Figure 2-8 • AC Loading**

**Table 2-47 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	3.3	1.4	5

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

## Timing Characteristics

### 1.2 V DC Core Voltage

**Table 2-48 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
4 mA	Std.	0.80	6.03	0.05	1.74	2.39	0.52	6.14	4.84	2.66	2.42	8.35	7.06	ns
	-1	0.68	5.13	0.05	1.48	2.03	0.44	5.22	4.12	2.27	2.06	7.11	6.00	ns
8 mA	Std.	0.80	4.93	0.05	1.74	2.39	0.52	5.02	4.14	3.01	3.03	7.23	6.35	ns
	-1	0.68	4.19	0.05	1.48	2.03	0.44	4.27	3.52	2.56	2.58	6.15	5.40	ns
12 mA	Std.	0.80	4.15	0.05	1.74	2.39	0.52	4.22	3.61	3.24	3.43	6.44	5.82	ns
	-1	0.68	3.53	0.05	1.48	2.03	0.44	3.59	3.07	2.76	2.92	5.47	4.95	ns
16 mA	Std.	0.80	3.92	0.05	1.74	2.39	0.52	3.99	3.49	3.29	3.54	6.21	5.71	ns
	-1	0.68	3.34	0.05	1.48	2.03	0.44	3.40	2.97	2.80	3.01	5.28	4.85	ns
24 mA	Std.	0.80	3.81	0.05	1.74	2.39	0.52	3.88	3.51	3.35	3.92	6.09	5.72	ns
	-1	0.68	3.24	0.05	1.48	2.03	0.44	3.30	2.98	2.85	3.34	5.18	4.87	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-49 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
4 mA	Std.	0.80	3.39	0.05	1.74	2.39	0.52	3.45	2.60	2.66	2.56	5.67	4.81	ns
	-1	0.68	2.89	0.05	1.48	2.03	0.44	2.94	2.21	2.27	2.18	4.82	4.10	ns
8 mA	Std.	0.80	2.79	0.05	1.74	2.39	0.52	2.84	2.08	3.02	3.18	5.05	4.30	ns
	-1	0.68	2.37	0.05	1.48	2.03	0.44	2.42	1.77	2.57	2.70	4.30	3.65	ns
12 mA	Std.	0.80	2.45	0.05	1.74	2.39	0.52	2.49	1.83	3.24	3.58	4.71	4.05	ns
	-1	0.68	2.08	0.05	1.48	2.03	0.44	2.12	1.56	2.76	3.04	4.00	3.44	ns
16 mA	Std.	0.80	2.39	0.05	1.74	2.39	0.52	2.43	1.79	3.30	3.69	4.65	4.00	ns
	-1	0.68	2.03	0.05	1.48	2.03	0.44	2.07	1.52	2.80	3.14	3.95	3.40	ns
24 mA	Std.	0.80	2.41	0.05	1.74	2.39	0.52	2.46	1.72	3.35	4.08	4.67	3.94	ns
	-1	0.68	2.05	0.05	1.48	2.03	0.44	2.09	1.47	2.85	3.47	3.97	3.35	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.



**1.5 V DC Core Voltage**
**Table 2-50 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 3.0\text{ V}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.61	6.03	0.04	1.74	2.39	0.40	6.14	4.84	2.66	2.42	8.35	7.06	ns
	-1	0.52	5.13	0.03	1.48	2.03	0.34	5.22	4.12	2.27	2.06	7.11	6.00	ns
8 mA	Std.	0.61	4.93	0.04	1.74	2.39	0.40	5.02	4.14	3.01	3.03	7.23	6.35	ns
	-1	0.52	4.19	0.03	1.48	2.03	0.34	4.27	3.52	2.56	2.58	6.15	5.40	ns
12 mA	Std.	0.61	4.15	0.04	1.74	2.39	0.40	4.22	3.61	3.24	3.43	6.44	5.82	ns
	-1	0.52	3.53	0.03	1.48	2.03	0.34	3.59	3.07	2.76	2.92	5.47	4.95	ns
16 mA	Std.	0.61	3.92	0.04	1.74	2.39	0.40	3.99	3.49	3.29	3.54	6.21	5.71	ns
	-1	0.52	3.34	0.03	1.48	2.03	0.34	3.40	2.97	2.80	3.01	5.28	4.85	ns
24 mA	Std.	0.61	3.81	0.04	1.74	2.39	0.40	3.88	3.51	3.35	3.92	6.09	5.72	ns
	-1	0.52	3.24	0.03	1.48	2.03	0.34	3.30	2.98	2.85	3.34	5.18	4.87	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-51 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 3.0\text{ V}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.61	3.39	0.04	1.74	2.39	0.40	3.45	2.60	2.66	2.56	5.67	4.81	ns
	-1	0.52	2.89	0.03	1.48	2.03	0.34	2.94	2.21	2.27	2.18	4.82	4.10	ns
8 mA	Std.	0.61	2.79	0.04	1.74	2.39	0.40	2.84	2.08	3.02	3.18	5.05	4.30	ns
	-1	0.52	2.37	0.03	1.48	2.03	0.34	2.42	1.77	2.57	2.70	4.30	3.65	ns
12 mA	Std.	0.61	2.45	0.04	1.74	2.39	0.40	2.49	1.83	3.24	3.58	4.71	4.05	ns
	-1	0.52	2.08	0.03	1.48	2.03	0.34	2.12	1.56	2.76	3.04	4.00	3.44	ns
16 mA	Std.	0.61	2.39	0.04	1.74	2.39	0.40	2.43	1.79	3.30	3.69	4.65	4.00	ns
	-1	0.52	2.03	0.03	1.48	2.03	0.34	2.07	1.52	2.80	3.14	3.95	3.40	ns
24 mA	Std.	0.61	2.41	0.04	1.74	2.39	0.40	2.46	1.72	3.35	4.08	4.67	3.94	ns
	-1	0.52	2.05	0.03	1.48	2.03	0.34	2.09	1.47	2.85	3.47	3.97	3.35	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-52 • 3.3 V LVTTTL / 3.3 V LVC MOS Low Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks for A3P1000 Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.63	6.25	0.05	1.12	0.45	6.37	5.29	2.91	2.70	8.83	7.75	ns
	-1	0.54	5.32	0.04	0.95	0.39	5.42	4.50	2.47	2.30	7.51	6.59	ns
6 mA	Std.	0.63	5.25	0.05	1.12	0.45	5.35	4.58	3.28	3.34	7.81	7.04	ns
	-1	0.54	4.47	0.04	0.95	0.39	4.55	3.90	2.79	2.85	6.65	5.99	ns
8 mA	Std.	0.63	5.25	0.05	1.12	0.45	5.35	4.58	3.28	3.34	7.81	7.04	ns
	-1	0.54	4.47	0.04	0.95	0.39	4.55	3.90	2.79	2.85	6.65	5.99	ns
12 mA	Std.	0.63	4.50	0.05	1.12	0.45	4.59	4.05	3.53	3.76	7.05	6.51	ns
	-1	0.54	3.83	0.04	0.95	0.39	3.90	3.45	3.00	3.20	5.99	5.54	ns
16 mA	Std.	0.63	4.27	0.05	1.12	0.45	4.35	3.93	3.58	3.86	6.81	6.39	ns
	-1	0.54	3.63	0.04	0.95	0.39	3.70	3.34	3.05	3.29	5.79	5.43	ns
24 mA	Std.	0.63	4.14	0.05	1.12	0.45	4.22	3.97	3.65	4.27	6.68	6.43	ns
	-1	0.54	3.53	0.04	0.95	0.39	3.59	3.38	3.10	3.63	5.68	5.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-53 • 3.3 V LVTTTL / 3.3 V LVC MOS High Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks for A3P1000 Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.63	3.55	0.05	1.12	0.45	3.62	2.79	2.91	2.87	6.07	5.25	ns
	-1	0.54	3.02	0.04	0.95	0.39	3.08	2.37	2.48	2.44	5.17	4.46	ns
6 mA	Std.	0.63	2.95	0.05	1.12	0.45	3.00	2.25	3.28	3.52	5.46	4.71	ns
	-1	0.54	2.51	0.04	0.95	0.39	2.55	1.91	2.79	3.00	4.65	4.01	ns
8 mA	Std.	0.63	2.95	0.05	1.12	0.45	3.00	2.25	3.28	3.52	5.46	4.71	ns
	-1	0.54	2.51	0.04	0.95	0.39	2.55	1.91	2.79	3.00	4.65	4.01	ns
12 mA	Std.	0.63	2.64	0.05	1.12	0.45	2.68	1.99	3.53	3.94	5.14	4.45	ns
	-1	0.54	2.24	0.04	0.95	0.39	2.28	1.70	3.00	3.35	4.38	3.79	ns
16 mA	Std.	0.63	2.58	0.05	1.12	0.45	2.63	1.95	3.59	4.05	5.09	4.41	ns
	-1	0.54	2.20	0.04	0.95	0.39	2.24	1.66	3.05	3.44	4.33	3.75	ns
24 mA	Std.	0.63	2.61	0.05	1.12	0.45	2.66	1.89	3.66	4.46	5.12	4.35	ns
	-1	0.54	2.22	0.04	0.95	0.39	2.26	1.61	3.11	3.80	4.35	3.70	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-54 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard Plus I/O Banks for A3P1000 Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.63	5.64	0.05	1.10	0.45	5.74	4.78	2.50	2.43	8.20	7.24	ns
	-1	0.54	4.79	0.04	0.94	0.39	4.88	4.06	2.13	2.07	6.98	6.16	ns
6 mA	Std.	0.63	4.64	0.05	1.10	0.45	4.73	4.16	2.84	3.01	7.19	6.62	ns
	-1	0.54	3.95	0.04	0.94	0.39	4.02	3.54	2.42	2.56	6.11	5.63	ns
8 mA	Std.	0.63	4.64	0.05	1.10	0.45	4.73	4.16	2.84	3.01	7.19	6.62	ns
	-1	0.54	3.95	0.04	0.94	0.39	4.02	3.54	2.42	2.56	6.11	5.63	ns
12 mA	Std.	0.63	3.94	0.05	1.10	0.45	4.01	3.67	3.07	3.39	6.47	6.13	ns
	-1	0.54	3.35	0.04	0.94	0.39	3.41	3.12	2.61	2.88	5.51	5.21	ns
16 mA	Std.	0.63	3.94	0.05	1.10	0.45	4.01	3.67	3.07	3.39	6.47	6.13	ns
	-1	0.54	3.35	0.04	0.94	0.39	3.41	3.12	2.61	2.88	5.51	5.21	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

**Table 2-55 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard Plus I/O Banks for A3P1000 Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.63	3.07	0.05	1.10	0.45	3.13	2.46	2.50	2.57	5.59	4.91	ns
	-1	0.54	2.61	0.04	0.94	0.39	2.66	2.09	2.13	2.19	4.75	4.18	ns
6 mA	Std.	0.63	2.51	0.05	1.10	0.45	2.55	1.97	2.84	3.16	5.01	4.43	ns
	-1	0.54	2.13	0.04	0.94	0.39	2.17	1.67	2.41	2.69	4.26	3.76	ns
8 mA	Std.	0.63	2.51	0.05	1.10	0.45	2.55	1.97	2.84	3.16	5.01	4.43	ns
	-1	0.54	2.13	0.04	0.94	0.39	2.17	1.67	2.41	2.69	4.26	3.76	ns
12 mA	Std.	0.63	2.24	0.05	1.10	0.45	2.28	1.72	3.07	3.54	4.74	4.18	ns
	-1	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56	ns
16 mA	Std.	0.63	2.24	0.05	1.10	0.45	2.28	1.72	3.07	3.54	4.74	4.18	ns
	-1	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

## 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V-tolerant input buffer and push-pull output buffer.

**Table 2-56 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	15	15
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	15	15
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	15	15
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	15	15
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-57 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks for A3P1000 Only

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	15	15
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	15	15
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	15	15
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	15	15
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	15	15
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	15	15
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	15	15

**Notes:**

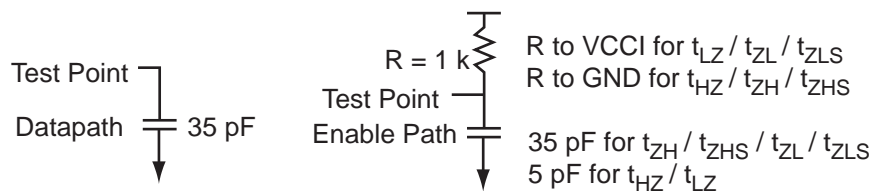
1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-58 • Minimum and Maximum DC Input and Output Levels**  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

2.5 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	15	15
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	15	15
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	15	15
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	15	15
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.



**Figure 2-9 • AC Loading**

**Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	2.5	1.2	5

\* Measuring point = V<sub>trip</sub>. See Table 2-27 on page 2-27 for a complete table of trip points.

## Timing Characteristics

### 1.2 V DC Core Voltage

**Table 2-60 • 2.5 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.61	6.86	0.04	2.04	2.54	0.40	6.99	5.83	2.69	2.17	9.20	8.04	ns
	-1	0.52	5.84	0.03	1.74	2.16	0.34	5.95	4.96	2.29	1.85	7.83	6.84	ns
8 mA	Std.	0.61	5.61	0.04	2.04	2.54	0.40	5.72	4.94	3.07	2.90	7.93	7.15	ns
	-1	0.52	4.77	0.03	1.74	2.16	0.34	4.86	4.20	2.61	2.47	6.75	6.08	ns
12 mA	Std.	0.61	4.72	0.04	2.04	2.54	0.40	4.81	4.30	3.33	3.36	7.02	6.51	ns
	-1	0.52	4.02	0.03	1.74	2.16	0.34	4.09	3.66	2.84	2.86	5.98	5.54	ns
16 mA	Std.	0.61	4.45	0.04	2.04	2.54	0.40	4.53	4.16	3.39	3.49	6.75	6.37	ns
	-1	0.52	3.79	0.03	1.74	2.16	0.34	3.86	3.54	2.88	2.97	5.74	5.42	ns
24 mA	Std.	0.61	4.33	0.04	2.04	2.54	0.40	4.41	4.18	3.46	3.96	6.63	6.39	ns
	-1	0.52	3.69	0.03	1.74	2.16	0.34	3.76	3.55	2.94	3.37	5.64	5.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-61 • 2.5 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.80	3.50	0.05	2.04	2.54	0.52	3.57	3.13	2.69	2.26	5.78	5.34	ns
	-1	0.68	2.98	0.05	1.74	2.16	0.44	3.03	2.66	2.29	1.93	4.92	4.54	ns
8 mA	Std.	0.80	2.87	0.05	2.04	2.54	0.52	2.92	2.41	3.07	3.00	5.13	4.62	ns
	-1	0.68	2.44	0.05	1.74	2.16	0.44	2.48	2.05	2.61	2.55	4.37	3.93	ns
12 mA	Std.	0.80	2.49	0.05	2.04	2.54	0.52	2.53	2.05	3.33	3.46	4.75	4.26	ns
	-1	0.68	2.12	0.05	1.74	2.16	0.44	2.16	1.74	2.84	2.94	4.04	3.63	ns
16 mA	Std.	0.80	2.42	0.05	2.04	2.54	0.52	2.47	1.99	3.39	3.59	4.68	4.20	ns
	-1	0.68	2.06	0.05	1.74	2.16	0.44	2.10	1.69	2.88	3.05	3.98	3.57	ns
24 mA	Std.	0.80	2.43	0.05	2.04	2.54	0.52	2.48	1.90	3.46	4.07	4.69	4.11	ns
	-1	0.68	2.07	0.05	1.74	2.16	0.44	2.11	1.61	2.94	3.46	3.99	3.50	ns

#### Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**1.5 V DC Core Voltage**
**Table 2-62 • 2.5 V LVCMOS Low Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 2.3\text{ V}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.61	6.86	0.04	2.04	2.54	0.40	6.99	5.83	2.69	2.17	9.20	8.04	ns
	-1	0.52	5.84	0.03	1.74	2.16	0.34	5.95	4.96	2.29	1.85	7.83	6.84	ns
8 mA	Std.	0.61	5.61	0.04	2.04	2.54	0.40	5.72	4.94	3.07	2.90	7.93	7.15	ns
	-1	0.52	4.77	0.03	1.74	2.16	0.34	4.86	4.20	2.61	2.47	6.75	6.08	ns
12 mA	Std.	0.61	4.72	0.04	2.04	2.54	0.40	4.81	4.30	3.33	3.36	7.02	6.51	ns
	-1	0.52	4.02	0.03	1.74	2.16	0.34	4.09	3.66	2.84	2.86	5.98	5.54	ns
16 mA	Std.	0.61	4.45	0.04	2.04	2.54	0.40	4.53	4.16	3.39	3.49	6.75	6.37	ns
	-1	0.52	3.79	0.03	1.74	2.16	0.34	3.86	3.54	2.88	2.97	5.74	5.42	ns
24 mA	Std.	0.61	4.33	0.04	2.04	2.54	0.40	4.41	4.18	3.46	3.96	6.63	6.39	ns
	-1	0.52	3.69	0.03	1.74	2.16	0.34	3.76	3.55	2.94	3.37	5.64	5.43	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-63 • 2.5 V LVCMOS High Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 2.3\text{ V}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.61	3.50	0.04	2.04	2.54	0.40	3.57	3.13	2.69	2.26	5.78	5.34	ns
	-1	0.52	2.98	0.03	1.74	2.16	0.34	3.03	2.66	2.29	1.93	4.92	4.54	ns
8 mA	Std.	0.61	2.87	0.04	2.04	2.54	0.40	2.92	2.41	3.07	3.00	5.13	4.62	ns
	-1	0.52	2.44	0.03	1.74	2.16	0.34	2.48	2.05	2.61	2.55	4.37	3.93	ns
12 mA	Std.	0.61	2.49	0.04	2.04	2.54	0.40	2.53	2.05	3.33	3.46	4.75	4.26	ns
	-1	0.52	2.12	0.03	1.74	2.16	0.34	2.16	1.74	2.84	2.94	4.04	3.63	ns
16 mA	Std.	0.61	2.42	0.04	2.04	2.54	0.40	2.47	1.99	3.39	3.59	4.68	4.20	ns
	-1	0.52	2.06	0.03	1.74	2.16	0.34	2.10	1.69	2.88	3.05	3.98	3.57	ns
24 mA	Std.	0.61	2.43	0.04	2.04	2.54	0.40	2.48	1.90	3.46	4.07	4.69	4.11	ns
	-1	0.52	2.07	0.03	1.74	2.16	0.34	2.11	1.61	2.94	3.46	3.99	3.50	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-64 • 2.5 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V  
 Applicable to Advanced I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.63	7.07	0.05	1.44	0.45	7.20	6.32	2.95	2.43	9.66	8.78	ns
	-1	0.54	6.02	0.04	1.23	0.39	6.13	5.38	2.51	2.06	8.22	7.47	ns
6 mA	Std.	0.63	5.91	0.05	1.44	0.45	6.02	5.42	3.35	3.18	8.48	7.88	ns
	-1	0.54	5.03	0.04	1.23	0.39	5.12	4.61	2.85	2.70	7.21	6.70	ns
8 mA	Std.	0.63	5.91	0.05	1.44	0.45	6.02	5.42	3.35	3.18	8.48	7.88	ns
	-1	0.54	5.03	0.04	1.23	0.39	5.12	4.61	2.85	2.70	7.21	6.70	ns
12 mA	Std.	0.63	5.05	0.05	1.44	0.45	5.15	4.79	3.63	3.66	7.61	7.25	ns
	-1	0.54	4.30	0.04	1.23	0.39	4.38	4.07	3.09	3.11	6.47	6.17	ns
16 mA	Std.	0.63	4.78	0.05	1.44	0.45	4.86	4.65	3.70	3.78	7.32	7.10	ns
	-1	0.54	4.06	0.04	1.23	0.39	4.14	3.95	3.14	3.22	6.23	6.04	ns
24 mA	Std.	0.63	4.71	0.05	1.44	0.45	4.73	4.71	3.78	4.26	7.19	7.17	ns
	-1	0.54	4.01	0.04	1.23	0.39	4.03	4.01	3.21	3.62	6.12	6.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-65 • 2.5 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V  
 Applicable to Advanced I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.63	3.63	0.05	1.44	0.45	3.70	3.34	2.94	2.53	6.16	5.80	ns
	-1	0.54	3.09	0.04	1.23	0.39	3.15	2.84	2.51	2.16	5.24	4.94	ns
6 mA	Std.	0.63	2.99	0.05	1.44	0.45	3.04	2.59	3.35	3.30	5.50	5.05	ns
	-1	0.54	2.54	0.04	1.23	0.39	2.59	2.20	2.85	2.81	4.68	4.30	ns
8 mA	Std.	0.63	2.99	0.05	1.44	0.45	3.04	2.59	3.35	3.30	5.50	5.05	ns
	-1	0.54	2.54	0.04	1.23	0.39	2.59	2.20	2.85	2.81	4.68	4.30	ns
12 mA	Std.	0.63	2.65	0.05	1.44	0.45	2.70	2.23	3.63	3.78	5.16	4.69	ns
	-1	0.54	2.26	0.04	1.23	0.39	2.30	1.89	3.09	3.22	4.39	3.99	ns
16 mA	Std.	0.63	2.59	0.05	1.44	0.45	2.64	2.16	3.70	3.90	5.10	4.62	ns
	-1	0.54	2.21	0.04	1.23	0.39	2.25	1.83	3.15	3.32	4.34	3.93	ns
24 mA	Std.	0.63	2.61	0.05	1.44	0.45	2.66	2.08	3.78	4.40	5.12	4.54	ns
	-1	0.54	2.22	0.04	1.23	0.39	2.26	1.77	3.22	3.74	4.35	3.87	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.



**Table 2-66 • 2.5 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.63	6.45	0.05	1.43	0.45	6.56	5.71	2.48	2.19	9.02	8.17	ns
	-1	0.54	5.48	0.04	1.21	0.39	5.58	4.86	2.11	1.86	7.68	6.95	ns
6 mA	Std.	0.63	5.28	0.05	1.43	0.45	5.38	4.92	2.85	2.88	7.84	7.38	ns
	-1	0.54	4.50	0.04	1.21	0.39	4.58	4.19	2.42	2.45	6.67	6.28	ns
8 mA	Std.	0.63	5.28	0.05	1.43	0.45	5.38	4.92	2.85	2.88	7.84	7.38	ns
	-1	0.54	4.50	0.04	1.21	0.39	4.58	4.19	2.42	2.45	6.67	6.28	ns
12 mA	Std.	0.63	4.48	0.05	1.43	0.45	4.56	4.35	3.11	3.31	7.02	6.81	ns
	-1	0.54	3.81	0.04	1.21	0.39	3.88	3.70	2.65	2.82	5.97	5.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-67 • 2.5 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
4 mA	Std.	0.63	3.18	0.05	1.43	0.45	3.23	2.92	2.48	2.28	5.69	5.38	ns
	-1	0.54	2.70	0.04	1.21	0.39	2.75	2.48	2.11	1.94	4.84	4.58	ns
6 mA	Std.	0.63	2.57	0.05	1.43	0.45	2.62	2.24	2.84	2.98	5.08	4.70	ns
	-1	0.54	2.19	0.04	1.21	0.39	2.23	1.90	2.42	2.54	4.32	4.00	ns
8 mA	Std.	0.63	2.57	0.05	1.43	0.45	2.62	2.24	2.84	2.98	5.08	4.70	ns
	-1	0.54	2.19	0.04	1.21	0.39	2.23	1.90	2.42	2.54	4.32	4.00	ns
12 mA	Std.	0.63	2.28	0.05	1.43	0.45	2.32	1.90	3.11	3.42	4.78	4.36	ns
	-1	0.54	1.94	0.04	1.21	0.39	1.97	1.62	2.64	2.91	4.07	3.71	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

### 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

**Table 2-68 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	2	2	9	11	15	15
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	4	4	17	22	15	15
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	6	6	35	44	15	15
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8	45	51	15	15
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	12	12	91	74	15	15
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	16	16	91	74	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-69 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks for A3P1000 Only

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	2	2	9	11	15	15
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	4	4	17	22	15	15
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	6	6	35	44	15	15
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8	45	51	15	15
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	12	12	91	74	15	15
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	16	16	91	74	15	15

**Notes:**

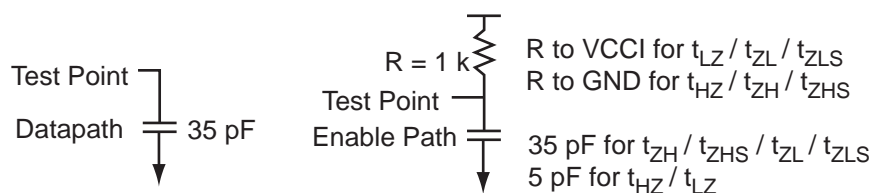
1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-70 • Minimum and Maximum DC Input and Output Levels**  
 Applicable to Standard Plus I/O I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	2	2	9	11	15	15
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	4	4	17	22	15	15
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	6	6	35	44	15	15
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8	35	44	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.


**Figure 2-10 • AC Loading**
**Table 2-71 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.8	0.9	5

\* Measuring point = V<sub>trip</sub>. See Table 2-27 on page 2-27 for a complete table of trip points.

## Timing Characteristics

### 1.2 V DC Core Voltage

**Table 2-72 • 1.8 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	0.80	9.15	0.05	1.98	2.80	0.52	9.32	7.69	2.75	1.57	11.54	9.90	ns
	-1	0.68	7.79	0.05	1.69	2.38	0.44	7.93	6.54	2.34	1.33	9.81	8.42	ns
4 mA	Std.	0.80	7.54	0.05	1.98	2.80	0.52	7.68	6.48	3.22	2.74	9.89	8.69	ns
	-1	0.68	6.41	0.05	1.69	2.38	0.44	6.53	5.51	2.74	2.33	8.42	7.39	ns
6 mA	Std.	0.80	6.39	0.05	1.98	2.80	0.52	6.51	5.65	3.53	3.32	8.72	7.86	ns
	-1	0.68	5.44	0.05	1.69	2.38	0.44	5.54	4.80	3.00	2.83	7.42	6.69	ns
8 mA	Std.	0.80	6.01	0.05	1.98	2.80	0.52	6.12	5.48	3.60	3.49	8.33	7.70	ns
	-1	0.68	5.11	0.05	1.69	2.38	0.44	5.20	4.66	3.07	2.97	7.09	6.55	ns
12 mA	Std.	0.80	5.89	0.05	1.98	2.80	0.52	6.00	5.49	3.70	4.07	8.22	7.71	ns
	-1	0.68	5.01	0.05	1.69	2.38	0.44	5.11	4.67	3.15	3.46	6.99	6.56	ns
16 mA	Std.	0.80	5.89	0.05	1.98	2.80	0.52	6.00	5.49	3.70	4.07	8.22	7.71	ns
	-1	0.68	5.01	0.05	1.69	2.38	0.44	5.11	4.67	3.15	3.46	6.99	6.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-73 • 1.8 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	0.80	4.14	0.05	1.98	2.80	0.52	4.21	4.05	2.75	1.62	6.43	6.27	ns
	-1	0.68	3.52	0.05	1.69	2.38	0.44	3.58	3.45	2.34	1.38	5.47	5.33	ns
4 mA	Std.	0.80	3.35	0.05	1.98	2.80	0.52	3.42	3.01	3.22	2.84	5.63	5.22	ns
	-1	0.68	2.85	0.05	1.69	2.38	0.44	2.91	2.56	2.74	2.41	4.79	4.44	ns
6 mA	Std.	0.80	2.87	0.05	1.98	2.80	0.52	2.93	2.49	3.53	3.43	5.14	4.71	ns
	-1	0.68	2.44	0.05	1.69	2.38	0.44	2.49	2.12	3.00	2.92	4.37	4.00	ns
8 mA	Std.	0.80	2.78	0.05	1.98	2.80	0.52	2.83	2.40	3.60	3.59	5.05	4.61	ns
	-1	0.68	2.37	0.05	1.69	2.38	0.44	2.41	2.04	3.06	3.05	4.29	3.92	ns
12 mA	Std.	0.80	2.77	0.05	1.98	2.80	0.52	2.82	2.28	3.70	4.19	5.03	4.49	ns
	-1	0.68	2.36	0.05	1.69	2.38	0.44	2.40	1.94	3.14	3.57	4.28	3.82	ns
16 mA	Std.	0.80	2.77	0.05	1.98	2.80	0.52	2.82	2.28	3.70	4.19	5.03	4.49	ns
	-1	0.68	2.36	0.05	1.69	2.38	0.44	2.40	1.94	3.14	3.57	4.28	3.82	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## 1.5 V DC Core Voltage

**Table 2-74 • 1.8 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 1.7\text{ V}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.61	9.15	0.04	1.98	2.80	0.40	9.32	7.69	2.75	1.57	11.54	9.90	ns
	-1	0.52	7.79	0.03	1.69	2.38	0.34	7.93	6.54	2.34	1.33	9.81	8.42	ns
4 mA	Std.	0.61	7.54	0.04	1.98	2.80	0.40	7.68	6.48	3.22	2.74	9.89	8.69	ns
	-1	0.52	6.41	0.03	1.69	2.38	0.34	6.53	5.51	2.74	2.33	8.42	7.39	ns
6 mA	Std.	0.61	6.39	0.04	1.98	2.80	0.40	6.51	5.65	3.53	3.32	8.72	7.86	ns
	-1	0.52	5.44	0.03	1.69	2.38	0.34	5.54	4.80	3.00	2.83	7.42	6.69	ns
8 mA	Std.	0.61	6.01	0.04	1.98	2.80	0.40	6.12	5.48	3.60	3.49	8.33	7.70	ns
	-1	0.52	5.11	0.03	1.69	2.38	0.34	5.20	4.66	3.07	2.97	7.09	6.55	ns
12 mA	Std.	0.61	5.89	0.04	1.98	2.80	0.40	6.00	5.49	3.70	4.07	8.22	7.71	ns
	-1	0.52	5.01	0.03	1.69	2.38	0.34	5.11	4.67	3.15	3.46	6.99	6.56	ns
16 mA	Std.	0.61	5.89	0.04	1.98	2.80	0.40	6.00	5.49	3.70	4.07	8.22	7.71	ns
	-1	0.52	5.01	0.03	1.69	2.38	0.34	5.11	4.67	3.15	3.46	6.99	6.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-75 • 1.8 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 1.7\text{ V}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.61	4.14	0.04	1.98	2.80	0.40	4.21	4.05	2.75	1.62	6.43	6.27	ns
	-1	0.52	3.52	0.03	1.69	2.38	0.34	3.58	3.45	2.34	1.38	5.47	5.33	ns
4 mA	Std.	0.61	3.35	0.04	1.98	2.80	0.40	3.42	3.01	3.22	2.84	5.63	5.22	ns
	-1	0.52	2.85	0.03	1.69	2.38	0.34	2.91	2.56	2.74	2.41	4.79	4.44	ns
6 mA	Std.	0.61	2.87	0.04	1.98	2.80	0.40	2.93	2.49	3.53	3.43	5.14	4.71	ns
	-1	0.52	2.44	0.03	1.69	2.38	0.34	2.49	2.12	3.00	2.92	4.37	4.00	ns
8 mA	Std.	0.61	2.78	0.04	1.98	2.80	0.40	2.83	2.40	3.60	3.59	5.05	4.61	ns
	-1	0.52	2.37	0.03	1.69	2.38	0.34	2.41	2.04	3.06	3.05	4.29	3.92	ns
12 mA	Std.	0.61	2.77	0.04	1.98	2.80	0.40	2.82	2.28	3.70	4.19	5.03	4.49	ns
	-1	0.52	2.36	0.03	1.69	2.38	0.34	2.40	1.94	3.14	3.57	4.28	3.82	ns
16 mA	Std.	0.61	2.77	0.04	1.98	2.80	0.40	2.82	2.28	3.70	4.19	5.03	4.49	ns
	-1	0.52	2.36	0.03	1.69	2.38	0.34	2.40	1.94	3.14	3.57	4.28	3.82	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-76 • 1.8 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
 Applicable to Advanced I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.63	9.50	0.05	1.44	0.45	9.68	8.31	3.06	1.76	12.14	10.77	ns
	-1	0.54	8.08	0.04	1.23	0.39	8.23	7.07	2.60	1.50	10.32	9.16	ns
4 mA	Std.	0.63	7.80	0.05	1.44	0.45	7.95	7.06	3.55	3.01	10.41	9.52	ns
	-1	0.54	6.64	0.04	1.23	0.39	6.76	6.00	3.02	2.56	8.85	8.10	ns
6 mA	Std.	0.63	6.70	0.05	1.44	0.45	6.82	6.25	3.89	3.60	9.28	8.70	ns
	-1	0.54	5.70	0.04	1.23	0.39	5.80	5.31	3.31	3.06	7.90	7.40	ns
8 mA	Std.	0.63	6.31	0.05	1.44	0.45	6.43	6.07	3.97	3.75	8.89	8.53	ns
	-1	0.54	5.37	0.04	1.23	0.39	5.47	5.17	3.37	3.19	7.56	7.26	ns
12 mA	Std.	0.63	6.18	0.05	1.44	0.45	6.30	6.15	4.08	4.34	8.76	8.61	ns
	-1	0.54	5.26	0.04	1.23	0.39	5.36	5.23	3.47	3.70	7.45	7.32	ns
16 mA	Std.	0.63	6.18	0.05	1.44	0.45	6.30	6.15	4.08	4.34	8.76	8.61	ns
	-1	0.54	5.26	0.04	1.23	0.39	5.36	5.23	3.47	3.70	7.45	7.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-77 • 1.8 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
 Applicable to Advanced I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.63	4.40	0.05	1.34	0.45	4.48	4.30	3.05	1.82	6.94	6.76	ns
	-1	0.54	3.74	0.04	1.14	0.39	3.81	3.66	2.59	1.55	5.90	5.75	ns
4 mA	Std.	0.63	3.44	0.05	1.34	0.45	3.50	3.23	3.54	3.12	5.96	5.69	ns
	-1	0.54	2.92	0.04	1.14	0.39	2.98	2.75	3.01	2.66	5.07	4.84	ns
6 mA	Std.	0.63	3.02	0.05	1.34	0.45	3.07	2.70	3.88	3.72	5.53	5.16	ns
	-1	0.54	2.57	0.04	1.14	0.39	2.61	2.30	3.30	3.16	4.71	4.39	ns
8 mA	Std.	0.63	2.94	0.05	1.34	0.45	2.99	2.60	3.96	3.87	5.45	5.06	ns
	-1	0.54	2.50	0.04	1.14	0.39	2.54	2.21	3.37	3.30	4.64	4.31	ns
12 mA	Std.	0.63	2.93	0.05	1.34	0.45	2.98	2.49	4.07	4.49	5.44	4.95	ns
	-1	0.54	2.49	0.04	1.14	0.39	2.54	2.12	3.46	3.82	4.63	4.21	ns
16 mA	Std.	0.63	2.93	0.05	1.34	0.45	2.98	2.49	4.07	4.49	5.44	4.95	ns
	-1	0.54	2.49	0.04	1.14	0.39	2.54	2.12	3.46	3.82	4.63	4.21	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-78 • 1.8 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7V  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.63	8.81	0.05	1.43	0.45	8.98	7.51	2.48	1.61	11.44	9.97	ns
	-1	0.54	7.50	0.04	1.21	0.39	7.64	6.39	2.11	1.37	9.73	8.48	ns
4 mA	Std.	0.63	7.10	0.05	1.43	0.45	7.23	6.43	2.92	2.75	9.69	8.89	ns
	-1	0.54	6.04	0.04	1.21	0.39	6.15	5.47	2.48	2.34	8.24	7.56	ns
6 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	-1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns
8 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	-1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-79 • 1.8 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.63	3.94	0.05	1.32	0.45	4.01	3.72	2.47	1.67	6.47	6.18	ns
	-1	0.54	3.35	0.04	1.12	0.39	3.41	3.16	2.10	1.42	5.51	5.26	ns
4 mA	Std.	0.63	3.03	0.05	1.32	0.45	3.09	2.75	2.91	2.86	5.55	5.21	ns
	-1	0.54	2.58	0.04	1.12	0.39	2.63	2.34	2.48	2.44	4.72	4.43	ns
6 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	-1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns
8 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	-1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**Table 2-80 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	2	2	13	16	15	15
4 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	4	4	25	33	15	15
6 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	6	6	32	39	15	15
8 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	8	8	66	55	15	15
12 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	12	12	66	55	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

**Table 2-81 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks for A3P1000 Only

1.5 V LVCMOS	VIL		VIH		V <sub>OL</sub>	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	2	2	13	16	15	15
4 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	4	4	25	33	15	15
6 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	6	6	32	39	15	15
8 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	8	8	66	55	15	15
12 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	12	12	66	55	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

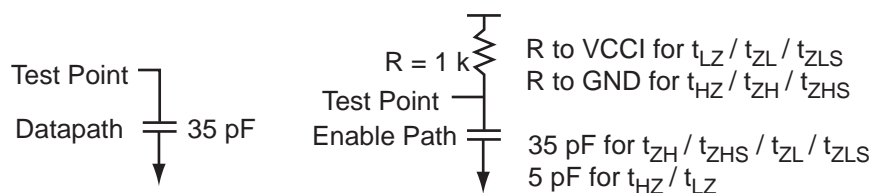


**Table 2-82 • Minimum and Maximum DC Input and Output Levels**  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

1.5 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
2 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	2	2	13	16	15	15
4 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.575	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	4	4	25	33	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.



**Figure 2-11 • AC Loading**

**Table 2-83 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.5	0.75	5

\* Measuring point = V<sub>trip</sub>. See Table 2-27 on page 2-27 for a complete table of trip points.

## Timing Characteristics

### 1.2 V DC Core Voltage

**Table 2-84 • 1.5 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.80	9.52	0.05	2.19	3.05	0.52	9.69	7.89	3.37	2.65	11.91	10.10	ns
	-1	0.68	8.10	0.05	1.86	2.59	0.44	8.25	6.71	2.87	2.26	10.13	8.59	ns
4 mA	Std.	0.80	8.14	0.05	2.19	3.05	0.52	8.29	6.89	3.73	3.32	10.50	9.10	ns
	-1	0.68	6.92	0.05	1.86	2.59	0.44	7.05	5.86	3.17	2.83	8.93	7.74	ns
6 mA	Std.	0.80	7.64	0.05	2.19	3.05	0.52	7.78	6.70	3.80	3.51	9.99	8.92	ns
	-1	0.68	6.50	0.05	1.86	2.59	0.44	6.62	5.70	3.24	2.99	8.50	7.59	ns
8 mA	Std.	0.80	7.54	0.05	2.19	3.05	0.52	7.68	6.71	3.93	4.18	9.89	8.92	ns
	-1	0.68	6.41	0.05	1.86	2.59	0.44	6.53	5.71	3.34	3.55	8.41	7.59	ns
12 mA	Std.	0.80	7.54	0.05	2.19	3.05	0.52	7.68	6.71	3.93	4.18	9.89	8.92	ns
	-1	0.68	6.41	0.05	1.86	2.59	0.44	6.53	5.71	3.34	3.55	8.41	7.59	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-85 • 1.5 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.80	3.91	0.05	2.19	3.05	0.52	3.98	3.54	3.36	2.76	6.19	5.76	ns
	-1	0.68	3.32	0.05	1.86	2.59	0.44	3.38	3.01	2.86	2.35	5.27	4.90	ns
4 mA	Std.	0.80	3.33	0.05	2.19	3.05	0.52	3.39	2.90	3.71	3.44	5.61	5.12	ns
	-1	0.68	2.83	0.05	1.86	2.59	0.44	2.89	2.47	3.16	2.93	4.77	4.35	ns
6 mA	Std.	0.80	3.22	0.05	2.19	3.05	0.52	3.28	2.78	3.80	3.63	5.49	5.00	ns
	-1	0.68	2.74	0.05	1.86	2.59	0.44	2.79	2.37	3.23	3.09	4.67	4.25	ns
8 mA	Std.	0.80	3.18	0.05	2.19	3.05	0.52	3.24	2.63	3.92	4.33	5.46	4.85	ns
	-1	0.68	2.71	0.05	1.86	2.59	0.44	2.76	2.24	3.34	3.68	4.64	4.12	ns
12 mA	Std.	0.80	3.18	0.05	2.19	3.05	0.52	3.24	2.63	3.92	4.33	5.46	4.85	ns
	-1	0.68	2.71	0.05	1.86	2.59	0.44	2.76	2.24	3.34	3.68	4.64	4.12	ns

#### Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**1.5 V DC Core Voltage**
**Table 2-86 • 1.5 V LVCMOS Low Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 1.4\text{ V}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.61	9.52	0.04	2.19	3.05	0.40	9.69	7.89	3.37	2.65	11.91	10.10	ns
	-1	0.52	8.10	0.03	1.86	2.59	0.34	8.25	6.71	2.87	2.26	10.13	8.59	ns
4 mA	Std.	0.61	8.14	0.04	2.19	3.05	0.40	8.29	6.89	3.73	3.32	10.50	9.10	ns
	-1	0.52	6.92	0.03	1.86	2.59	0.34	7.05	5.86	3.17	2.83	8.93	7.74	ns
6 mA	Std.	0.61	7.64	0.04	2.19	3.05	0.40	7.78	6.70	3.80	3.51	9.99	8.92	ns
	-1	0.52	6.50	0.03	1.86	2.59	0.34	6.62	5.70	3.24	2.99	8.50	7.59	ns
8 mA	Std.	0.61	7.54	0.04	2.19	3.05	0.40	7.68	6.71	3.93	4.18	9.89	8.92	ns
	-1	0.52	6.41	0.03	1.86	2.59	0.34	6.53	5.71	3.34	3.55	8.41	7.59	ns
12 mA	Std.	0.61	7.54	0.04	2.19	3.05	0.40	7.68	6.71	3.93	4.18	9.89	8.92	ns
	-1	0.52	6.41	0.03	1.86	2.59	0.34	6.53	5.71	3.34	3.55	8.41	7.59	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-87 • 1.5 V LVCMOS High Slew**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 1.4\text{ V}$   
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{PYS}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.61	3.91	0.04	2.19	3.05	0.40	3.98	3.54	3.36	2.76	6.19	5.76	ns
	-1	0.52	3.32	0.03	1.86	2.59	0.34	3.38	3.01	2.86	2.35	5.27	4.90	ns
4 mA	Std.	0.61	3.33	0.04	2.19	3.05	0.40	3.39	2.90	3.71	3.44	5.61	5.12	ns
	-1	0.52	2.83	0.03	1.86	2.59	0.34	2.89	2.47	3.16	2.93	4.77	4.35	ns
6 mA	Std.	0.61	3.22	0.04	2.19	3.05	0.40	3.28	2.78	3.80	3.63	5.49	5.00	ns
	-1	0.52	2.74	0.03	1.86	2.59	0.34	2.79	2.37	3.23	3.09	4.67	4.25	ns
8 mA	Std.	0.61	3.18	0.04	2.19	3.05	0.40	3.24	2.63	3.92	4.33	5.46	4.85	ns
	-1	0.52	2.71	0.03	1.86	2.59	0.34	2.76	2.24	3.34	3.68	4.64	4.12	ns
12 mA	Std.	0.61	3.18	0.04	2.19	3.05	0.40	3.24	2.63	3.92	4.33	5.46	4.85	ns
	-1	0.52	2.71	0.03	1.86	2.59	0.34	2.76	2.24	3.34	3.68	4.64	4.12	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-88 • 1.5 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V  
 Applicable to Advanced I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.63	9.78	0.05	1.44	0.45	9.96	8.57	3.74	2.91	12.42	11.03	ns
	-1	0.54	8.32	0.04	1.23	0.39	8.47	7.29	3.18	2.47	10.56	9.38	ns
4 mA	Std.	0.63	8.44	0.05	1.44	0.45	8.60	7.59	4.12	3.60	11.06	10.05	ns
	-1	0.54	7.18	0.04	1.23	0.39	7.32	6.46	3.51	3.06	9.41	8.55	ns
6 mA	Std.	0.63	7.95	0.05	1.44	0.45	8.10	7.39	4.21	3.78	10.56	9.85	ns
	-1	0.54	6.77	0.04	1.23	0.39	6.89	6.29	3.58	3.21	8.98	8.38	ns
8 mA	Std.	0.63	7.84	0.05	1.44	0.45	7.98	7.47	4.35	4.45	10.44	9.92	ns
	-1	0.54	6.67	0.04	1.23	0.39	6.79	6.35	3.70	3.79	8.88	8.44	ns
12 mA	Std.	0.63	7.84	0.05	1.44	0.45	7.98	7.47	4.35	4.45	10.44	9.92	ns
	-1	0.54	6.67	0.04	1.23	0.39	6.79	6.35	3.70	3.79	8.88	8.44	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-89 • 1.5 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V  
 Applicable to Advanced I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.63	3.98	0.05	1.58	0.45	4.06	3.80	3.73	3.04	6.52	6.26	ns
	-1	0.54	3.39	0.04	1.35	0.39	3.45	3.23	3.17	2.59	5.54	5.32	ns
4 mA	Std.	0.63	3.47	0.05	1.58	0.45	3.53	3.15	4.11	3.74	5.99	5.61	ns
	-1	0.54	2.95	0.04	1.35	0.39	3.01	2.68	3.50	3.18	5.10	4.77	ns
6 mA	Std.	0.63	3.37	0.05	1.58	0.45	3.43	3.02	4.20	3.92	5.89	5.48	ns
	-1	0.54	2.87	0.04	1.35	0.39	2.92	2.57	3.57	3.33	5.01	4.66	ns
8 mA	Std.	0.63	3.35	0.05	1.58	0.45	3.41	2.88	4.34	4.62	5.87	5.34	ns
	-1	0.54	2.85	0.04	1.35	0.39	2.90	2.45	3.69	3.93	4.99	4.55	ns
12 mA	Std.	0.63	3.35	0.05	1.58	0.45	3.41	2.88	4.34	4.62	5.87	5.34	ns
	-1	0.54	2.85	0.04	1.35	0.39	2.90	2.45	3.69	3.93	4.99	4.55	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-90 • 1.5 V LVCMOS Low Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.63	8.94	0.05	1.43	0.45	9.11	7.80	2.99	2.67	11.57	10.26	ns
	-1	0.54	7.61	0.04	1.21	0.39	7.75	6.64	2.54	2.27	9.84	8.73	ns
4 mA	Std.	0.63	7.68	0.05	1.43	0.45	7.83	6.91	3.34	3.30	10.29	9.37	ns
	-1	0.54	6.54	0.04	1.21	0.39	6.66	5.88	2.84	2.80	8.75	7.97	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

**Table 2-91 • 1.5 V LVCMOS High Slew**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.63	3.55	0.05	1.56	0.45	3.61	3.22	2.98	2.80	6.07	5.68	ns
	-1	0.54	3.02	0.04	1.33	0.39	3.07	2.74	2.54	2.39	5.16	4.83	ns
4 mA	Std.	0.63	3.09	0.05	1.56	0.45	3.14	2.62	3.34	3.44	5.60	5.08	ns
	-1	0.54	2.62	0.04	1.33	0.39	2.67	2.23	2.84	2.93	4.77	4.32	ns

*Notes:*

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

## 1.2 V LVCMOS (JESD8-12A)

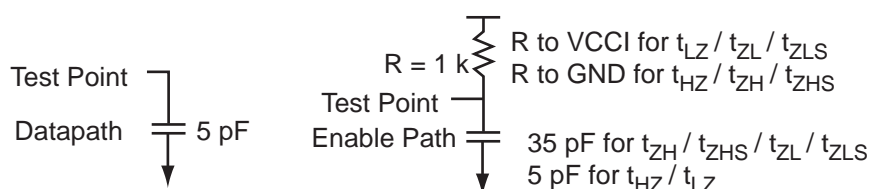
Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

**Table 2-92 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Operating at 1.2 V Core Voltage

1.2 V LVCMOS	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSH</sub> <sup>1</sup>	I <sub>OSL</sub> <sup>1</sup>	I <sub>IL</sub> <sup>2</sup>	I <sub>IH</sub> <sup>2</sup>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA	Max. mA	μA	μA
2 mA	-0.3	0.35 * V <sub>CCI</sub>	0.65 * V <sub>CCI</sub>	1.26	0.25 * V <sub>CCI</sub>	0.75 * V <sub>CCI</sub>	2	2	TBD	TBD	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.



**Figure 2-12 • AC Loading**

**Table 2-93 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.2	0.6	5

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

#### 1.2 V DC Core Voltage

**Table 2-94 • 1.2 V LVCMOS Low Slew**

Military-Case Conditions:  $T_j = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Unit
2 mA	Std.	0.80	12.62	0.05	2.62	3.76	0.52	12.07	9.47	5.12	4.68	14.20	11.60	ns
	-1	0.68	10.73	0.05	2.23	3.20	0.44	10.27	8.05	4.36	3.98	12.08	9.87	ns

**Note:** For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-95 • 1.2 V LVCMOS High Slew**

Military-Case Conditions:  $T_j = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V  
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Unit
2 mA	Std.	0.80	5.17	0.05	2.62	3.76	0.52	4.95	4.36	5.11	4.83	7.08	6.49	ns
	-1	0.68	4.40	0.05	2.23	3.20	0.44	4.21	3.71	4.35	4.11	6.02	5.52	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

### 3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

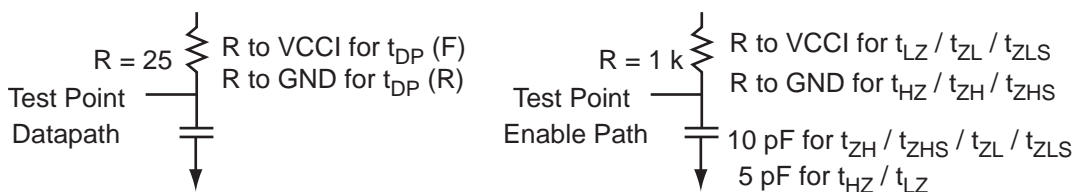
**Table 2-96 • Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
Per PCI specification	Per PCI curves										15	15

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the database; Actel loadings for enable path characterization are described in [Figure 2-13](#).



**Figure 2-13 • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in [Table 2-97](#).

**Table 2-97 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$	10

\* Measuring point =  $V_{trip}$ . See [Table 2-27](#) on page 2-27 for a complete table of trip points.

## Timing Characteristics

### 1.2 V DC Core Voltage

**Table 2-98 • 3.3 V PCI/PCI-X**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.78	0.05	2.72	3.67	0.52	2.83	1.98	3.24	3.58	5.04	4.19	ns
-1	0.68	2.36	0.05	2.31	3.12	0.44	2.41	1.68	2.76	3.04	4.29	3.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

### 1.5 V DC Core Voltage

**Table 2-99 • 3.3 V PCI/PCI-X**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.78	0.04	2.72	3.67	0.40	2.83	1.98	3.24	3.58	5.04	4.19	ns
-1	0.52	2.36	0.03	2.31	3.12	0.34	2.41	1.68	2.76	3.04	4.29	3.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-100 • 3.3 V PCI/PCI-X**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Advanced I/O Banks for A3P1000 Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.63	2.95	0.05	0.95	0.45	2.81	1.98	3.53	3.94	5.46	4.61	0.63	ns
-1	0.54	2.51	0.04	0.81	0.39	2.39	1.68	3.00	3.35	4.65	3.92	0.54	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

**Table 2-101 • 3.3 V PCI/PCI-X**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Standard Plus I/O Banks for A3P1000 Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>PYS</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.63	2.54	0.05	0.94	0.45	2.39	1.71	3.07	3.54	5.04	4.33	0.63	ns
-1	0.54	2.16	0.04	0.80	0.39	2.03	1.45	2.61	3.01	4.29	3.69	0.54	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.



## Voltage-Referenced I/O Characteristics

### 3.3 V GTL

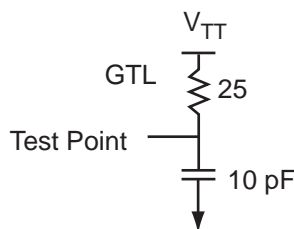
Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The  $V_{CCI}$  pin should be connected to 3.3 V.

**Table 2-102 • Minimum and Maximum DC Input and Output Levels**

3.3 V GTL Drive Strength	VIL		VIH		VOL	VOH	IOL	IOH	IosL	IosH	IIL	IiH
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
25 mA <sup>3</sup>	-0.3	VREF - 0.05	VREF + 0.05	3.6	0.4	-	25	25	268	181	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Output drive strength is below JEDEC specification.



**Figure 2-14 • AC Loading**

**Table 2-103 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.05	VREF + 0.05	0.8	0.8	1.2	10

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

**Table 2-104 • 3.3 V GTL**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V,  
Worst-Case VCCI = 3.0 V, VREF = 0.8 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.05	0.05	2.33	0.52	2.02	2.05			4.23	4.27	ns
-1	0.68	1.75	0.05	1.98	0.44	1.72	1.75			3.60	3.63	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-105 • 3.3 V GTL**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V,  
Worst-Case VCCI = 3.0 V, VREF = 0.8 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.05	0.04	2.33	0.40	2.02	2.05			4.23	4.27	ns
-1	0.52	1.75	0.03	1.98	0.34	1.72	1.75			3.60	3.63	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## 2.5 V GTL

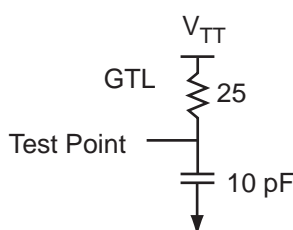
Gunning Transceiver Logic is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The  $V_{CCI}$  pin should be connected to 2.5 V.

**Table 2-106 • Minimum and Maximum DC Input and Output Levels**

2.5 GTL	VIL		VIH		VOL	VOH	IO <sub>L</sub>	IO <sub>H</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
25 mA <sup>3</sup>	-0.3	VREF - 0.05	VREF + 0.05	2.7	0.4	-	25	25	169	124	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Output drive strength is below JEDEC specification.



**Figure 2-15 • AC Loading**

**Table 2-107 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	V <sub>TT</sub> (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.05	VREF + 0.05	0.8	0.8	1.2	10

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

**Table 2-108 • 2.5 V GTL**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V,  
Worst-Case VCCI = 3.0 V, VREF = 0.8 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.11	0.05	2.26	0.52	2.14	2.11			4.35	4.32	ns
-1	0.68	1.79	0.05	1.92	0.44	1.82	1.79			3.70	3.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-109 • 2.5 V GTL**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V,  
Worst-Case VCCI = 3.0 V, VREF = 0.8 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.11	0.04	2.26	0.40	2.14	2.11			4.35	4.32	ns
-1	0.52	1.79	0.03	1.92	0.34	1.82	1.79			3.70	3.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

### 3.3 V GTL+

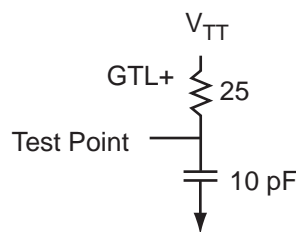
Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

**Table 2-110 • Minimum and Maximum DC Input and Output Levels**

3.3 V GTL+	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
35 mA	-0.3	VREF - 0.1	VREF + 0.1	3.6	0.6	-	35	35	268	181	15	15

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.



**Figure 2-16 • AC Loading**

**Table 2-111 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.1	VREF + 0.1	1.0	1.0	1.5	10

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

**Table 2-112 • 3.3 V GTL+**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V,  
Worst-Case VCCI = 3.0 V, VREF = 1.0 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.03	0.05	2.33	0.52	2.07	2.03			4.29	4.25	ns
-1	0.68	1.73	0.05	1.98	0.44	1.76	1.73			3.65	3.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-113 • 3.3 V GTL+**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V,  
Worst-Case VCCI = 3.0 V, VREF = 1.0 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.03	0.04	2.33	0.40	2.07	2.03			4.29	4.25	ns
-1	0.52	1.73	0.03	1.98	0.34	1.76	1.73			3.65	3.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## 2.5 V GTL+

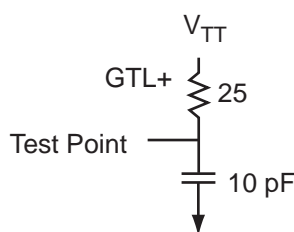
Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The  $V_{CCI}$  pin should be connected to 2.5 V.

**Table 2-114 • Minimum and Maximum DC Input and Output Levels**

2.5 V GTL+	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>oSL</sub>	I <sub>oSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
33 mA	-0.3	VREF - 0.1	VREF + 0.1	2.7	0.6	-	33	33	169	124	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.



**Figure 2-17 • AC Loading**

**Table 2-115 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.1	VREF + 0.1	1.0	1.0	1.5	10

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

**Table 2-116 • 2.5 V GTL+**

**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V**  
**Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.18	0.05	2.26	0.52	2.22	2.08			4.44	4.29	ns
-1	0.68	1.86	0.05	1.92	0.44	1.89	1.77			3.78	3.65	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-117 • 2.5 V GTL+**

**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.0 V**  
**Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.18	0.04	2.26	0.40	2.22	2.08			4.44	4.29	ns
-1	0.52	1.86	0.03	1.92	0.34	1.89	1.77			3.78	3.65	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## HSTL Class I

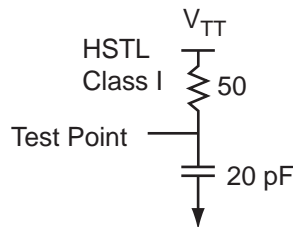
High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Military ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-118 • Minimum and Maximum DC Input and Output Levels**

HSTL Class I	VIL		VIH		VOL	VOH	IOL	IOH	IosL	IosH	IIL	IiH
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
8 mA	-0.3	VREF - 0.1	VREF + 0.1	1.575	0.4	VCCI - 0.4 T	8	8	32	39	15	15

Notes:

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.



**Figure 2-18 • AC Loading**

**Table 2-119 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.1	VREF + 0.1	0.75	0.75	0.75	20

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

## Timing Characteristics

**Table 2-120 • HSTL Class I**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V,  
Worst-Case VCCI = 1.4 V, VREF = 0.75 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	3.15	0.05	2.75	0.52	3.21	3.11			5.42	5.33	ns
-1	0.68	2.68	0.05	2.34	0.44	2.73	2.65			4.61	4.53	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-121 • HSTL Class I**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V,  
Worst-Case VCCI = 1.4 V, VREF = 0.75 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	3.15	0.04	2.75	0.40	3.21	3.11			5.42	5.33	ns
-1	0.52	2.68	0.03	2.34	0.34	2.73	2.65			4.61	4.53	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## HSTL Class II

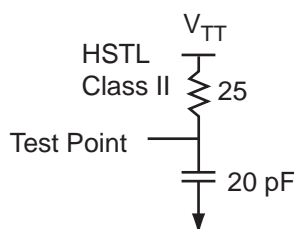
High-Speed Transceiver Logic is a general-purpose high-speed 1.5 V bus standard (EIA/JESD8-6). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-122 • Minimum and Maximum DC Input and Output Levels**

HSTL Class II	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
15 mA <sup>3</sup>	-0.3	VREF - 0.1	VREF + 0.1	1.575	0.4	VCCI - 0.4	15	15	66	55	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Output drive strength is below JEDEC specification.



**Figure 2-19 • AC Loading**

**Table 2-123 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
V <sub>REF</sub> - 0.1	V <sub>REF</sub> + 0.1	0.75	0.75	0.75	20

\* Measuring point = V<sub>trip</sub>. See Table 2-27 on page 2-27 for a complete table of trip points.

## Timing Characteristics

**Table 2-124 • HSTL Class II**

Military-Case Conditions: T<sub>J</sub> = 125°C, Worst-Case VCC = 1.14 V,  
Worst-Case VCCI = 1.4 V, VREF = 0.75 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.99	0.05	2.75	0.52	3.05	2.69			5.26	4.90	ns
-1	0.68	2.55	0.05	2.34	0.44	2.59	2.29			4.48	4.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-125 • HSTL Class II**

Military-Case Conditions: T<sub>J</sub> = 125°C, VCC = 1.425 V,  
Worst-Case VCCI = 1.4 V, VREF = 0.75 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.99	0.04	2.75	0.40	3.05	2.69			5.26	4.90	ns
-1	0.52	2.55	0.03	2.34	0.34	2.59	2.29			4.48	4.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## SSTL2 Class I

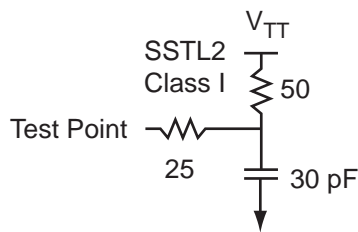
Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Military ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-126 • Minimum and Maximum DC Input and Output Levels**

SSTL2 Class I	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
15 mA	-0.3	VREF - 0.2	VREF + 0.2	2.7	0.54	VCCI - 0.62	15	15	83	87	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.



**Figure 2-20 • AC Loading**

**Table 2-127 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.2	VREF + 0.2	1.25	1.25	1.25	30

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

**Table 2-128 • SSTL2 Class I**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V,  
Worst-Case VCCI = 2.3 V, VREF = 1.25 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.11	0.05	2.08	0.52	2.14	1.83			2.14	1.83	ns
-1	0.68	1.79	0.05	1.77	0.44	1.82	1.56			1.82	1.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-129 • SSTL2 Class I**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , V<sub>CC</sub> = 1.425 V,  
Worst-Case VCCI = 2.3 V, VREF = 1.25 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.11	0.04	2.08	0.40	2.14	1.83			2.14	1.83	ns
-1	0.52	1.79	0.03	1.77	0.34	1.82	1.56			1.82	1.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## SSTL2 Class II

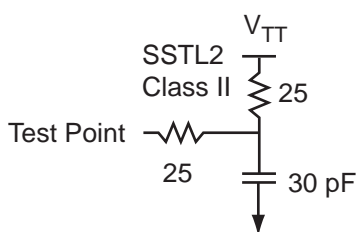
Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-130 • Minimum and Maximum DC Input and Output Levels**

SSTL2 Class II	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>oSL</sub>	I <sub>oSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
18 mA	-0.3	VREF - 0.2	VREF + 0.2	2.7	0.35	VCCI - 0.43	18	18	169	124	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.



**Figure 2-21 • AC Loading**

**Table 2-131 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.2	VREF + 0.2	1.25	1.25	1.25	30

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

**Table 2-132 • SSTL2 Class II**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V,  
Worst-Case VCCI = 2.3 V, VREF = 1.25 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.15	0.05	2.08	0.52	2.19	1.75			2.19	1.75	ns
-1	0.68	1.83	0.05	1.77	0.44	1.86	1.49			1.86	1.49	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-133 • SSTL2 Class II**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V,  
Worst-Case VCCI = 2.3 V, VREF = 1.25 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.15	0.04	2.08	0.40	2.19	1.75			2.19	1.75	ns
-1	0.52	1.83	0.03	1.77	0.34	1.86	1.49			1.86	1.49	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.



## SSTL3 Class I

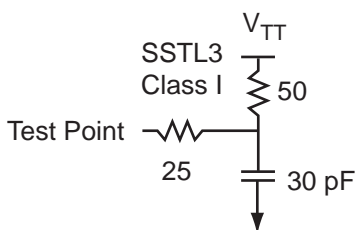
Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Military ProASIC3E devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-134 • Minimum and Maximum DC Input and Output Levels**

SSTL3 Class I	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
14 mA	-0.3	VREF - 0.2	VREF + 0.2	3.6	0.7	VCCI - 1.1	14	14	51	54	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.



**Figure 2-22 • AC Loading**

**Table 2-135 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.2	VREF + 0.2	1.5	1.5	1.485	30

\* Measuring point = V<sub>trip</sub>. See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

**Table 2-136 • SSTL3 Class I**

Military-Case Conditions: T<sub>J</sub> = 125°C, Worst-Case VCC = 1.14 V,  
Worst-Case VCCI = 3.0 V, VREF = 1.5 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.28	0.05	1.99	0.52	2.33	1.82			2.33	1.82	ns
-1	0.68	1.94	0.05	1.69	0.44	1.98	1.55			1.98	1.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-137 • SSTL3 Class I**

Military-Case Conditions: T<sub>J</sub> = 125°C, VCC = 1.425 V,  
Worst-Case VCCI = 3.0 V, VREF = 1.5 V  
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.28	0.04	1.99	0.40	2.33	1.82			2.33	1.82	ns
-1	0.52	1.94	0.03	1.69	0.34	1.98	1.55			1.98	1.55	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## SSTL3 Class II

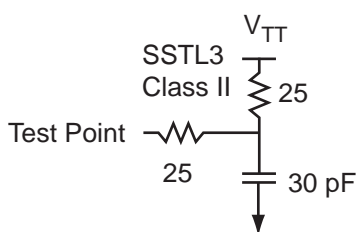
Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Military ProASIC3E devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

**Table 2-138 • Minimum and Maximum DC Input and Output Levels**

SSTL3 Class II	VIL		VIH		VOL	VOH	I <sub>OL</sub>	I <sub>OH</sub>	I <sub>OSL</sub>	I <sub>OSH</sub>	I <sub>IL</sub>	I <sub>IH</sub>
	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>1</sup>	Max. mA <sup>1</sup>	μA <sup>2</sup>	μA <sup>2</sup>
21 mA	-0.3	VREF - 0.2	VREF + 0.2	3.6	0.5	VCCI - 0.9	21	21	103	109	15	15

**Notes:**

1. Currents are measured at 100°C junction temperature and maximum voltage.
2. Currents are measured at 125°C junction temperature.



**Figure 2-23 • AC Loading**

**Table 2-139 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C <sub>LOAD</sub> (pF)
VREF - 0.2	VREF + 0.2	1.5	1.5	1.485	30

\* Measuring point = V<sub>trip</sub>. See Table 2-27 on page 2-27 for a complete table of trip points.

### Timing Characteristics

**Table 2-140 • SSTL3 Class II**

**Military-Case Conditions: T<sub>J</sub> = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V**  
**Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.80	2.04	0.05	1.99	0.52	2.08	1.65			2.08	1.65	ns
-1	0.68	1.74	0.05	1.69	0.44	1.77	1.41			1.77	1.41	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-141 • SSTL3 Class II**

**Military-Case Conditions: T<sub>J</sub> = 125°C, VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V**  
**Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
Std.	0.61	2.04	0.04	1.99	0.40	2.08	1.65			2.08	1.65	ns
-1	0.52	1.74	0.03	1.69	0.34	1.77	1.41			1.77	1.41	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

## Differential I/O Characteristics

### Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

### LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-24](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, military ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

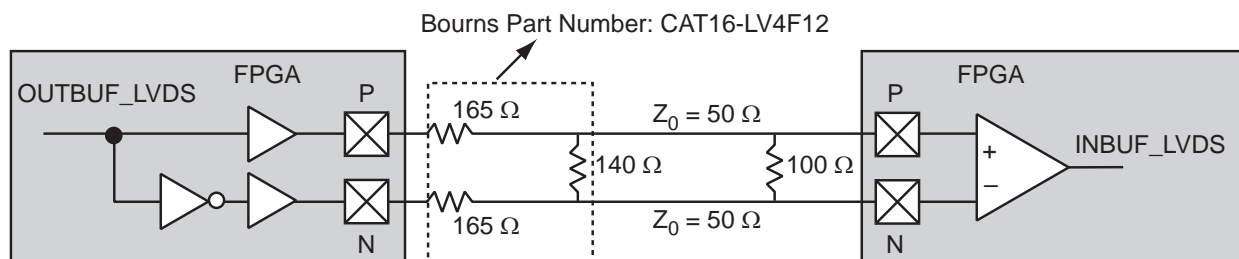


Figure 2-24 • LVDS Circuit Diagram and Board-Level Implementation

**Table 2-142 • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
$I_{OL}^4$	Output Lower Current	0.65	0.91	1.16	mA
$I_{OH}^4$	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
$I_{IH}^3$	Input High Leakage Current			10	$\mu$ A
$I_{IL}^3$	Input Low Leakage Current			10	$\mu$ A
V <sub>ODIFF</sub>	Differential Output Voltage	250	350	450	mV
V <sub>OCM</sub>	Output Common Mode Voltage	1.125	1.25	1.375	V
V <sub>ICM</sub>	Input Common Mode Voltage	0.05	1.25	2.35	V
V <sub>IDIFF</sub>	Input Differential Voltage	100	350		mV

**Notes:**

1.  $\pm 5\%$
2. Differential input voltage =  $\pm 350$  mV.
3. Currents are measured at 125°C junction temperature.
4.  $I_{OL}/I_{OH}$  is defined by  $V_{ODIFF}/(\text{Resistor Network})$ .

**Table 2-143 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.075	1.325	Cross point

\* Measuring point =  $V_{trip}$ . See Table 2-27 on page 2-27 for a complete table of trip points.

## Timing Characteristics

### 1.2 V DC Core Voltage

**Table 2-144 • LVDS**

**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Speed Grade	$t_{\text{DOUT}}$	$t_{\text{DP}}$	$t_{\text{DIN}}$	$t_{\text{PY}}$	Units
Std.	0.80	1.81	0.05	2.39	ns
-1	0.68	1.57	0.05	2.04	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

### 1.5 V DC Core Voltage

**Table 2-145 • LVDS**

**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Pro I/Os for A3PE600L and A3PE3000L Only**

Speed Grade	$t_{\text{DOUT}}$	$t_{\text{DP}}$	$t_{\text{DIN}}$	$t_{\text{PY}}$	Units
Std.	0.61	1.81	0.04	2.39	ns
-1	0.52	1.57	0.03	2.04	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-146 • LVDS**

**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**  
**Applicable to Advanced I/O Banks for A3P1000 Only**

Speed Grade	$t_{\text{DOUT}}$	$t_{\text{DP}}$	$t_{\text{DIN}}$	$t_{\text{PY}}$	Units
Std.	0.63	2.01	0.05	1.76	ns
-1	0.54	1.71	0.04	1.50	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

### B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF\_LVDS and BIBUF\_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-25. The input and output buffer delays are available in the LVDS section in Table 2-142 on page 2-78.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver:  $R_S = 60 \Omega$  and  $R_T = 70 \Omega$ , given  $Z_0 = 50 \Omega$  (2") and  $Z_{stub} = 50 \Omega$  (~1.5").

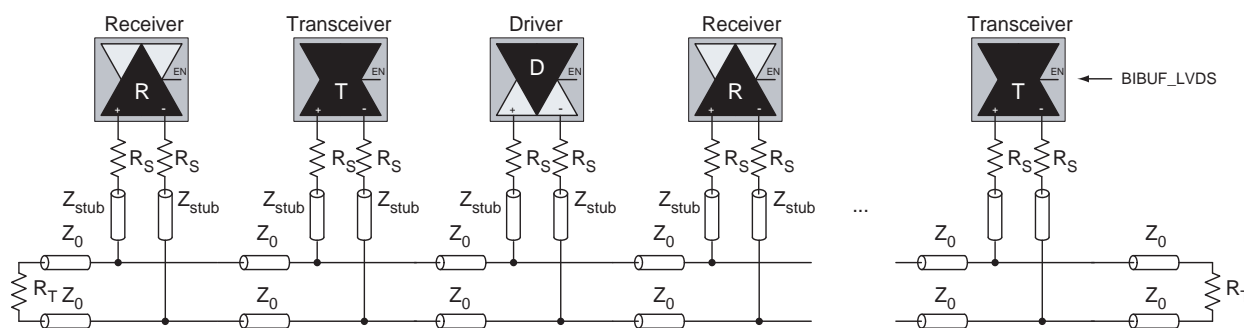
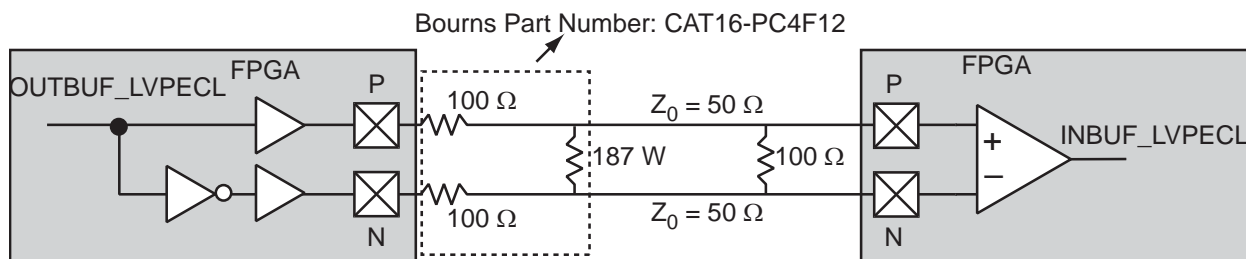


Figure 2-25 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

## LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-26](#). The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.



**Figure 2-26 • LVPECL Circuit Diagram and Board-Level Implementation**

**Table 2-147 • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output LOW Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output HIGH Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input LOW, Input HIGH Voltages	0	3.3	0	3.6	0	3.9	V
V <sub>ODIFF</sub>	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V <sub>OCM</sub>	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V <sub>ICM</sub>	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V <sub>IDIFF</sub>	Input Differential Voltage	300		300		300		mV

**Table 2-148 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.64	1.94	Cross point

\* Measuring point =  $V_{trip}$ . See [Table 2-27](#) on page 2-27 for a complete table of trip points.

## Timing Characteristics

### 1.2 V DC Core Voltage

**Table 2-149 • LVPECL**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	Units
Std.	0.80	1.81	0.05	2.16	ns
-1	0.68	1.54	0.05	1.84	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

### 1.5 V DC Core Voltage

**Table 2-150 • LVPECL**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	Units
Std.	0.61	1.81	0.04	2.16	ns
-1	0.52	1.54	0.03	1.84	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-151 • LVPECL**

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Advanced I/O Banks for A3P1000 Only

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	Units
Std.	0.63	1.98	0.05	1.54	ns
-1	0.54	1.68	0.04	1.31	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.



## I/O Register Specifications

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

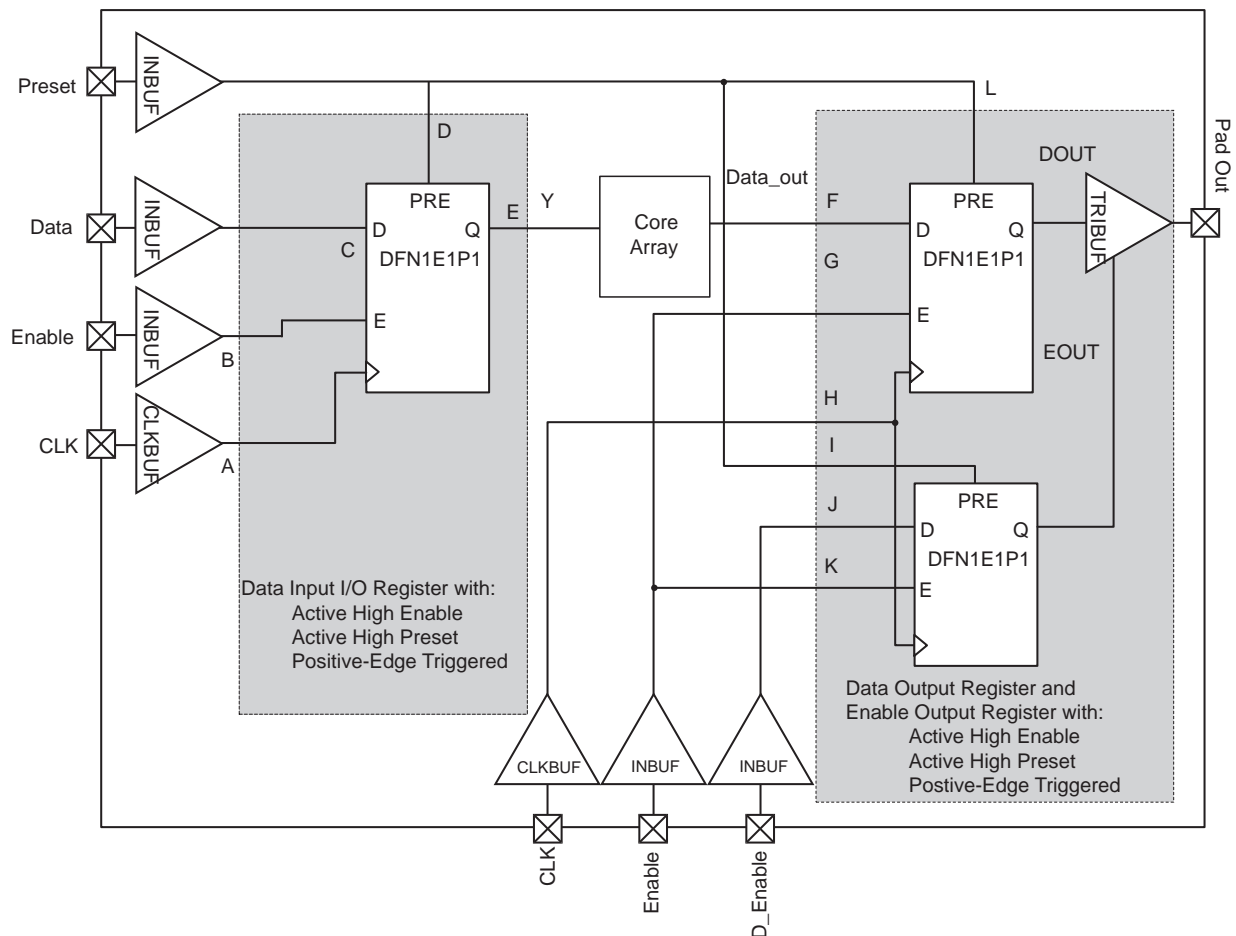


Figure 2-27 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

**Table 2-152 • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
$t_{OCLKQ}$	Clock-to-Q of the Output Data Register	H, DOUT
$t_{OSUD}$	Data Setup Time for the Output Data Register	F, H
$t_{OHD}$	Data Hold Time for the Output Data Register	F, H
$t_{OSUE}$	Enable Setup Time for the Output Data Register	G, H
$t_{OHE}$	Enable Hold Time for the Output Data Register	G, H
$t_{OPRE2Q}$	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	H, EOUT
$t_{OESUD}$	Data Setup Time for the Output Enable Register	J, H
$t_{OEHD}$	Data Hold Time for the Output Enable Register	J, H
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	K, H
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
$t_{ICLKQ}$	Clock-to-Q of the Input Data Register	A, E
$t_{ISUD}$	Data Setup Time for the Input Data Register	C, A
$t_{IHD}$	Data Hold Time for the Input Data Register	C, A
$t_{ISUE}$	Enable Setup Time for the Input Data Register	B, A
$t_{IHE}$	Enable Hold Time for the Input Data Register	B, A
$t_{IPRE2Q}$	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

\* See Figure 2-27 on page 2-83 for more information.

**Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

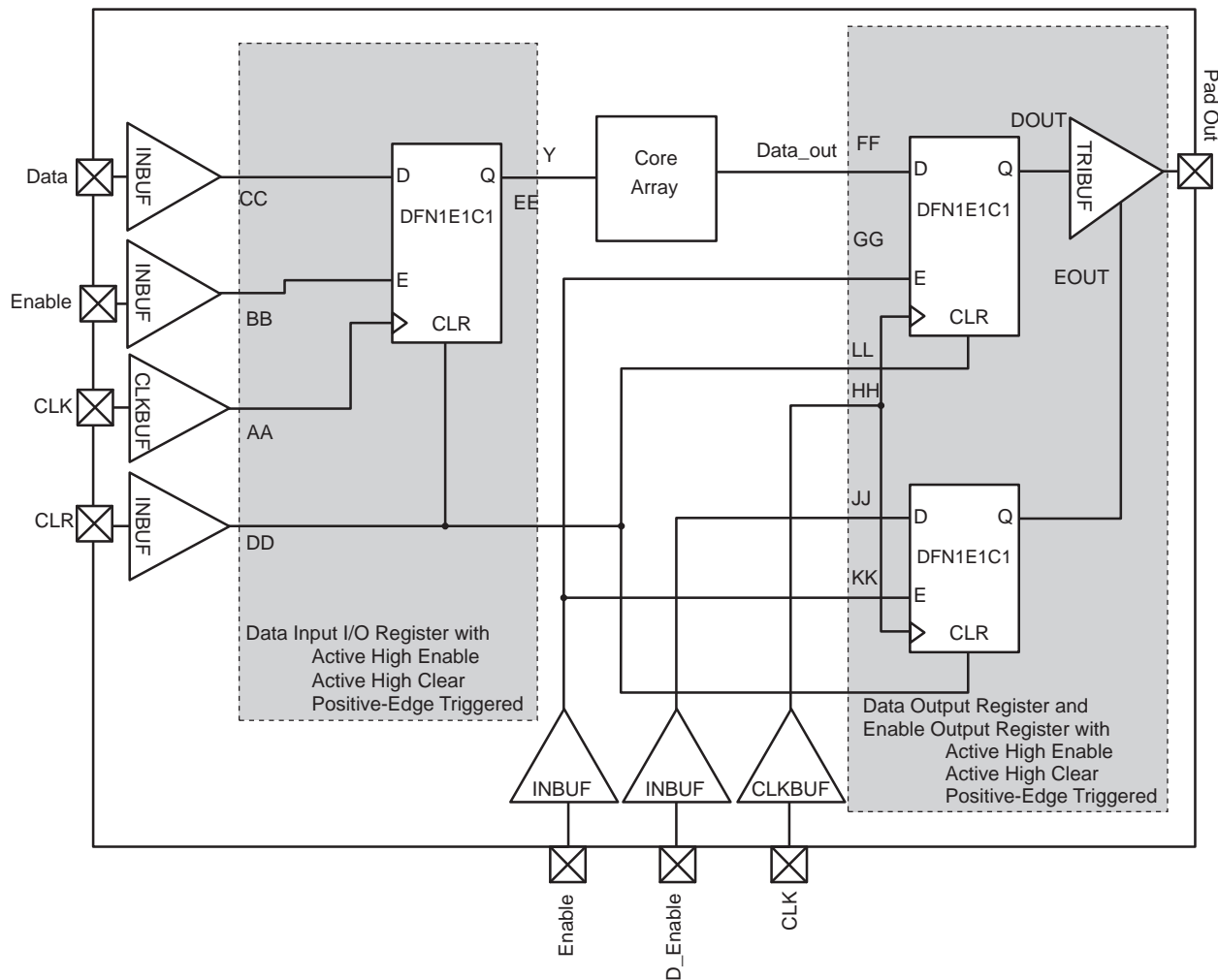


Figure 2-28 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

**Table 2-153 • Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
$t_{OCLKQ}$	Clock-to-Q of the Output Data Register	HH, DOUT
$t_{OSUD}$	Data Setup Time for the Output Data Register	FF, HH
$t_{OHD}$	Data Hold Time for the Output Data Register	FF, HH
$t_{OSUE}$	Enable Setup Time for the Output Data Register	GG, HH
$t_{OHE}$	Enable Hold Time for the Output Data Register	GG, HH
$t_{OCLR2Q}$	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	HH, EOUT
$t_{OESUD}$	Data Setup Time for the Output Enable Register	JJ, HH
$t_{OEHD}$	Data Hold Time for the Output Enable Register	JJ, HH
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	KK, HH
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
$t_{ICLKQ}$	Clock-to-Q of the Input Data Register	AA, EE
$t_{ISUD}$	Data Setup Time for the Input Data Register	CC, AA
$t_{IHD}$	Data Hold Time for the Input Data Register	CC, AA
$t_{ISUE}$	Enable Setup Time for the Input Data Register	BB, AA
$t_{IHE}$	Enable Hold Time for the Input Data Register	BB, AA
$t_{ICLR2Q}$	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

\* See Figure 2-28 on page 2-85 for more information.

## Input Register

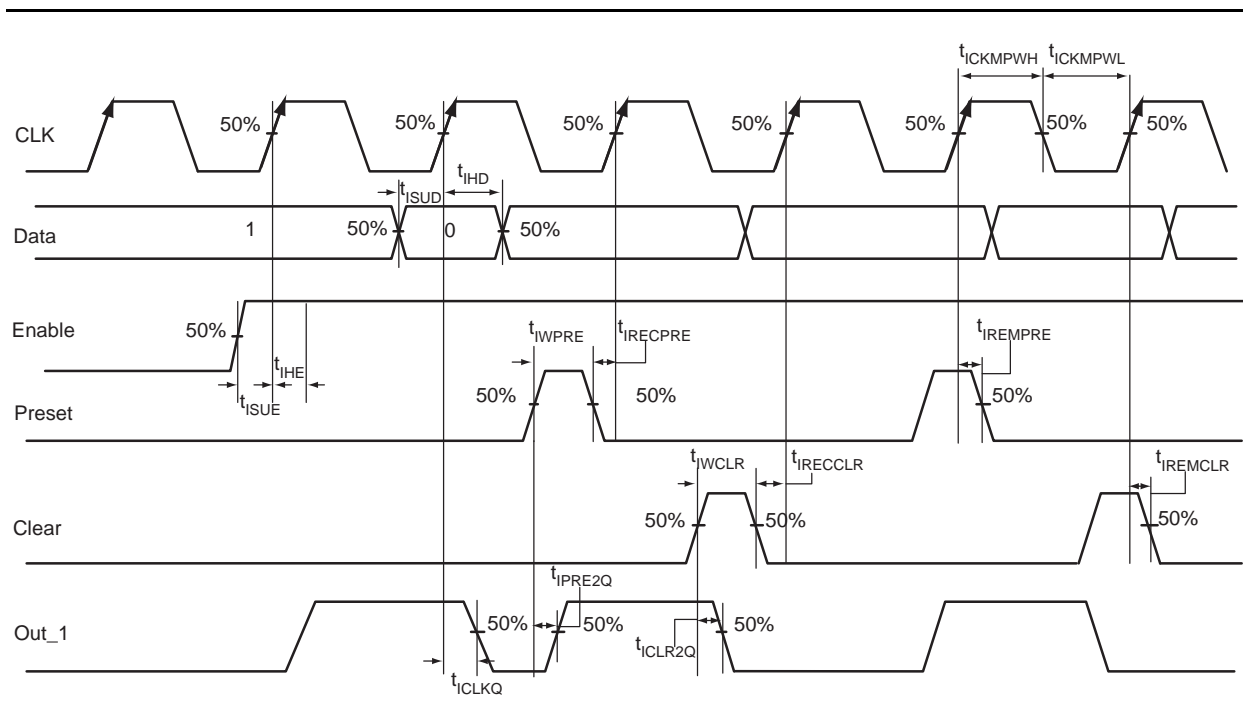


Figure 2-29 • Input Register Timing Diagram

### Timing Characteristics

**Table 2-154 • Input Data Register Propagation Delays**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{\text{CLKQ}}$	Clock-to-Q of the Input Data Register	0.33	0.39	ns
$t_{\text{ISUD}}$	Data Setup Time for the Input Data Register	0.36	0.43	ns
$t_{\text{IHD}}$	Data Hold Time for the Input Data Register	0.00	0.00	ns
$t_{\text{ISUE}}$	Enable Setup Time for the Input Data Register	0.51	0.60	ns
$t_{\text{IHE}}$	Enable Hold Time for the Input Data Register	0.00	0.00	ns
$t_{\text{ICLR2Q}}$	Asynchronous Clear-to-Q of the Input Data Register	0.63	0.74	ns
$t_{\text{IPRE2Q}}$	Asynchronous Preset-to-Q of the Input Data Register	0.63	0.74	ns
$t_{\text{IREMCLR}}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{\text{IRECCLR}}$	Asynchronous Clear Recovery Time for the Input Data Register	0.31	0.36	ns
$t_{\text{IREMPRE}}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{\text{IRECPRE}}$	Asynchronous Preset Recovery Time for the Input Data Register	0.31	0.36	ns
$t_{\text{IWCLR}}$	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{\text{IWPRE}}$	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{\text{ICKMPWH}}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	0.36	ns
$t_{\text{ICKMPWL}}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	0.32	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-155 • Input Data Register Propagation Delays**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{\text{CLKQ}}$	Clock-to-Q of the Input Data Register	0.25	0.30	ns
$t_{\text{ISUD}}$	Data Setup Time for the Input Data Register	0.28	0.33	ns
$t_{\text{IHD}}$	Data Hold Time for the Input Data Register	0.00	0.00	ns
$t_{\text{ISUE}}$	Enable Setup Time for the Input Data Register	0.39	0.46	ns
$t_{\text{IHE}}$	Enable Hold Time for the Input Data Register	0.00	0.00	ns
$t_{\text{ICLR2Q}}$	Asynchronous Clear-to-Q of the Input Data Register	0.48	0.56	ns
$t_{\text{IPRE2Q}}$	Asynchronous Preset-to-Q of the Input Data Register	0.48	0.56	ns
$t_{\text{IREMCLR}}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{\text{IRECCLR}}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	0.28	ns
$t_{\text{IREMPRE}}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{\text{IRECPRE}}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	0.28	ns
$t_{\text{IWCLR}}$	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{\text{IWPRE}}$	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	0.22	ns
$t_{\text{ICKMPWH}}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	0.36	ns
$t_{\text{ICKMPWL}}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	0.32	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-156 • Input Data Register Propagation Delays**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$  for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{iCLKQ}$	Clock-to-Q of the Input Data Register	0.29	0.34	ns
$t_{iSUD}$	Data Setup Time for the Input Data Register	0.32	0.37	ns
$t_{iHD}$	Data Hold Time for the Input Data Register	0.00	0.00	ns
$t_{iSUE}$	Enable Setup Time for the Input Data Register	0.45	0.53	ns
$t_{iHE}$	Enable Hold Time for the Input Data Register	0.00	0.00	ns
$t_{iCLR2Q}$	Asynchronous Clear-to-Q of the Input Data Register	0.55	0.64	ns
$t_{iPRE2Q}$	Asynchronous Preset-to-Q of the Input Data Register	0.55	0.64	ns
$t_{iREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{iRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.27	0.31	ns
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.27	0.31	ns
$t_{iWCLR}$	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
$t_{iWPRE}$	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
$t_{iCKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.41	0.48	ns
$t_{iCKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.37	0.43	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

### Output Register

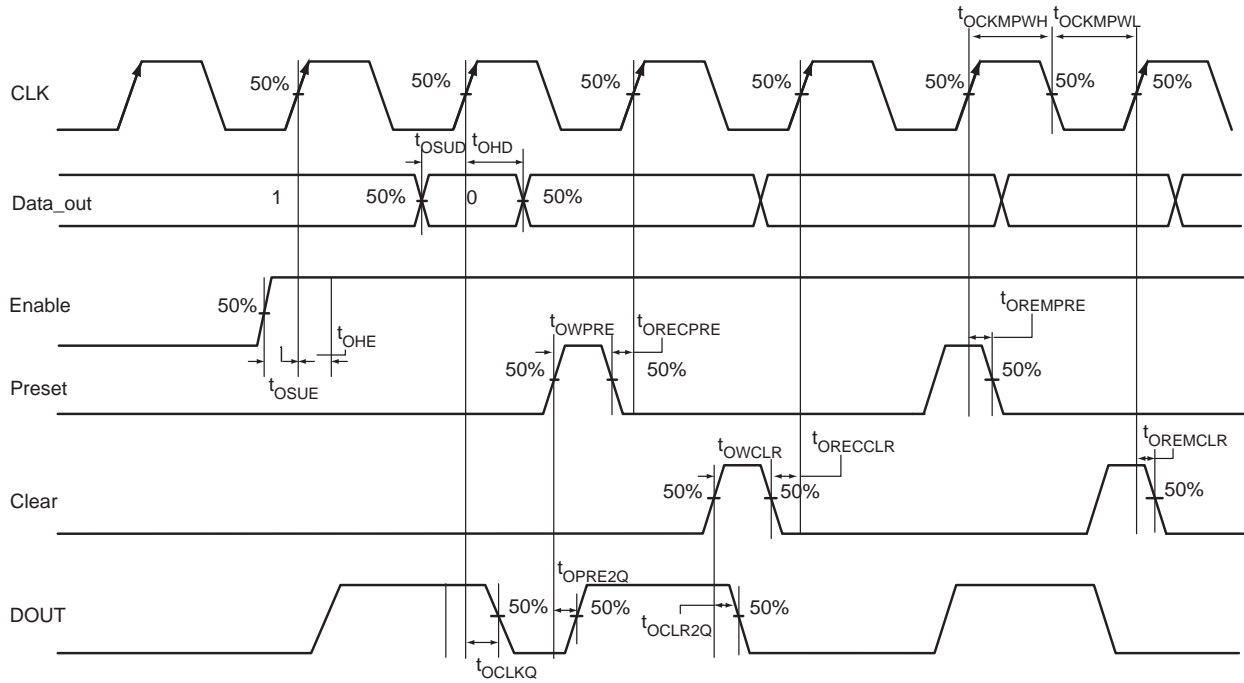


Figure 2-30 • Output Register Timing Diagram



### Timing Characteristics

**Table 2-157 • Output Data Register Propagation Delays**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{\text{CLKQ}}$	Clock-to-Q of the Output Data Register	0.81	0.96	ns
$t_{\text{OSUD}}$	Data Setup Time for the Output Data Register	0.43	0.51	ns
$t_{\text{OHD}}$	Data Hold Time for the Output Data Register	0.00	0.00	ns
$t_{\text{OSUE}}$	Enable Setup Time for the Output Data Register	0.61	0.71	ns
$t_{\text{OHE}}$	Enable Hold Time for the Output Data Register	0.00	0.00	ns
$t_{\text{OCLR2Q}}$	Asynchronous Clear-to-Q of the Output Data Register	1.11	1.31	ns
$t_{\text{OPRE2Q}}$	Asynchronous Preset-to-Q of the Output Data Register	1.11	1.31	ns
$t_{\text{OEMCLR}}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{\text{ORECCLR}}$	Asynchronous Clear Recovery Time for the Output Data Register	0.31	0.36	ns
$t_{\text{OREMPRE}}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{\text{ORECPRE}}$	Asynchronous Preset Recovery Time for the Output Data Register	0.31	0.36	ns
$t_{\text{OWCLR}}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{\text{OWPRE}}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{\text{OCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	0.36	ns
$t_{\text{OCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	0.32	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-158 • Output Data Register Propagation Delays**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{\text{CLKQ}}$	Clock-to-Q of the Output Data Register	0.62	0.73	ns
$t_{\text{OSUD}}$	Data Setup Time for the Output Data Register	0.33	0.39	ns
$t_{\text{OHD}}$	Data Hold Time for the Output Data Register	0.00	0.00	ns
$t_{\text{OSUE}}$	Enable Setup Time for the Output Data Register	0.46	0.55	ns
$t_{\text{OHE}}$	Enable Hold Time for the Output Data Register	0.00	0.00	ns
$t_{\text{OCLR2Q}}$	Asynchronous Clear-to-Q of the Output Data Register	0.85	1.00	ns
$t_{\text{OPRE2Q}}$	Asynchronous Preset-to-Q of the Output Data Register	0.85	1.00	ns
$t_{\text{OEMCLR}}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{\text{ORECCLR}}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	0.28	ns
$t_{\text{OREMPRE}}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{\text{ORECPRE}}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	0.28	ns
$t_{\text{OWCLR}}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{\text{OWPRE}}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	0.22	ns
$t_{\text{OCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	0.36	ns
$t_{\text{OCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	0.32	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-159 • Output Data Register Propagation Delays**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{\text{OCLKQ}}$	Clock-to-Q of the Output Data Register	0.71	0.83	ns
$t_{\text{OSUD}}$	Data Setup Time for the Output Data Register	0.38	0.44	ns
$t_{\text{OHD}}$	Data Hold Time for the Output Data Register	0.00	0.00	ns
$t_{\text{OSUE}}$	Enable Setup Time for the Output Data Register	0.53	0.62	ns
$t_{\text{OHE}}$	Enable Hold Time for the Output Data Register	0.00	0.00	ns
$t_{\text{OCLR2Q}}$	Asynchronous Clear-to-Q of the Output Data Register	0.97	1.14	ns
$t_{\text{OPRE2Q}}$	Asynchronous Preset-to-Q of the Output Data Register	0.97	1.14	ns
$t_{\text{OREMCLR}}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{\text{ORECCLR}}$	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
$t_{\text{OREMPRE}}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{\text{ORECPRE}}$	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
$t_{\text{OWCLR}}$	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
$t_{\text{OWPRE}}$	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
$t_{\text{OCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.41	0.48	ns
$t_{\text{OCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.37	0.43	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

## Output Enable Register

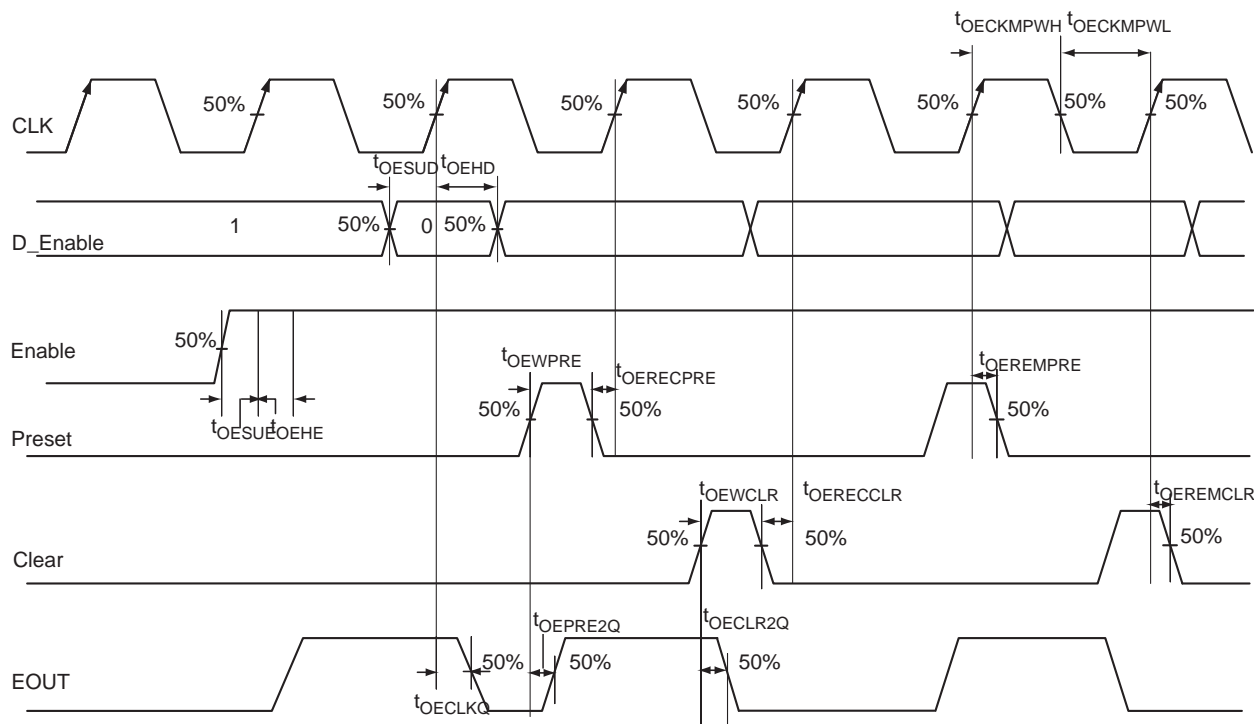


Figure 2-31 • Output Enable Register Timing Diagram

### Timing Characteristics

**Table 2-160 • Output Enable Register Propagation Delays**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	0.62	0.72	ns
$t_{OESUD}$	Data Setup Time for the Output Enable Register	0.43	0.51	ns
$t_{OEHD}$	Data Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	0.60	0.71	ns
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.92	1.08	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.92	1.08	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.31	0.36	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.31	0.36	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OEWPPE}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	0.32	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-161 • Output Enable Register Propagation Delays**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	0.47	0.55	ns
$t_{OESUD}$	Data Setup Time for the Output Enable Register	0.33	0.39	ns
$t_{OEHD}$	Data Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	0.46	0.54	ns
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.70	0.83	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.70	0.83	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	0.28	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	0.28	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OEWPPE}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	0.22	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	0.36	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	0.32	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-162 • Output Enable Register Propagation Delays**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$  for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{OECLKQ}$	Clock-to-Q of the Output Enable Register	0.54	0.63	ns
$t_{OESUD}$	Data Setup Time for the Output Enable Register	0.38	0.44	ns
$t_{OEHD}$	Data Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OESUE}$	Enable Setup Time for the Output Enable Register	0.52	0.62	ns
$t_{OEHE}$	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.80	0.94	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.80	0.94	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.31	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.31	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.37	0.43	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

## DDR Module Specifications

### Input DDR Module

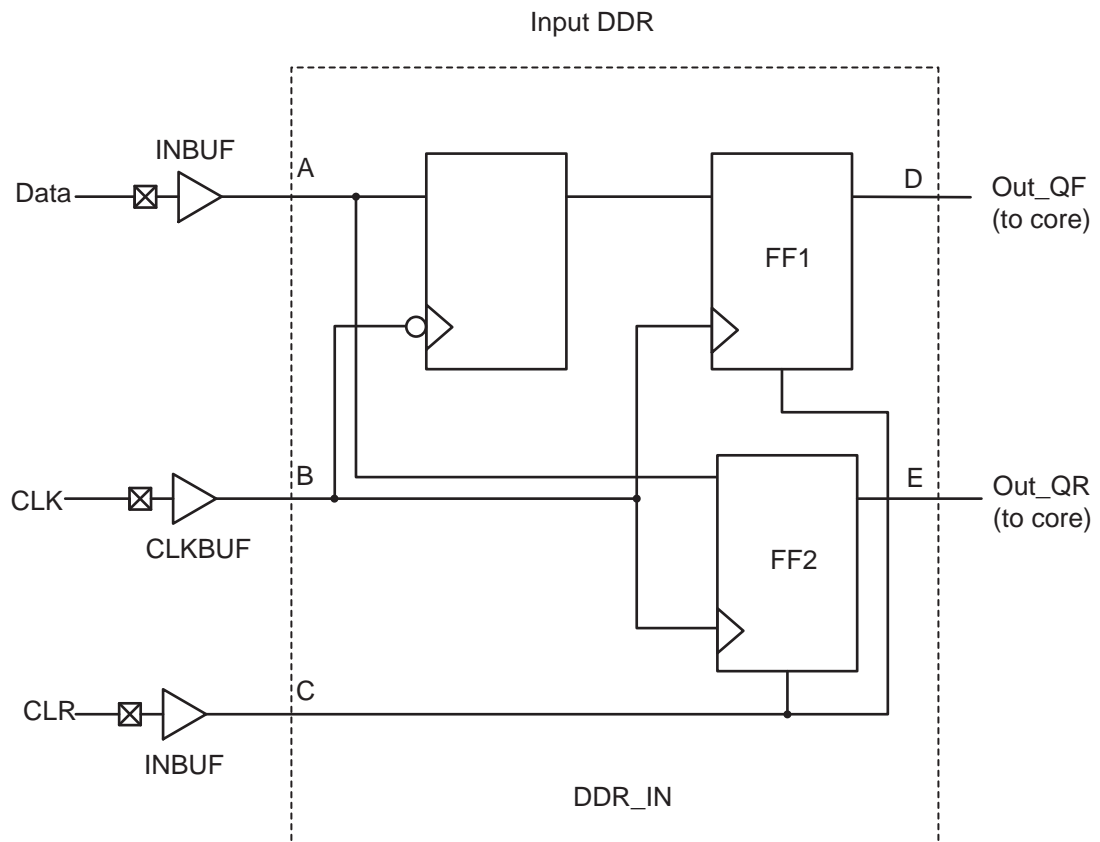
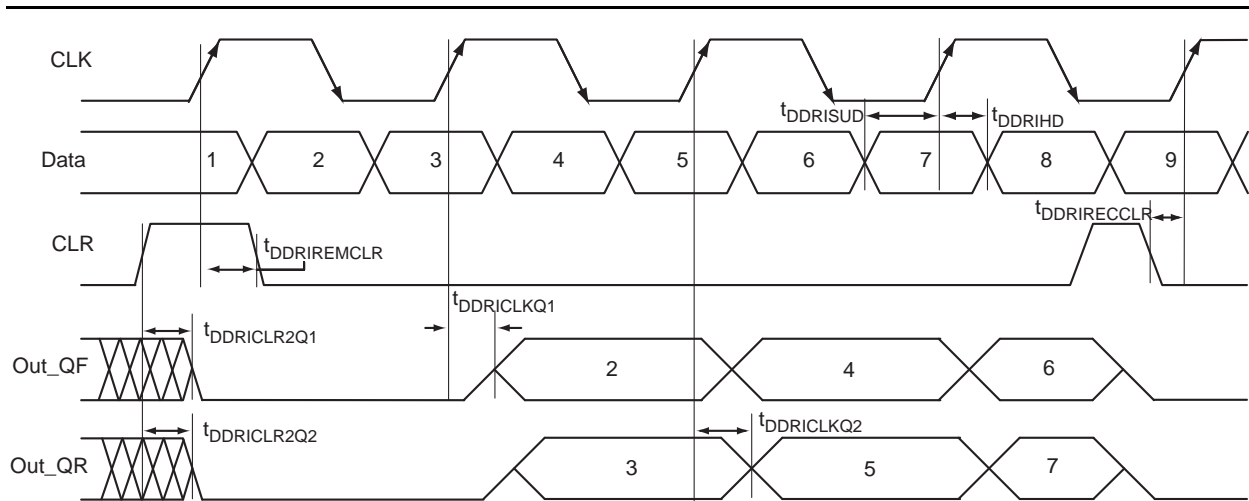


Figure 2-32 • Input DDR Timing Model

Table 2-163 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
$t_{DDRIHD}$	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B


**Figure 2-33 • Input DDR Timing Diagram**

### Timing Characteristics

**Table 2-164 • Input DDR Propagation Delays**

 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{\text{DDRICKQ1}}$	Clock-to-Out Out_QR for Input DDR	0.38	0.45	ns
$t_{\text{DDRICKQ2}}$	Clock-to-Out Out_QF for Input DDR	0.54	0.63	ns
$t_{\text{DDRISUD1}}$	Data Setup for Input DDR (fall)	0.39	0.46	ns
$t_{\text{DDRISUD2}}$	Data Setup for Input DDR (rise)	0.34	0.40	ns
$t_{\text{DDRHD1}}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{\text{DDRHD2}}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.64	0.75	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.79	0.93	ns
$t_{\text{DDRREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.31	0.36	ns
$t_{\text{DDRWCLR}}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	0.36	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	0.32	ns
$F_{\text{DDRIMAX}}$	Maximum Frequency for Input DDR	TBD	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-165 • Input DDR Propagation Delays**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for any A3PE600L/A3PE3000L**

Parameter	Description	-1	Std.	Units
$t_{\text{DDRICKQ1}}$	Clock-to-Out Out_QR for Input DDR	0.29	0.34	ns
$t_{\text{DDRICKQ2}}$	Clock-to-Out Out_QF for Input DDR	0.41	0.48	ns
$t_{\text{DDRISUD1}}$	Data Setup for Input DDR (fall)	0.30	0.35	ns
$t_{\text{DDRISUD2}}$	Data Setup for Input DDR (rise)	0.26	0.31	ns
$t_{\text{DDRIHD1}}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{\text{DDRIHD2}}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.49	0.58	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.60	0.71	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.24	0.28	ns
$t_{\text{DDRIWCLR}}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	0.22	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	0.36	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	0.32	ns
$F_{\text{DDRIMAX}}$	Maximum Frequency for Input DDR	TBD	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-166 • Input DDR Propagation Delays**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$  for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{\text{DDRICKQ1}}$	Clock-to-Out Out_QR for Input DDR	0.33	0.39	ns
$t_{\text{DDRICKQ2}}$	Clock-to-Out Out_QF for Input DDR	0.47	0.55	ns
$t_{\text{DDRISUD1}}$	Data Setup for Input DDR (fall)	0.30	0.35	ns
$t_{\text{DDRISUD2}}$	Data Setup for Input DDR (rise)	0.30	0.35	ns
$t_{\text{DDRIHD1}}$	Data Hold for Input DDR (fall)	0.00	0.00	ns
$t_{\text{DDRIHD2}}$	Data Hold for Input DDR (rise)	0.00	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.56	0.65	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.69	0.81	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.27	0.31	ns
$t_{\text{DDRIWCLR}}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.25	0.30	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.41	0.48	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.37	0.43	ns
$F_{\text{DDRIMAX}}$	Maximum Frequency for Input DDR	TBD	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.



## Output DDR Module

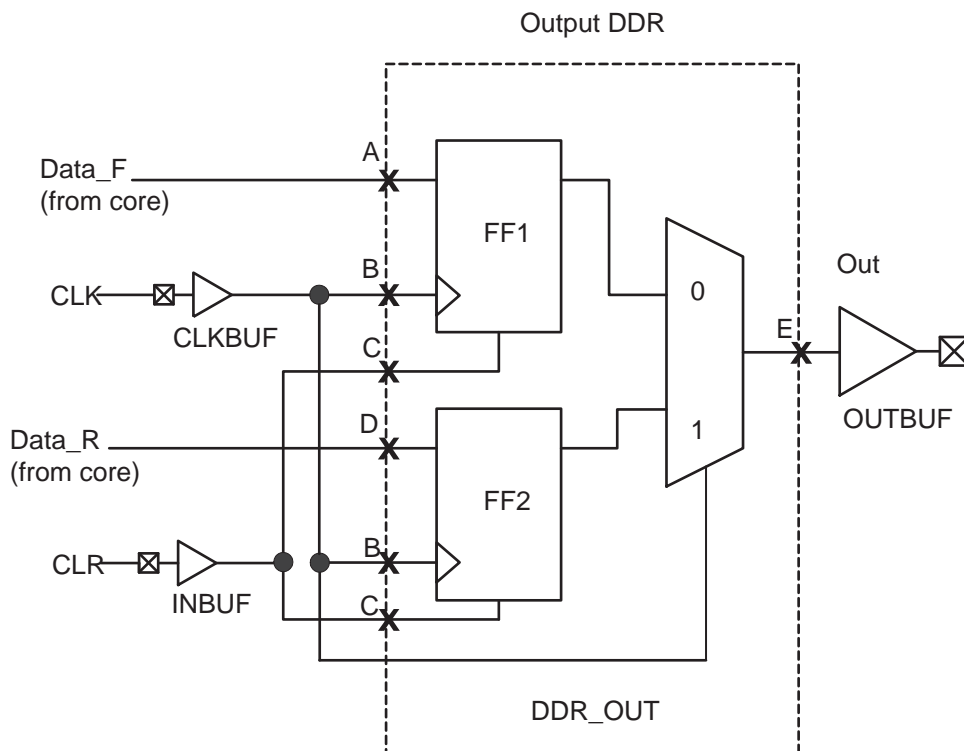
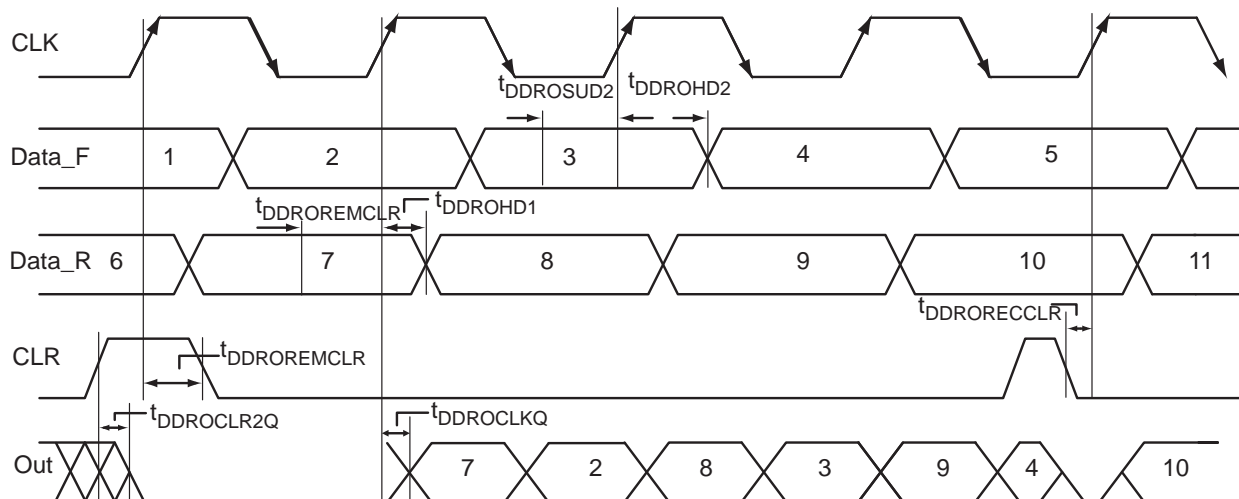


Figure 2-34 • Output DDR Timing Model

Table 2-167 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B


**Figure 2-35 • Output DDR Timing Diagram**

### Timing Characteristics

**Table 2-168 • Output DDR Propagation Delays**

 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{\text{DDROCLKQ}}$	Clock-to-Out of DDR for Output DDR	0.97	1.14	ns
$t_{\text{DDRISUD1}}$	Data_F Data Setup for Output DDR	0.52	0.62	ns
$t_{\text{DDROSUD2}}$	Data_R Data Setup for Output DDR	0.52	0.62	ns
$t_{\text{DDROHD1}}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROHD2}}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	1.11	1.30	ns
$t_{\text{DDROEMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{\text{DDROECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.31	0.36	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	0.36	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	0.32	ns
$F_{\text{DDOMAX}}$	Maximum Frequency for the Output DDR	TBD	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-169 • Output DDR Propagation Delays****Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L/A3PE3000L**

Parameter	Description	-1	Std.	Units
$t_{\text{DDROCLKQ}}$	Clock-to-Out of DDR for Output DDR	0.74	0.87	ns
$t_{\text{DDRISUD1}}$	Data_F Data Setup for Output DDR	0.40	0.47	ns
$t_{\text{DDROSUD2}}$	Data_R Data Setup for Output DDR	0.40	0.47	ns
$t_{\text{DDROHD1}}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROHD2}}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.85	1.00	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{\text{DDRORECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.24	0.28	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	0.36	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	0.32	ns
$F_{\text{DDOMAX}}$	Maximum Frequency for the Output DDR	TBD	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-170 • Output DDR Propagation Delays**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{\text{DDROCLKQ}}$	Clock-to-Out of DDR for Output DDR	0.84	0.99	ns
$t_{\text{DDRISUD1}}$	Data_F Data Setup for Output DDR	0.46	0.54	ns
$t_{\text{DDROSUD2}}$	Data_R Data Setup for Output DDR	0.46	0.54	ns
$t_{\text{DDROHD1}}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROHD2}}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.96	1.13	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{\text{DDRORECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.31	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.41	0.48	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output DDR	0.37	0.43	ns
$F_{\text{DDOMAX}}$	Maximum Frequency for the Output DDR	TBD	TBD	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

## VersaTile Characteristics

### VersaTile Specifications as a Combinatorial Module

The military ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

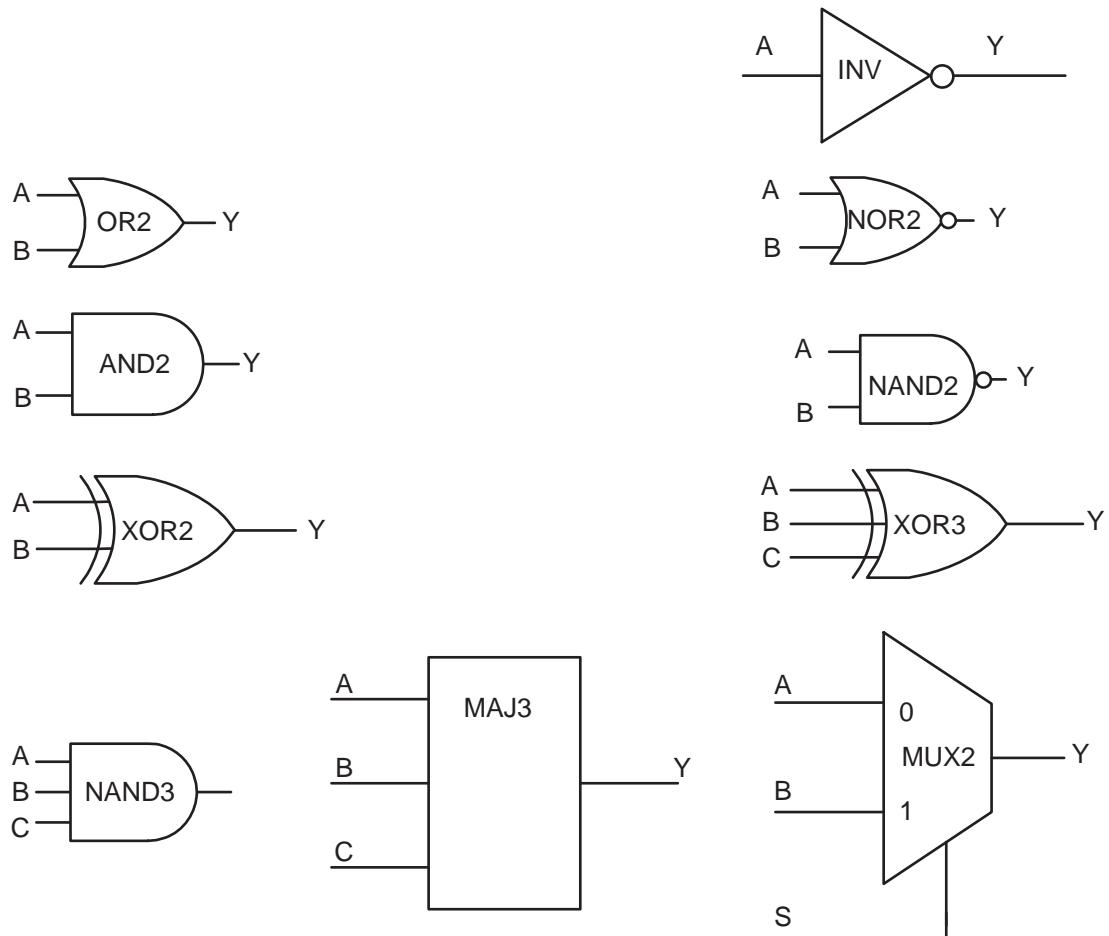


Figure 2-36 • Sample of Combinatorial Cells

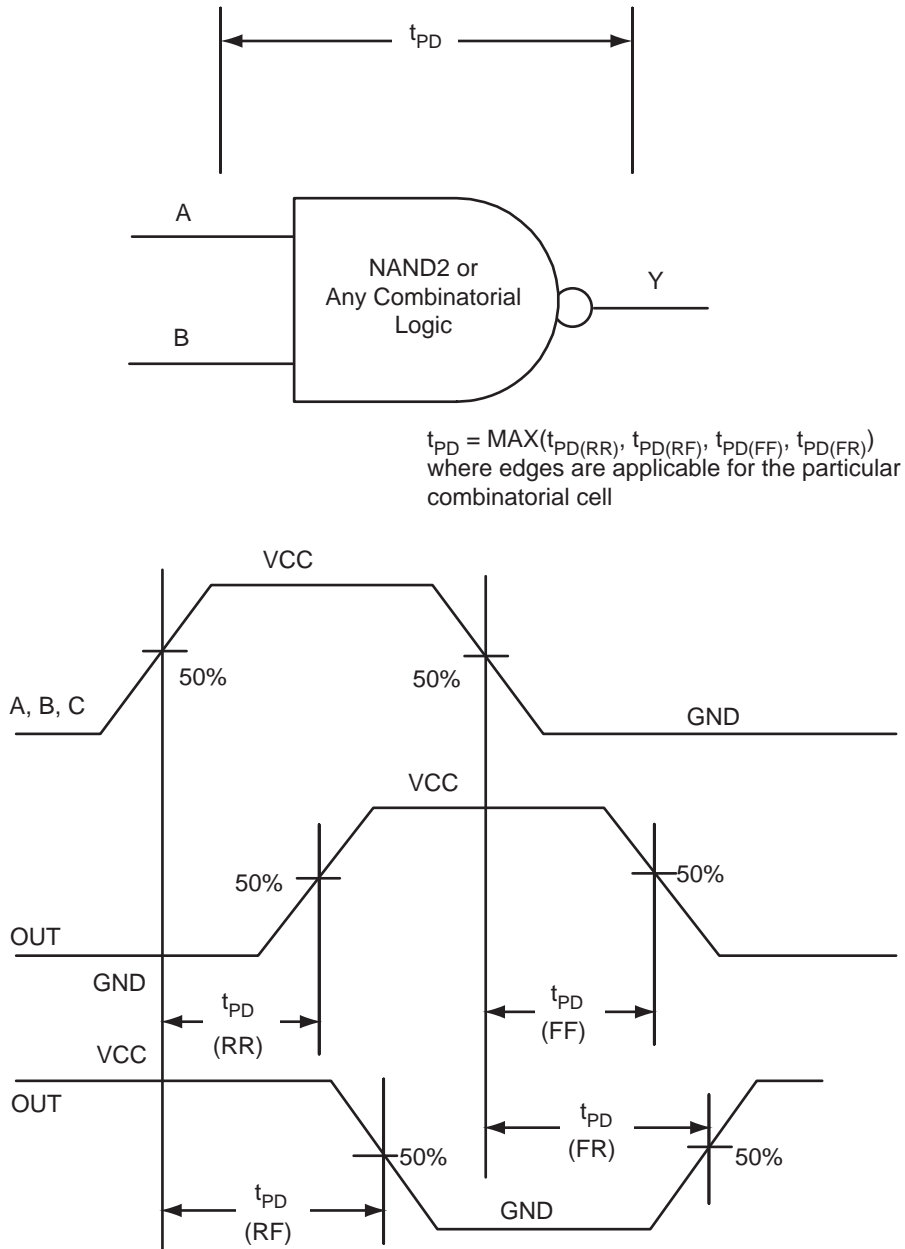


Figure 2-37 • Timing Model and Waveforms

## Timing Characteristics

**Table 2-171 • Combinatorial Cell Propagation Delays**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	$t_{PD}$	0.56	0.65	ns
AND2	$Y = A \cdot B$	$t_{PD}$	0.65	0.77	ns
NAND2	$Y = !(A \cdot B)$	$t_{PD}$	0.65	0.77	ns
OR2	$Y = A + B$	$t_{PD}$	0.67	0.79	ns
NOR2	$Y = !(A + B)$	$t_{PD}$	0.67	0.79	ns
XOR2	$Y = A \oplus B$	$t_{PD}$	1.02	1.20	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	$t_{PD}$	0.97	1.14	ns
XOR3	$Y = A \oplus B \oplus C$	$t_{PD}$	1.21	1.42	ns
MUX2	$Y = A !S + B S$	$t_{PD}$	0.70	0.82	ns
AND3	$Y = A \cdot B \cdot C$	$t_{PD}$	0.78	0.91	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-172 • Combinatorial Cell Propagation Delays**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for any A3PE600L/A3PE3000L

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	$t_{PD}$	0.43	0.50	ns
AND2	$Y = A \cdot B$	$t_{PD}$	0.50	0.59	ns
NAND2	$Y = !(A \cdot B)$	$t_{PD}$	0.50	0.59	ns
OR2	$Y = A + B$	$t_{PD}$	0.51	0.61	ns
NOR2	$Y = !(A + B)$	$t_{PD}$	0.51	0.61	ns
XOR2	$Y = A \oplus B$	$t_{PD}$	0.78	0.92	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	$t_{PD}$	0.74	0.87	ns
XOR3	$Y = A \oplus B \oplus C$	$t_{PD}$	0.93	1.09	ns
MUX2	$Y = A !S + B S$	$t_{PD}$	0.54	0.63	ns
AND3	$Y = A \cdot B \cdot C$	$t_{PD}$	0.59	0.70	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-173 • Combinatorial Cell Propagation Delays**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$  for A3P1000**

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	$t_{PD}$	0.48	0.57	ns
AND2	$Y = A \cdot B$	$t_{PD}$	0.57	0.67	ns
NAND2	$Y = !(A \cdot B)$	$t_{PD}$	0.57	0.67	ns
OR2	$Y = A + B$	$t_{PD}$	0.59	0.69	ns
NOR2	$Y = !(A + B)$	$t_{PD}$	0.59	0.69	ns
XOR2	$Y = A \oplus B$	$t_{PD}$	0.89	1.04	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	$t_{PD}$	0.84	0.99	ns
XOR3	$Y = A \oplus B \oplus C$	$t_{PD}$	1.05	1.24	ns
MUX2	$Y = A !S + B S$	$t_{PD}$	0.61	0.72	ns
AND3	$Y = A \cdot B \cdot C$	$t_{PD}$	0.68	0.79	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.



## VersaTile Specifications as a Sequential Module

The military ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

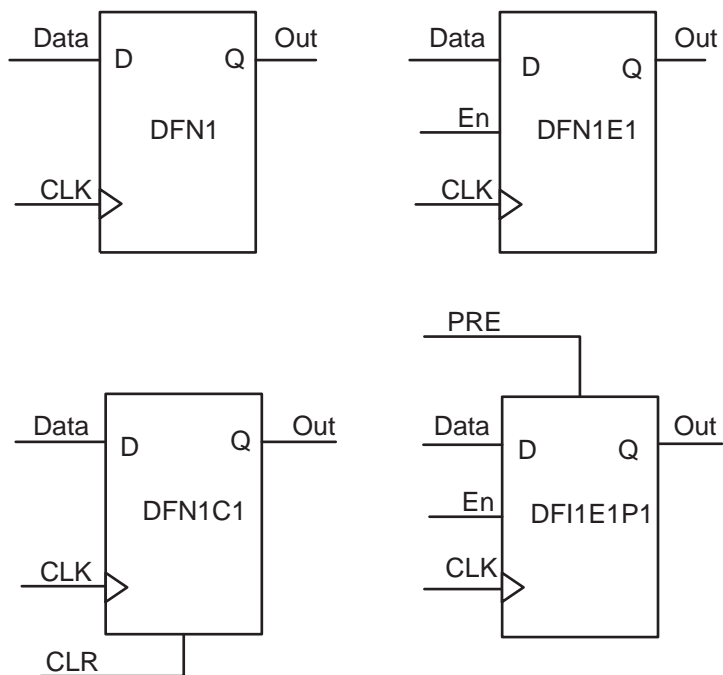


Figure 2-38 • Sample of Sequential Cells

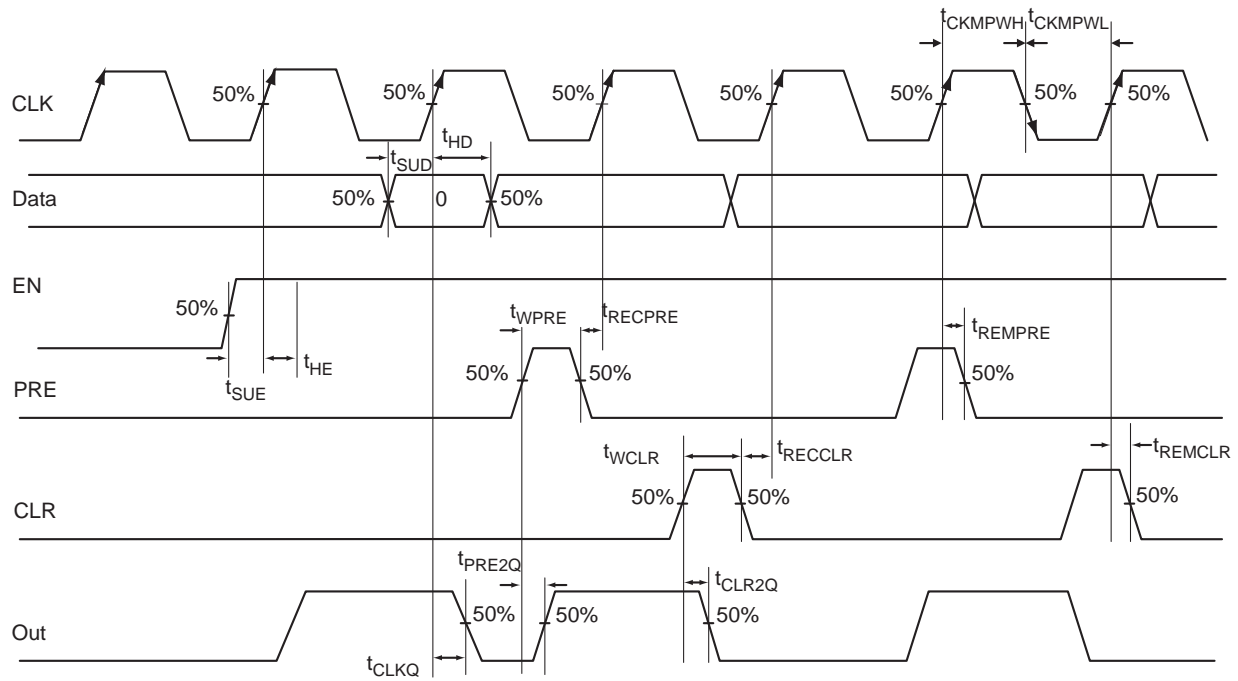


Figure 2-39 • Timing Model and Waveforms

**Timing Characteristics****Table 2-174 • Register Delays****Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L**

Parameter	Description	-1	Std.	Units
$t_{CLKQ}$	Clock-to-Q of the Core Register	0.76	0.90	ns
$t_{SUD}$	Data Setup Time for the Core Register	0.59	0.70	ns
$t_{HD}$	Data Hold Time for the Core Register	0.00	0.00	ns
$t_{SUE}$	Enable Setup Time for the Core Register	0.63	0.74	ns
$t_{HE}$	Enable Hold Time for the Core Register	0.00	0.00	ns
$t_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.55	0.65	ns
$t_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.55	0.65	ns
$t_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
$t_{RECLR}$	Asynchronous Clear Recovery Time for the Core Register	0.31	0.36	ns
$t_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
$t_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.31	0.36	ns
$t_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
$t_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
$t_{CKMPWH}$	Clock Minimum Pulse Width HIGH for the Core Register	0.56	0.64	ns
$t_{CKMPWL}$	Clock Minimum Pulse Width LOW for the Core Register	0.56	0.64	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-175 • Register Delays**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L and A3PE3000L**

Parameter	Description	-1	Std.	Units
$t_{CLKQ}$	Clock-to-Q of the Core Register	0.58	0.69	ns
$t_{SUD}$	Data Setup Time for the Core Register	0.45	0.53	ns
$t_{HD}$	Data Hold Time for the Core Register	0.00	0.00	ns
$t_{SUE}$	Enable Setup Time for the Core Register	0.48	0.57	ns
$t_{HE}$	Enable Hold Time for the Core Register	0.00	0.00	ns
$t_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.42	0.50	ns
$t_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.42	0.50	ns
$t_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
$t_{RECLR}$	Asynchronous Clear Recovery Time for the Core Register	0.24	0.28	ns
$t_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
$t_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.24	0.28	ns
$t_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
$t_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
$t_{CKMPWH}$	Clock Minimum Pulse Width HIGH for the Core Register	0.56	0.64	ns
$t_{CKMPWL}$	Clock Minimum Pulse Width LOW for the Core Register	0.56	0.64	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-176 • Register Delays****Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$  for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{CLKQ}$	Clock-to-Q of the Core Register	0.66	0.78	ns
$t_{SUD}$	Data Setup Time for the Core Register	0.52	0.61	ns
$t_{HD}$	Data Hold Time for the Core Register	0.00	0.00	ns
$t_{SUE}$	Enable Setup Time for the Core Register	0.55	0.64	ns
$t_{HE}$	Enable Hold Time for the Core Register	0.00	0.00	ns
$t_{CLR2Q}$	Asynchronous Clear-to-Q of the Core Register	0.48	0.56	ns
$t_{PRE2Q}$	Asynchronous Preset-to-Q of the Core Register	0.48	0.56	ns
$t_{REMCLR}$	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
$t_{RECLR}$	Asynchronous Clear Recovery Time for the Core Register	0.27	0.31	ns
$t_{REMPRE}$	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
$t_{RECPRE}$	Asynchronous Preset Recovery Time for the Core Register	0.27	0.31	ns
$t_{WCLR}$	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.30	ns
$t_{WPRE}$	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.30	ns
$t_{CKMPWH}$	Clock Minimum Pulse Width HIGH for the Core Register	0.41	0.48	ns
$t_{CKMPWL}$	Clock Minimum Pulse Width LOW for the Core Register	0.37	0.43	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

## Global Resource Characteristics

### A3P1000 Clock Tree Topology

Clock delays are device-specific. Figure 2-40 is an example of a global tree used for clock routing. The global tree presented in Figure 2-40 is driven by a CCC located on the west side of the A3P1000 device. It is used to drive all D-flip-flops in the device.

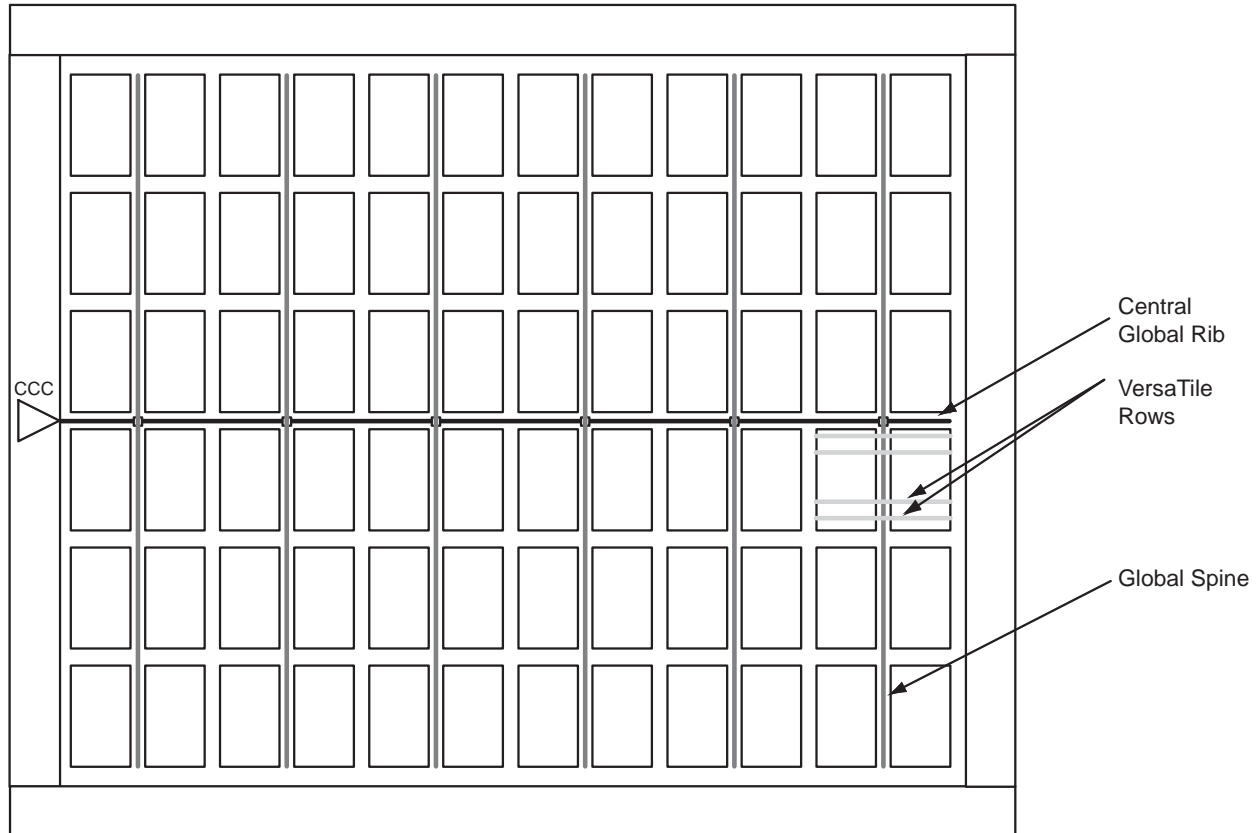


Figure 2-40 • Example of Global Tree Use in an A3P1000 Device for Clock Routing

## Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-116. Table 2-177 to Table 2-181 on page 2-115 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

#### 1.2 V DC Core Voltage

**Table 2-177 • A3PE600L Global Resource**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$

Parameter	Description	-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
t <sub>RCKL</sub>	Input LOW Delay for Global Clock					ns
t <sub>RCKH</sub>	Input HIGH Delay for Global Clock					ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width HIGH for Global Clock					ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width LOW for Global Clock					ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock					ns
F <sub>RMAX</sub>	Maximum Frequency for Global Clock					MHz

#### Notes:

- Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-178 • A3PE3000L Global Resource**  
 Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$

Parameter	Description	-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
t <sub>RCKL</sub>	Input LOW Delay for Global Clock	1.80	2.06	2.12	2.42	ns
t <sub>RCKH</sub>	Input HIGH Delay for Global Clock	1.79	2.09	2.11	2.45	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width HIGH for Global Clock					ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width LOW for Global Clock					ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.30		0.35	ns
F <sub>RMAX</sub>	Maximum Frequency for Global Clock					MHz

#### Notes:

- Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
- Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
- For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**1.5 V DC Core Voltage**
**Table 2-179 • A3PE600L Global Resource**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$** 

Parameter	Description	-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input LOW Delay for Global Clock					ns
$t_{RCKH}$	Input HIGH Delay for Global Clock					ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
$t_{RCKSW}$	Maximum Skew for Global Clock					ns
$F_{RMAX}$	Maximum Frequency for Global Clock					MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-180 • A3P1000 Global Resource**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$** 

Parameter	Description	-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input LOW Delay for Global Clock	1.18	1.44	1.39	1.70	ns
$t_{RCKH}$	Input HIGH Delay for Global Clock	1.17	1.48	1.37	1.74	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.32		0.37	ns
$F_{RMAX}$	Maximum Frequency for Global Clock					MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.



**Table 2-181 • A3PE3000L Global Resource**  
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input LOW Delay for Global Clock	1.61	1.85	1.89	2.17	ns
$t_{RCKH}$	Input HIGH Delay for Global Clock	1.60	1.87	1.88	2.20	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock					ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock					ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.27		0.32	ns
$F_{RMAX}$	Maximum Frequency for Global Clock					MHz

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

## Clock Conditioning Circuits

### CCC Electrical Specifications

#### Timing Characteristics

**Table 2-182 • Military ProASIC3/EL CCC/PLL Specification**  
 For Devices Operating at 1.2 V DC Core Voltage: Applicable to A3PE600L and A3PE3000L Only

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$	0.75		250	MHz
Delay Increments in Programmable Delay Blocks <sup>1, 2</sup>		270		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL <sup>3</sup>			100	MHz
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$	Max Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 250 MHz	2.50%	3.75%	2.75%	
Acquisition Time	LockControl = 0		300	μs
		LockControl = 1		6.0
Tracking Jitter	LockControl = 0		2	ns
		LockControl = 1		1
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 <sup>1, 2</sup>	1.2		15.65	ns
Delay Range in Block: Programmable Delay 2 <sup>1, 2</sup>	0.025		15.65	ns
Delay Range in Block: Fixed Delay <sup>1, 2</sup>		3.1		ns

**Notes:**

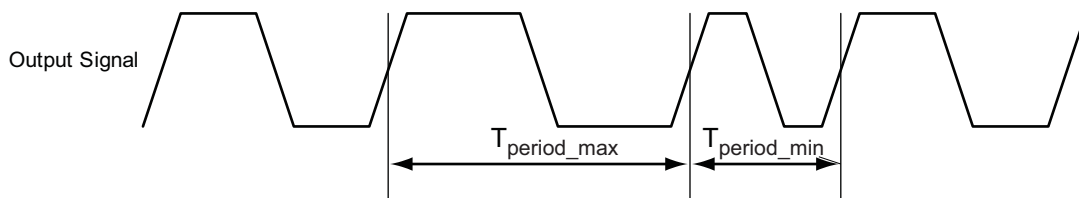
1. This delay is a function of voltage and temperature. See [Table 2-5 on page 2-8](#) for deratings.
2.  $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 1.2\text{ V}$
3. Maximum value obtained for a Std. speed grade device in worst-case military conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.
4. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.

**Table 2-183 • Military ProASIC3/EL CCC/PLL Specification  
For Devices Operating at 1.5 V DC Core Voltage**

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$	0.75		350	MHz
Serial Clock (SCLK) for Dynamic PLL <sup>5</sup>			110	MHz
Delay Increments in Programmable Delay Blocks <sup>1,2</sup>		200		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time				
	LockControl = 0		300	$\mu$ s
	LockControl = 1		6.0	ms
Tracking Jitter				
	LockControl = 0		1.6	ns
	LockControl = 1		0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 <sup>1,2</sup>	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 <sup>1,2</sup>	0.025		5.56	ns
Delay Range in Block: Fixed Delay <sup>1,2</sup>		2.2		ns

**Notes:**

1. This delay is a function of voltage and temperature. See [Table 2-5 on page 2-8](#) for deratings.
2.  $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 1.5\text{ V}$
3. Maximum value obtained for a Std. speed grade device in worst-case military conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.
4. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.
5. Maximum value obtained for a -1 speed grade device in worst-case military conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.



**Note:** Peak-to-peak jitter measurements are defined by  $T_{peak-to-peak} = T_{period\_max} - T_{period\_min}$

**Figure 2-41 • Peak-to-Peak Jitter Definition**

# Embedded SRAM and FIFO Characteristics

## SRAM

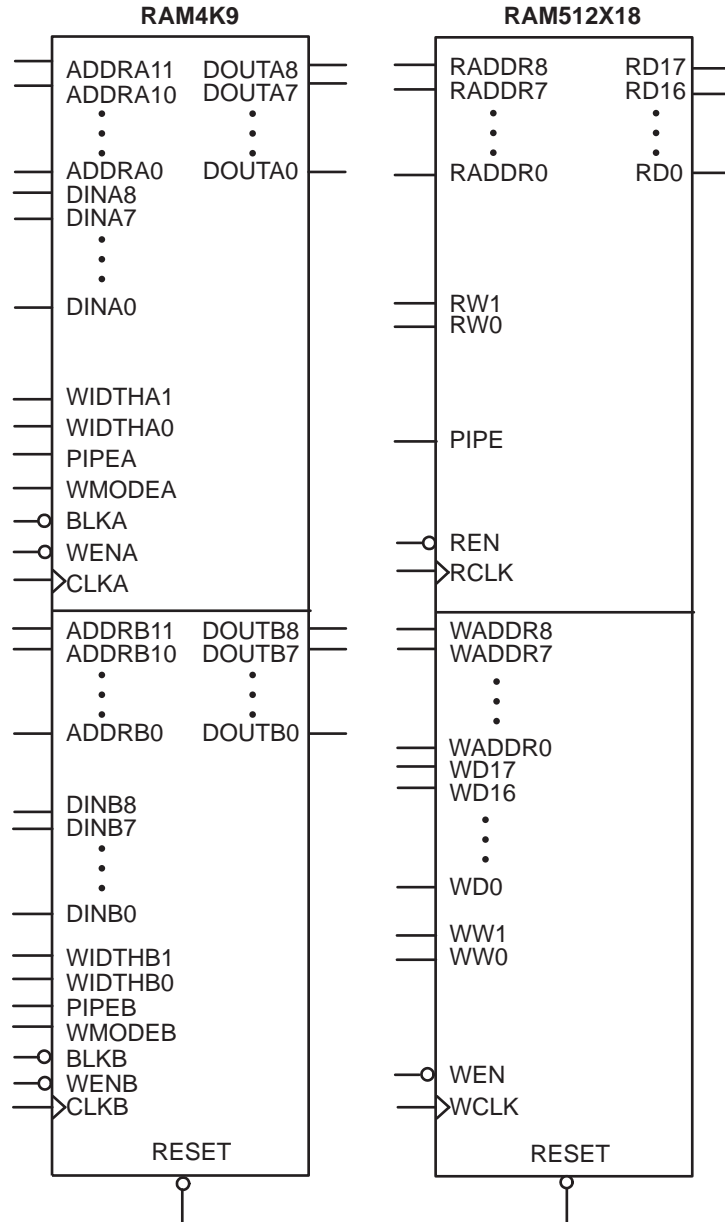


Figure 2-42 • RAM Models

## Timing Waveforms

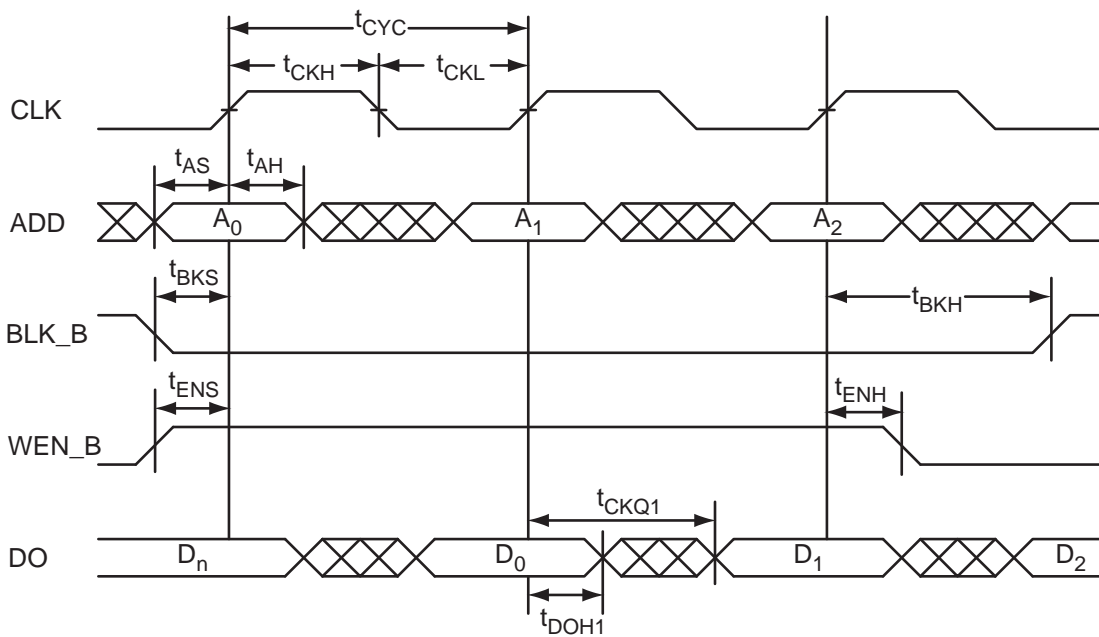


Figure 2-43 • RAM Read for Pass-Through Output

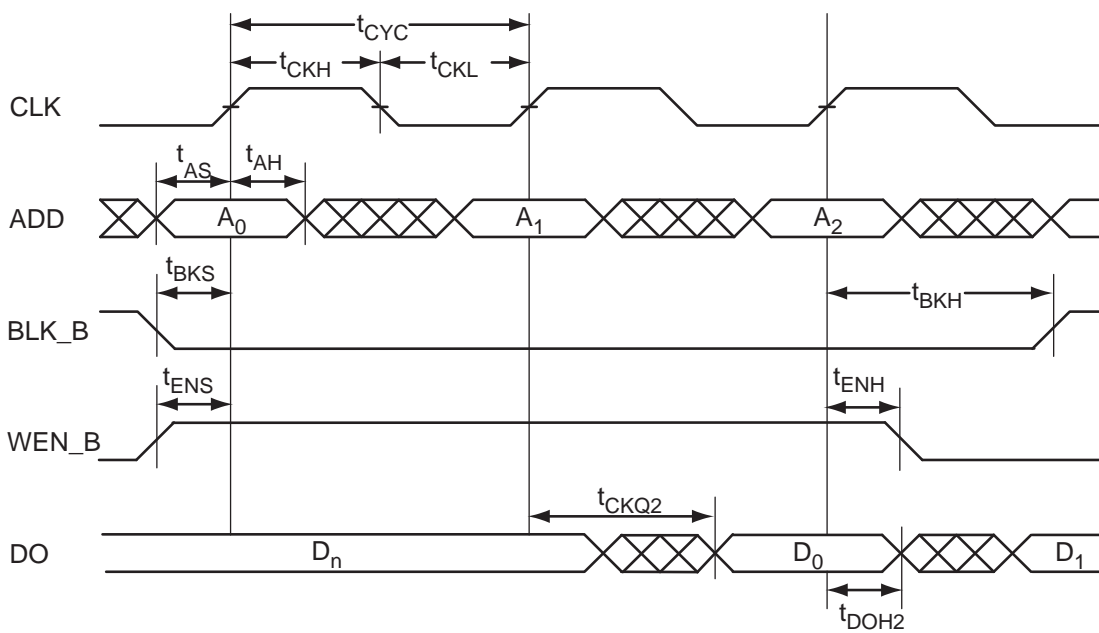


Figure 2-44 • RAM Read for Pipelined Output

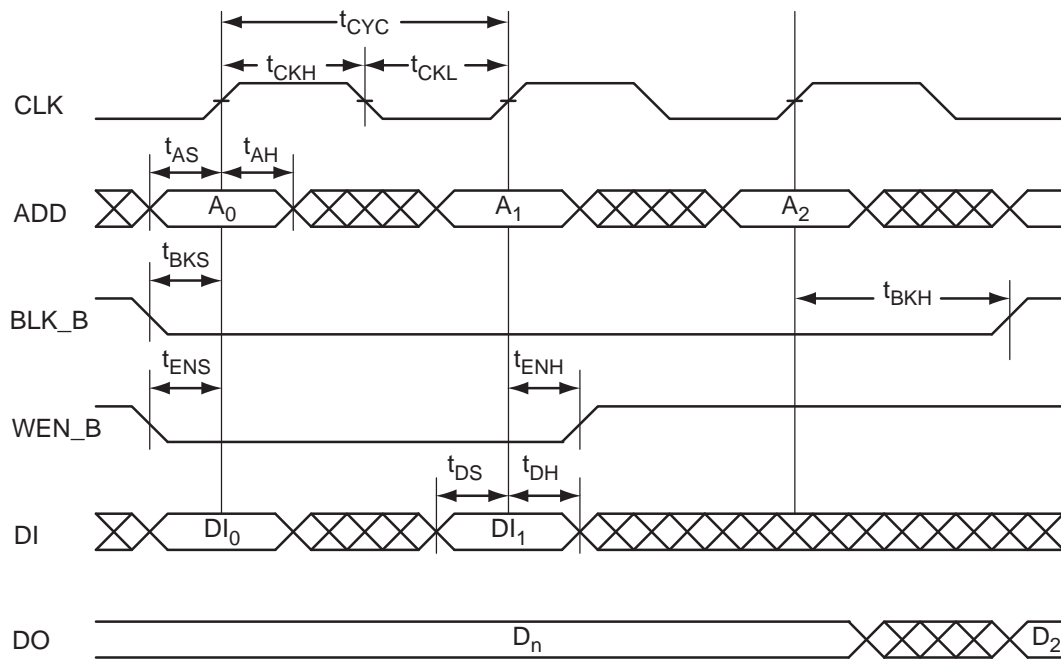


Figure 2-45 • RAM Write, Output Retained (WMODE = 0)

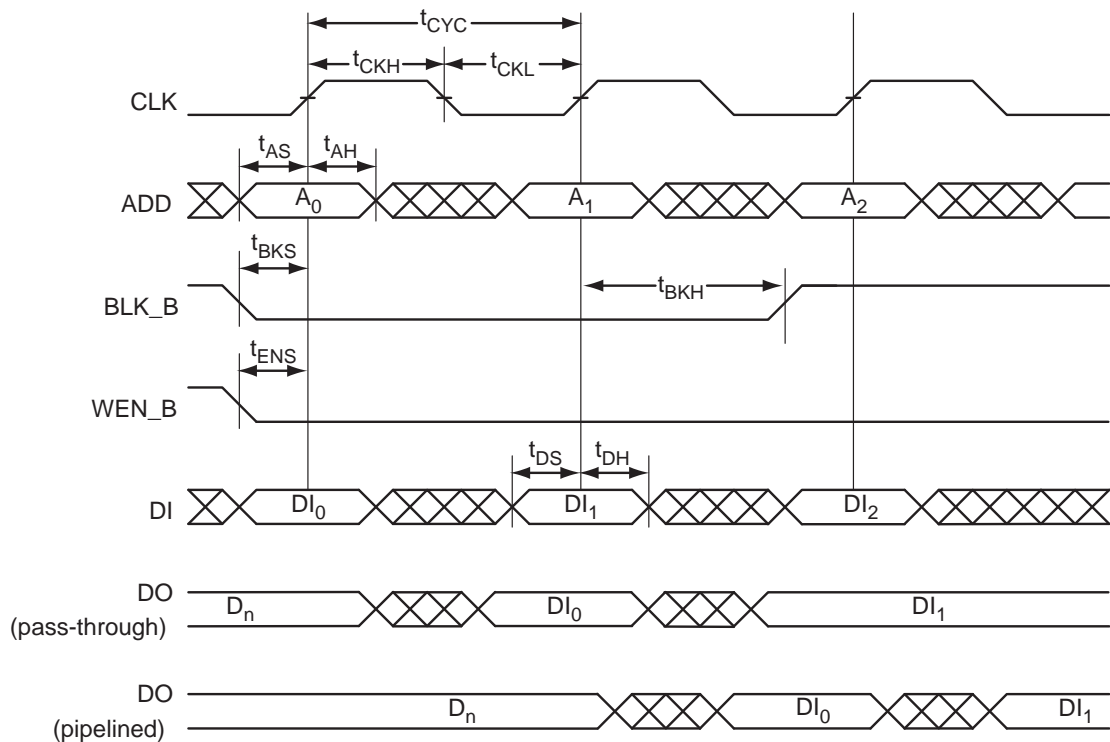


Figure 2-46 • RAM Write, Output as Write Data (WMODE = 1)

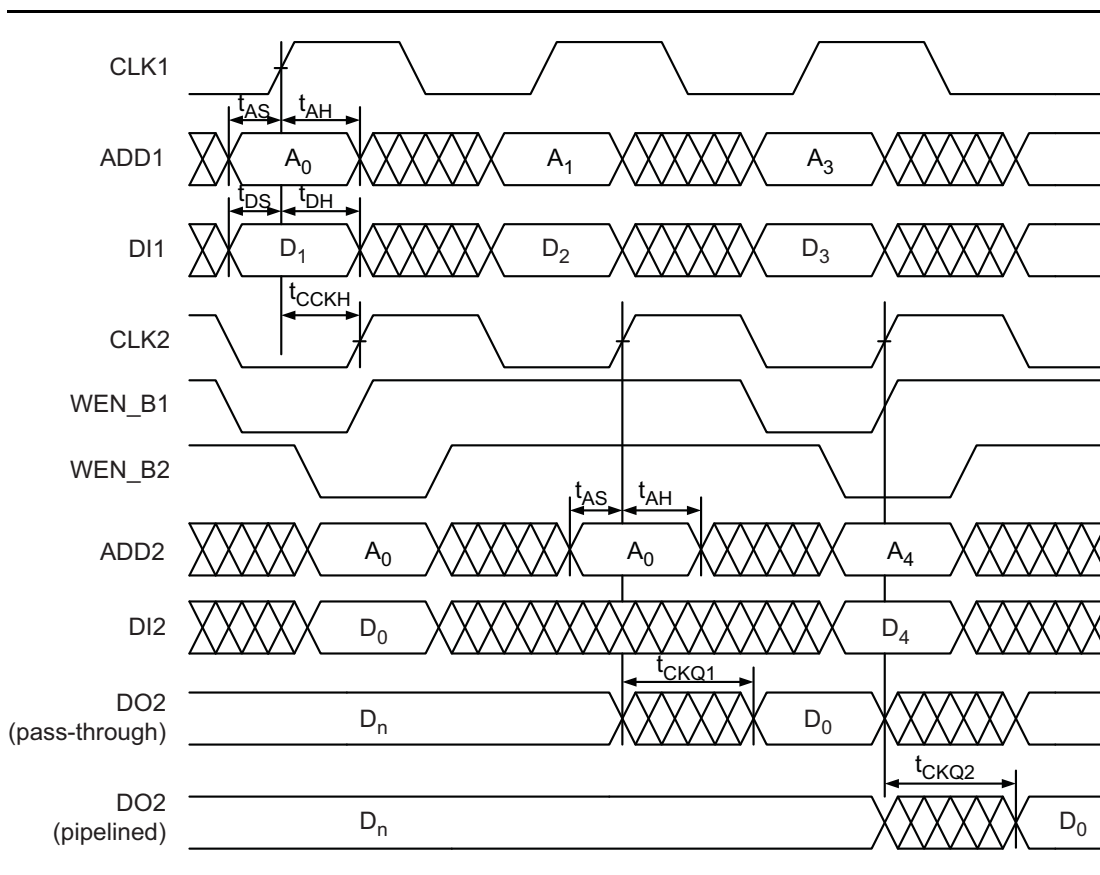


Figure 2-47 • Write Access after Write onto Same Address

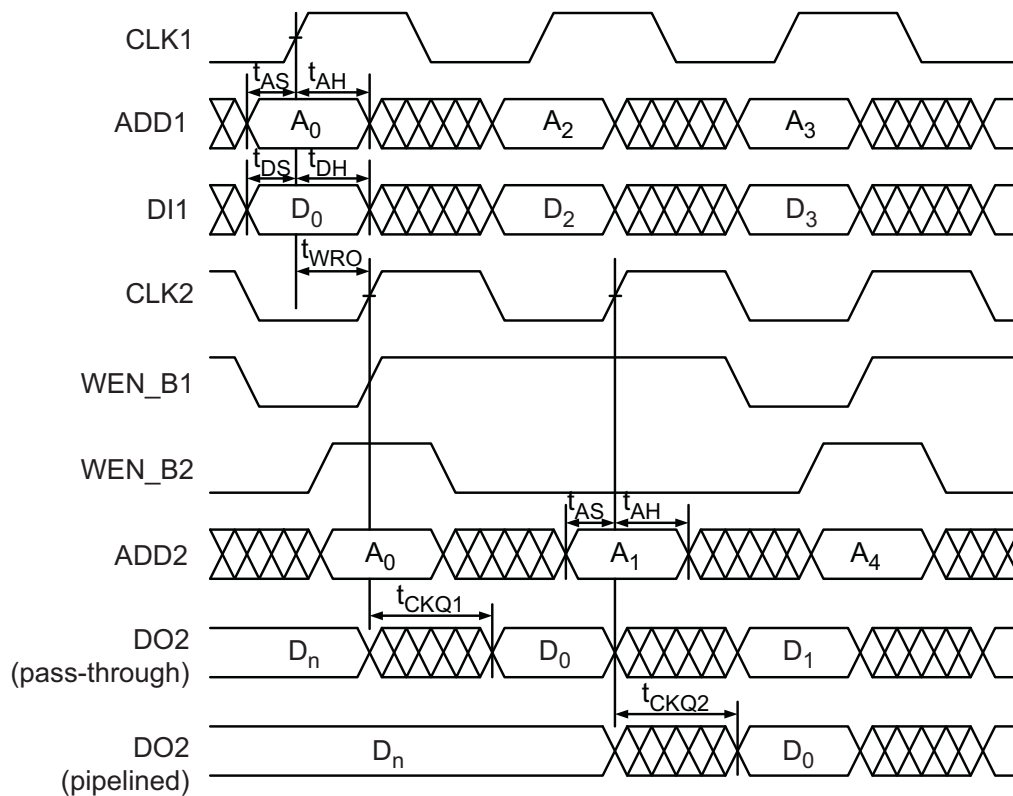
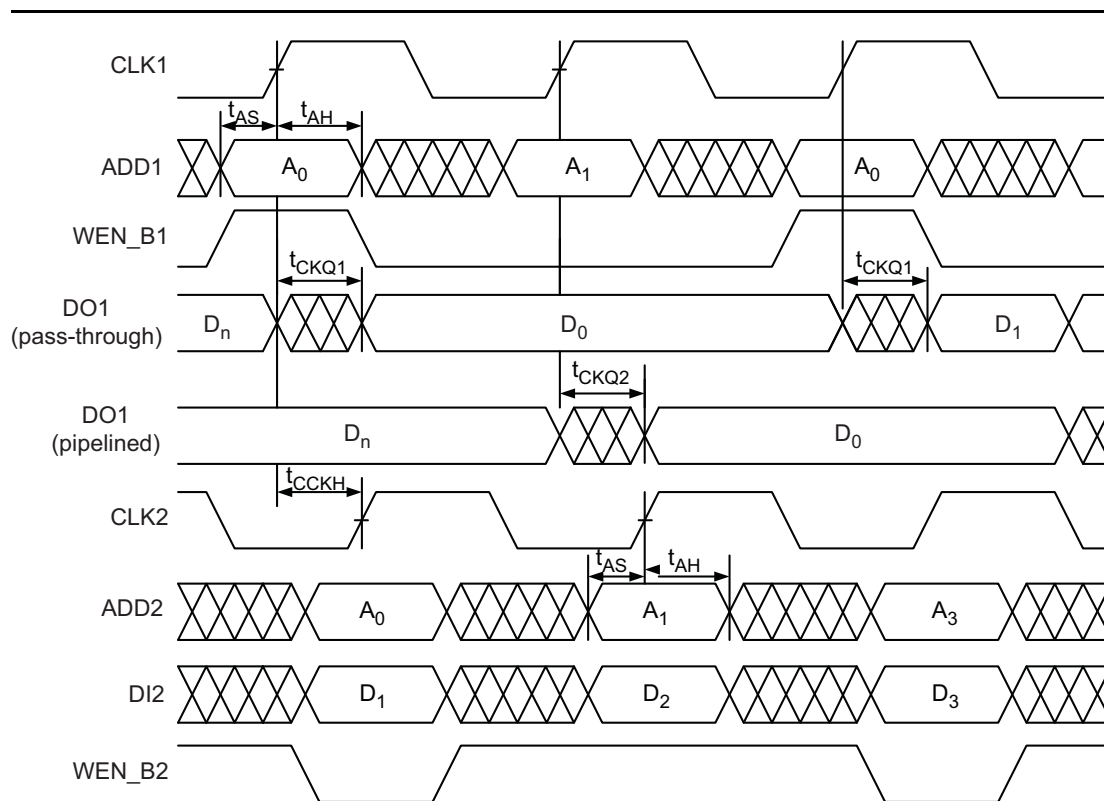
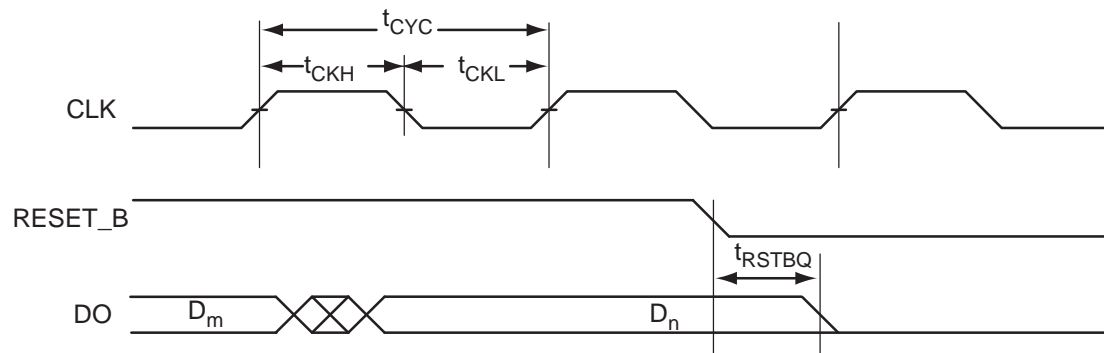


Figure 2-48 • Read Access after Write onto Same Address





**Figure 2-49 • Write Access after Read onto Same Address**



**Figure 2-50 • RAM Reset**

## Timing Characteristics

**Table 2-184 • RAM4K9**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L**

Parameter	Description	-1	Std.	Units
$t_{AS}$	Address setup time	0.35	0.41	ns
$t_{AH}$	Address hold time	0.00	0.00	ns
$t_{ENS}$	REN_B, WEN_B setup time	0.20	0.23	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.13	0.16	ns
$t_{BKS}$	BLK_B setup time	0.32	0.38	ns
$t_{BKH}$	BLK_B hold time	0.03	0.03	ns
$t_{DS}$	Input data (DI) setup time	0.25	0.30	ns
$t_{DH}$	Input data (DI) hold time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	2.47	2.91	ns
	Clock HIGH to new data valid on DO (flow-through, WMODE = 1)	3.26	3.84	ns
$t_{CKQ2}$	Clock HIGH to new data valid on DO (pipelined)	1.24	1.46	ns
$t_{WRO}$	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
$t_{CCKH}$	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
$t_{RSTBQ}$	RESET_B LOW to data out LOW on DO (flow-through)	1.28	1.50	ns
	RESET_B LOW to data out LOW on DO (pipelined)	1.28	1.50	ns
$t_{REMRSTB}$	RESET_B removal	0.40	0.47	ns
$t_{RECRSTB}$	RESET_B recovery	2.08	2.44	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.66	0.76	ns
$t_{CYC}$	Clock cycle time	6.08	6.99	ns
$F_{MAX}$	Maximum frequency	164	143	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

Table 2-185 • RAM4K9

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{AS}$	Address setup time	0.26	0.31	ns
$t_{AH}$	Address hold time	0.00	0.00	ns
$t_{ENS}$	REN_B, WEN_B setup time	0.15	0.18	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.10	0.12	ns
$t_{BKS}$	BLK_B setup time	0.25	0.29	ns
$t_{BKH}$	BLK_B hold time	0.02	0.02	ns
$t_{DS}$	Input data (DI) setup time	0.19	0.23	ns
$t_{DH}$	Input data (DI) hold time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	1.89	2.22	ns
	Clock HIGH to new data valid on DO (flow-through, WMODE = 1)	2.50	2.93	ns
$t_{CKQ2}$	Clock HIGH to new data valid on DO (pipelined)	0.95	1.11	ns
$t_{WRO}$	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
$t_{CCKH}$	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
$t_{RSTBQ}$	RESET_B LOW to data out LOW on DO (flow-through)	0.98	1.15	ns
	RESET_B LOW to data out LOW on DO (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET_B removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET_B recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.59	0.67	ns
$t_{CYC}$	Clock cycle time	5.39	6.20	ns
$F_{MAX}$	Maximum frequency	185	161	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-186 • RAM4K9**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$  for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{AS}$	Address setup time	0.30	0.35	ns
$t_{AH}$	Address hold time	0.00	0.00	ns
$t_{ENS}$	REN_B, WEN_B setup time	0.17	0.20	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.12	0.14	ns
$t_{BKS}$	BLK_B setup time	0.28	0.33	ns
$t_{BKH}$	BLK_B hold time	0.02	0.03	ns
$t_{DS}$	Input data (DI) setup time	0.22	0.26	ns
$t_{DH}$	Input data (DI) hold time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	2.15	2.53	ns
	Clock HIGH to new data valid on DO (flow-through, WMODE = 1)	2.84	3.33	ns
$t_{CKQ2}$	Clock HIGH to new data valid on DO (pipelined)	1.08	1.27	ns
$t_{WRO}$	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
$t_{CCKH}$	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
$t_{RSTBQ}$	RESET_B LOW to data out LOW on DO (flow-through)	1.11	1.31	ns
	RESET_B LOW to data out LOW on DO (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET_B removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET_B recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.26	0.30	ns
$t_{CYC}$	Clock cycle time	3.89	4.57	ns
$F_{MAX}$	Maximum frequency	257	219	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

Table 2-187 • RAM512X18

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{AS}$	Address setup time	0.35	0.41	ns
$t_{AH}$	Address hold time	0.00	0.00	ns
$t_{ENS}$	REN_B, WEN_B setup time	0.13	0.15	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.08	0.09	ns
$t_{DS}$	Input data (DI) setup time	0.25	0.30	ns
$t_{DH}$	Input data (DI) hold time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	2.99	3.52	ns
$t_{CKQ2}$	Clock HIGH to new data valid on DO (pipelined)	1.24	1.46	ns
$t_{WRO}$	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
$t_{CCKH}$	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
$t_{RSTBQ}$	RESET_B LOW to data out LOW on DO (flow through)	1.28	1.50	ns
	RESET_B LOW to data out LOW on DO (pipelined)	1.28	1.50	ns
$t_{REMRSTB}$	RESET_B removal	0.40	0.47	ns
$t_{RECRSTB}$	RESET_B recovery	2.08	2.44	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.66	0.76	ns
$t_{CYC}$	Clock cycle time	6.08	6.99	ns
$F_{MAX}$	Maximum frequency	164	143	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-188 • RAM512X18**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L and A3PE3000L**

Parameter	Description	-1	Std.	Units
$t_{AS}$	Address setup time	0.26	0.31	ns
$t_{AH}$	Address hold time	0.00	0.00	ns
$t_{ENS}$	REN_B, WEN_B setup time	0.10	0.11	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.06	0.07	ns
$t_{DS}$	Input data (DI) setup time	0.19	0.23	ns
$t_{DH}$	Input data (DI) hold time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	2.29	2.69	ns
$t_{CKQ2}$	Clock HIGH to new data valid on DO (pipelined)	0.95	1.12	ns
$t_{WRO}$	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
$t_{CCKH}$	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
$t_{RSTBQ}$	RESET_B LOW to data out LOW on DO (flow through)	0.98	1.15	ns
	RESET_B LOW to data out LOW on DO (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET_B removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET_B recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.59	0.67	ns
$t_{CYC}$	Clock cycle time	5.39	6.20	ns
$F_{MAX}$	Maximum frequency	185	161	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-8](#) for derating values.

**Table 2-189 • RAM512X18**
**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{AS}$	Address setup time	0.30	0.35	ns
$t_{AH}$	Address hold time	0.00	0.00	ns
$t_{ENS}$	REN_B, WEN_B setup time	0.11	0.13	ns
$t_{ENH}$	REN_B, WEN_B hold time	0.07	0.08	ns
$t_{DS}$	Input data (DI) setup time	0.22	0.26	ns
$t_{DH}$	Input data (DI) hold time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	2.60	3.06	ns
$t_{CKQ2}$	Clock HIGH to new data valid on DO (pipelined)	1.08	1.27	ns
$t_{WRO}$	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
$t_{CCKH}$	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
$t_{RSTBQ}$	RESET_B LOW to data out LOW on DO (flow through)	1.11	1.31	ns
	RESET_B LOW to data out LOW on DO (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET_B removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET_B recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.26	0.30	ns
$t_{CYC}$	Clock cycle time	3.89	4.57	ns
$F_{MAX}$	Maximum frequency	257	219	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

## FIFO

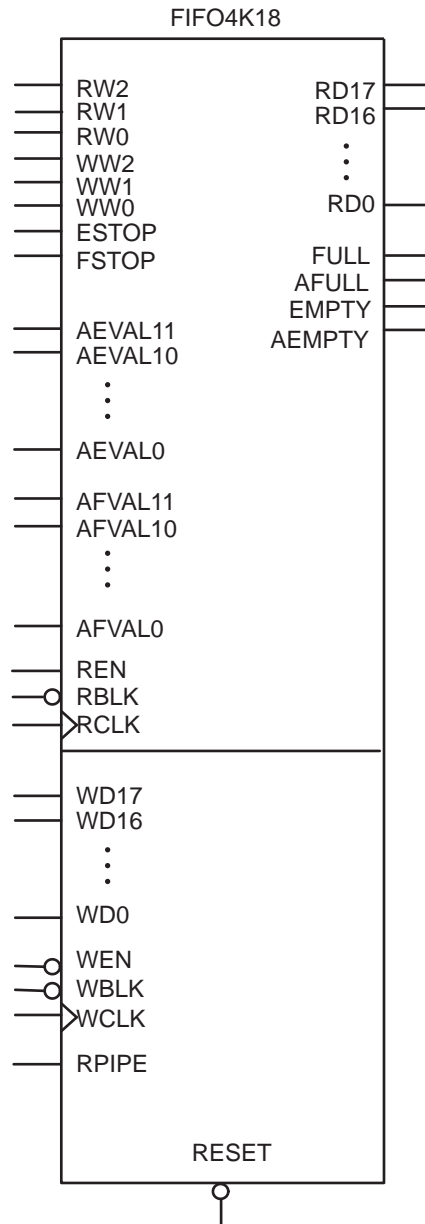


Figure 2-51 • FIFO Model



## Timing Waveforms

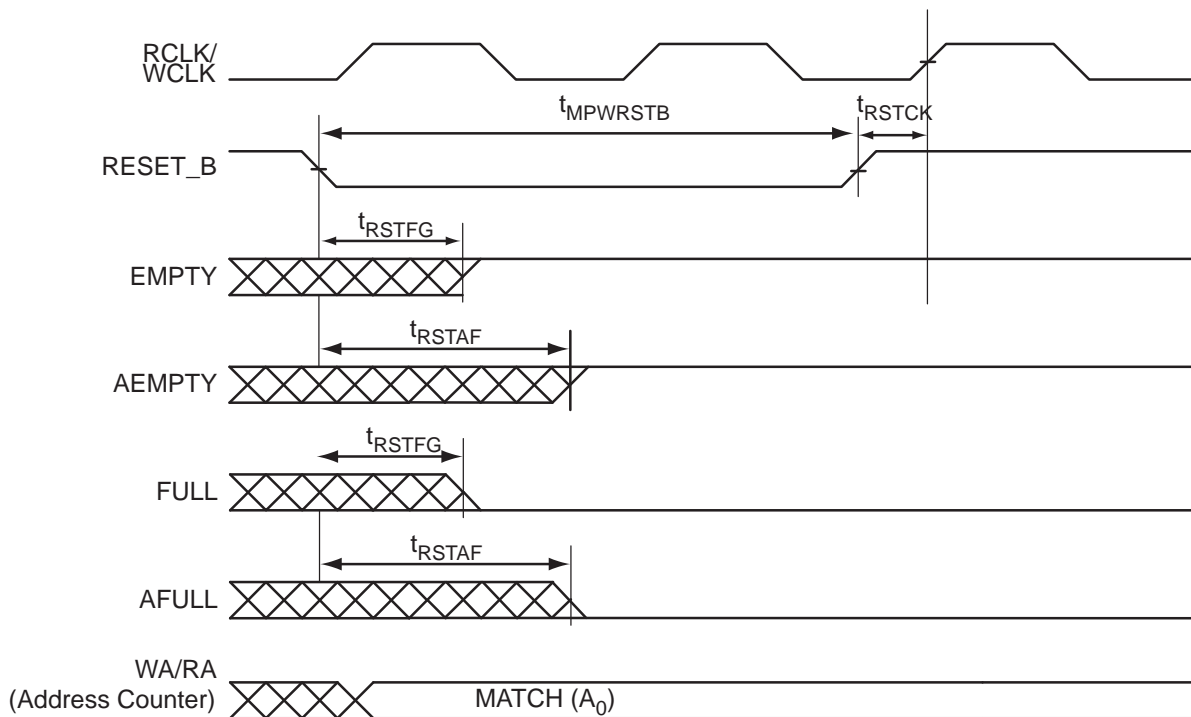


Figure 2-52 • FIFO Reset

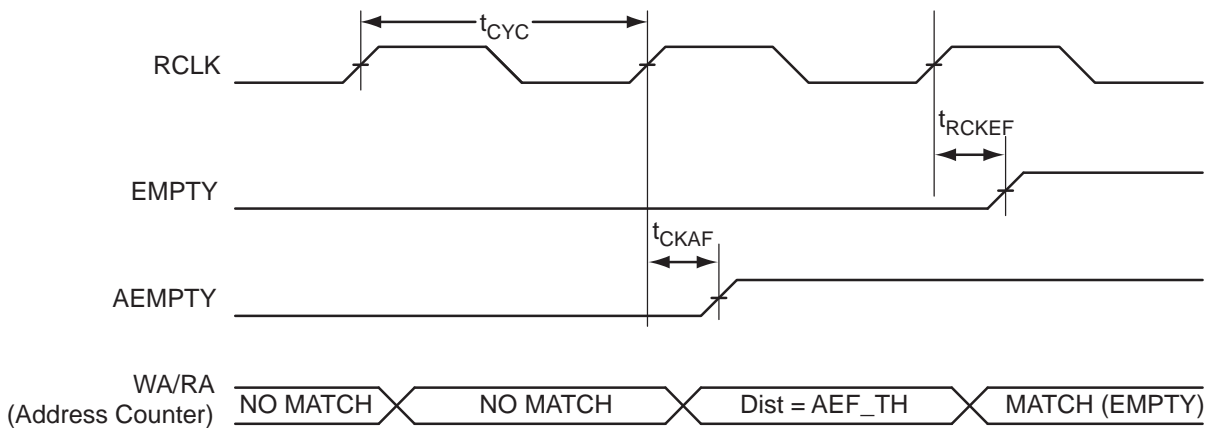


Figure 2-53 • FIFO EMPTY Flag and AEMPTY Flag Assertion

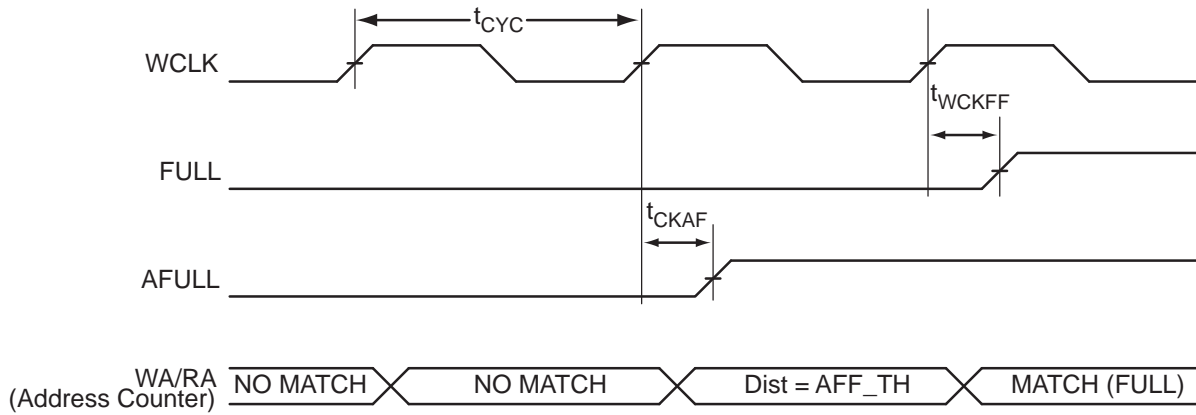


Figure 2-54 • FIFO FULL Flag and AFULL Flag Assertion

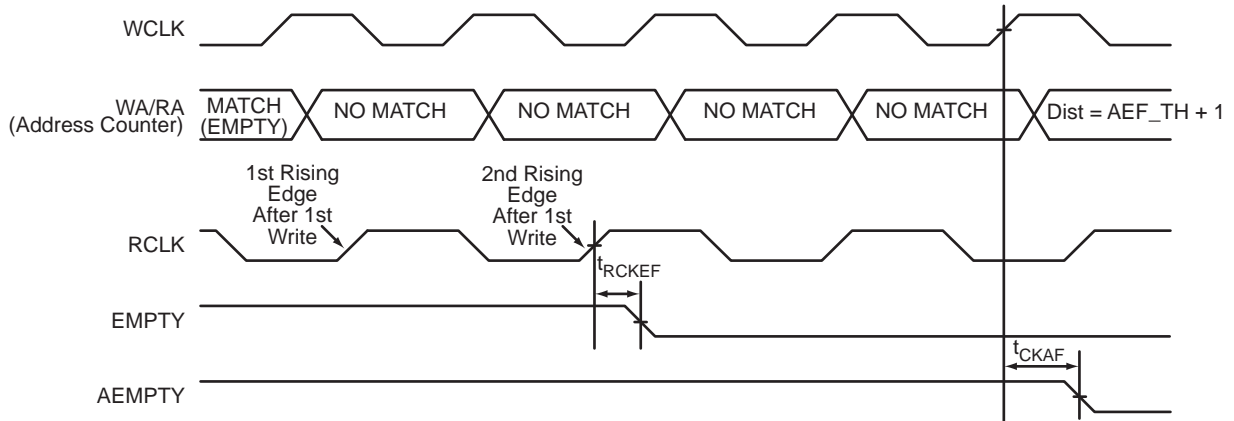


Figure 2-55 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

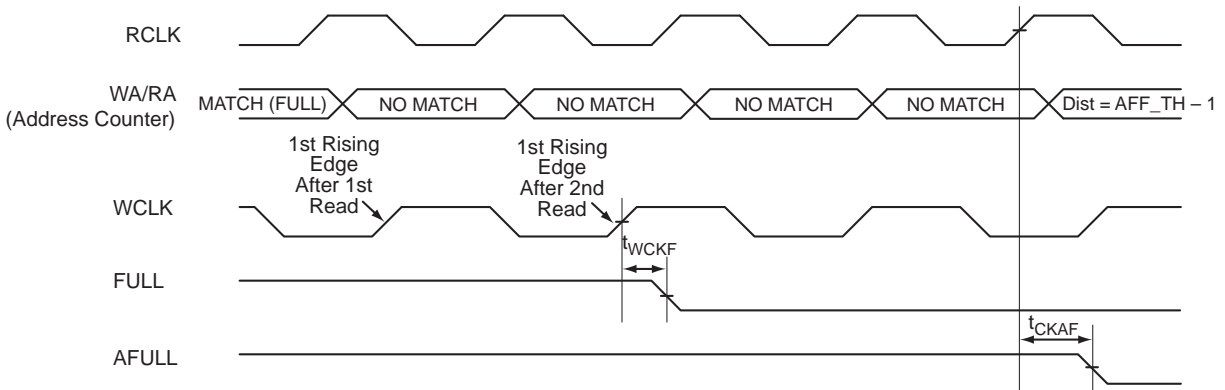


Figure 2-56 • FIFO FULL Flag and AFULL Flag Deassertion

## Timing Characteristics

Table 2-190 • FIFO

Worst Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{ENS}$	REN_B, WEN_B Setup Time	1.91	2.24	ns
$t_{ENH}$	REN_B, WEN_B Hold Time	0.03	0.03	ns
$t_{BKS}$	BLK_B Setup Time	0.40	0.47	ns
$t_{BKH}$	BLK_B Hold Time	0.00	0.00	ns
$t_{DS}$	Input Data (DI) Setup Time	0.25	0.30	ns
$t_{DH}$	Input Data (DI) Hold Time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to New Data Valid on DO (flow-through)	3.26	3.84	ns
$t_{CKQ2}$	Clock HIGH to New Data Valid on DO (pipelined)	1.24	1.46	ns
$t_{RCKEF}$	RCLK HIGH to Empty Flag Valid	2.38	2.80	ns
$t_{WCKFF}$	WCLK HIGH to Full Flag Valid	2.26	2.66	ns
$t_{CKAF}$	Clock HIGH to Almost Empty/Full Flag Valid	8.57	10.08	ns
$t_{RSTFG}$	RESET_B LOW to Empty/Full Flag Valid	2.34	2.76	ns
$t_{RSTAF}$	RESET_B LOW to Almost Empty/Full Flag Valid	8.48	9.97	ns
$t_{RSTBQ}$	RESET_B LOW to Data Out LOW on DO (flow-through)	1.28	1.50	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.28	1.50	ns
$t_{REMRSTB}$	RESET_B Removal	0.40	0.47	ns
$t_{RECRSTB}$	RESET_B Recovery	2.08	2.44	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.66	0.76	ns
$t_{CYC}$	Clock Cycle Time	6.08	6.99	ns
$F_{MAX}$	Maximum Frequency for FIFO	164	143	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-191 • FIFO**
**Worst Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L and A3PE3000L**

Parameter	Description	-1	Std.	Units
$t_{ENS}$	REN_B, WEN_B Setup Time	1.46	1.71	ns
$t_{ENH}$	REN_B, WEN_B Hold Time	0.02	0.02	ns
$t_{BKS}$	BLK_B Setup Time	0.40	0.47	ns
$t_{BKH}$	BLK_B Hold Time	0.00	0.00	ns
$t_{DS}$	Input Data (DI) Setup Time	0.19	0.23	ns
$t_{DH}$	Input Data (DI) Hold Time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to New Data Valid on DO (flow-through)	2.50	2.93	ns
$t_{CKQ2}$	Clock HIGH to New Data Valid on DO (pipelined)	0.95	1.11	ns
$t_{RCKEF}$	RCLK HIGH to Empty Flag Valid	1.82	2.14	ns
$t_{WCKFF}$	WCLK HIGH to Full Flag Valid	1.73	2.03	ns
$t_{CKAF}$	Clock HIGH to Almost Empty/Full Flag Valid	6.56	7.71	ns
$t_{RSTFG}$	RESET_B LOW to Empty/Full Flag Valid	1.79	2.11	ns
$t_{RSTAF}$	RESET_B LOW to Almost Empty/Full Flag Valid	6.49	7.63	ns
$t_{RSTBQ}$	RESET_B LOW to Data Out LOW on DO (flow-through)	0.98	1.15	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	0.98	1.15	ns
$t_{REMRSTB}$	RESET_B Removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET_B Recovery	1.59	1.87	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.59	0.67	ns
$t_{CYC}$	Clock Cycle Time	5.39	6.20	ns
$F_{MAX}$	Maximum Frequency for FIFO	185	161	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-192 • FIFO**
**Worst Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3P1000**

Parameter	Description	-1	Std.	Units
$t_{ENS}$	REN_B, WEN_B Setup Time	1.66	1.95	ns
$t_{ENH}$	REN_B, WEN_B Hold Time	0.02	0.03	ns
$t_{BKS}$	BLK_B Setup Time	0.40	0.47	ns
$t_{BKH}$	BLK_B Hold Time	0.00	0.00	ns
$t_{DS}$	Input Data (DI) Setup Time	0.22	0.26	ns
$t_{DH}$	Input Data (DI) Hold Time	0.00	0.00	ns
$t_{CKQ1}$	Clock HIGH to New Data Valid on DO (flow-through)	2.84	3.33	ns
$t_{CKQ2}$	Clock HIGH to New Data Valid on DO (pipelined)	1.08	1.27	ns
$t_{RCKEF}$	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
$t_{WCKFF}$	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
$t_{CKAF}$	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
$t_{RSTFG}$	RESET_B LOW to Empty/Full Flag Valid	2.04	2.40	ns
$t_{RSTAF}$	RESET_B LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
$t_{RSTBQ}$	RESET_B LOW to Data Out LOW on DO (flow-through)	1.11	1.31	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET_B Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET_B Recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.26	0.30	ns
$t_{CYC}$	Clock Cycle Time	3.89	4.57	ns
$F_{MAX}$	Maximum Frequency for FIFO	257	219	MHz

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-8](#) for derating values.

## Embedded FlashROM Characteristics

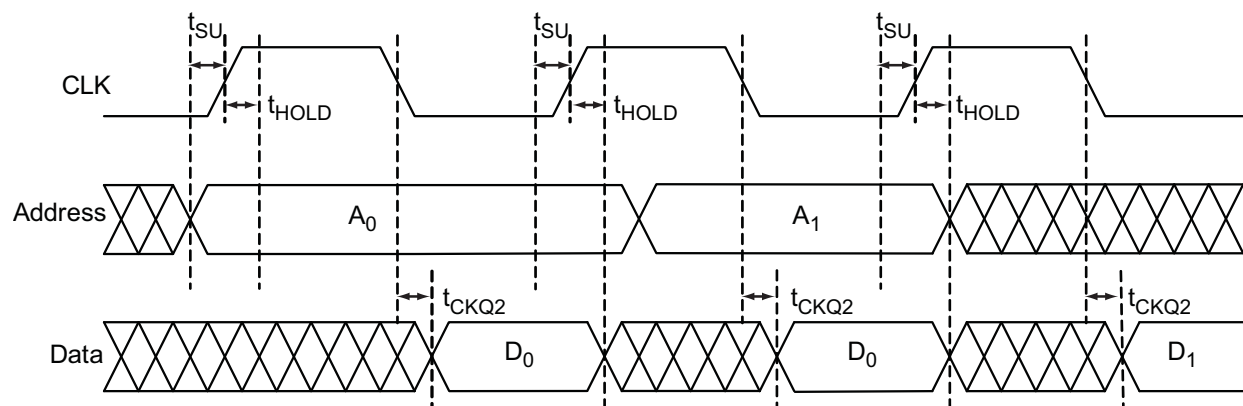


Figure 2-57 • Timing Diagram

### Timing Characteristics

Table 2-193 • Embedded FlashROM Access Time

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.14\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{SU}$	Address Setup Time	0.74	0.87	ns
$t_{HOLD}$	Address Hold Time	0.00	0.00	ns
$t_{CKQ2}$	Clock to Out	22.47	26.42	ns
$F_{MAX}$	Maximum Clock Frequency	15	15	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

Table 2-194 • Embedded FlashROM Access Time

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$  for A3PE600L and A3PE3000L

Parameter	Description	-1	Std.	Units
$t_{SU}$	Address Setup Time	0.56	0.66	ns
$t_{HOLD}$	Address Hold Time	0.00	0.00	ns
$t_{CKQ2}$	Clock to Out	17.19	20.21	ns
$F_{MAX}$	Maximum Clock Frequency	15	15	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

Table 2-195 • Embedded FlashROM Access Time

Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$  for A3P1000

Parameter	Description	-1	Std.	Units
$t_{SU}$	Address Setup Time	0.64	0.75	ns
$t_{HOLD}$	Address Hold Time	0.00	0.00	ns
$t_{CKQ2}$	Clock to Out	19.54	22.97	ns
$F_{MAX}$	Maximum Clock Frequency	15	15	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-8 for derating values.

## JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

### Timing Characteristics

**Table 2-196 • JTAG 1532**

**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L**

Parameter	Description	-1	Std.	Units
$t_{\text{DISU}}$	Test Data Input Setup Time	0.80	0.94	ns
$t_{\text{DIHD}}$	Test Data Input Hold Time	1.60	1.88	ns
$t_{\text{TMSSU}}$	Test Mode Select Setup Time	0.80	0.94	ns
$t_{\text{TMDHD}}$	Test Mode Select Hold Time	1.60	1.88	ns
$t_{\text{TCK2Q}}$	Clock to Q (data out)	6.39	7.52	ns
$t_{\text{RSTB2Q}}$	Reset to Q (data out)	26.63	31.33	ns
$F_{\text{TCKMAX}}$	TCK Maximum Frequency	18.70	15.90	MHz
$t_{\text{TRSTREM}}$	ResetB Removal Time	0.48	0.56	ns
$t_{\text{TRSTREC}}$	ResetB Recovery Time	0.00	0.00	ns
$t_{\text{TRSTMPW}}$	ResetB Minimum Pulse	TBD	TBD	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.

**Table 2-197 • JTAG 1532**

**Military-Case Conditions:  $T_J = 125^\circ\text{C}$ , Worst-Case VCC = 1.425 V for All Dies**

Parameter	Description	-1	Std.	Units
$t_{\text{DISU}}$	Test Data Input Setup Time	0.60	0.71	ns
$t_{\text{DIHD}}$	Test Data Input Hold Time	1.21	1.42	ns
$t_{\text{TMSSU}}$	Test Mode Select Setup Time	0.60	0.71	ns
$t_{\text{TMDHD}}$	Test Mode Select Hold Time	1.21	1.42	ns
$t_{\text{TCK2Q}}$	Clock to Q (data out)	6.04	7.10	ns
$t_{\text{RSTB2Q}}$	Reset to Q (data out)	24.15	28.41	ns
$F_{\text{TCKMAX}}$	TCK Maximum Frequency	22.00	19.00	MHz
$t_{\text{TRSTREM}}$	ResetB Removal Time	0.00	0.00	ns
$t_{\text{TRSTREC}}$	ResetB Recovery Time	0.24	0.28	ns
$t_{\text{TRSTMPW}}$	ResetB Minimum Pulse	TBD	TBD	ns

*Note:* For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-8 for derating values.





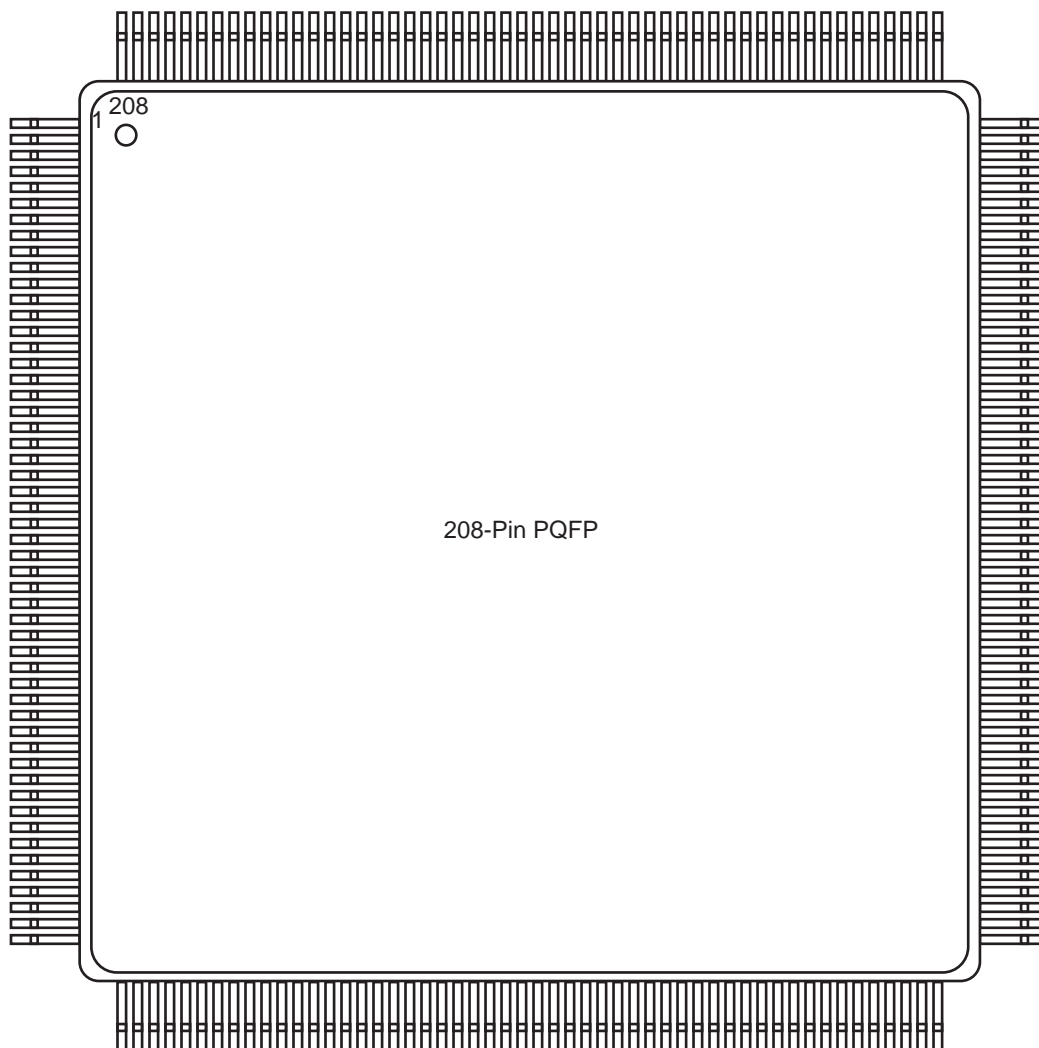
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## 3 – Package Pin Assignments

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### 208-Pin PQFP

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*Note:* This is the top view of the package.

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#### **Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

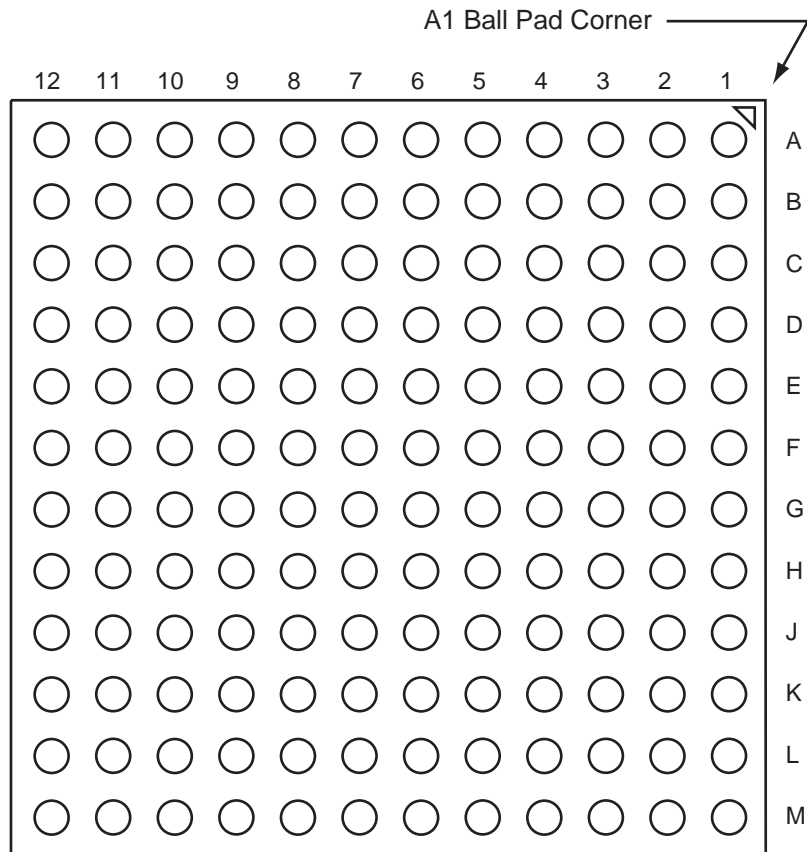
208-Pin PQFP		208-Pin PQFP		208-Pin PQFP	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
1	GND	37	IO199PDB3	73	IO162RSB2
2	GAA2/IO225PDB3	38	IO199NDB3	74	IO160RSB2
3	IO225NDB3	39	IO197PSB3	75	IO158RSB2
4	GAB2/IO224PDB3	40	VCCIB3	76	IO156RSB2
5	IO224NDB3	41	GND	77	IO154RSB2
6	GAC2/IO223PDB3	42	IO191PDB3	78	IO152RSB2
7	IO223NDB3	43	IO191NDB3	79	IO150RSB2
8	IO222PDB3	44	GEC1/IO190PDB3	80	IO148RSB2
9	IO222NDB3	45	GEC0/IO190NDB3	81	GND
10	IO220PDB3	46	GEB1/IO189PDB3	82	IO143RSB2
11	IO220NDB3	47	GEB0/IO189NDB3	83	IO141RSB2
12	IO218PDB3	48	GEA1/IO188PDB3	84	IO139RSB2
13	IO218NDB3	49	GEA0/IO188NDB3	85	IO137RSB2
14	IO216PDB3	50	VMV3	86	IO135RSB2
15	IO216NDB3	51	GNDQ	87	IO133RSB2
16	VCC	52	GND	88	VCC
17	GND	53	VMV2	89	VCCIB2
18	VCCIB3	54	GEA2/IO187RSB2	90	IO128RSB2
19	IO212PDB3	55	GEB2/IO186RSB2	91	IO126RSB2
20	IO212NDB3	56	GEC2/IO185RSB2	92	IO124RSB2
21	GFC1/IO209PDB3	57	IO184RSB2	93	IO122RSB2
22	GFC0/IO209NDB3	58	IO183RSB2	94	IO120RSB2
23	GFB1/IO208PDB3	59	IO182RSB2	95	IO118RSB2
24	GFB0/IO208NDB3	60	IO181RSB2	96	GDC2/IO116RSB2
25	VCOMPLF	61	IO180RSB2	97	GND
26	GFA0/IO207NPB3	62	VCCIB2	98	GDB2/IO115RSB2
27	VCCPLF	63	IO178RSB2	99	GDA2/IO114RSB2
28	GFA1/IO207PPB3	64	IO176RSB2	100	GNDQ
29	GND	65	GND	101	TCK
30	GFA2/IO206PDB3	66	IO174RSB2	102	TDI
31	IO206NDB3	67	IO172RSB2	103	TMS
32	GFB2/IO205PDB3	68	IO170RSB2	104	VMV2
33	IO205NDB3	69	IO168RSB2	105	GND
34	GFC2/IO204PDB3	70	IO166RSB2	106	VPUMP
35	IO204NDB3	71	VCC	107	GNDQ
36	VCC	72	VCCIB2	108	TDO

208-Pin PQFP	
Pin Number	A3P1000 Function
109	TRST
110	VJTAG
111	GDA0/IO113NDB1
112	GDA1/IO113PDB1
113	GDB0/IO112NDB1
114	GDB1/IO112PDB1
115	GDC0/IO111NDB1
116	GDC1/IO111PDB1
117	IO109NDB1
118	IO109PDB1
119	IO106NDB1
120	IO106PDB1
121	IO104PSB1
122	GND
123	VCCIB1
124	IO99NDB1
125	IO99PDB1
126	NC
127	IO96NDB1
128	GCC2/IO96PDB1
129	GCB2/IO95PSB1
130	GND
131	GCA2/IO94PSB1
132	GCA1/IO93PDB1
133	GCA0/IO93NDB1
134	GCB0/IO92NDB1
135	GCB1/IO92PDB1
136	GCC0/IO91NDB1
137	GCC1/IO91PDB1
138	IO88NDB1
139	IO88PDB1
140	VCCIB1
141	GND
142	VCC
143	IO86PSB1
144	IO84NDB1

208-Pin PQFP	
Pin Number	A3P1000 Function
145	IO84PDB1
146	IO82NDB1
147	IO82PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	VCCIB0
171	VCC
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0

208-Pin PQFP	
Pin Number	A3P1000 Function
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	VCCIB0
187	VCC
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

## 144-Pin FBGA



*Note:* This is the bottom view of the package.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

144-Pin FBGA	
Pin Number	A3P1000 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

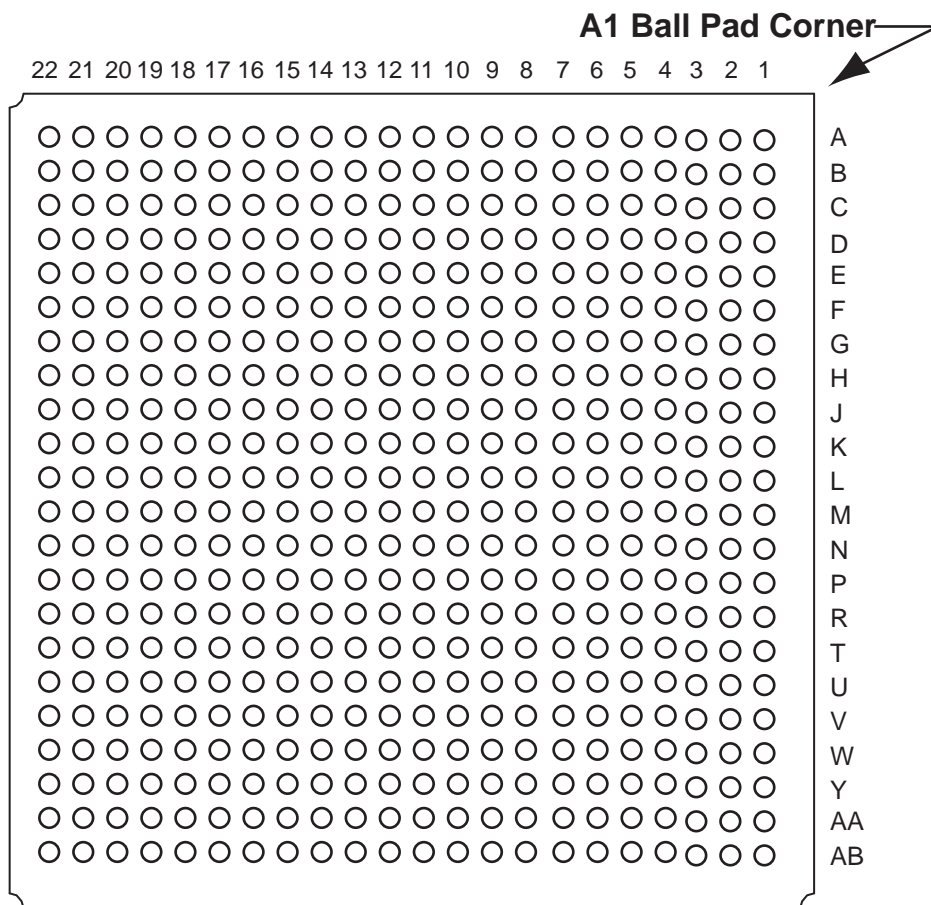
144-Pin FBGA	
Pin Number	A3P1000 Function
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

144-Pin FBGA	
Pin Number	A3P1000 Function
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	VCC
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

144-Pin FBGA	
Pin Number	A3P1000 Function
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO186RSB 2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2

144-Pin FBGA	
Pin Number	A3P1000 Function
M11	VPUMP
M12	GNDQ

## 484-Pin FBGA



*Note:* This is the bottom view of the package.

**Note**

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE600L Function	Pin Number	A3PE600L Function	Pin Number	A3PE600L Function
A1	GND	B15	NC	D7	GAB0/IO01NDB0V0
A2	GND	B16	IO30NDB1V1	D8	IO05PDB0V0
A3	VCCIB0	B17	IO30PDB1V1	D9	IO10PDB0V1
A4	IO06NDB0V1	B18	IO32PDB1V1	D10	IO12PDB0V2
A5	IO06PDB0V1	B19	NC	D11	IO16NDB0V2
A6	IO08NDB0V1	B20	NC	D12	IO23NDB1V0
A7	IO08PDB0V1	B21	VCCIB2	D13	IO23PDB1V0
A8	IO11PDB0V1	B22	GND	D14	IO28NDB1V1
A9	IO17PDB0V2	C1	VCCIB7	D15	IO28PDB1V1
A10	IO18NDB0V2	C2	NC	D16	GBB1/IO34PDB1V1
A11	IO18PDB0V2	C3	NC	D17	GBA0/IO35NDB1V1
A12	IO22PDB1V0	C4	NC	D18	GBA1/IO35PDB1V1
A13	IO26PDB1V0	C5	GND	D19	GND
A14	IO29NDB1V1	C6	IO04NDB0V0	D20	NC
A15	IO29PDB1V1	C7	IO04PDB0V0	D21	NC
A16	IO31NDB1V1	C8	VCC	D22	NC
A17	IO31PDB1V1	C9	VCC	E1	NC
A18	IO32NDB1V1	C10	IO14NDB0V2	E2	NC
A19	NC	C11	IO19NDB0V2	E3	GND
A20	VCCIB1	C12	NC	E4	GAB2/IO133PDB7V1
A21	GND	C13	NC	E5	GAA2/IO134PDB7V1
A22	GND	C14	VCC	E6	GNDQ
B1	GND	C15	VCC	E7	GAB1/IO01PDB0V0
B2	VCCIB7	C16	NC	E8	IO05NDB0V0
B3	NC	C17	NC	E9	IO10NDB0V1
B4	IO03NDB0V0	C18	GND	E10	IO12NDB0V2
B5	IO03PDB0V0	C19	NC	E11	IO16PDB0V2
B6	IO07NDB0V1	C20	NC	E12	IO20NDB1V0
B7	IO07PDB0V1	C21	NC	E13	IO24NDB1V0
B8	IO11NDB0V1	C22	VCCIB2	E14	IO24PDB1V0
B9	IO17NDB0V2	D1	NC	E15	GBC1/IO33PDB1V1
B10	IO14PDB0V2	D2	NC	E16	GBB0/IO34NDB1V1
B11	IO19PDB0V2	D3	NC	E17	GNDQ
B12	IO22NDB1V0	D4	GND	E18	GBA2/IO36PDB2V0
B13	IO26NDB1V0	D5	GAA0/IO00NDB0V0	E19	IO42NDB2V0
B14	NC	D6	GAA1/IO00PDB0V0	E20	GND



484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE600L Function	Pin Number	A3PE600L Function	Pin Number	A3PE600L Function
E21	NC	G13	IO25PDB1V0	J5	IO125PDB7V0
E22	NC	G14	IO27NDB1V0	J6	IO126PDB7V0
F1	NC	G15	GNDQ	J7	IO130NDB7V1
F2	IO131NDB7V1	G16	VCOMPLB	J8	VCCIB7
F3	IO131PDB7V1	G17	GBB2/IO37PDB2V0	J9	GND
F4	IO133NDB7V1	G18	IO39PDB2V0	J10	VCC
F5	IO134NDB7V1	G19	IO39NDB2V0	J11	VCC
F6	VMV7	G20	IO43PDB2V0	J12	VCC
F7	VCCPLA	G21	IO43NDB2V0	J13	VCC
F8	GAC0/IO02NDB0V0	G22	NC	J14	GND
F9	GAC1/IO02PDB0V0	H1	NC	J15	VCCIB2
F10	IO15NDB0V2	H2	NC	J16	IO38NDB2V0
F11	IO15PDB0V2	H3	VCC	J17	IO40NDB2V0
F12	IO20PDB1V0	H4	IO128NDB7V1	J18	IO40PDB2V0
F13	IO25NDB1V0	H5	IO129NDB7V1	J19	IO45PDB2V1
F14	IO27PDB1V0	H6	IO132NDB7V1	J20	NC
F15	GBC0/IO33NDB1V1	H7	IO130PDB7V1	J21	IO48PDB2V1
F16	VCCPLB	H8	VMV0	J22	IO46PDB2V1
F17	VMV2	H9	VCCIB0	K1	IO121NDB7V0
F18	IO36NDB2V0	H10	VCCIB0	K2	IO121PDB7V0
F19	IO42PDB2V0	H11	IO13NDB0V2	K3	NC
F20	NC	H12	IO21NDB1V0	K4	IO124NDB7V0
F21	NC	H13	VCCIB1	K5	IO125NDB7V0
F22	NC	H14	VCCIB1	K6	IO126NDB7V0
G1	IO127NDB7V1	H15	VMV1	K7	GFC1/IO120PPB7V0
G2	IO127PDB7V1	H16	GBC2/IO38PDB2V0	K8	VCCIB7
G3	NC	H17	IO37NDB2V0	K9	VCC
G4	IO128PDB7V1	H18	IO41NDB2V0	K10	GND
G5	IO129PDB7V1	H19	IO41PDB2V0	K11	GND
G6	GAC2/IO132PDB7V1	H20	VCC	K12	GND
G7	VCOMPLA	H21	NC	K13	GND
G8	GNDQ	H22	NC	K14	VCC
G9	IO09NDB0V1	J1	IO123NDB7V0	K15	VCCIB2
G10	IO09PDB0V1	J2	IO123PDB7V0	K16	GCC1/IO50PPB2V1
G11	IO13PDB0V2	J3	NC	K17	IO44NDB2V1
G12	IO21PDB1V0	J4	IO124PDB7V0	K18	IO44PDB2V1

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE600L Function	Pin Number	A3PE600L Function	Pin Number	A3PE600L Function
K19	IO49NPB2V1	M11	GND	P3	IO115NDB6V1
K20	IO45NDB2V1	M12	GND	P4	IO113NPB6V1
K21	IO48NDB2V1	M13	GND	P5	IO109PPB6V0
K22	IO46NDB2V1	M14	VCC	P6	IO108PDB6V0
L1	NC	M15	GCB2/IO54PPB3V0	P7	IO108NDB6V0
L2	IO122PDB7V0	M16	GCA1/IO52PPB3V0	P8	VCCIB6
L3	IO122NDB7V0	M17	GCC2/IO55PPB3V0	P9	GND
L4	GFB0/IO119NPB7V0	M18	VCCPLC	P10	VCC
L5	GFA0/IO118NDB6V1	M19	GCA2/IO53PDB3V0	P11	VCC
L6	GFB1/IO119PPB7V0	M20	IO53NDB3V0	P12	VCC
L7	VCOMPLF	M21	IO56PDB3V0	P13	VCC
L8	GFC0/IO120NPB7V0	M22	NC	P14	GND
L9	VCC	N1	IO114PDB6V1	P15	VCCIB3
L10	GND	N2	IO111NDB6V1	P16	GDB0/IO66NPB3V1
L11	GND	N3	NC	P17	IO60NDB3V1
L12	GND	N4	GFC2/IO115PDB6V1	P18	IO60PDB3V1
L13	GND	N5	IO113PPB6V1	P19	IO61PDB3V1
L14	VCC	N6	IO112PDB6V1	P20	NC
L15	GCC0/IO50NPB2V1	N7	IO112NDB6V1	P21	IO59PDB3V0
L16	GCB1/IO51PPB2V1	N8	VCCIB6	P22	IO58NDB3V0
L17	GCA0/IO52NPB3V0	N9	VCC	R1	NC
L18	VCOMPLC	N10	GND	R2	IO110PDB6V0
L19	GCB0/IO51NPB2V1	N11	GND	R3	VCC
L20	IO49PPB2V1	N12	GND	R4	IO109NPB6V0
L21	IO47NDB2V1	N13	GND	R5	IO106NDB6V0
L22	IO47PDB2V1	N14	VCC	R6	IO106PDB6V0
M1	NC	N15	VCCIB3	R7	GEC0/IO104NPB6V0
M2	IO114NDB6V1	N16	IO54NPB3V0	R8	VMV5
M3	IO117NDB6V1	N17	IO57NPB3V0	R9	VCCIB5
M4	GFA2/IO117PDB6V1	N18	IO55NPB3V0	R10	VCCIB5
M5	GFA1/IO118PDB6V1	N19	IO57PPB3V0	R11	IO84NDB5V0
M6	VCCPLF	N20	NC	R12	IO84PDB5V0
M7	IO116NDB6V1	N21	IO56NDB3V0	R13	VCCIB4
M8	GFB2/IO116PDB6V1	N22	IO58PDB3V0	R14	VCCIB4
M9	VCC	P1	NC	R15	VMV3
M10	GND	P2	IO111PDB6V1	R16	VCCPLD

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE600L Function	Pin Number	A3PE600L Function	Pin Number	A3PE600L Function
R17	GDB1/IO66PPB3V1	U9	IO95PPB5V1	W1	NC
R18	GDC1/IO65PDB3V1	U10	IO92PDB5V1	W2	NC
R19	IO61NDB3V1	U11	IO90PDB5V1	W3	NC
R20	VCC	U12	IO82PDB5V0	W4	GND
R21	IO59NDB3V0	U13	IO76NDB4V1	W5	IO100NDB5V2
R22	IO62PDB3V1	U14	IO76PDB4V1	W6	GEB2/IO100PDB5V2
T1	NC	U15	VMV4	W7	IO99NDB5V2
T2	IO110NDB6V0	U16	TCK	W8	IO88NDB5V0
T3	NC	U17	VPUMP	W9	IO88PDB5V0
T4	IO105PDB6V0	U18	TRST	W10	IO89NDB5V0
T5	IO105NDB6V0	U19	GDA0/IO67NDB3V1	W11	IO80NDB4V1
T6	GEC1/IO104PPB6V0	U20	NC	W12	IO81NDB4V1
T7	VCOMPLE	U21	IO64NDB3V1	W13	IO81PDB4V1
T8	GNDQ	U22	IO63PDB3V1	W14	IO70NDB4V0
T9	GEA2/IO101PPB5V2	V1	NC	W15	GDC2/IO70PDB4V0
T10	IO92NDB5V1	V2	NC	W16	IO68NDB4V0
T11	IO90NDB5V1	V3	GND	W17	GDA2/IO68PDB4V0
T12	IO82NDB5V0	V4	GEA1/IO102PDB6V0	W18	TMS
T13	IO74NDB4V1	V5	GEA0/IO102NDB6V0	W19	GND
T14	IO74PDB4V1	V6	GNDQ	W20	NC
T15	GNDQ	V7	GEC2/IO99PDB5V2	W21	NC
T16	VCOMPLD	V8	IO95NPB5V1	W22	NC
T17	VJTAG	V9	IO91NDB5V1	Y1	VCCIB6
T18	GDC0/IO65NDB3V1	V10	IO91PDB5V1	Y2	NC
T19	GDA1/IO67PDB3V1	V11	IO83NDB5V0	Y3	NC
T20	NC	V12	IO83PDB5V0	Y4	IO98NDB5V2
T21	IO64PDB3V1	V13	IO77NDB4V1	Y5	GND
T22	IO62NDB3V1	V14	IO77PDB4V1	Y6	IO94NDB5V1
U1	NC	V15	IO69NDB4V0	Y7	IO94PDB5V1
U2	IO107PDB6V0	V16	GDB2/IO69PDB4V0	Y8	VCC
U3	IO107NDB6V0	V17	TDI	Y9	VCC
U4	GEB1/IO103PDB6V0	V18	GNDQ	Y10	IO89PDB5V0
U5	GEB0/IO103NDB6V0	V19	TDO	Y11	IO80PDB4V1
U6	VMV6	V20	GND	Y12	IO78NPB4V1
U7	VCCPLE	V21	NC	Y13	NC
U8	IO101NPB5V2	V22	IO63NDB3V1	Y14	VCC

484-Pin FBGA	
Pin Number	A3PE600L Function
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB3
AA1	GND
AA2	VCCIB6
AA3	NC
AA4	IO98PDB5V2
AA5	IO96NDB5V2
AA6	IO96PDB5V2
AA7	IO86NDB5V0
AA8	IO86PDB5V0
AA9	IO85PDB5V0
AA10	IO85NDB5V0
AA11	IO78PPB4V1
AA12	IO79NDB4V1
AA13	IO79PDB4V1
AA14	NC
AA15	NC
AA16	IO71NDB4V0
AA17	IO71PDB4V0
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB3
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB5
AB4	IO97NDB5V2
AB5	IO97PDB5V2
AB6	IO93NDB5V1

484-Pin FBGA	
Pin Number	A3PE600L Function
AB7	IO93PDB5V1
AB8	IO87NDB5V0
AB9	IO87PDB5V0
AB10	NC
AB11	NC
AB12	IO75NDB4V1
AB13	IO75PDB4V1
AB14	IO72NDB4V0
AB15	IO72PDB4V0
AB16	IO73NDB4V0
AB17	IO73PDB4V0
AB18	NC
AB19	NC
AB20	VCCIB4
AB21	GND
AB22	GND

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
A1	GND	AA14	IO170NDB4V2	B5	IO08PDB0V0
A2	GND	AA15	IO170PDB4V2	B6	IO14NDB0V1
A3	VCCIB0	AA16	IO166NDB4V1	B7	IO14PDB0V1
A4	IO10NDB0V1	AA17	IO166PDB4V1	B8	IO18NDB0V2
A5	IO10PDB0V1	AA18	IO160NDB4V0	B9	IO24NDB0V2
A6	IO16NDB0V1	AA19	IO160PDB4V0	B10	IO34PDB0V4
A7	IO16PDB0V1	AA20	IO158NPB4V0	B11	IO40PDB0V4
A8	IO18PDB0V2	AA21	VCCIB3	B12	IO46NDB1V0
A9	IO24PDB0V2	AA22	GND	B13	IO54NDB1V1
A10	IO28NDB0V3	AB1	GND	B14	IO62NDB1V2
A11	IO28PDB0V3	AB2	GND	B15	IO62PDB1V2
A12	IO46PDB1V0	AB3	VCCIB5	B16	IO68NDB1V3
A13	IO54PDB1V1	AB4	IO216NDB5V2	B17	IO68PDB1V3
A14	IO56NDB1V1	AB5	IO216PDB5V2	B18	IO72PDB1V3
A15	IO56PDB1V1	AB6	IO210NDB5V2	B19	IO74PDB1V4
A16	IO64NDB1V2	AB7	IO210PDB5V2	B20	IO76NPB1V4
A17	IO64PDB1V2	AB8	IO208NDB5V1	B21	VCCIB2
A18	IO72NDB1V3	AB9	IO208PDB5V1	B22	GND
A19	IO74NDB1V4	AB10	IO197NDB5V0	C1	VCCIB7
A20	VCCIB1	AB11	IO197PDB5V0	C2	IO303PDB7V3
A21	GND	AB12	IO174NDB4V2	C3	IO305PDB7V3
A22	GND	AB13	IO174PDB4V2	C4	IO06NPB0V0
AA1	GND	AB14	IO172NDB4V2	C5	GND
AA2	VCCIB6	AB15	IO172PDB4V2	C6	IO12NDB0V1
AA3	IO228PDB5V4	AB16	IO168NDB4V1	C7	IO12PDB0V1
AA4	IO224PDB5V3	AB17	IO168PDB4V1	C8	VCC
AA5	IO218NDB5V3	AB18	IO162NDB4V1	C9	VCC
AA6	IO218PDB5V3	AB19	IO162PDB4V1	C10	IO34NDB0V4
AA7	IO212NDB5V2	AB20	VCCIB4	C11	IO40NDB0V4
AA8	IO212PDB5V2	AB21	GND	C12	IO48NDB1V0
AA9	IO198PDB5V0	AB22	GND	C13	IO48PDB1V0
AA10	IO198NDB5V0	B1	GND	C14	VCC
AA11	IO188PPB4V4	B2	VCCIB7	C15	VCC
AA12	IO180NDB4V3	B3	IO06PPB0V0	C16	IO70NDB1V3
AA13	IO180PDB4V3	B4	IO08NDB0V0	C17	IO70PDB1V3

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
C18	GND	E9	IO22NDB0V2	F22	IO98NDB2V2
C19	IO76PPB1V4	E10	IO30NDB0V3	G1	IO289NDB7V1
C20	IO88NDB2V0	E11	IO38PDB0V4	G2	IO289PDB7V1
C21	IO94PPB2V1	E12	IO44NDB1V0	G3	IO291PPB7V2
C22	VCCIB2	E13	IO58NDB1V2	G4	IO295PDB7V2
D1	IO293PDB7V2	E14	IO58PDB1V2	G5	IO297PDB7V2
D2	IO303NDB7V3	E15	GBC1/IO79PDB1V4	G6	GAC2/IO307PDB7V4
D3	IO305NDB7V3	E16	GGB0/IO80NDB1V4	G7	VCOMPLA
D4	GND	E17	GNDQ	G8	GNDQ
D5	GAA0/IO00NDB0V0	E18	GBA2/IO82PDB2V0	G9	IO26NDB0V3
D6	GAA1/IO00PDB0V0	E19	IO86NDB2V0	G10	IO26PDB0V3
D7	GAB0/IO01NDB0V0	E20	GND	G11	IO36PDB0V4
D8	IO20PDB0V2	E21	IO90NDB2V1	G12	IO42PDB1V0
D9	IO22PDB0V2	E22	IO98PDB2V2	G13	IO50PDB1V1
D10	IO30PDB0V3	F1	IO299NPB7V3	G14	IO60NDB1V2
D11	IO38NDB0V4	F2	IO301NDB7V3	G15	GNDQ
D12	IO52NDB1V1	F3	IO301PDB7V3	G16	VCOMPLB
D13	IO52PDB1V1	F4	IO308NDB7V4	G17	GGB2/IO83PDB2V0
D14	IO66NDB1V3	F5	IO309NDB7V4	G18	IO92PDB2V1
D15	IO66PDB1V3	F6	VMV7	G19	IO92NDB2V1
D16	GGB1/IO80PDB1V4	F7	VCCPLA	G20	IO102PDB2V2
D17	GBA0/IO81NDB1V4	F8	GAC0/IO02NDB0V0	G21	IO102NDB2V2
D18	GBA1/IO81PDB1V4	F9	GAC1/IO02PDB0V0	G22	IO105NDB2V2
D19	GND	F10	IO32NDB0V3	H1	IO286PSB7V1
D20	IO88PDB2V0	F11	IO32PDB0V3	H2	IO291NPB7V2
D21	IO90PDB2V1	F12	IO44PDB1V0	H3	VCC
D22	IO94NPB2V1	F13	IO50NDB1V1	H4	IO295NDB7V2
E1	IO293NDB7V2	F14	IO60PDB1V2	H5	IO297NDB7V2
E2	IO299PPB7V3	F15	GBC0/IO79NDB1V4	H6	IO307NDB7V4
E3	GND	F16	VCCPLB	H7	IO287PDB7V1
E4	GAB2/IO308PDB7V4	F17	VMV2	H8	VMV0
E5	GAA2/IO309PDB7V4	F18	IO82NDB2V0	H9	VCCIB0
E6	GNDQ	F19	IO86PDB2V0	H10	VCCIB0
E7	GAB1/IO01PDB0V0	F20	IO96PDB2V1	H11	IO36NDB0V4
E8	IO20NDB0V2	F21	IO96NDB2V1	H12	IO42NDB1V0

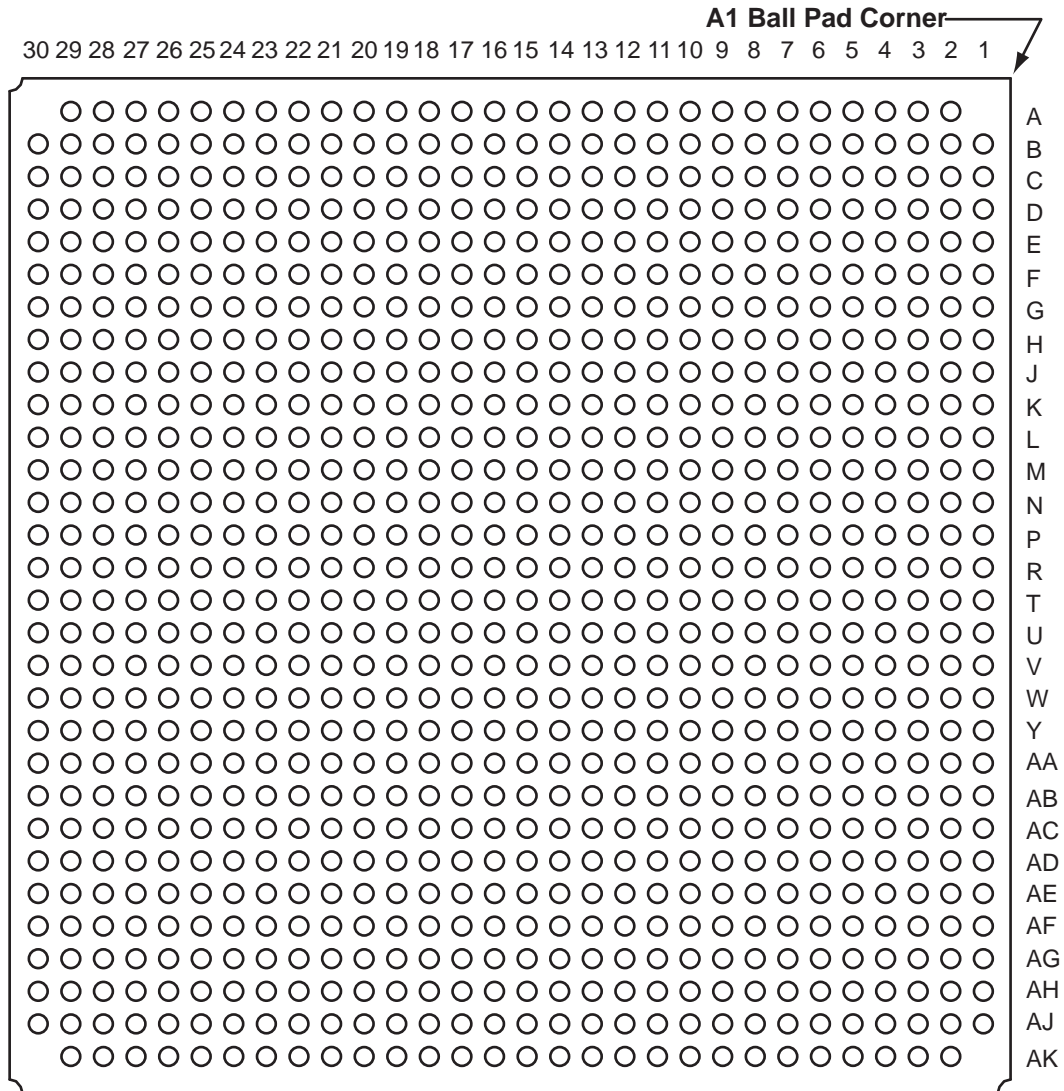
484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
H13	VCCIB1	K4	IO279NDB7V0	L17	GCA0/IO114NPB3V0
H14	VCCIB1	K5	IO283NDB7V1	L18	VCOMPLC
H15	VMV1	K6	IO281NDB7V0	L19	GCB0/IO113NPB2V3
H16	GBC2/IO84PDB2V0	K7	GFC1/IO275PPB7V0	L20	IO110PPB2V3
H17	IO83NDB2V0	K8	VCCIB7	L21	IO111NDB2V3
H18	IO100NDB2V2	K9	VCC	L22	IO111PDB2V3
H19	IO100PDB2V2	K10	GND	M1	GNDQ
H20	VCC	K11	GND	M2	IO255NPB6V2
H21	VMV2	K12	GND	M3	IO272NDB6V4
H22	IO105PDB2V2	K13	GND	M4	GFA2/IO272PDB6V4
J1	IO285NDB7V1	K14	VCC	M5	GFA1/IO273PDB6V4
J2	IO285PDB7V1	K15	VCCIB2	M6	VCCPLF
J3	VMV7	K16	GCC1/IO112PPB2V3	M7	IO271NDB6V4
J4	IO279PDB7V0	K17	IO108NDB2V3	M8	GFB2/IO271PDB6V4
J5	IO283PDB7V1	K18	IO108PDB2V3	M9	VCC
J6	IO281PDB7V0	K19	IO110NPB2V3	M10	GND
J7	IO287NDB7V1	K20	IO106NPB2V3	M11	GND
J8	VCCIB7	K21	IO109NDB2V3	M12	GND
J9	GND	K22	IO107NDB2V3	M13	GND
J10	VCC	L1	IO257PSB6V2	M14	VCC
J11	VCC	L2	IO276PDB7V0	M15	GCB2/IO116PPB3V0
J12	VCC	L3	IO276NDB7V0	M16	GCA1/IO114PPB3V0
J13	VCC	L4	GFB0/IO274NPB7V0	M17	GCC2/IO117PPB3V0
J14	GND	L5	GFA0/IO273NDB6V4	M18	VCCPLC
J15	VCCIB2	L6	GFB1/IO274PPB7V0	M19	GCA2/IO115PDB3V0
J16	IO84NDB2V0	L7	VCOMPLF	M20	IO115NDB3V0
J17	IO104NDB2V2	L8	GFC0/IO275NPB7V0	M21	IO126PDB3V1
J18	IO104PDB2V2	L9	VCC	M22	IO124PSB3V1
J19	IO106PPB2V3	L10	GND	N1	IO255PPB6V2
J20	GNDQ	L11	GND	N2	IO253NDB6V2
J21	IO109PDB2V3	L12	GND	N3	VMV6
J22	IO107PDB2V3	L13	GND	N4	GFC2/IO270PPB6V4
K1	IO277NDB7V0	L14	VCC	N5	IO261PPB6V3
K2	IO277PDB7V0	L15	GCC0/IO112NPB2V3	N6	IO263PDB6V3
K3	GNDQ	L16	GCB1/IO113PPB2V3	N7	IO263NDB6V3

484-Pin FBGA		484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
N8	VCCIB6	P21	IO130PDB3V2	T12	IO194NDB5V0
N9	VCC	P22	IO128NDB3V1	T13	IO186NDB4V4
N10	GND	R1	IO247NDB6V1	T14	IO186PDB4V4
N11	GND	R2	IO245PDB6V1	T15	GNDQ
N12	GND	R3	VCC	T16	VCOMPLD
N13	GND	R4	IO249NPB6V1	T17	VJTAG
N14	VCC	R5	IO251NDB6V2	T18	GDC0/IO151NDB3V4
N15	VCCIB3	R6	IO251PDB6V2	T19	GDA1/IO153PDB3V4
N16	IO116NPB3V0	R7	GEC0/IO236NPB6V0	T20	IO144PDB3V3
N17	IO132NPB3V2	R8	VMV5	T21	IO140PDB3V3
N18	IO117NPB3V0	R9	VCCIB5	T22	IO134NDB3V2
N19	IO132PPB3V2	R10	VCCIB5	U1	IO240PPB6V0
N20	GNDQ	R11	IO196NDB5V0	U2	IO238PDB6V0
N21	IO126NDB3V1	R12	IO196PDB5V0	U3	IO238NDB6V0
N22	IO128PDB3V1	R13	VCCIB4	U4	GEB1/IO235PDB6V0
P1	IO247PDB6V1	R14	VCCIB4	U5	GEB0/IO235NDB6V0
P2	IO253PDB6V2	R15	VMV3	U6	VMV6
P3	IO270NPB6V4	R16	VCCPLD	U7	VCCPLE
P4	IO261NPB6V3	R17	GDB1/IO152PPB3V4	U8	IO233NPB5V4
P5	IO249PPB6V1	R18	GDC1/IO151PDB3V4	U9	IO222PPB5V3
P6	IO259PDB6V3	R19	IO138NDB3V3	U10	IO206PDB5V1
P7	IO259NDB6V3	R20	VCC	U11	IO202PDB5V1
P8	VCCIB6	R21	IO130NDB3V2	U12	IO194PDB5V0
P9	GND	R22	IO134PDB3V2	U13	IO176NDB4V2
P10	VCC	T1	IO243PPB6V1	U14	IO176PDB4V2
P11	VCC	T2	IO245NDB6V1	U15	VMV4
P12	VCC	T3	IO243NPB6V1	U16	TCK
P13	VCC	T4	IO241PDB6V0	U17	VPUMP
P14	GND	T5	IO241NDB6V0	U18	TRST
P15	VCCIB3	T6	GEC1/IO236PPB6V0	U19	GDA0/IO153NDB3V4
P16	GDB0/IO152NPB3V4	T7	VCOMPLE	U20	IO144NDB3V3
P17	IO136NDB3V2	T8	GNDQ	U21	IO140NDB3V3
P18	IO136PDB3V2	T9	GEA2/IO233PPB5V4	U22	IO142PDB3V3
P19	IO138PDB3V3	T10	IO206NDB5V1	V1	IO239PDB6V0
P20	VMV3	T11	IO202NDB5V1	V2	IO240NPB6V0



484-Pin FBGA		484-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
V3	GND	W16	IO154NDB4V0
V4	GEA1/IO234PDB6V0	W17	GDA2/IO154PDB4V0
V5	GEA0/IO234NDB6V0	W18	TMS
V6	GNDQ	W19	GND
V7	GEC2/IO231PDB5V4	W20	IO150NDB3V4
V8	IO222NPB5V3	W21	IO146NDB3V4
V9	IO204NDB5V1	W22	IO148PPB3V4
V10	IO204PDB5V1	Y1	VCCIB6
V11	IO195NDB5V0	Y2	IO237NDB6V0
V12	IO195PDB5V0	Y3	IO228NDB5V4
V13	IO178NDB4V3	Y4	IO224NDB5V3
V14	IO178PDB4V3	Y5	GND
V15	IO155NDB4V0	Y6	IO220NDB5V3
V16	GDB2/IO155PDB4V0	Y7	IO220PDB5V3
V17	TDI	Y8	VCC
V18	GNDQ	Y9	VCC
V19	TDO	Y10	IO200PDB5V0
V20	GND	Y11	IO192PDB4V4
V21	IO146PDB3V4	Y12	IO188NPB4V4
V22	IO142NDB3V3	Y13	IO187PSB4V4
W1	IO239NDB6V0	Y14	VCC
W2	IO237PDB6V0	Y15	VCC
W3	IO230PSB5V4	Y16	IO164NDB4V1
W4	GND	Y17	IO164PDB4V1
W5	IO232NDB5V4	Y18	GND
W6	FF/GEB2/IO232PDB5V4	Y19	IO158PPB4V0
W7	IO231NDB5V4	Y20	IO150PDB3V4
W8	IO214NDB5V2	Y21	IO148NPB3V4
W9	IO214PDB5V2	Y22	VCCIB3
W10	IO200NDB5V0		
W11	IO192NDB4V4		
W12	IO184NDB4V3		
W13	IO184PDB4V3		
W14	IO156NDB4V0		
W15	GDC2/IO156PDB4V0		

## 896-Pin FBGA



*Note:* This is the bottom view.

### Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
A2	GND	AA9	GEB1/IO235PPB6V0	AB15	IO198PDB5V0
A3	GND	AA10	VCC	AB16	IO192NDB4V4
A4	IO14NPB0V1	AA11	IO226PPB5V4	AB17	IO192PDB4V4
A5	GND	AA12	VCCIB5	AB18	IO178NDB4V3
A6	IO07NPB0V0	AA13	VCCIB5	AB19	IO178PDB4V3
A7	GND	AA14	VCCIB5	AB20	IO174NDB4V2
A8	IO09NDB0V1	AA15	VCCIB5	AB21	IO162NPB4V1
A9	IO17NDB0V2	AA16	VCCIB4	AB22	VCC
A10	IO17PDB0V2	AA17	VCCIB4	AB23	VCCPLD
A11	IO21NDB0V2	AA18	VCCIB4	AB24	VCCIB3
A12	IO21PDB0V2	AA19	VCCIB4	AB25	IO150PDB3V4
A13	IO33NDB0V4	AA20	IO174PDB4V2	AB26	IO148PDB3V4
A14	IO33PDB0V4	AA21	VCC	AB27	IO147NDB3V4
A15	IO35NDB0V4	AA22	IO142NPB3V3	AB28	IO145PDB3V3
A16	IO35PDB0V4	AA23	IO144NDB3V3	AB29	IO143PDB3V3
A17	IO41NDB1V0	AA24	IO144PDB3V3	AB30	IO137PDB3V2
A18	IO43NDB1V0	AA25	IO146NDB3V4	AC1	IO254PDB6V2
A19	IO43PDB1V0	AA26	IO146PDB3V4	AC2	IO254NDB6V2
A20	IO45NDB1V0	AA27	IO147PDB3V4	AC3	IO240PDB6V0
A21	IO45PDB1V0	AA28	IO139NDB3V3	AC4	GEC1/IO236PDB6V0
A22	IO57NDB1V2	AA29	IO139PDB3V3	AC5	IO237PDB6V0
A23	IO57PDB1V2	AA30	IO133NDB3V2	AC6	IO237NDB6V0
A24	GND	AB1	IO256NDB6V2	AC7	VCOMPLE
A25	IO69PPB1V3	AB2	IO244PDB6V1	AC8	GND
A26	GND	AB3	IO244NDB6V1	AC9	IO226NPB5V4
A27	GBC1/IO79PPB1V4	AB4	IO241PDB6V0	AC10	IO222NDB5V3
A28	GND	AB5	IO241NDB6V0	AC11	IO216NPB5V2
A29	GND	AB6	IO243NPB6V1	AC12	IO210NPB5V2
AA1	IO256PDB6V2	AB7	VCCIB6	AC13	IO204NDB5V1
AA2	IO248PDB6V1	AB8	VCCPLE	AC14	IO204PDB5V1
AA3	IO248NDB6V1	AB9	VCC	AC15	IO194NDB5V0
AA4	IO246NDB6V1	AB10	IO222PDB5V3	AC16	IO188NDB4V4
AA5	GEA1/IO234PDB6V0	AB11	IO218PPB5V3	AC17	IO188PDB4V4
AA6	GEA0/IO234NDB6V0	AB12	IO206NDB5V1	AC18	IO182PPB4V3
AA7	IO243PPB6V1	AB13	IO206PDB5V1	AC19	IO170NPB4V2
AA8	IO245NDB6V1	AB14	IO198NDB5V0	AC20	IO164NDB4V1

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
AC21	IO164PDB4V1	AD26	VCCIB3	AE30	IO149PDB3V4
AC22	IO162PPB4V1	AD27	GDA0/IO153NDB3V4	AF1	GND
AC23	GND	AD28	GDC0/IO151NDB3V4	AF2	IO238PPB6V0
AC24	VCOMPLD	AD29	GDC1/IO151PDB3V4	AF3	VCCIB6
AC25	IO150NDB3V4	AD30	GND	AF4	IO220NPB5V3
AC26	IO148NDB3V4	AE1	IO242PPB6V1	AF5	VCC
AC27	GDA1/IO153PDB3V4	AE2	VCC	AF6	IO228NDB5V4
AC28	IO145NDB3V3	AE3	IO239PDB6V0	AF7	VCCIB5
AC29	IO143NDB3V3	AE4	IO239NDB6V0	AF8	IO230PDB5V4
AC30	IO137NDB3V2	AE5	VMV6	AF9	IO229NDB5V4
AD1	GND	AE5	VMV6	AF10	IO229PDB5V4
AD2	IO242NPB6V1	AE6	GND	AF11	IO214PPB5V2
AD3	IO240NDB6V0	AE7	GNDQ	AF12	IO208NDB5V1
AD4	GEC0/IO236NDB6V0	AE8	IO230NDB5V4	AF13	IO208PDB5V1
AD5	VCCIB6	AE9	IO224NPB5V3	AF14	IO200PDB5V0
AD6	GNDQ	AE10	IO214NPB5V2	AF15	IO196NDB5V0
AD6	GNDQ	AE11	IO212NDB5V2	AF16	IO186NDB4V4
AD7	VCC	AE12	IO212PDB5V2	AF17	IO186PDB4V4
AD8	VMV5	AE13	IO202NPB5V1	AF18	IO180NDB4V3
AD9	VCCIB5	AE14	IO200NDB5V0	AF19	IO180PDB4V3
AD10	IO224PPB5V3	AE15	IO196PDB5V0	AF20	IO168NDB4V1
AD11	IO218NPB5V3	AE16	IO190NDB4V4	AF21	IO168PDB4V1
AD12	IO216PPB5V2	AE17	IO184PDB4V3	AF22	IO160NDB4V0
AD13	IO210PPB5V2	AE18	IO184NDB4V3	AF23	IO158NPB4V0
AD14	IO202PPB5V1	AE19	IO172PDB4V2	AF24	VCCIB4
AD15	IO194PDB5V0	AE20	IO172NDB4V2	AF25	IO154NPB4V0
AD16	IO190PDB4V4	AE21	IO166NDB4V1	AF26	VCC
AD17	IO182NPB4V3	AE22	IO160PDB4V0	AF27	TDO
AD18	IO176NDB4V2	AE23	GNDQ	AF28	VCCIB3
AD19	IO176PDB4V2	AE24	VMV4	AF29	GNDQ
AD20	IO170PPB4V2	AE25	GND	AF29	GNDQ
AD21	IO166PDB4V1	AE26	GDB0/IO152NDB3V4	AF30	GND
AD22	VCCIB4	AE27	GDB1/IO152PDB3V4	AG1	IO238NPB6V0
AD23	TCK	AE28	VMV3	AG2	VCC
AD24	VCC	AE28	VMV3	AG3	IO232NPB5V4
AD25	TRST	AE29	VCC	AG4	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
AG5	IO220PPB5V3
AG6	IO228PDB5V4
AG7	IO231NDB5V4
AG8	GEC2/IO231PDB5V4
AG9	IO225NPB5V3
AG10	IO223NPB5V3
AG11	IO221PDB5V3
AG12	IO221NDB5V3
AG13	IO205NPB5V1
AG14	IO199NDB5V0
AG15	IO199PDB5V0
AG16	IO187NDB4V4
AG17	IO187PDB4V4
AG18	IO181NDB4V3
AG19	IO171PPB4V2
AG20	IO165NPB4V1
AG21	IO161NPB4V0
AG22	IO159NDB4V0
AG23	IO159PDB4V0
AG24	IO158PPB4V0
AG25	GDB2/IO155PDB4V0
AG26	GDA2/IO154PPB4V0
AG27	GND
AG28	VJTAG
AG29	VCC
AG30	IO149NDB3V4
AH1	GND
AH2	IO233NPB5V4
AH3	VCC
AH4	FF/GEB2/IO232PPB5V4
AH5	VCCIB5
AH6	IO219NDB5V3
AH7	IO219PDB5V3
AH8	IO227NDB5V4
AH9	IO227PDB5V4

896-Pin FBGA	
Pin Number	A3PE3000L Function
AH10	IO225PPB5V3
AH11	IO223PPB5V3
AH12	IO211NDB5V2
AH13	IO211PDB5V2
AH14	IO205PPB5V1
AH15	IO195NDB5V0
AH16	IO185NDB4V3
AH17	IO185PDB4V3
AH18	IO181PDB4V3
AH19	IO177NDB4V2
AH20	IO171NPB4V2
AH21	IO165PPB4V1
AH22	IO161PPB4V0
AH23	IO157NDB4V0
AH24	IO157PDB4V0
AH25	IO155NDB4V0
AH26	VCCIB4
AH27	TDI
AH28	VCC
AH29	VPUMP
AH30	GND
AJ1	GND
AJ2	GND
AJ3	GEA2/IO233PPB5V4
AJ4	VCC
AJ5	IO217NPB5V2
AJ6	VCC
AJ7	IO215NPB5V2
AJ8	IO213NDB5V2
AJ9	IO213PDB5V2
AJ10	IO209NDB5V1
AJ11	IO209PDB5V1
AJ12	IO203NDB5V1
AJ13	IO203PDB5V1
AJ14	IO197NDB5V0
AJ15	IO195PDB5V0

896-Pin FBGA	
Pin Number	A3PE3000L Function
AJ16	IO183NDB4V3
AJ17	IO183PDB4V3
AJ18	IO179NPB4V3
AJ19	IO177PDB4V2
AJ20	IO173NDB4V2
AJ21	IO173PDB4V2
AJ22	IO163NDB4V1
AJ23	IO163PDB4V1
AJ24	IO167NPB4V1
AJ25	VCC
AJ26	IO156NPB4V0
AJ27	VCC
AJ28	TMS
AJ29	GND
AJ30	GND
AK2	GND
AK3	GND
AK4	IO217PPB5V2
AK5	GND
AK6	IO215PPB5V2
AK7	GND
AK8	IO207NDB5V1
AK9	IO207PDB5V1
AK10	IO201NDB5V0
AK11	IO201PDB5V0
AK12	IO193NDB4V4
AK13	IO193PDB4V4
AK14	IO197PDB5V0
AK15	IO191NDB4V4
AK16	IO191PDB4V4
AK17	IO189NDB4V4
AK18	IO189PDB4V4
AK19	IO179PPB4V3
AK20	IO175NDB4V2
AK21	IO175PDB4V2
AK22	IO169NDB4V1

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
AK23	IO169PDB4V1	B30	GND	D6	GAC1/IO02PDB0V0
AK24	GND	C1	GND	D7	IO06NPB0V0
AK25	IO167PPB4V1	C2	IO309NPB7V4	D8	GAB0/IO01NDB0V0
AK26	GND	C3	VCC	D9	IO05NDB0V0
AK27	GDC2/IO156PPB4V0	C4	GAA0/IO00NPB0V0	D10	IO11NDB0V1
AK28	GND	C5	VCCIB0	D11	IO11PDB0V1
AK29	GND	C6	IO03PDB0V0	D12	IO23NDB0V2
B1	GND	C7	IO03NDB0V0	D13	IO23PDB0V2
B2	GND	C8	GAB1/IO01PDB0V0	D14	IO27PDB0V3
B3	GAA2/IO309PPB7V4	C9	IO05PDB0V0	D15	IO40PDB0V4
B4	VCC	C10	IO15NPB0V1	D16	IO47NDB1V0
B5	IO14PPB0V1	C11	IO25NDB0V3	D17	IO47PDB1V0
B6	VCC	C12	IO25PDB0V3	D18	IO55NPB1V1
B7	IO07PPB0V0	C13	IO31NPB0V3	D19	IO65NDB1V3
B8	IO09PDB0V1	C14	IO27NDB0V3	D20	IO65PDB1V3
B9	IO15PPB0V1	C15	IO39NDB0V4	D21	IO71NDB1V3
B10	IO19NDB0V2	C16	IO39PDB0V4	D22	IO71PDB1V3
B11	IO19PDB0V2	C17	IO55PPB1V1	D23	IO73NDB1V4
B12	IO29NDB0V3	C18	IO51PDB1V1	D24	IO73PDB1V4
B13	IO29PDB0V3	C19	IO59NDB1V2	D25	IO74NDB1V4
B14	IO31PPB0V3	C20	IO63NDB1V2	D26	GBB0/IO80NPB1V4
B15	IO37NDB0V4	C21	IO63PDB1V2	D27	GND
B16	IO37PDB0V4	C22	IO67NDB1V3	D28	GBA0/IO81NPB1V4
B17	IO41PDB1V0	C23	IO67PDB1V3	D29	VCC
B18	IO51NDB1V1	C24	IO75NDB1V4	D30	GBA2/IO82PPB2V0
B19	IO59PDB1V2	C25	IO75PDB1V4	E1	GND
B20	IO53PDB1V1	C26	VCCIB1	E2	IO303NPB7V3
B21	IO53NDB1V1	C27	IO64PPB1V2	E3	VCCIB7
B22	IO61NDB1V2	C28	VCC	E4	IO305PPB7V3
B23	IO61PDB1V2	C29	GBA1/IO81PPB1V4	E5	VCC
B24	IO69NPB1V3	C30	GND	E6	GAC0/IO02NDB0V0
B25	VCC	D1	IO303PPB7V3	E7	VCCIB0
B26	GBC0/IO79NPB1V4	D2	VCC	E8	IO06PPB0V0
B27	VCC	D3	IO305NPB7V3	E9	IO24NDB0V2
B28	IO64NPB1V2	D4	GND	E10	IO24PDB0V2
B29	GND	D5	GAA1/IO00PPB0V0	E11	IO13NDB0V1

896-Pin FBGA	
Pin Number	A3PE3000L Function
E12	IO13PDB0V1
E13	IO34NDB0V4
E14	IO34PDB0V4
E15	IO40NDB0V4
E16	IO49NDB1V1
E17	IO49PDB1V1
E18	IO50PDB1V1
E19	IO58PDB1V2
E20	IO60NDB1V2
E21	IO77PDB1V4
E22	IO68NDB1V3
E23	IO68PDB1V3
E24	VCCIB1
E25	IO74PDB1V4
E26	VCC
E27	GBB1/IO80PPB1V4
E28	VCCIB2
E29	IO82NPB2V0
E30	GND
F1	IO296PPB7V2
F2	VCC
F3	IO306PDB7V4
F4	IO297PDB7V2
F5	VMV7
F5	VMV7
F6	GND
F7	GNDQ
F8	IO12NDB0V1
F9	IO12PDB0V1
F10	IO10PDB0V1
F11	IO16PDB0V1
F12	IO22NDB0V2
F13	IO30NDB0V3
F14	IO30PDB0V3
F15	IO36PDB0V4
F16	IO48NDB1V0

896-Pin FBGA	
Pin Number	A3PE3000L Function
F17	IO48PDB1V0
F18	IO50NDB1V1
F19	IO58NDB1V2
F20	IO60PDB1V2
F21	IO77NDB1V4
F22	IO72NDB1V3
F23	IO72PDB1V3
F24	GNDQ
F25	GND
F26	VMV2
F26	VMV2
F27	IO86PDB2V0
F28	IO92PDB2V1
F29	VCC
F30	IO100NPB2V2
G1	GND
G2	IO296NPB7V2
G3	IO306NDB7V4
G4	IO297NDB7V2
G5	VCCIB7
G6	GNDQ
G6	GNDQ
G7	VCC
G8	VMV0
G9	VCCIB0
G10	IO10NDB0V1
G11	IO16NDB0V1
G12	IO22PDB0V2
G13	IO26PPB0V3
G14	IO38NPB0V4
G15	IO36NDB0V4
G16	IO46NDB1V0
G17	IO46PDB1V0
G18	IO56NDB1V1
G19	IO56PDB1V1
G20	IO66NDB1V3

896-Pin FBGA	
Pin Number	A3PE3000L Function
G21	IO66PDB1V3
G22	VCCIB1
G23	VMV1
G24	VCC
G25	GNDQ
G25	GNDQ
G26	VCCIB2
G27	IO86NDB2V0
G28	IO92NDB2V1
G29	IO100PPB2V2
G30	GND
H1	IO294PDB7V2
H2	IO294NDB7V2
H3	IO300NDB7V3
H4	IO300PDB7V3
H5	IO295PDB7V2
H6	IO299PDB7V3
H7	VCOMPLA
H8	GND
H9	IO08NDB0V0
H10	IO08PDB0V0
H11	IO18PDB0V2
H12	IO26NPB0V3
H13	IO28NDB0V3
H14	IO28PDB0V3
H15	IO38PPB0V4
H16	IO42NDB1V0
H17	IO52NDB1V1
H18	IO52PDB1V1
H19	IO62NDB1V2
H20	IO62PDB1V2
H21	IO70NDB1V3
H22	IO70PDB1V3
H23	GND
H24	VCOMPLB
H25	GBC2/IO84PDB2V0

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
H26	IO84NDB2V0	K2	IO288PDB7V1	L8	IO293PDB7V2
H27	IO96PDB2V1	K3	IO304NDB7V3	L9	IO293NDB7V2
H28	IO96NDB2V1	K4	IO304PDB7V3	L10	IO307NPB7V4
H29	IO89PDB2V0	K5	GAB2/IO308PDB7V4	L11	VCC
H30	IO89NDB2V0	K6	IO308NDB7V4	L12	VCC
J1	IO290NDB7V2	K7	IO301PDB7V3	L13	VCC
J2	IO290PDB7V2	K8	IO301NDB7V3	L14	VCC
J3	IO302NDB7V3	K9	GAC2/IO307PPB7V4	L15	VCC
J4	IO302PDB7V3	K10	VCC	L16	VCC
J5	IO295NDB7V2	K11	IO04PPB0V0	L17	VCC
J6	IO299NDB7V3	K12	VCCIB0	L18	VCC
J7	VCCIB7	K13	VCCIB0	L19	VCC
J8	VCCPLA	K14	VCCIB0	L20	VCC
J9	VCC	K15	VCCIB0	L21	IO78NPB1V4
J10	IO04NPB0V0	K16	VCCIB1	L22	IO104NPB2V2
J11	IO18NDB0V2	K17	VCCIB1	L23	IO98NDB2V2
J12	IO20NDB0V2	K18	VCCIB1	L24	IO98PDB2V2
J13	IO20PDB0V2	K19	VCCIB1	L25	IO87PDB2V0
J14	IO32NDB0V3	K20	IO76PPB1V4	L26	IO87NDB2V0
J15	IO32PDB0V3	K21	VCC	L27	IO97PDB2V1
J16	IO42PDB1V0	K22	IO78PPB1V4	L28	IO101PDB2V2
J17	IO44NDB1V0	K23	IO88NDB2V0	L29	IO103PDB2V2
J18	IO44PDB1V0	K24	IO88PDB2V0	L30	IO119NDB3V0
J19	IO54NDB1V1	K25	IO94PDB2V1	M1	IO282NDB7V1
J20	IO54PDB1V1	K26	IO94NDB2V1	M2	IO282PDB7V1
J21	IO76NPB1V4	K27	IO85PDB2V0	M3	IO292NDB7V2
J22	VCC	K28	IO85NDB2V0	M4	IO292PDB7V2
J23	VCCPLB	K29	IO93PDB2V1	M5	IO283NDB7V1
J24	VCCIB2	K30	IO93NDB2V1	M6	IO285PDB7V1
J25	IO90PDB2V1	L1	IO286NDB7V1	M7	IO287PDB7V1
J26	IO90NDB2V1	L2	IO286PDB7V1	M8	IO289PDB7V1
J27	GBB2/IO83PDB2V0	L3	IO298NDB7V3	M9	IO289NDB7V1
J28	IO83NDB2V0	L4	IO298PDB7V3	M10	VCCIB7
J29	IO91PDB2V1	L5	IO283PDB7V1	M11	VCC
J30	IO91NDB2V1	L6	IO291NDB7V2	M12	GND
K1	IO288NDB7V1	L7	IO291PDB7V2	M13	GND



896-Pin FBGA	
Pin Number	A3PE3000L Function
M14	GND
M15	GND
M16	GND
M17	GND
M18	GND
M19	GND
M20	VCC
M21	VCCIB2
M22	NC
M23	IO104PPB2V2
M24	IO102PDB2V2
M25	IO102NDB2V2
M26	IO95PDB2V1
M27	IO97NDB2V1
M28	IO101NDB2V2
M29	IO103NDB2V2
M30	IO119PDB3V0
N1	IO276PDB7V0
N2	IO278PDB7V0
N3	IO280PDB7V0
N4	IO284PDB7V1
N5	IO279PDB7V0
N6	IO285NDB7V1
N7	IO287NDB7V1
N8	IO281NDB7V0
N9	IO281PDB7V0
N10	VCCIB7
N11	VCC
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
N18	GND
N19	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
N20	VCC
N21	VCCIB2
N22	IO106NDB2V3
N23	IO106PDB2V3
N24	IO108PDB2V3
N25	IO108NDB2V3
N26	IO95NDB2V1
N27	IO99NDB2V2
N28	IO99PDB2V2
N29	IO107PDB2V3
N30	IO107NDB2V3
P1	IO276NDB7V0
P2	IO278NDB7V0
P3	IO280NDB7V0
P4	IO284NDB7V1
P5	IO279NDB7V0
P6	GFC1/IO275PDB7V0
P7	GFC0/IO275NDB7V0
P8	IO277PDB7V0
P9	IO277NDB7V0
P10	VCCIB7
P11	VCC
P12	GND
P13	GND
P14	GND
P15	GND
P16	GND
P17	GND
P18	GND
P19	GND
P20	VCC
P21	VCCIB2
P22	GCC1/IO112PDB2V3
P23	IO110PDB2V3
P24	IO110NDB2V3
P25	IO109PPB2V3

896-Pin FBGA	
Pin Number	A3PE3000L Function
P26	IO111NPB2V3
P27	IO105PDB2V2
P28	IO105NDB2V2
P29	GCC2/IO117PDB3V0
P30	IO117NDB3V0
R1	GFC2/IO270PDB6V4
R2	GFB1/IO274PPB7V0
R3	VCOMPLF
R4	GFA0/IO273NDB6V4
R5	GFB0/IO274NPB7V0
R6	IO271NDB6V4
R7	GFB2/IO271PDB6V4
R8	IO269PDB6V4
R9	IO269NDB6V4
R10	VCCIB7
R11	VCC
R12	GND
R13	GND
R14	GND
R15	GND
R16	GND
R17	GND
R18	GND
R19	GND
R20	VCC
R21	VCCIB2
R22	GCC0/IO112NDB2V3
R23	GCB2/IO116PDB3V0
R24	IO118PDB3V0
R25	IO111PPB2V3
R26	IO122PPB3V1
R27	GCA0/IO114NPB3V0
R28	VCOMPLC
R29	GCB1/IO113PPB2V3
R30	IO115NPB3V0
T1	IO270NDB6V4

896-Pin FBGA		896-Pin FBGA		896-Pin FBGA	
Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function	Pin Number	A3PE3000L Function
T2	VCCPLF	U8	IO265NDB6V3	V14	GND
T3	GFA2/IO272PPB6V4	U9	IO263NDB6V3	V15	GND
T4	GFA1/IO273PDB6V4	U10	VCCIB6	V16	GND
T5	IO272NPB6V4	U11	VCC	V17	GND
T6	IO267NDB6V4	U12	GND	V18	GND
T7	IO267PDB6V4	U13	GND	V19	GND
T8	IO265PDB6V3	U14	GND	V20	VCC
T9	IO263PDB6V3	U15	GND	V21	VCCIB3
T10	VCCIB6	U16	GND	V22	IO120NDB3V0
T11	VCC	U17	GND	V23	IO128NDB3V1
T12	GND	U18	GND	V24	IO132PDB3V2
T13	GND	U19	GND	V25	IO130PPB3V2
T14	GND	U20	VCC	V26	IO126NDB3V1
T15	GND	U21	VCCIB3	V27	IO129NDB3V1
T16	GND	U22	IO120PDB3V0	V28	IO127NDB3V1
T17	GND	U23	IO128PDB3V1	V29	IO125NDB3V1
T18	GND	U24	IO124PDB3V1	V30	IO123PDB3V1
T19	GND	U25	IO124NDB3V1	W1	IO266NDB6V4
T20	VCC	U26	IO126PDB3V1	W2	IO262NDB6V3
T21	VCCIB3	U27	IO129PDB3V1	W3	IO260NDB6V3
T22	IO109NPB2V3	U28	IO127PDB3V1	W4	IO252NDB6V2
T23	IO116NDB3V0	U29	IO125PDB3V1	W5	IO251NDB6V2
T24	IO118NDB3V0	U30	IO121NDB3V0	W6	IO251PDB6V2
T25	IO122NPB3V1	V1	IO268NDB6V4	W7	IO255NDB6V2
T26	GCA1/IO114PPB3V0	V2	IO262PDB6V3	W8	IO249PPB6V1
T27	GCB0/IO113NPB2V3	V3	IO260PDB6V3	W9	IO253PDB6V2
T28	GCA2/IO115PPB3V0	V4	IO252PDB6V2	W10	VCCIB6
T29	VCCPLC	V5	IO257NPB6V2	W11	VCC
T30	IO121PDB3V0	V6	IO261NPB6V3	W12	GND
U1	IO268PDB6V4	V7	IO255PDB6V2	W13	GND
U2	IO264NDB6V3	V8	IO259PDB6V3	W14	GND
U3	IO264PDB6V3	V9	IO259NDB6V3	W15	GND
U4	IO258PDB6V3	V10	VCCIB6	W16	GND
U5	IO258NDB6V3	V11	VCC	W17	GND
U6	IO257PPB6V2	V12	GND	W18	GND
U7	IO261PPB6V3	V13	GND	W19	GND

896-Pin FBGA	
Pin Number	A3PE3000L Function
W20	VCC
W21	VCCIB3
W22	IO134PDB3V2
W23	IO138PDB3V3
W24	IO132NDB3V2
W25	IO136NPB3V2
W26	IO130NPB3V2
W27	IO141PDB3V3
W28	IO135PDB3V2
W29	IO131PDB3V2
W30	IO123NDB3V1
Y1	IO266PDB6V4
Y2	IO250PDB6V2
Y3	IO250NDB6V2
Y4	IO246PDB6V1
Y5	IO247NDB6V1
Y6	IO247PDB6V1
Y7	IO249NPB6V1
Y8	IO245PDB6V1
Y9	IO253NDB6V2
Y10	GEB0/IO235NPB6V0
Y11	VCC
Y12	VCC
Y13	VCC
Y14	VCC
Y15	VCC
Y16	VCC
Y17	VCC
Y18	VCC
Y19	VCC
Y20	VCC
Y21	IO142PPB3V3
Y22	IO134NDB3V2
Y23	IO138NDB3V3
Y24	IO140NDB3V3
Y25	IO140PDB3V3

896-Pin FBGA	
Pin Number	A3PE3000L Function
Y26	IO136PPB3V2
Y27	IO141NDB3V3
Y28	IO135NDB3V2
Y29	IO131NDB3V2
Y30	IO133PDB3V2



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## 4 – Datasheet Information

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### Datasheet Categories

#### ***Categories***

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Military ProASIC3/EL Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

#### ***Product Brief***

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

#### ***Advance***

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

#### ***Preliminary***

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

#### ***Unmarked (production)***

This version contains information that is considered to be final.

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