



Advanced
Micro
Devices

MACH130-15/20

High-Density EE CMOS Programmable Logic

DISTINCTIVE CHARACTERISTICS

- 84 Pins
- 64 Macrocells
- 15 ns t_{PD} Commercial
18 ns t_{PD} Industrial
- 66.6 MHz f_{CNT}
- 70 Inputs
- 64 Outputs
- 64 Flip-flops; 4 clock choices
- 4 "PAL26V16" Blocks
- Pin-compatible with MACH131, MACH230,
MACH231, MACH435

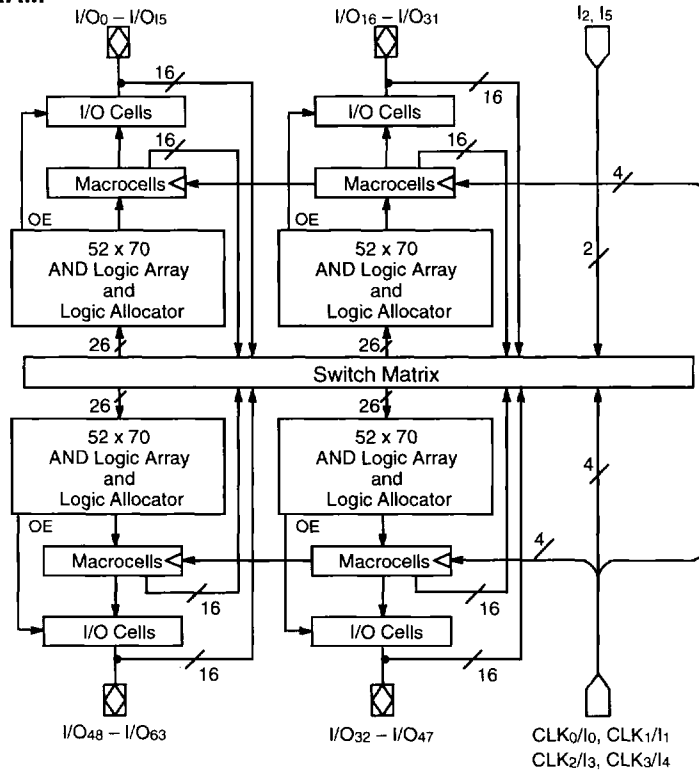
GENERAL DESCRIPTION

The MACH130 is a member of AMD's high-performance EE CMOS MACH 1 family. This device has approximately six times the logic macrocell capability of the popular PAL22V10 without loss of speed.

The MACH130 consists of four PAL blocks interconnected by a programmable switch matrix. The switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH130 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

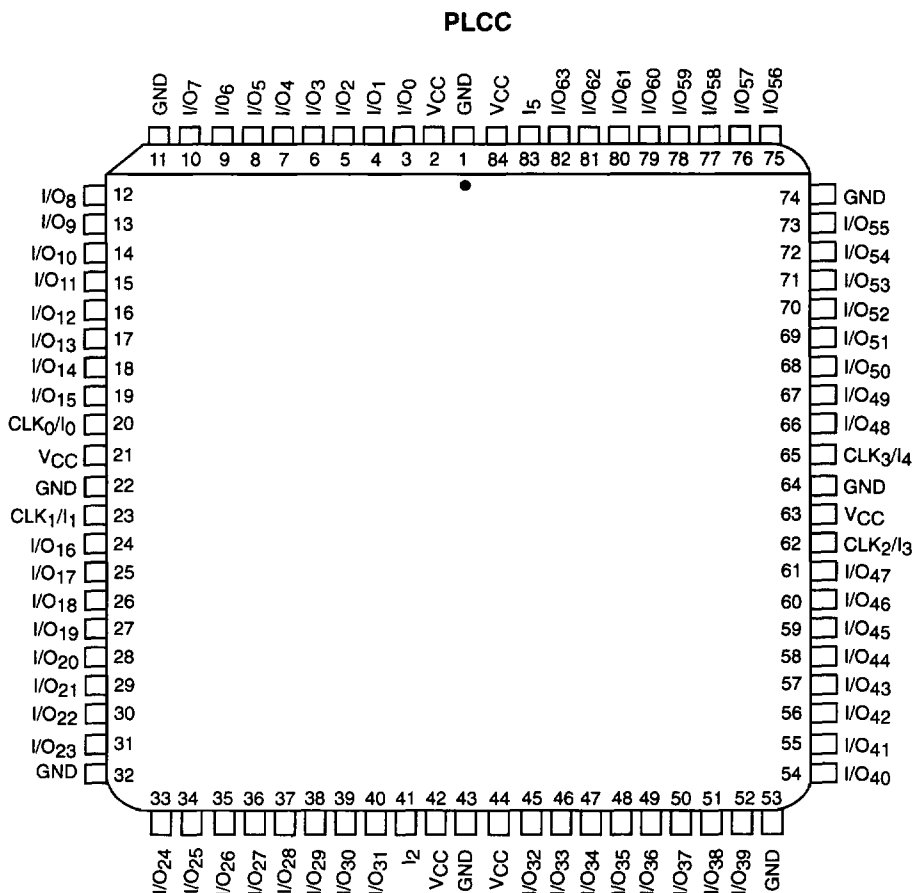
BLOCK DIAGRAM



14131H-1

CONNECTION DIAGRAM

Top View



Note:
Pin-compatible with MACH131, MACH230, MACH231, and MACH435.

14131H-2

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

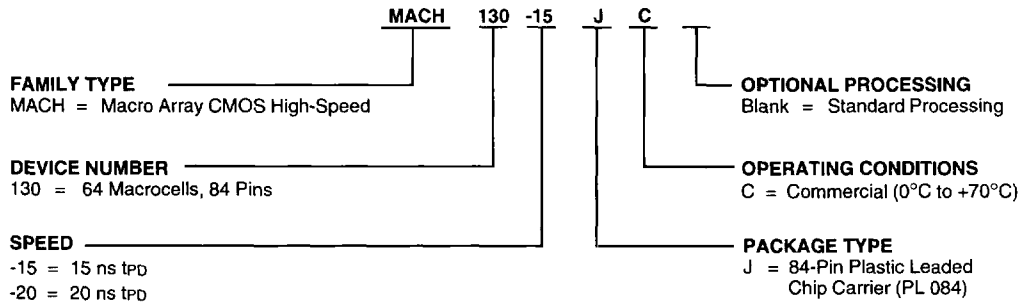
I/O = Input/Output

V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH130-15	JC
MACH130-20	

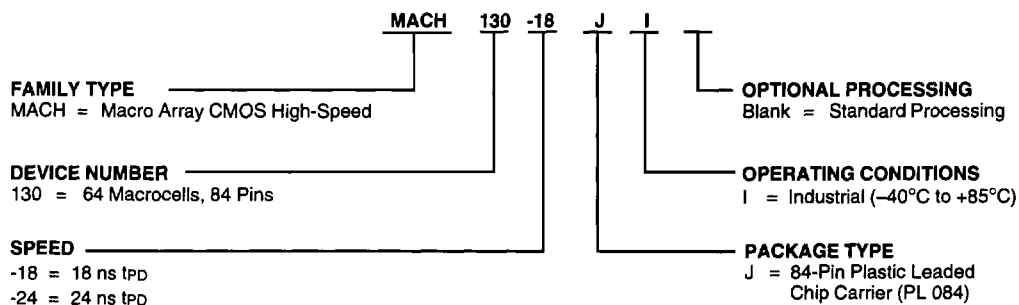
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

AMD programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH130-18	JI
MACH130-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH130 consists of four PAL blocks connected by a switch matrix. There are 64 I/O pins and 2 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are 4 clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH130 (Figure 1) contains a 64-product-term logic array, a logic allocator, 16 macrocells and 16 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PAL26V16".

There are four additional output enable product terms in each PAL block. For purposes of output enable, the 16 I/O cells are divided into 2 banks of 8 macrocells. Each bank is allocated two of the output enable product terms.

An asynchronous reset product term and an asynchronous preset product term are provided for flip-flop initialization. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH130 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 16 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-Term Array

The MACH130 product-term array consists of 64 product terms for logic use, and 6 special-purpose product terms. Four of the special-purpose product terms provide programmable output enable, one provides asynchronous reset, and one provides asynchronous preset. Two of the output enable product terms are used for the first eight I/O cells; the other two control the last eight macrocells.

The Logic Allocator

The logic allocator in the MACH130 takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁
M ₁	C ₀ , C ₁ , C ₂
M ₂	C ₁ , C ₂ , C ₃
M ₃	C ₂ , C ₃ , C ₄
M ₄	C ₃ , C ₄ , C ₅
M ₅	C ₄ , C ₅ , C ₆
M ₆	C ₅ , C ₆ , C ₇
M ₇	C ₆ , C ₇ , C ₈
M ₈	C ₇ , C ₈ , C ₉
M ₉	C ₈ , C ₉ , C ₁₀
M ₁₀	C ₉ , C ₁₀ , C ₁₁
M ₁₁	C ₁₀ , C ₁₁ , C ₁₂
M ₁₂	C ₁₁ , C ₁₂ , C ₁₃
M ₁₃	C ₁₂ , C ₁₃ , C ₁₄
M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₁₅	C ₁₄ , C ₁₅

The Macrocell

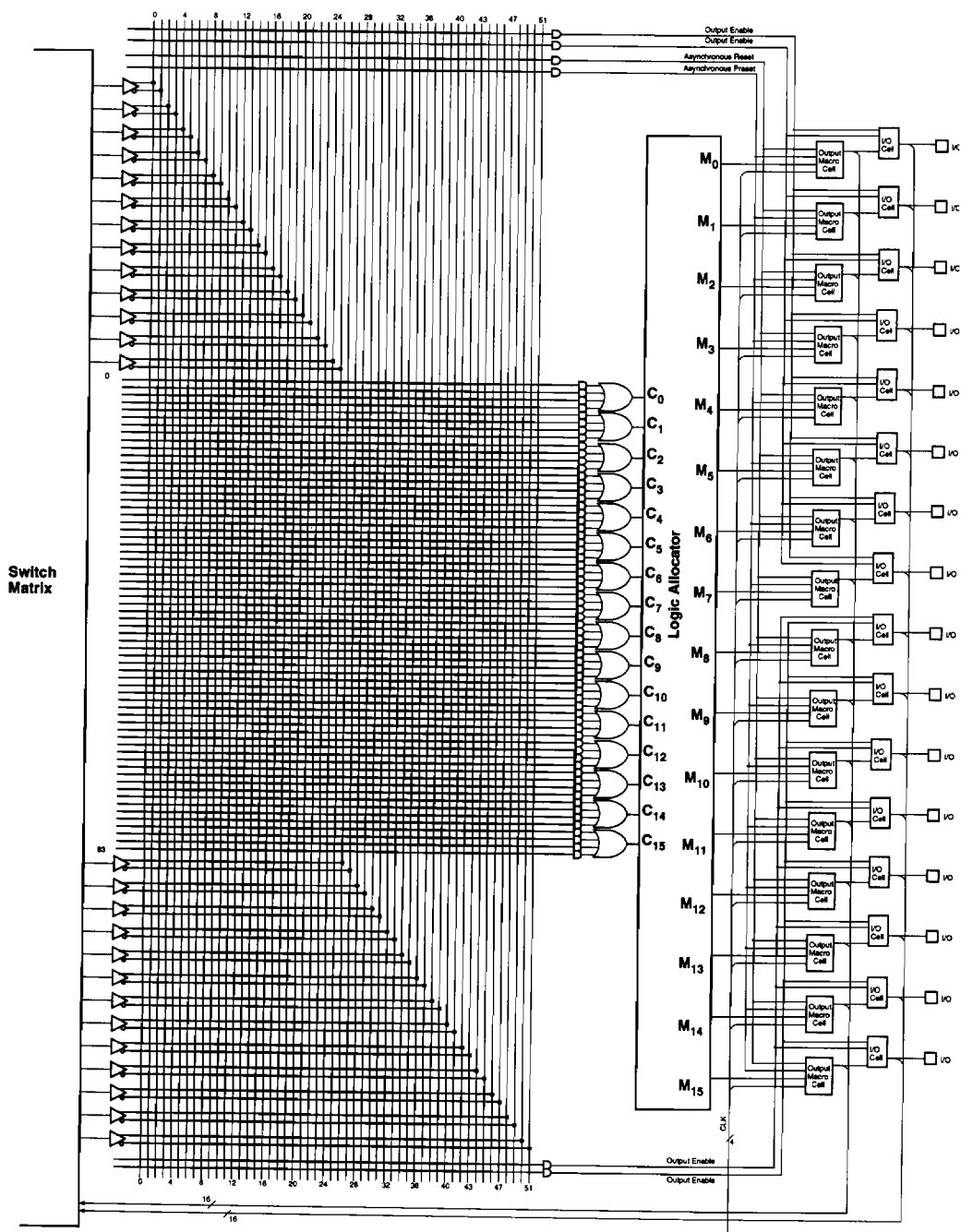
The MACH130 macrocells can be configured as either registered or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured as registered or combinatorial. The flip-flops can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of four global clock pins, which are also available as logic inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The I/O Cell

The I/O cell in the MACH130 consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to eight I/O cells. Within each PAL block, two product terms are available for selection by the first eight three-state outputs; two other product terms are available for selection by the last eight three-state outputs.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.



14131H-

Figure 1. MACH130 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature	
With Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O	
Pin Voltage	−0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current	
($T_A = 0^\circ\text{C}$ to 70°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	
Operating in Free Air	0°C to $+70^\circ\text{C}$
Supply Voltage (V_{CC})	
with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 16$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 2)			10	μA
I_{IL}	Input LOW Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 2)			−10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			−10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)	−30		−130	mA
I_{CC}	Supply Current (Typical)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$, $f = 25$ MHz (Note 4)		190		mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.
 $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.
- Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V, T _A = 25°C	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		-15		-20		Unit
			Min	Max	Min	Max	
t _{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)			15		20	ns
t _S	Setup Time from Input, I/O, or Feedback to Clock	D-type	10		13		ns
		T-type	11		14		ns
t _H	Hold Time		0		0		ns
t _{CO}	Clock to Output (Note 3)			10		12	ns
t _{WL}	Clock Width	LOW	6		8		ns
t _{WH}		HIGH	6		8		ns
f _{MAX}	Maximum Frequency (Note 1)	External Feedback	1/(t _S + t _{CO})		D-type	50	MHz
					T-type	47.6	MHz
		Internal Feedback (f _{CNT})			D-type	66.6	MHz
					T-type	55.5	MHz
		No Feedback	1/(t _{WL} + t _{WH})			83.3	MHz
t _{AR}	Asynchronous Reset to Registered Output			20		25	ns
t _{ARW}	Asynchronous Reset Width (Note 1)		15		20		ns
t _{ARR}	Asynchronous Reset Recovery Time (Note 1)		10		15		ns
t _{AP}	Asynchronous Preset to Registered Output			20		25	ns
t _{APW}	Asynchronous Preset Width (Note 1)		15		20		ns
t _{APR}	Asynchronous Preset Recovery Time (Note 1)		10		15		ns
t _{EA}	Input, I/O, or Feedback to Output Enable (Note 3)			15		20	ns
t _{ED}	Input, I/O, or Feedback to Output Disable (Note 3)			15		20	ns

Notes:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
2. See Switching Test Circuit, for test conditions.
3. Parameters measured with 32 outputs switching.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature	
With Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	−0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A)	
Operating in Free Air	−40°C to +85°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 16$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 2)			10	μA
I_{IL}	Input LOW Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 2)			−10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			−10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 3)	−30		−130	mA
I_{CC}	Supply Current (Typical)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$, $f = 25$ MHz (Note 4)		190		mA

Notes:

- These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.
- I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.
- Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0\text{ V}$	$V_{CC} = 5.0\text{ V}, T_A = 25^\circ\text{C}$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0\text{ V}$	$f = 1\text{ MHz}$	8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

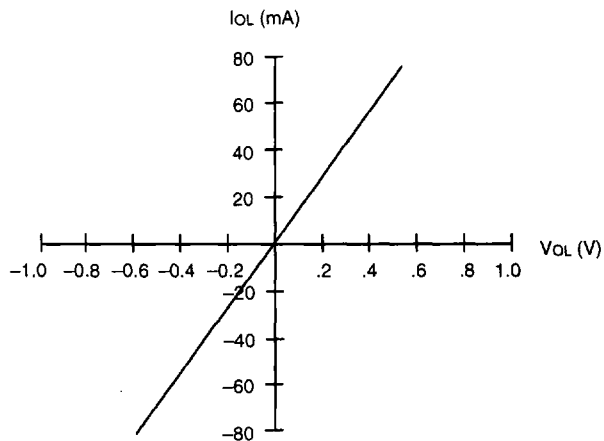
Parameter Symbol	Parameter Description			-18		-24		Unit	
				Min	Max	Min	Max		
t _{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)				18		24	ns	
t _S	Setup Time from Input, I/O, or Feedback to Clock		D-type	12		16		ns	
			T-type	13.5		17		ns	
t _H	Hold Time			0		0		ns	
t _{CO}	Clock to Output (Note 3)				12		14.5	ns	
t _{WL}	Clock Width		LOW	7.5		10		ns	
t _{WH}			HIGH	7.5		10		ns	
f _{MAX}	Maximum Frequency (Note 1)	External Feedback	1/(t _S + t _{CO})		D-type	40		32	MHz
					T-type	38		30	MHz
		Internal Feedback (f _{CNT})			D-type	53		38	MHz
					T-type	44		34.5	MHz
		No Feedback	1/(t _{WL} + t _{WH})			66.5		50	MHz
t _{AR}	Asynchronous Reset to Registered Output				24		30	ns	
t _{ARW}	Asynchronous Reset Width (Note 1)			18		24		ns	
t _{ARR}	Asynchronous Reset Recovery Time (Note 1)			12		18		ns	
t _{AP}	Asynchronous Preset to Registered Output				24		30	ns	
t _{APW}	Asynchronous Preset Width (Note 1)			18		24		ns	
t _{APR}	Asynchronous Preset Recovery Time (Note 1)			12		18		ns	
t _{EA}	Input, I/O, or Feedback to Output Enable (Note 3)				18		24	ns	
t _{ED}	Input, I/O, or Feedback to Output Disable (Note 3)				18		24	ns	

Notes:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
2. See Switching Test Circuit, for test conditions.
3. Parameters measured with 32 outputs switching.

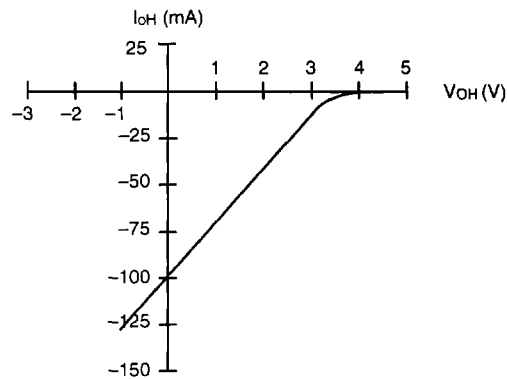
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

$V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$



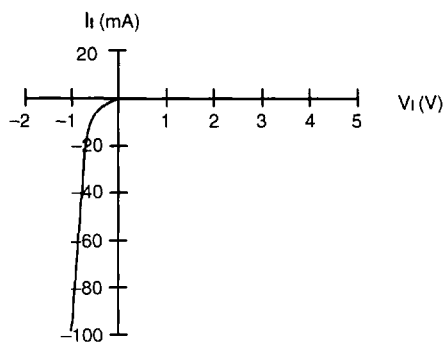
14131H-4

Output, LOW



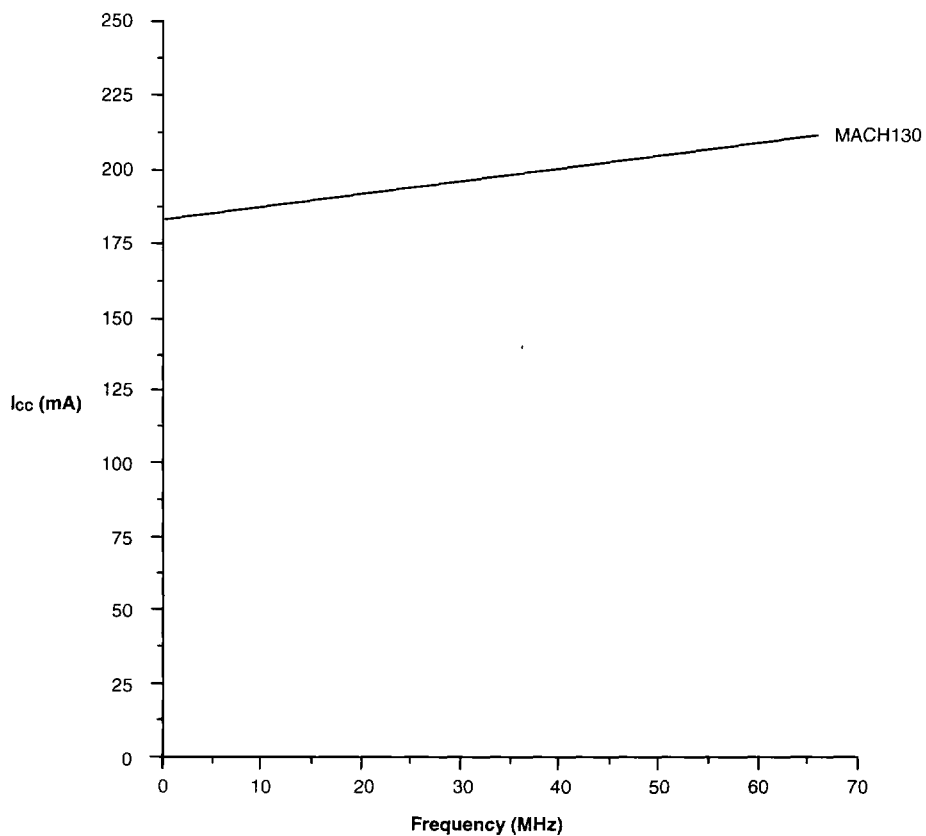
14131H-5

Output, HIGH



14131H-6

Input

TYPICAL I_{CC} CHARACTERISTICS $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ 

14131H-7

The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ	Unit
			PLCC	
θ_{jc}	Thermal impedance, junction to case		13	°C/W
θ_{ja}	Thermal impedance, junction to ambient		34	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	30	°C/W
		400 lfpm air	28	°C/W
		600 lfpm air	26	°C/W
		800 lfpm air	25	°C/W

Plastic θ_{jc} Considerations

The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.