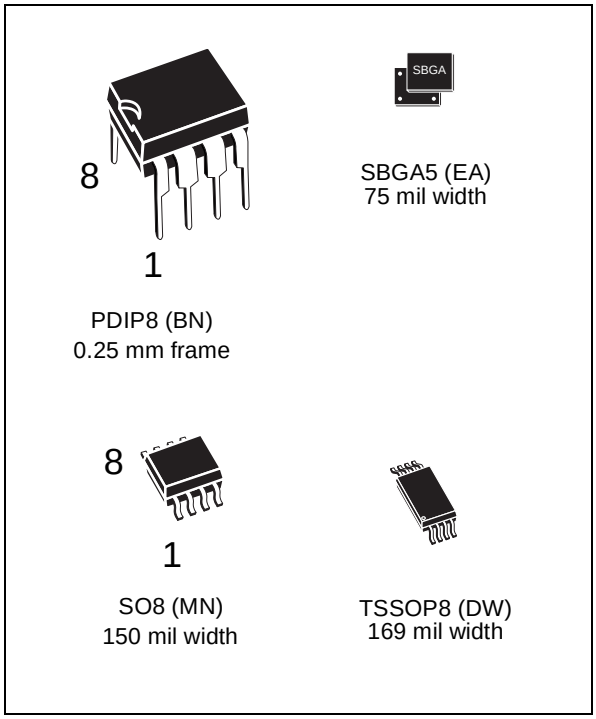
M24C16, M24C08
M24C04, M24C02, M24C01

16/8/4/2/1 Kbit Serial I²C Bus EEPROM

- Two Wire I^2C Serial Interface Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24Cxx
  - 2.5V to 5.5V for M24Cxx-W
  - 1.8V to 5.5V for M24Cxx-R
  - 1.8V to 3.6V for M24Cxx-S
- Write Control Input
- BYTE and PAGE WRITE (up to 16 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- More than 1 Million Erase/Write Cycles
- More than 40 Year Data Retention



DESCRIPTION

These I^2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 2048/1024/512/256/128 x 8 bit (M24C16, M24C08, M24C04, M24C02, M24C01), and operate with a power supply down to 2.5 V (for the -W version of each device), and down to 1.8 V (for the -R and -S versions of each device).

The M24C16, M24C08, M24C04, M24C02, M24C01 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages. The M24C16-S is also available in a Chip Scale package.

Table 1. Signal Names

E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

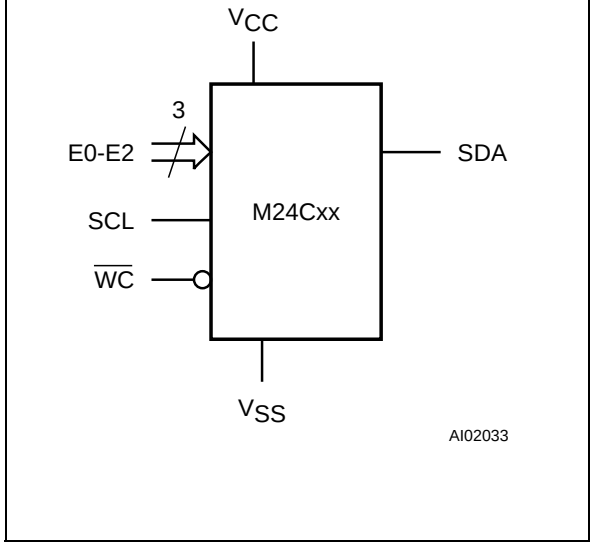
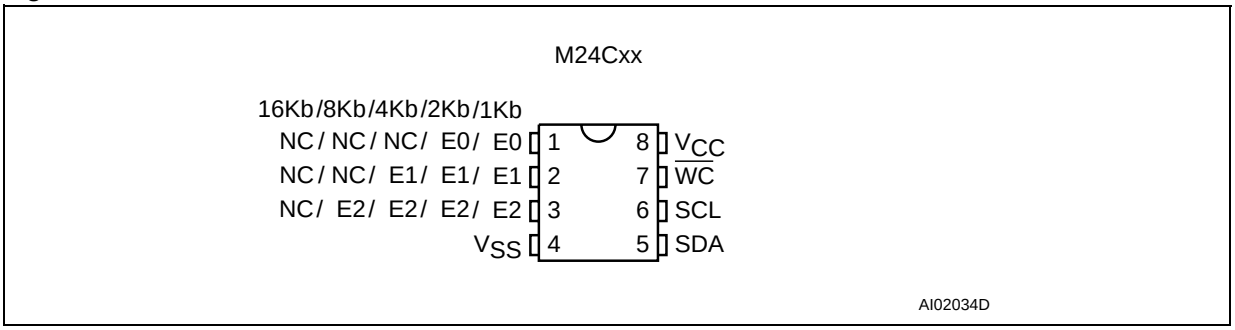
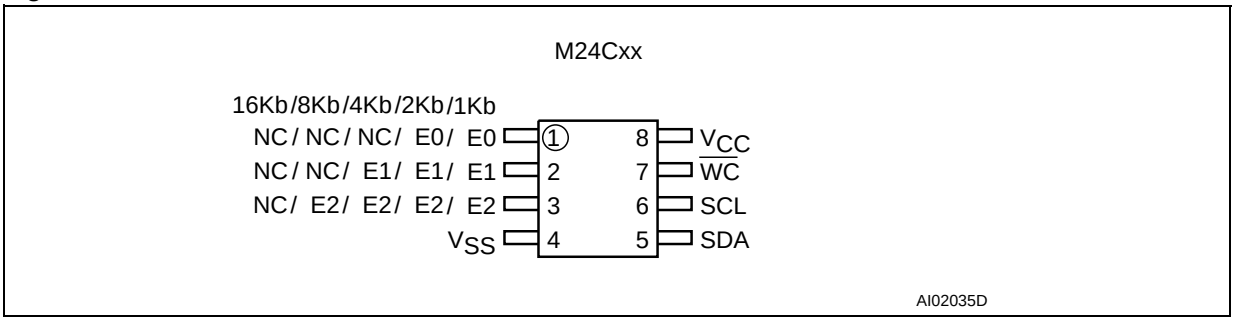


Figure 2A. DIP Connections



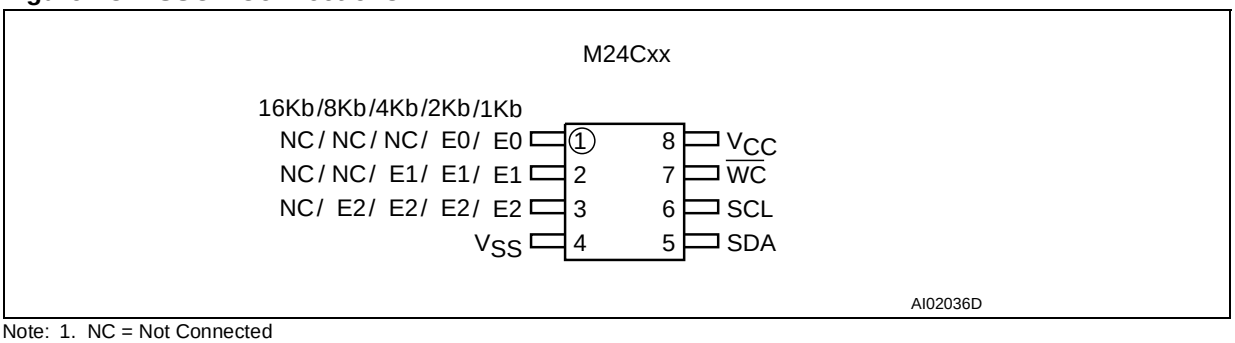
Note: 1. NC = Not Connected

Figure 2B. SO Connections



Note: 1. NC = Not Connected

Figure 2C. TSSOP Connections



Note: 1. NC = Not Connected

Figure 2D. SBGA Connections (top view, marking side, with balls on the underside)

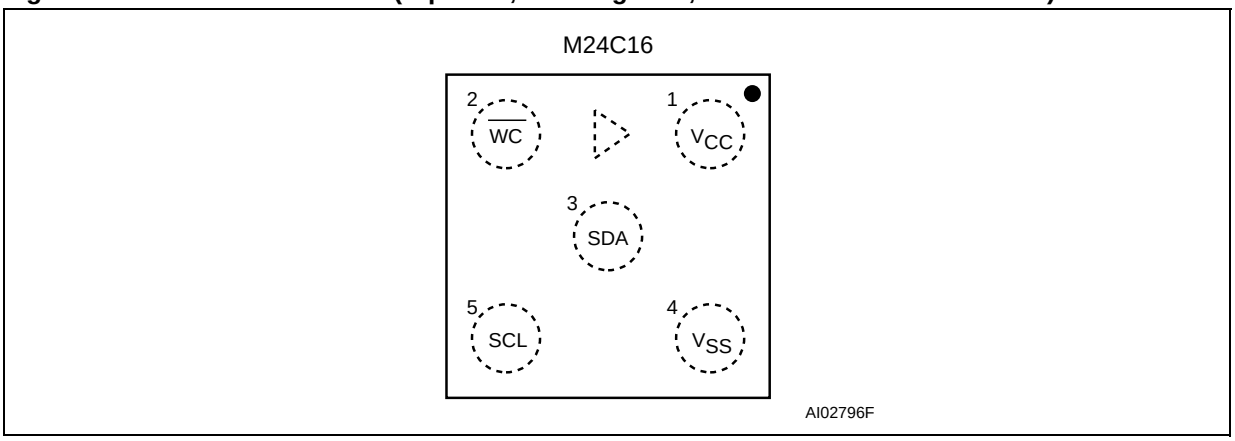


Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PDIP8: 10 seconds SO8: 20 seconds (max) [2] TSSOP8: 20 seconds (max) [2]	260 235 235	°C
V_{IO}	Input or Output range		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [3]		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. IPC/JEDEC J-STD-020A
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

These devices are compatible with the I^2C memory protocol. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a Device Select Code and $\overline{RW}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included. The internal reset is held active until V_{CC} has reached the POR

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

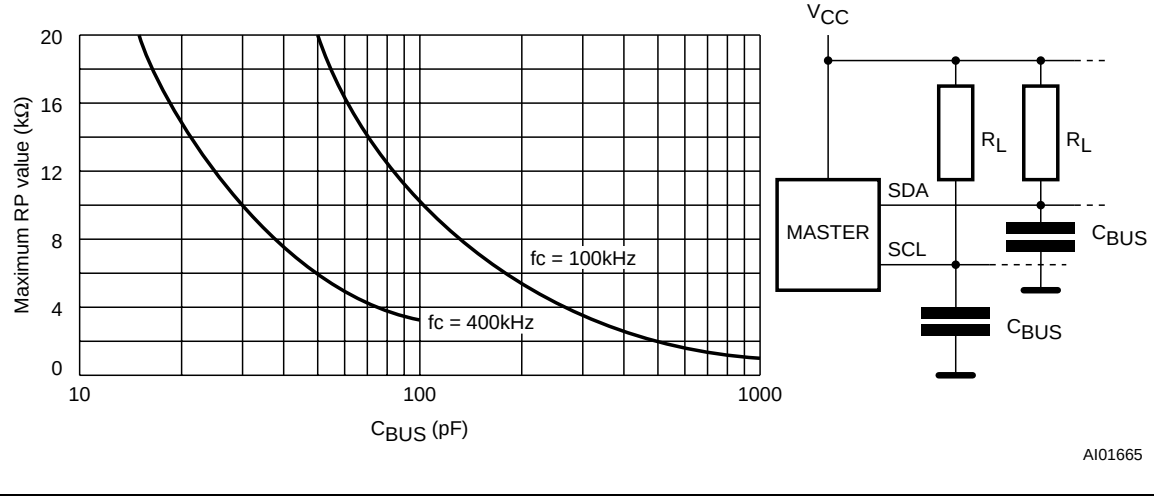
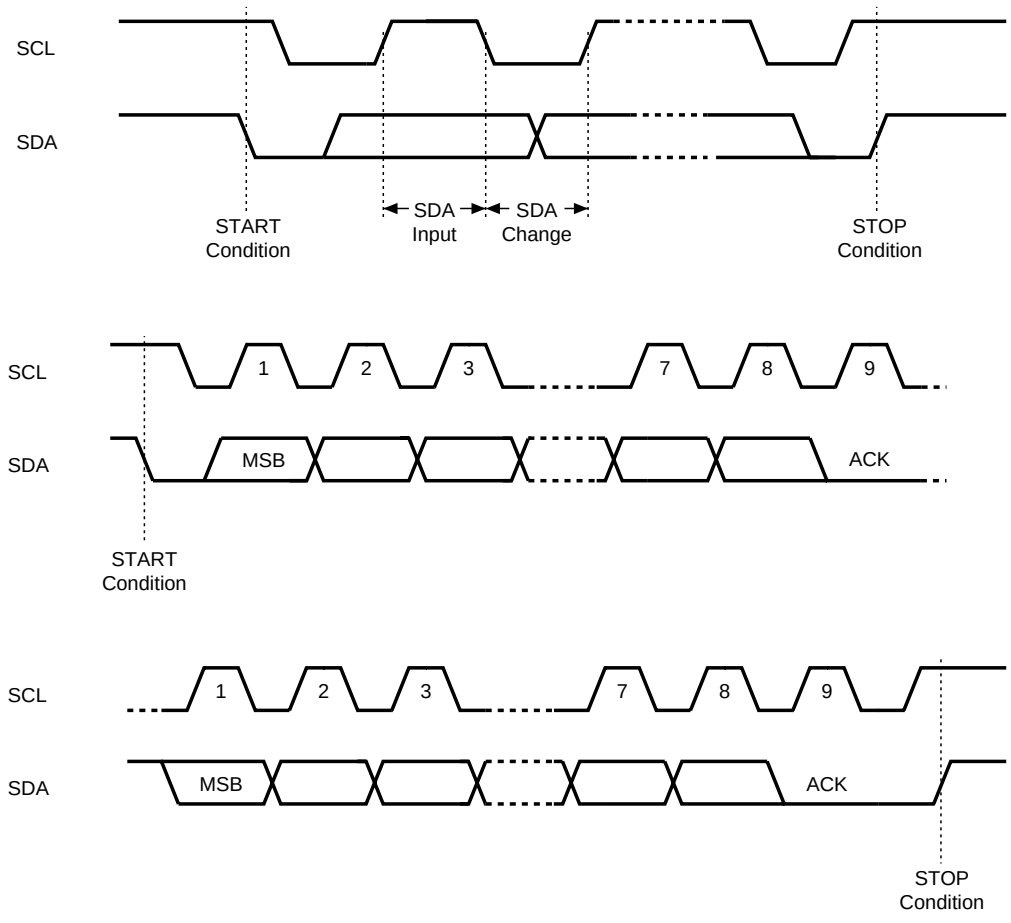


Figure 4. I²C Bus Protocol



threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E0, E1, E2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Device Select Code. These inputs must be tied to V_{CC} or V_{SS}, to establish the Device Select Code.

Table 3. Device Select Code [1]

	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
M24C01 Select Code	1	0	1	0	E2	E1	E0	RW
M24C02 Select Code	1	0	1	0	E2	E1	E0	RW
M24C04 Select Code	1	0	1	0	E2	E1	A8	RW
M24C08 Select Code	1	0	1	0	E2	A9	A8	RW
M24C16 Select Code	1	0	1	0	A10	A9	A8	RW

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.
3. A10, A9 and A8 represent most significant bits of the address.

Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven High. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven High, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

DEVICE OPERATION

The device supports the I^2C protocol. This is summarized in Figure 4. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M24Cxx device is always a slave in all communication.

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Stand-by mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

Acknowledge Bit (ACK)

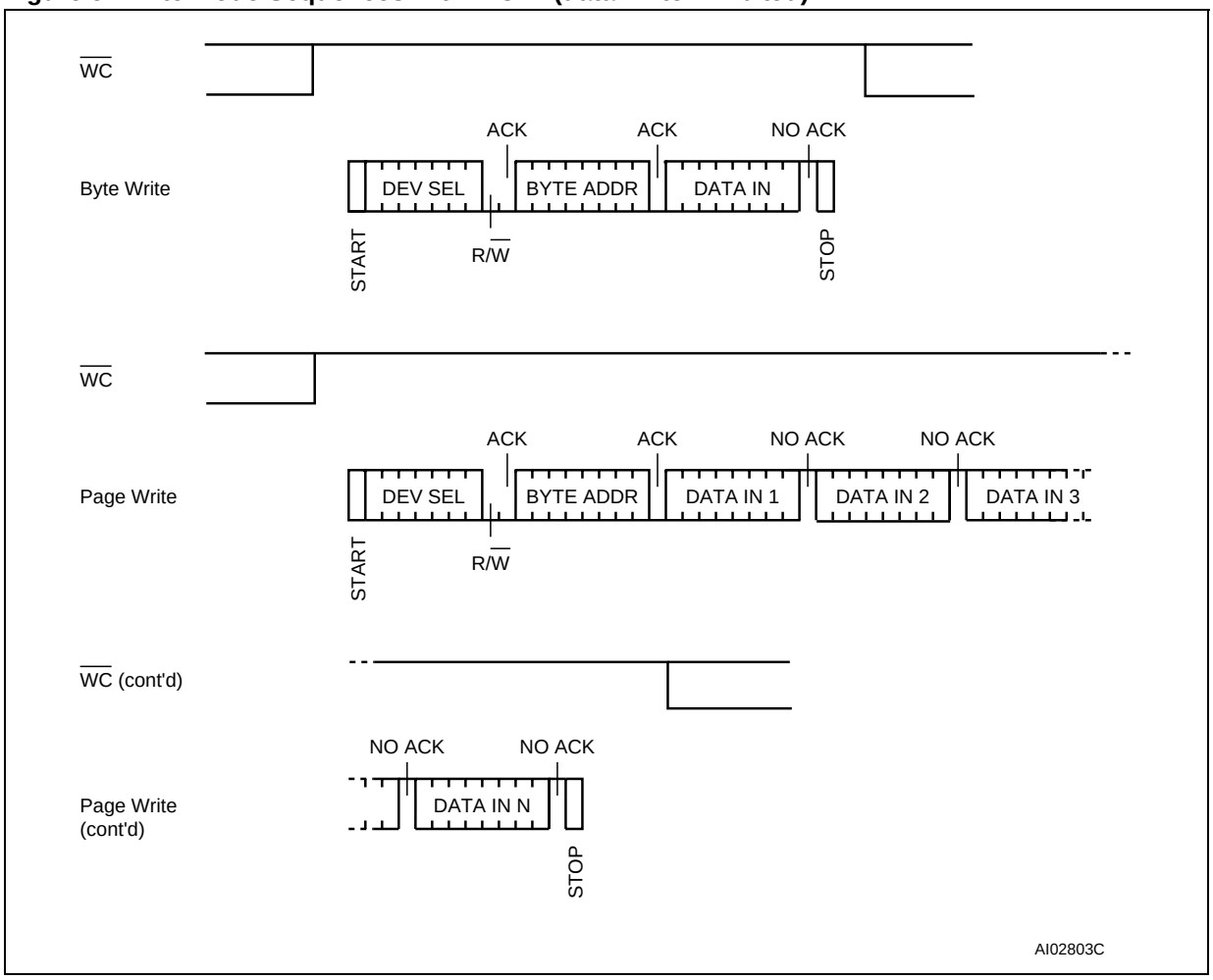
The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

Table 4. Operating Modes

Mode	RW bit	$\overline{WC}$ [1]	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, RW = 1
Random Address Read	0	X	1	START, Device Select, RW = 0, Address
	1	X		reSTART, Device Select, RW = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, RW = 0
Page Write	0	V_{IL}	≤ 16	START, Device Select, RW = 0

Note: 1. X = V_{IH} or V_{IL}.

Figure 5. Write Mode Sequences with $\overline{WC}$=1 (data write inhibited)



Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 3 (on Serial Data (SDA), most significant bit first).

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0). To address the memory array, the 4-bit Device Type Identifier is 1010b.

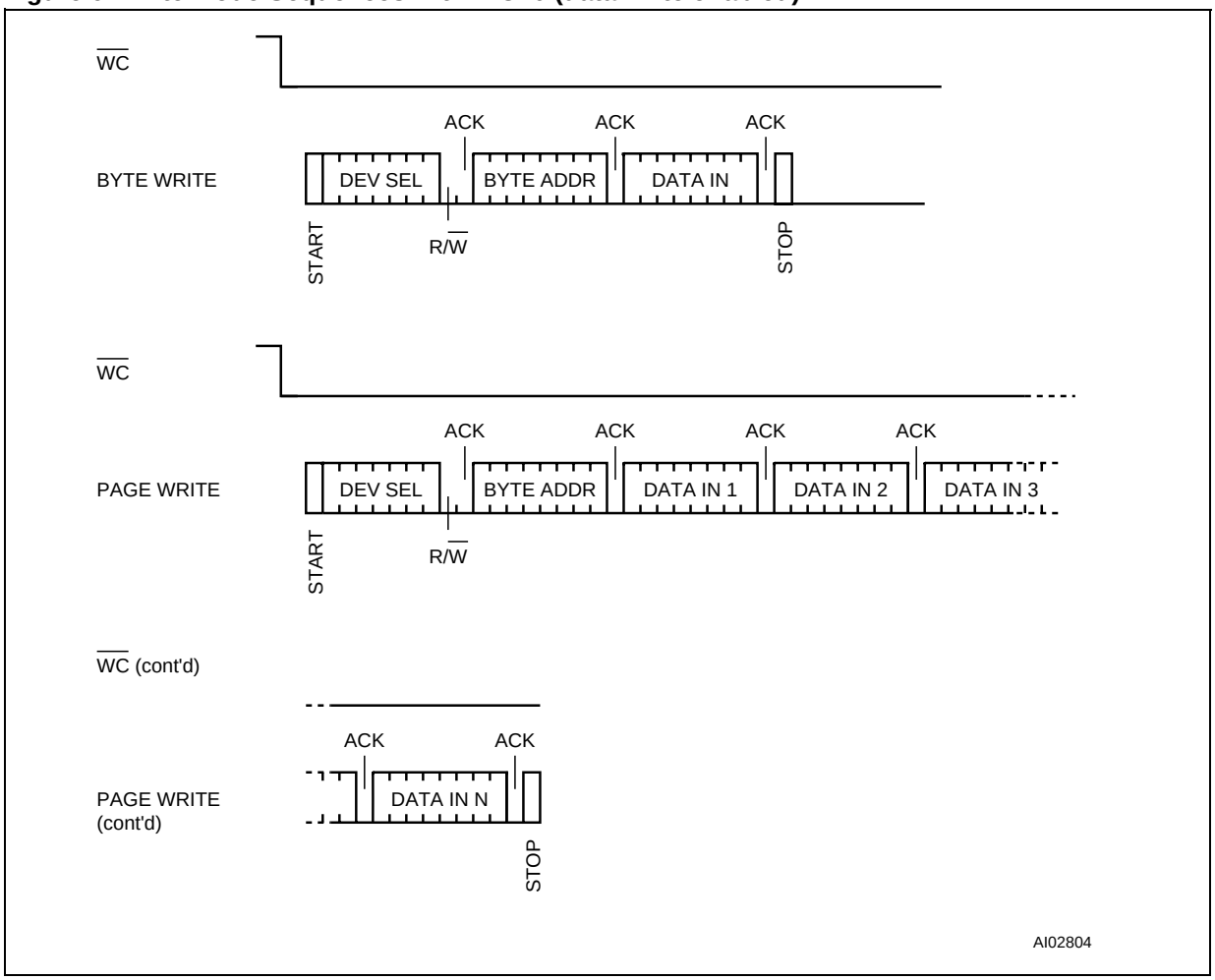
When the Device Select Code is received on Serial Data (SDA), the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E0, E1, E2) inputs.

The 8th bit is the Read/$\overline{Write}$ bit (R$\overline{W}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, it deselects itself from the bus, and goes into Stand-by mode.

Devices with larger memory capacities (the M24C16, M24C08 and M24C04) need more address bits. E0 is not available for use on devices that need to use address line A8; E1 is not available for devices that need to use address line A9, and E2 is not available for devices that need to use address line A10 (see Figures 2A to 2D and Table 3 for details). Using the E0, E1 and E2 inputs pins, up to eight M24C02 (or M24C01), four M24C04, two M24C08 or one M24C16 device can be connected to one I^{2}C bus. In each case, and in

Figure 6. Write Mode Sequences with $\overline{WC}$=0 (data write enabled)



the hybrid cases, this gives a total memory capacity of 16 Kbits, 2 KBytes (except where M24C01 devices are used).

Write Operations

Following a Start condition the bus master sends a Device Select Code with the R$\overline{W}$ bit reset to 0. The device acknowledges this, as shown in Figure 6, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if Write Control ($\overline{WC}$) is driven High. Any Write instruction with Write Control ($\overline{WC}$) driven High (during a period of time from the Start condition until the end of the address byte) will not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in Figure 5.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

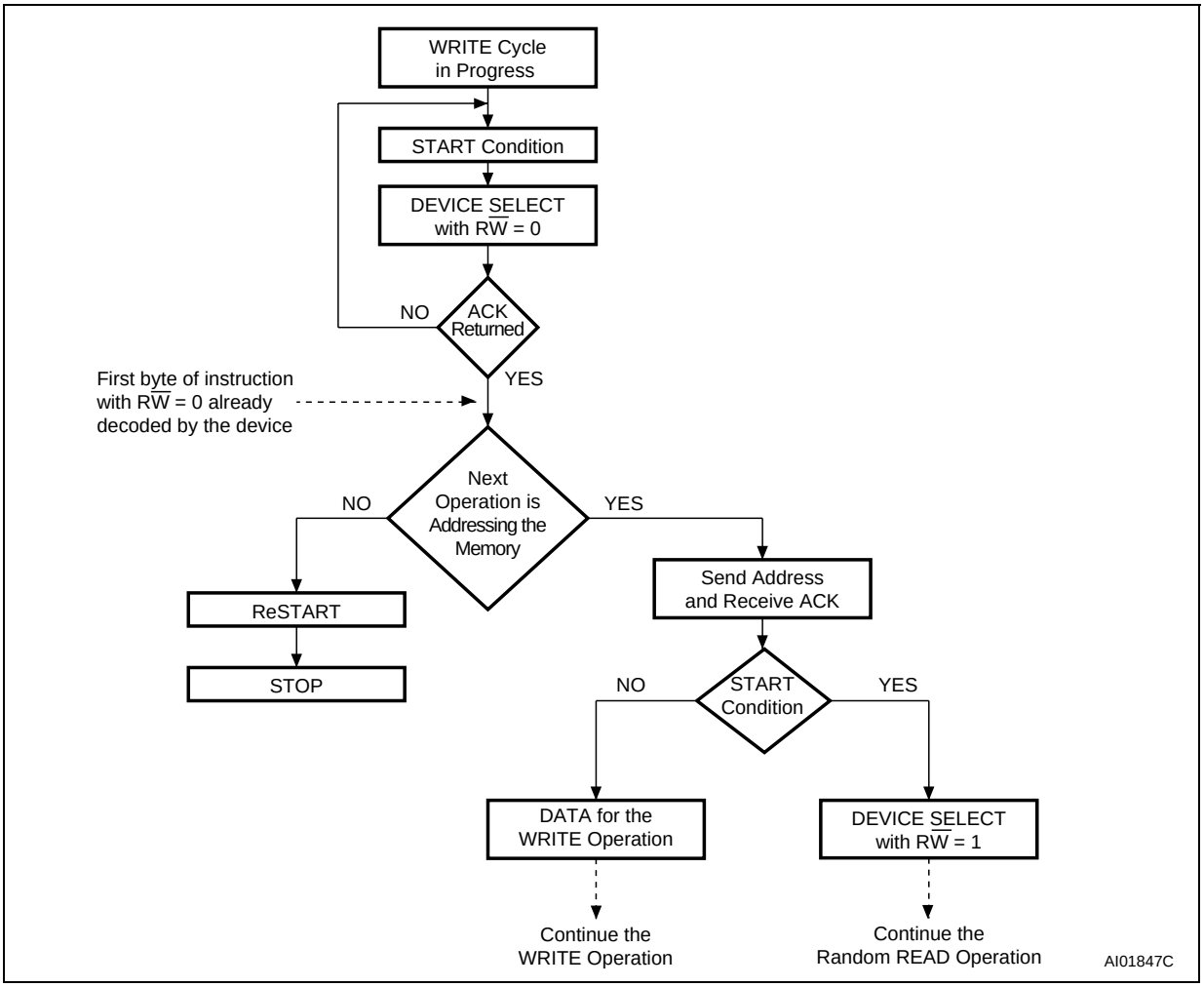
Byte Write

After the Device Select code and the address byte, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven High, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 6.

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory:

Figure 7. Write Cycle Polling Flowchart using ACK



that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is Low. If Write Control ($\overline{WC}$) is High, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 4 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Minimizing System Delays by Polling On ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Tables 8A and 8B, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

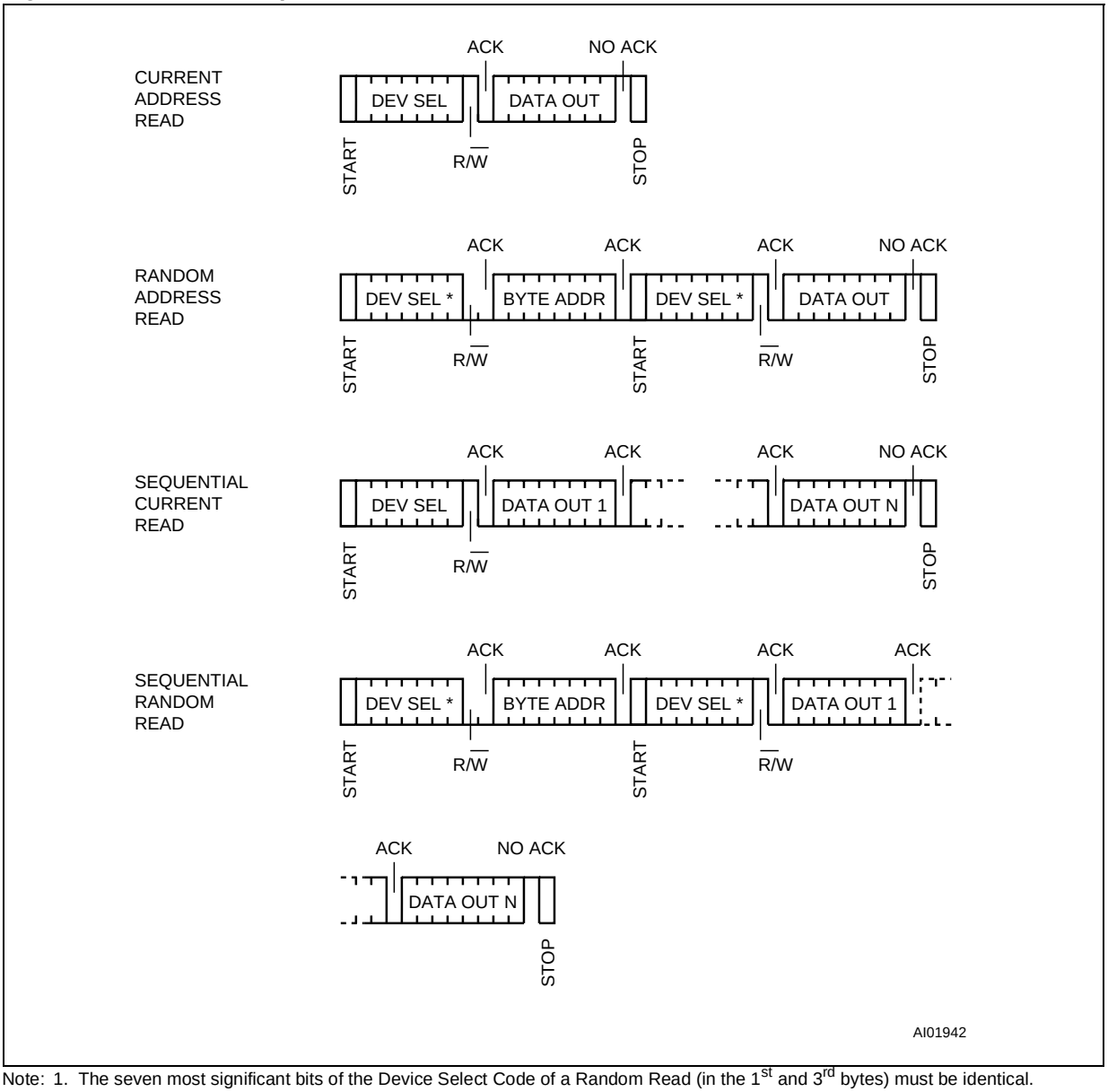
The sequence, as shown in Figure 7, is:

– Initial condition: a Write cycle is in progress.

– Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).

– Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the

Figure 8. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 3rd bytes) must be identical.

first byte of this instruction having been sent during Step 1).

Read Operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

Random Address Read

A dummy Write is performed to load the address into the address counter (as shown in Figure 8) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master

terminates the transfer with a Stop condition, as shown in Figure 8, *without* acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in Figure 8.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

Acknowledge in Read Mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and switches to its Stand-by mode.

Table 5. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 9. AC Testing Input Output Waveforms

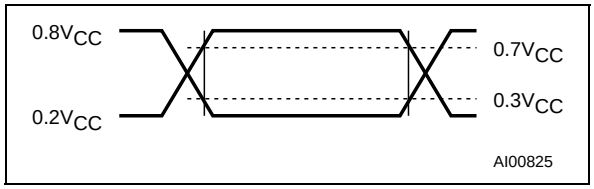


Table 6. Input Parameters[1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	V_{IN} < 0.5 V	5	70	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	V_{IN} > $0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

Note: 1. Sampled only, not 100% tested.

Table 7A. DC Characteristics
(T_A = –40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.5 to 5.5 V)
(T_A = –40 to 85 °C; V_{CC} = 1.8 to 5.5 V or 1.8 to 3.6 V)

Symbol	Parameter		Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)		$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current		$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current		V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		-W series:	V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
		-R series:	V_{CC} =1.8V, f_c=100kHz (rise/fall time < 30ns)		0.8[1]	mA
		-S series:	V_{CC} =1.8V, f_c=400kHz (rise/fall time < 30ns)		0.8[1]	mA
I_{CC1}	Supply Current (Stand-by)		$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5 V		1	µA
		-W series:	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.5 V		0.5	µA
		-R,S series:	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 1.8 V		0.3[1]	µA
V_{IL}	Input Low Voltage (E0, E1, E2, SCL, SDA)		4.5 V ≤ V_{CC} ≤ 5.5 V	– 0.3	0.3 V_{CC}	V
		-W series:	2.5 V ≤ V_{CC} ≤ 5.5 V	– 0.3	0.3 V_{CC}	V
		-R,S series:	2.5 V ≤ V_{CC}	– 0.3	0.3 V_{CC}[1]	V
			1.8 V ≤ V_{CC} < 2.5 V	– 0.3	0.25 V_{CC}[1]	V
V_{IH}	Input High Voltage (E0, E1, E2, SCL, SDA)			0.7V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)			– 0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)			0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage		I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V
		-W series:	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V
		-R,S series:	I_{OL} = 0.7 mA, V_{CC} = 1.8 V		0.2[1]	V

Note: 1. This is preliminary data.

Table 7B. DC Characteristics[1]
(T_A = –40 to 125 °C; V_{CC} = 4.5 to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	V_{IN} = V_{SS} or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		3	mA
I_{CC1}	Supply Current (Stand-by)	V_{IN} = V_{SS} or V_{CC} , V_{CC} = 5 V		5	µA
V_{IL}	Input Low Voltage (E0, E1, E2, SCL, SDA)		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (E0, E1, E2, SCL, SDA)		0.7V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage ($\overline{WC}$)		– 0.3	0.5	V
V_{IH}	Input High Voltage ($\overline{WC}$)		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V

Note: 1. This is preliminary data.

Table 8A. AC Characteristics

Symbol	Alt.	Parameter	M24C16, M24C08, M24C04, M24C02, M24C01				Unit
			V_{CC}=4.5 to 5.5 V T_A=–40 to 85°C		V_{CC}=4.5 to 5.5 V; T_A=–40 to 125°C[4]		
			Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300	ns
t_{DH1DH2} [2]	t_R	SDA Rise Time	20	300	20	300	ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	20	300	ns
t_{CHDX} [1]	$t_{SU:STA}$	Clock High to Input Transition	600		600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		1.3		µs
t_{CLQV} [3]	t_{AA}	Clock Low to Data Out Valid	200	900	200	900	ns
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400	kHz
t_W	t_{WR}	Write Time		5		10	ms

Note: 1. For a reSTART condition, or following a write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. This is preliminary data.

Table 8B. AC Characteristics

Symbol	Alt.	Parameter	M24C16, M24C08, M24C04, M24C02, M24C01						Unit
			-W series V_{CC}=2.5 to 5.5 V T_A=–40 to 85°C		-R series V_{CC}=1.8 to 5.5 V T_A=–40 to 85°C[4]		-S series V_{CC}=1.8 to 3.6 V T_A=–40 to 85°C[4]		
			Min	Max	Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		1000		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300		300	ns
t_{DH1DH2} [2]	t_R	SDA Rise Time	20	300	20	1000	20	300	ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	20	300	20	300	ns
t_{CHDX} [1]	$t_{SU:STA}$	Clock High to Input Transition	600		4700		600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		4000		600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		4000		600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		4.7		1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		250		100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		4000		600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		4.7		1.3		µs
t_{CLQV} [3]	t_{AA}	Clock Low to Data Out Valid	200	900	200	3500	200	900	ns
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	200		200		200		ns
f_C	f_{SCL}	Clock Frequency		400		100		400	kHz
t_W	t_{WR}	Write Time		10		10		10	ms

Note: 1. For a reSTART condition, or following a write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. This is preliminary data.

Figure 10. AC Waveforms

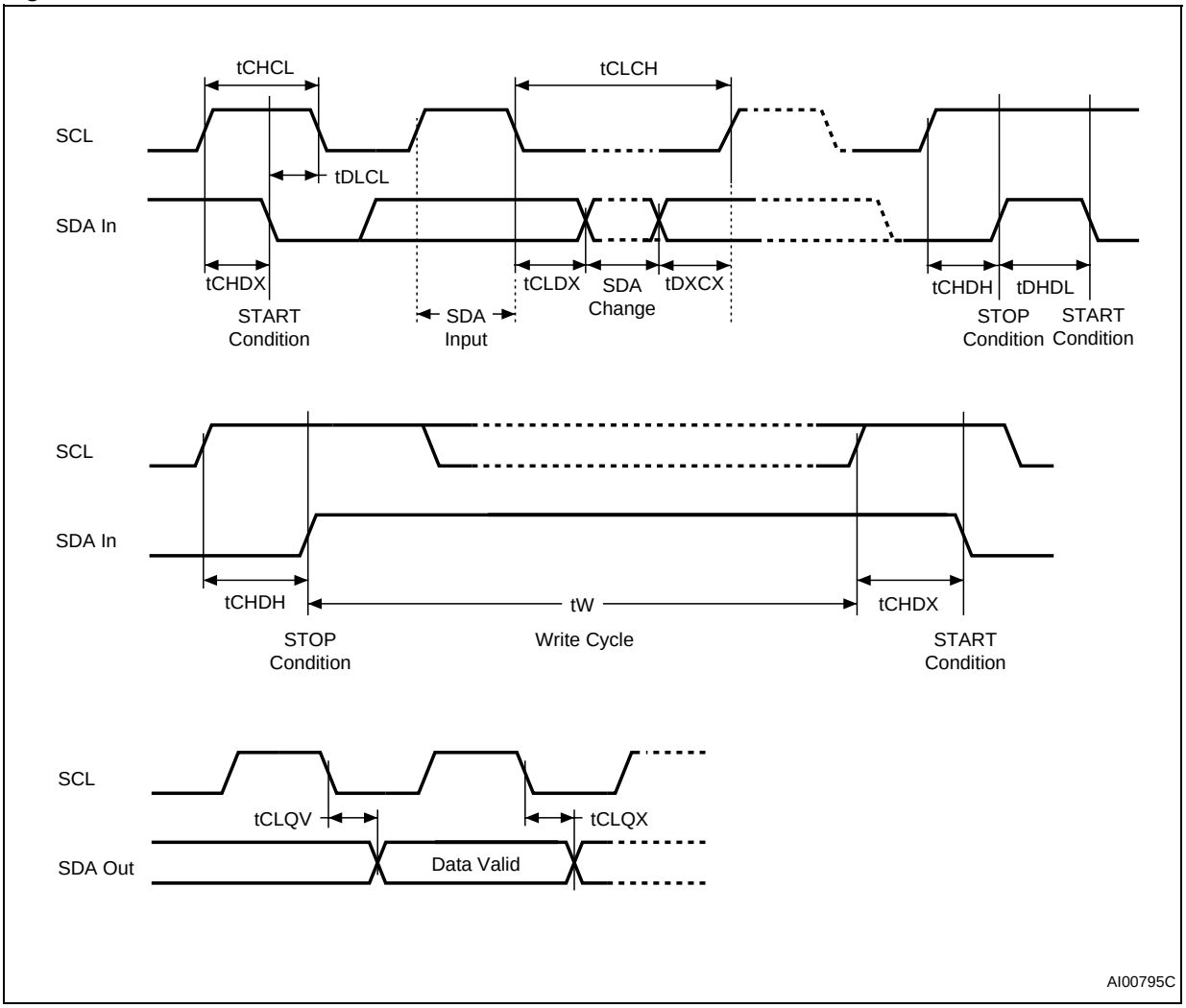


Table 9. Ordering Information Scheme

Example: M24C08 – W DW 6 T

Memory Capacity	
16	16 Kbit (2048 x 8)
08	8 Kbit (1024 x 8)
04	4 Kbit (512 x 8)
02	2 Kbit (256 x 8)
01	1 Kbit (128 x 8)

Operating Voltage	
blank	4.5 V to 5.5 V (400 kHz)
W	2.5 V to 5.5 V (400 kHz)
R	1.8 V to 5.5 V (100 kHz)
S	1.8 V to 3.6 V (400 kHz)

Option	
T	Tape and Reel Packing

Temperature Range	
6	–40 °C to 85 °C
3	–40 °C to 125 °C

Package	
BN	PDIP8 (0.25 mm frame)
MN	SO8 (150 mil width)
DW	TSSOP8 (169 mil width)
EA[1]	SBGA5 (75 mil width)

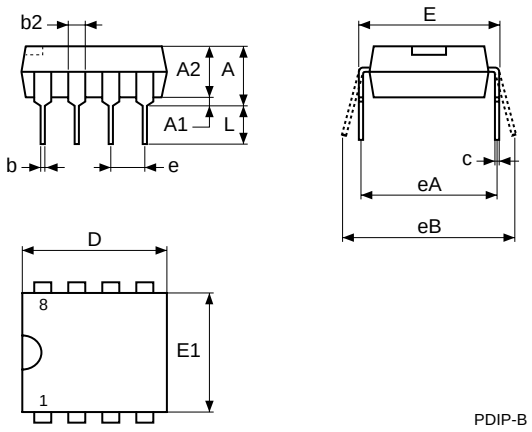
Note: 1. SBGA5 package available only for the M24C16, 1.8V to 3.6V (400 kHz), –40°C to 85°C (M24C16-SEA6)

ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all 1s (FFh).

The notation used for the device number is as shown in Table 9. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame

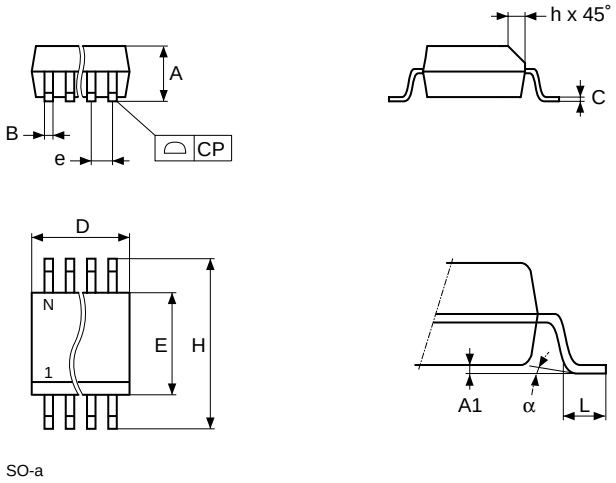


Note: 1. Drawing is not to scale.

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width



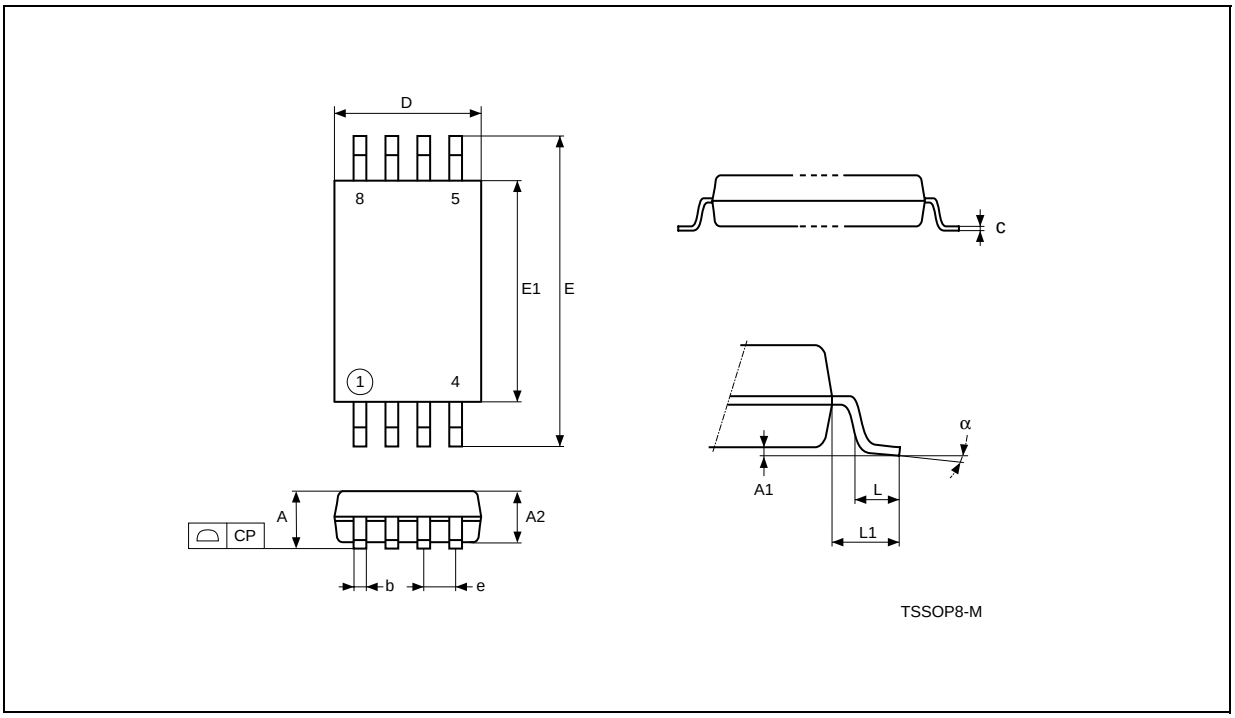
SO-a

Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

TSSOP8 – 8 lead Thin Shrink Small Outline

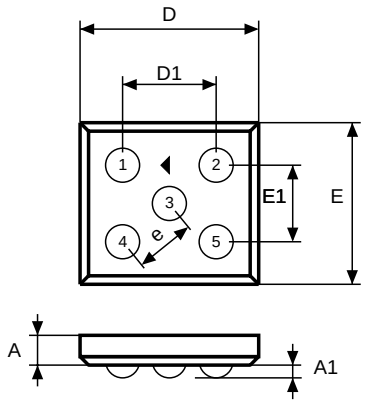


Note: 1. Drawing is not to scale.

TSSOP8 – 8 lead Thin Shrink Small Outline

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

SBGA5 – 5 ball Shell Ball Grid Array – Underside view (ball side)



Note: 1. Drawing is not to scale.

SBGA5 – 5 ball Shell Ball Grid Array

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.430	0.380	0.480	0.017	0.015	0.019
A1	0.180	0.150	0.210	0.007	0.006	0.008
D	1.900	1.870	1.930	0.075	0.074	0.076
D1	1.190	1.160	1.220	0.047	0.046	0.048
E	1.750	1.720	1.780	0.069	0.068	0.070
E1	1.070	1.040	1.100	0.042	0.041	0.043
e	0.800	0.770	0.830	0.031	0.030	0.033
ball diameter	0.350	0.320	0.380	0.014	0.013	0.015
N	5			5		

Table 10. Revision History

Date	Rev.	Description of Revision
10-Dec-1999	2.4	TSSOP8 Turned-Die package removed (p 2 and order information) Lead temperature added for TSSOP8 in table 2
18-Apr-2000	2.5	Labelling change to Fig-2D, correction of values for 'E' and main caption for Tab-13
05-May-2000	2.6	Extra labelling to Fig-2D
23-Nov-2000	3.0	SBGA package information removed to an annex document -R range changed to being the -S range, and the new -R range added
19-Feb-2001	3.1	SBGA package information put back in this document Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated References to PSDIP changed to PDIP and Package Mechanical data updated Wording brought in to line with standard glossary
20-Apr-2001	3.2	Revision of DC and AC characteristics for the -S series
08-Oct-2001	3.3	Ball numbers added to the SBGA connections and package mechanical illustrations
09-Nov-2001	3.4	Specification of Test Condition for Leakage Currents in the DC Characteristics table improved