LF411QML

LF411QML Low Offset, Low Drift JFET Input Operational Amplifier

![Texas Instruments logo](Texas Instruments)

Literature Number: SNOSAO6B

National Semiconductor

June 30, 2011

LF411QML

Low Offset, Low Drift JFET Input Operational Amplifier

General Description

This device is a low cost, high speed, JFET input operational amplifier with very low input offset voltage and guaranteed input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411QML is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

This amplifier may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Available with radiation guarantee
  — ELDRS FREE — 100 krad(Si)
- Internally trimmed offset voltage: — 0.5 mV(Typ)
- Input offset voltage drift: — 10 µV/°C
- Low input bias current: — 50 pA
- Low input noise current: — 0.01 pA/√Hz
- Wide gain bandwidth: — 3 MHz
- High slew rate: — 10V/µs
- Low supply current: — 1.8 mA
- High input impedance: — $10^{12}\Omega$
- Low total harmonic distortion: — <0.02%
  $A_V = 10$, $R_L = 10K\Omega$,
  $V_O = 20V_{P-P}$, BW = 20Hz - 20KHz
- Low 1/f noise corner: — 50 Hz
- Fast settling time to 0.01%: — 2 µs

Ordering Information

| NS Part Number	SMD Part Number	NS Package Number	Package Description
LF411MH/883		H08C	8LD T0–99 Can
LF411MWG/883		WG10A	10LD Ceramic SOIC
LF411MWG-MLS 50 krad(Si) (*Note 9*)		WG10A	10LD Ceramic SOIC
LF411MWGRLQMLV 100 krad(Si) (*Note 10*)	5962R1122201VZA ELDRS Free	WG10A	10LD Ceramic SOIC

Connection Diagrams

Metal Can Package
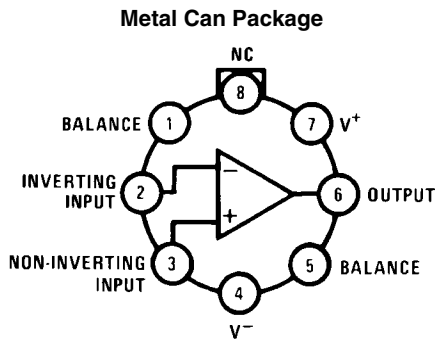
20149205

Note: Pin 4 connected to case.
Top View
See NS Package Number H08A

10LD Ceramic SOIC Package
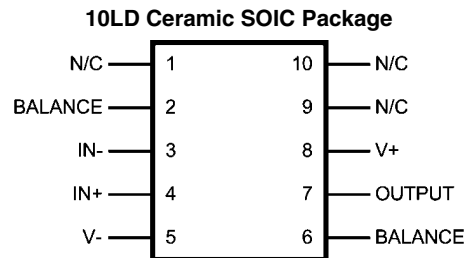
20149244

Top View
See NS Package Number WG10A

BI-FET II™ is a trademark of National Semiconductor Corporation.

Simplified Schematic
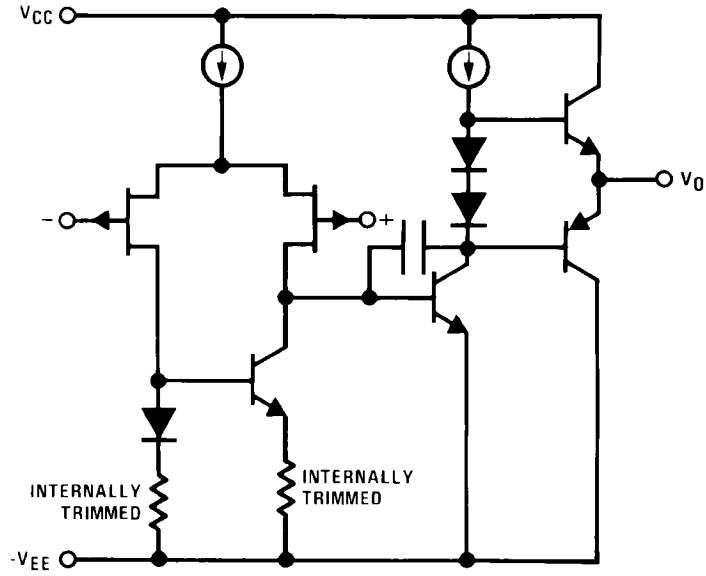
20149206

Detailed Schematic
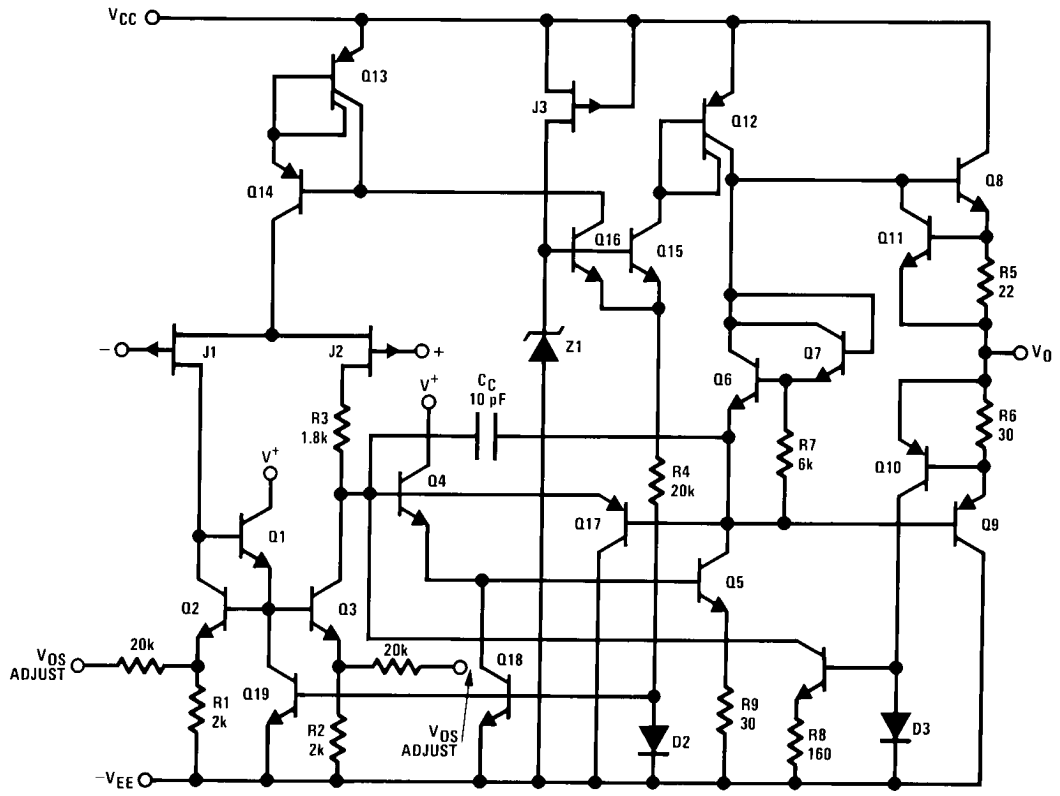
20149234

Absolute Maximum Ratings (*Note 1*)

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (*Note 4*)	±15V
Output Short Circuit Duration	Continuous
Power Dissipation (*Note 2*), (*Note 3*)	
H Package	670mW
WG Package	670mW
T_{Jmax}	
H Package	150°C
WG Package	150°C
Thermal Resistance	
θ_{JA}	
H Package Still Air	162°C/W
H Package 500LF/Min Air Flow	65°C/W
WG Package Still Air	170°C/W
WG Package 500LF/Min Air Flow	120°C/W
θ_{JC}	
H Package	20°C/W
WG Package	26°C/W
Operating Temperature Range	$-55°C \leq T_A \leq 125°C$
Storage Temperature Range	$-65°C \leq T_A \leq 150°C$
Lead Temperature (Soldering, 10 seconds)	260°C
Package Weight (Typical)	
H Package	TBD
WG Package	220mg
ESD Tolerance (*Note 5*)	750V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LF411 883 Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified.

DC: $V_{CC} = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$R_S = 10K\Omega$		-2.0	2.0	mV	1
				-3.7	3.7	mV	2
				-3.3	3.3	mV	3
I_{IO}	Input Offset Current			-0.1	0.1	nA	1
			(*Note 8*)	-25	25	nA	2
$\pm I_{IB}$	Input Bias Current			-0.2	0.2	nA	1
			(*Note 8*)	-50	50	nA	2
V_{CM}	Input Common Mode Voltage Range		(*Note 6*)	±9.0		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	$R_S \leq 10K\Omega$, $V_{CM} = \pm9V$		70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	$+V_{CC} = 6V$, $-V_{CC} = -15V$		70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	$+V_{CC} = 15V$, $-V_{CC} = -6V$		70		dB	1, 2, 3
I_S	Supply Current				3.4	mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	$+V_I = -11V$, $-V_I = 11V$, $R_S = 10K\Omega$		13	50	mA	1
				6.0	60	mA	2, 3
$+I_{OS}$	Output Short Circuit Current	$+V_I = 11V$, $-V_I = -11V$, $R_S = 10K\Omega$		-50	-13	mA	1
				-60	-6.0	mA	2, 3
$+V_{IO\ Adj}$	Input Offset Voltage Adjustment			8.0		mV	1
$-V_{IO\ Adj}$	Input Offset Voltage Adjustment				-8.0	mV	1
$+A_{VS}$	Large Signal Voltage Gain	$V_O = 0$ to $10V$, $R_L = 2K\Omega$	(*Note 7*)	25		V/mV	4
		$V_O = 0$ to $10V$, $R_L = 2K\Omega$	(*Note 7*)	15		V/mV	5, 6
$-A_{VS}$	Large Signal Voltage Gain	$V_O = 0$ to $-10V$, $R_L = 2K\Omega$	(*Note 7*)	25		V/mV	4
		$V_O = 0$ to $-10V$, $R_L = 2K\Omega$	(*Note 7*)	15		V/mV	5, 6
V_O+	Output Voltage Swing	$R_L = 10K\Omega$, $+V_I = 11V$, $-V_I = -11V$, $R_S = 10K\Omega$		12		V	4, 5, 6
V_O-	Output Voltage Swing	$R_L = 10K\Omega$, $+V_I = -11V$, $-V_I = 11V$, $R_S = 10K\Omega$			-12	V	4, 5, 6

AC Parameters

The following conditions apply, unless otherwise specified.

AC: $V_{CC} = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR+	Slew Rate	$V_O = -5V$ to $5V$		8.0		V/µS	7
SR-	Slew Rate	$V_O = 5V$ to $-5V$		8.0		V/µS	7
GBW	Gain Bandwidth Product			2.7		MHz	7

Space Level Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified.

DC: $V_{CC} = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$R_S = 10K\Omega$		-2.0	2.0	mV	1
				-3.7	3.7	mV	2
				-3.3	3.3	mV	3
I_{IO}	Input Offset Current			-0.1	0.1	nA	1
			(Note 8)	-25	25	nA	2
$\pm I_{IB}$	Input Bias Current			-0.2	0.2	nA	1
			(Note 8)	-50	50	nA	2
V_{CM}	Input Common Mode Voltage Range		(Note 6)	±9.0		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	$R_S \leq 10K\Omega$, $V_{CM} = \pm9V$		70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	$+V_{CC} = 6V$, $-V_{CC} = -15V$		70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	$+V_{CC} = 15V$, $-V_{CC} = -6V$		70		dB	1, 2, 3
I_S	Supply Current				3.4	mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	$+V_I = -11V$, $-V_I = 11V$,		13	50	mA	1
		$R_S = 10K\Omega$		6.0	60	mA	2, 3
$+I_{OS}$	Output Short Circuit Current	$+V_I = 11V$, $-V_I = -11V$,		-50	-13	mA	1
		$R_S = 10K\Omega$		-60	-6.0	mA	2, 3
$+V_{IO Adj}$	Input Offset Voltage Adjustment			8.0		mV	1
$-V_{IO Adj}$	Input Offset Voltage Adjustment				-8.0	mV	1
$+A_{VS}$	Large Signal Voltage Gain	$V_O = 0$ to $10V$, $R_L = 2K\Omega$	(Note 7)	25		V/mV	4
		$V_O = 0$ to $10V$, $R_L = 2K\Omega$	(Note 7)	15		V/mV	5, 6
$-A_{VS}$	Large Signal Voltage Gain	$V_O = 0$ to $-10V$, $R_L = 2K\Omega$	(Note 7)	25		V/mV	4
		$V_O = 0$ to $-10V$, $R_L = 2K\Omega$	(Note 7)	15		V/mV	5, 6
V_O+	Output Voltage Swing	$R_L = 10K\Omega$, $+V_I = 11V$, $-V_I = -11V$, $R_S = 10K\Omega$		12		V	4, 5, 6
V_O-	Output Voltage Swing	$R_L = 10K\Omega$, $+V_I = -11V$, $-V_I = 11V$, $R_S = 10K\Omega$			-12	V	4, 5, 6

AC Parameters

The following conditions apply, unless otherwise specified.

AC: $V_{CC} = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SR+	Slew Rate	$V_O = -5V$ to $5V$		8.0		V/µS	7
SR-	Slew Rate	$V_O = 5V$ to $-5V$		8.0		V/µS	7
GBW	Gain Bandwidth Product			2.7		MHz	7

Space Level Electrical Characteristics (Continued)

DC Parameters - Drift Values

The following conditions apply, unless otherwise specified.

DC: $V_{CC} = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$ "Delta calculations performed on Space Level devices at Group B Subgroup 5 ONLY"

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			−1	1	mV	1
$+I_{IB}$	Input Bias Current			−0.1	0.1	nA	1
$-I_{IB}$	Input Bias Current			−0.1	0.1	nA	1

LF411–MLS 50k Radiation Electrical Characteristics
DC Parameters - Post Radiation Limits *(Note 9)*

The following conditions apply, unless otherwise specified.

DC: $V_{CC} = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$ Post Radiation Limits +25°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{IO}	Input Offset Current			−0.25	0.25	nA	1
I_{IB+}	Input Bias Current			−1.0	1.0	nA	1
I_{IB-}	Input Bias Current			−1.0	1.0	nA	1

LF411MWGRLQMLV 100k Radiation Electrical Characteristics — ELDRS Free Only SMD# 5962R1122201
DC Parameters - Post Radiation Limits *(Note 10)*

The following conditions apply, unless otherwise specified.

DC: $V_{CC} = \pm15V$, $V_{CM} = 0V$, $R_S = 0\Omega$ Post Radiation Limits +25°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{IO}	Input Offset Current			−1.0	1.0	nA	1
I_{IB+}	Input Bias Current			−0.20	6.0	nA	1
I_{IB-}	Input Bias Current			−0.20	6.0	nA	1

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 4: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 5: Human body model, 100pF discharged through 1.5KΩ.

Note 6: Parameters guaranteed by CMRR test.

Note 7: Datalog in K = V/mV.

Note 8: $R_S = 10K\Omega$ @ +125°C.

Note 9: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, Method 1019

Note 10: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose rate environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per Test Method 1019, Condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS).

Typical Connection
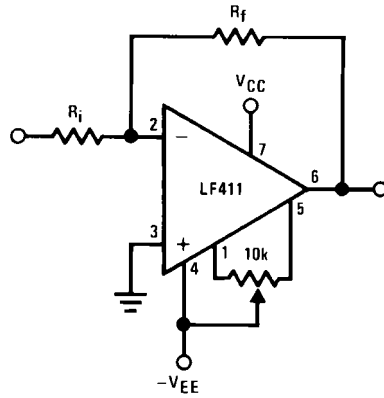
20149201

Typical Performance Characteristics

Input Bias Current

$V_S = \pm 15V$
$T_A = 25°C$

INPUT BIAS CURRENT (pA)

COMMON-MODE VOLTAGE (V)

20149211

Input Bias Current

$V_{CM} = 0V$
$V_S = \pm 15V$

INPUT BIAS CURRENT (pA)

TEMPERATURE (°C)

20149212

Supply Current

SUPPLY CURRENT (mA)

−55°C, 25°C

125°C

SUPPLY VOLTAGE (± V)

20149213

Positive Common-Mode Input Voltage Limit

$-55°C \leq T_A \leq 125°C$

POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT (V)

POSITIVE SUPPLY VOLTAGE (V)
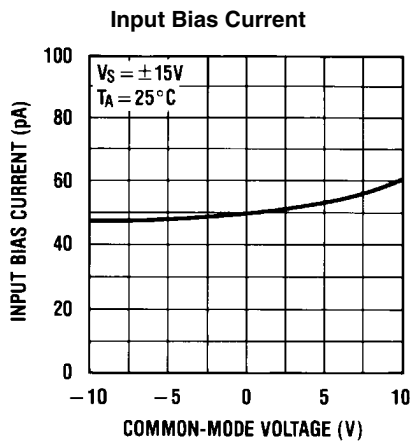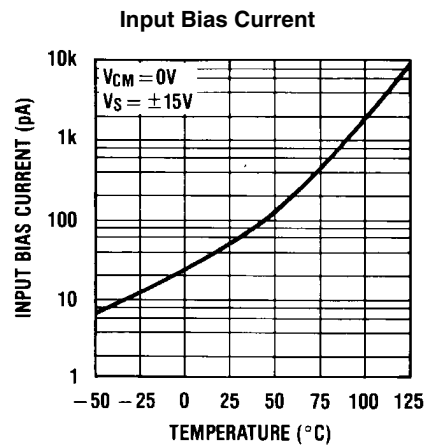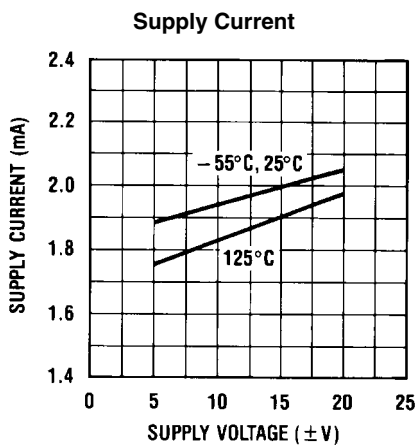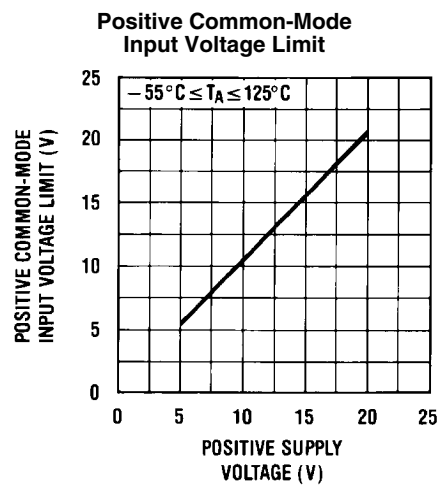
20149214

**Negative Common-Mode
Input Voltage Limit**

NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT (V)

$-55°C \leq T_A \leq 125°C$

NEGATIVE SUPPLY
VOLTAGE (V)
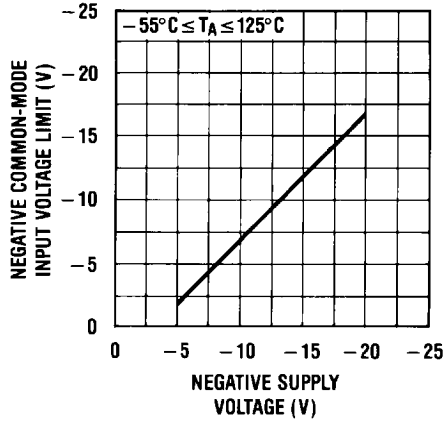
20149215

Positive Current Limit

POSITIVE OUTPUT VOLTAGE SWING (V)

$V_S = \pm 15V$

25°C

125°C

$-55°C$

OUTPUT SOURCE
CURRENT (mA)
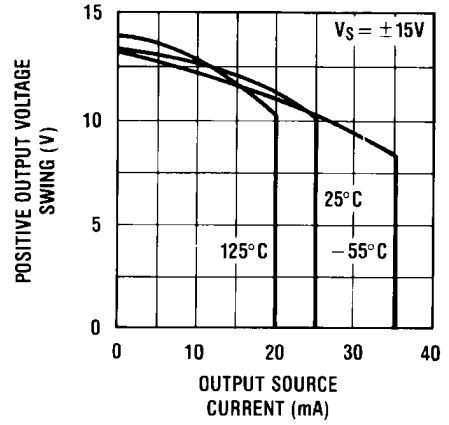
20149216

Negative Current Limit

NEGATIVE OUTPUT VOLTAGE SWING (V)

$V_S = \pm 15V$

$-55°C$

125°C   25°C

OUTPUT SINK CURRENT (mA)
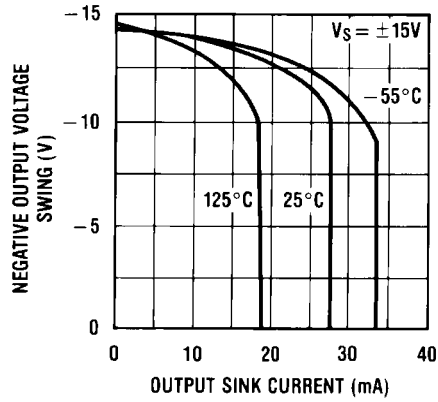
20149217

Output Voltage Swing

OUTPUT VOLTAGE SWING (Vp-p)

$R_L = 2k$
$T_A = 25°C$

SUPPLY VOLTAGE ($\pm V$)
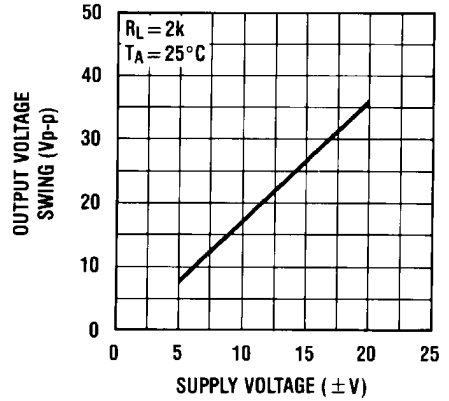
20149218

Output Voltage Swing

OUTPUT VOLTAGE SWING (Vp-p)

R_L—OUTPUT LOAD (kΩ)
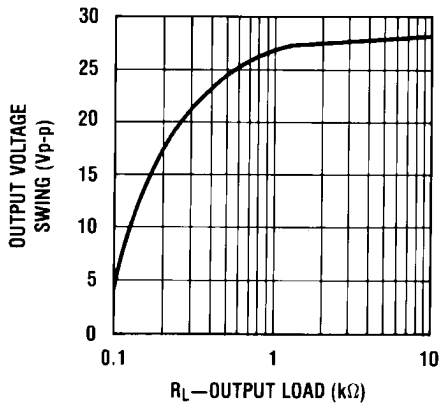
20149219

Gain Bandwidth
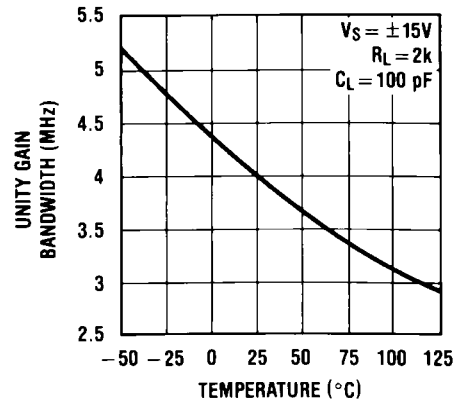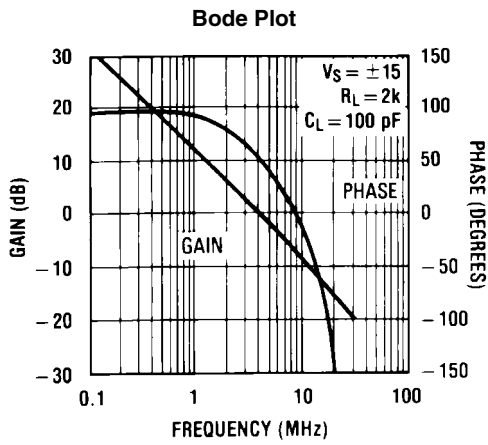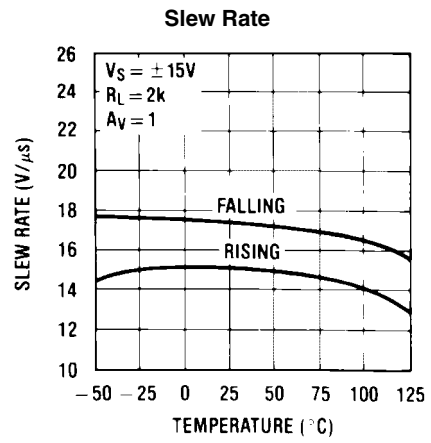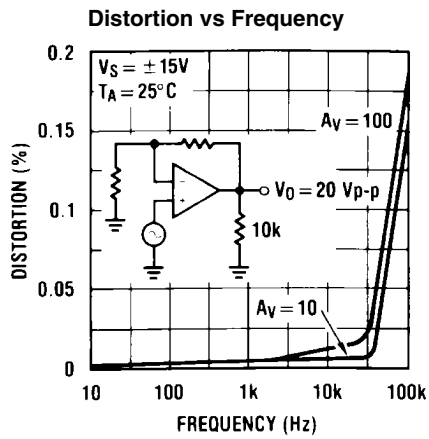
UNITY GAIN BANDWIDTH (MHz)

$V_S = \pm 15V$
$R_L = 2k$
$C_L = 100$ pF

TEMPERATURE (°C)

20149220

Bode Plot

20149221

Slew Rate

20149222

Distortion vs Frequency

20149223

Undistorted Output Voltage Swing

20149224

Open Loop Frequency Response

20149225

Common-Mode Rejection Ratio

20149226

**Power Supply
Rejection Ratio**

20149227

**Equivalent Input Noise
Voltage**

20149228

Open Loop Voltage Gain

20149229

Output Impedance

20149230

Inverter Settling Time
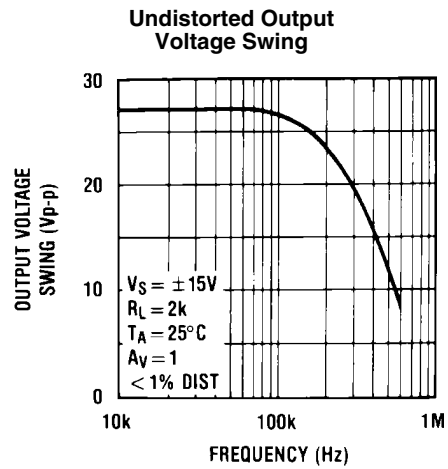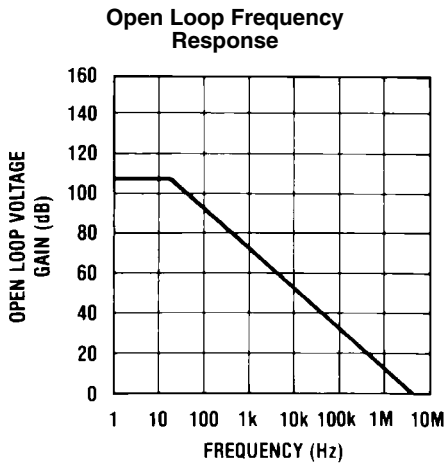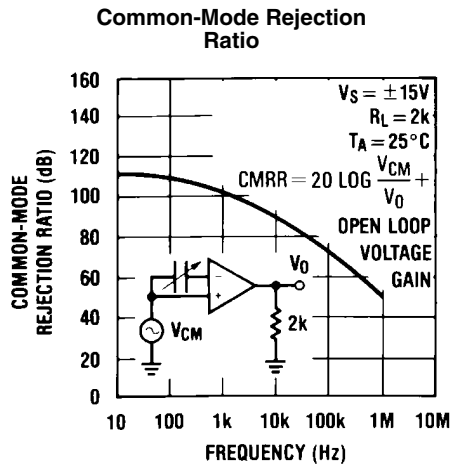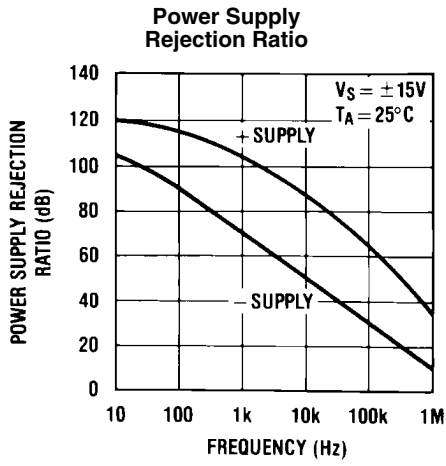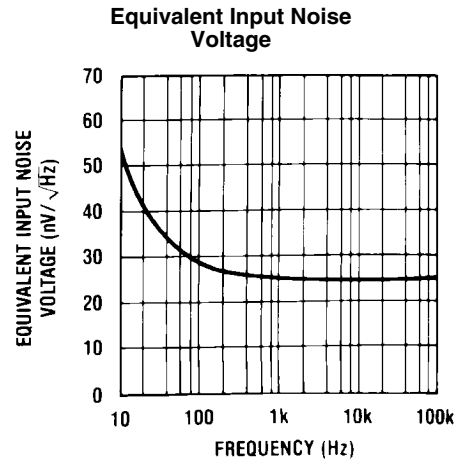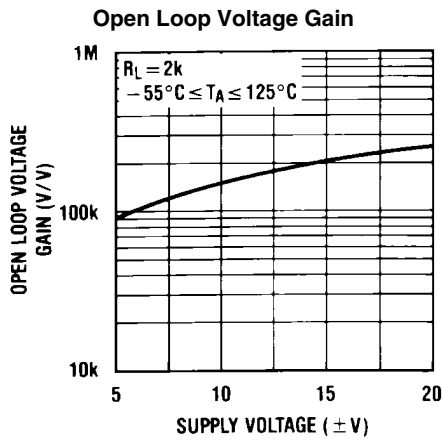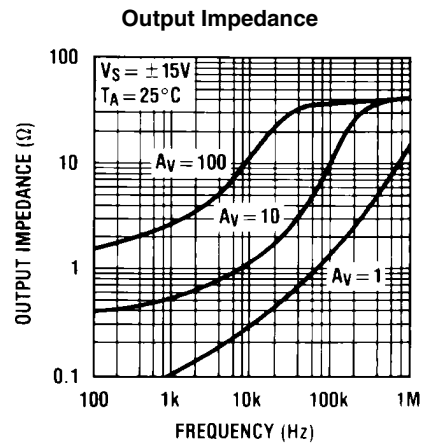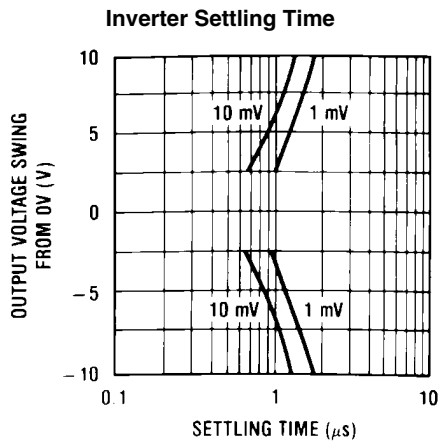
20149231

Pulse Response

R_L=2 kΩ, C_L10 pF

Small Signal Inverting
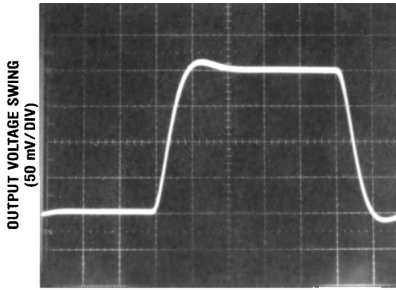
20149239

Small Signal Non-Inverting
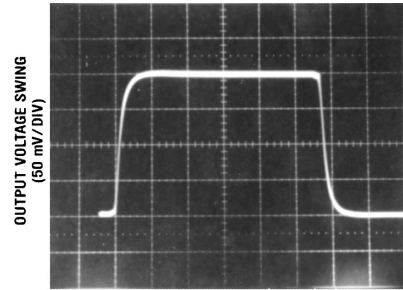
20149240

Large Signal Inverting
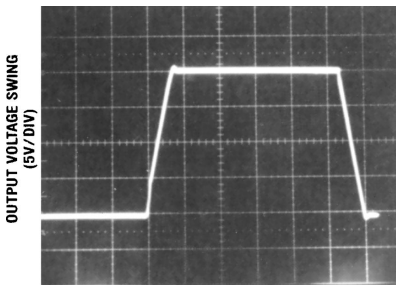
20149241

Large Signal Non-Inverting
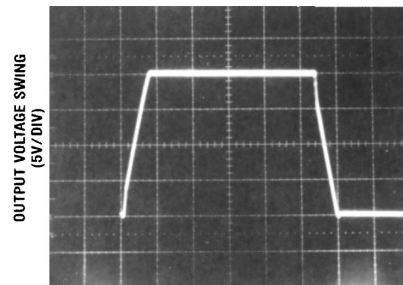
20149242

Current Limit (R_L=100Ω)
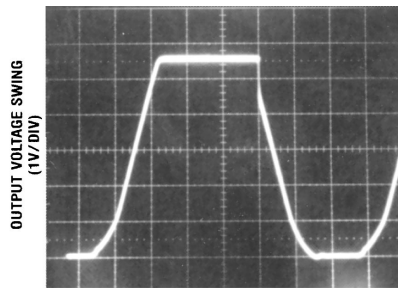
20149243

Application Hints

The LF411QML series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411QML is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411QML will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster
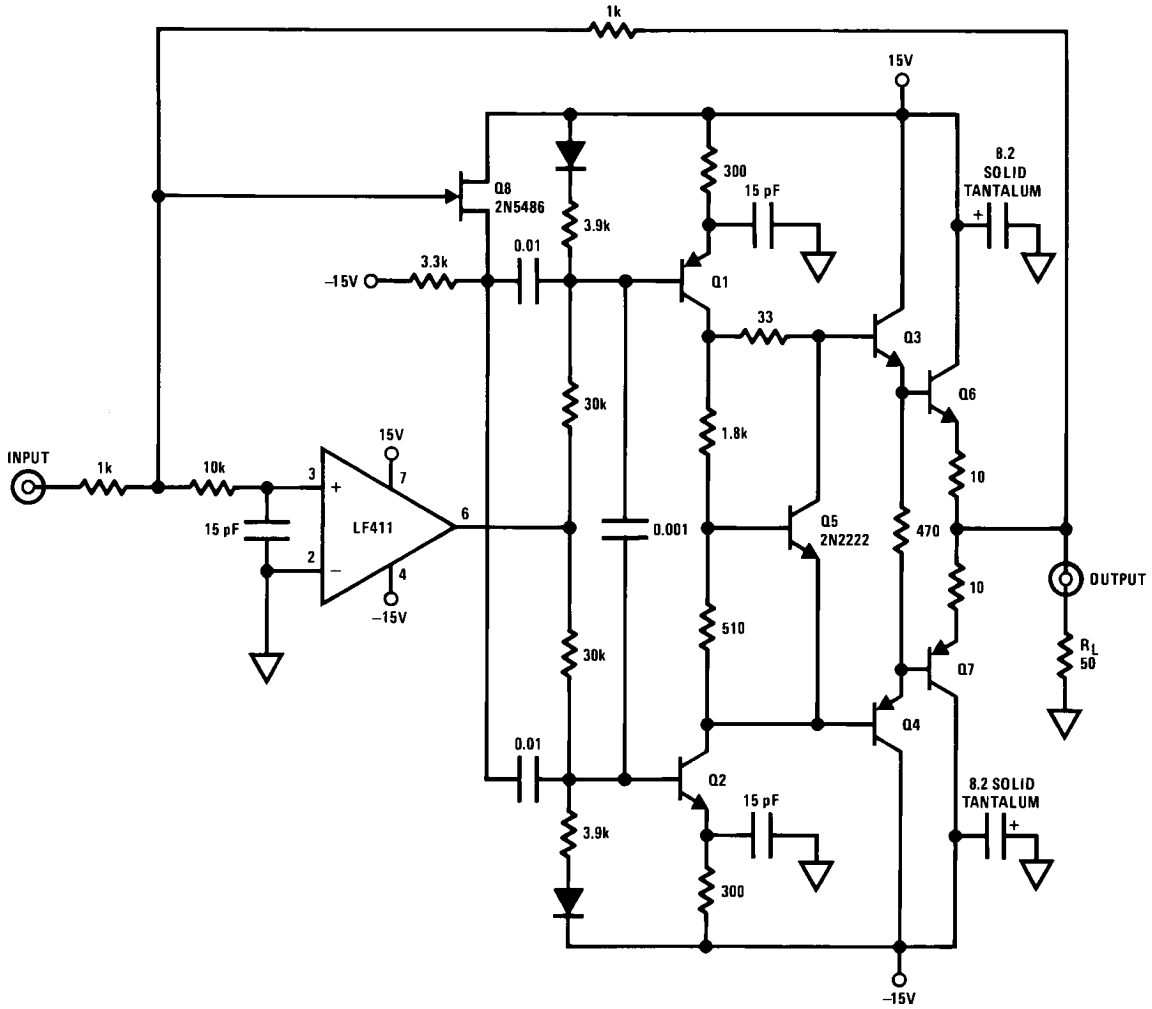
20149209

PNP=2N2905
NPN=2N2219 unless noted
TO-5 heat sinks for Q6-Q7

10-Bit Linear DAC with No V_{OS} Adjust
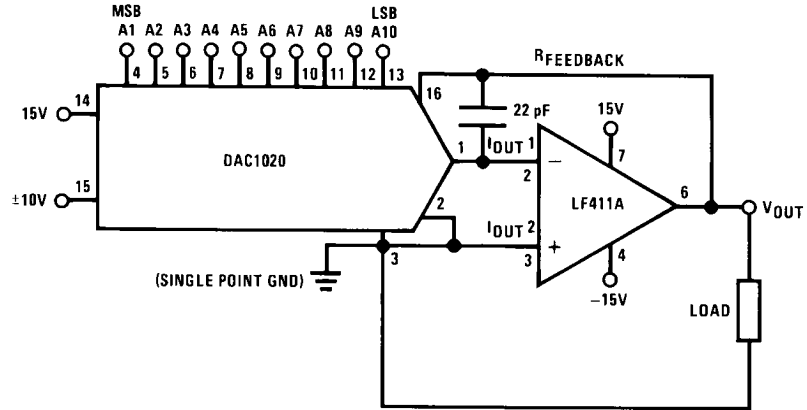
20149232

$$V_{OUT} = -V_{REF} \left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024} \right)$$

$$-10V \leq V_{REF} \leq 10V$$

$$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$$

where $A_N=1$ if the A_N digital input is high
$A_N=0$ if the A_N digital input is low

Single Supply Analog Switch with Buffered Output
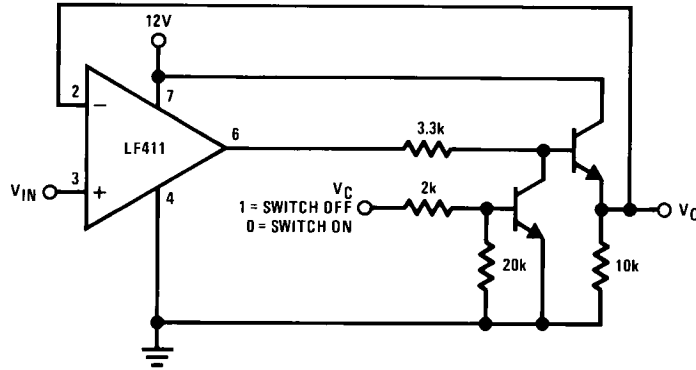
20149233

Revision History

Date Released	Revision	Section	Originator	Changes
10/11/05	A	New Release to corporate format	L. Lytle	1 MDS data sheet was converted into the corporate data sheet format. MDS MNLF411M-X Rev 2A2 will be archived.
05/07/07	B	Features, Ordering Information Table, LF411-MLS Electricals	L. McGee	Added reference to Radiation and Radiation Electricals for LF411-MLS device. Revision A will be archived.
06/30/11	C	Features, Ordering Information Table, LF411-MLS 50k Post Radiation Electricals, LF411MWGRLQMLV Post Radiation Electricals	L. McGee & K.Kruckmeyer	Added LF411MWGRLQMLV to Ordering Info and modified Radiation Electricals to "Radiation" devices. Added 50k and 100k Post Radiation DC parameter tables. Revision B will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted

Ø .130±.015
[3.3±0.38]

Ø .360±.010
[9.14±0.25]

Ø .200±.005
[5.08±0.12]

.037±.008
[0.94±0.2]

.0175±.0015 TYP
[0.445±0.038]

45° TYP

.031±.003
[0.79±0.07]

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE IN MILLIMETERS

REFERENCE PLANE

.500 MIN
[12.7]

.175±.010
[4.45±0.25]

SEATING PLANE

Ø .325±.010
[8.26±0.25]

.035 MAX
[0.89]

.015-.040
[0.38-1.02]

.025 MAX
[0.64]
UNCONTROLLED
LEAD DIA
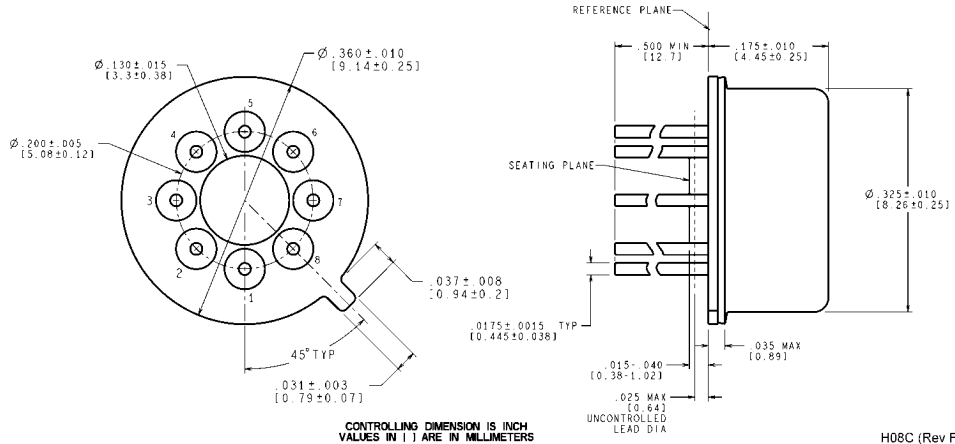
H08C (Rev F)

Metal Can Package (H)
NS Package Number H08C

.270 MAX
[6.86]

.005 MIN
[0.12]
TYP

.410±.010
[10.41±0.25]

.241 +.020 -.005
[6.12 +0.50 -0.12]

SUPPLIER'S
OPTION

LEAD 1 ID

.010±.002
[0.25±0.05]

8X .050±.002
[1.27±0.05]

10X .017±.002
[0.43±0.05]

(.370)
[9.4]

(10X .090)
[2.29]

(10X .027)
[0.69]

(8X .050)
[1.27]

RECOMMENDED LAND PATTERN

.070 +.010 -.020
[1.78 +0.25 -0.50]

.004 [0.1]

.045 MAX
[1.14]
TYP

SEATING PLANE

.008±.004
[0.2±0.1]

(R .015 TYP)
[0.38]

0° - 4° TYP

.040±.003
[1.02±0.07]
TYP

.006±.002 TYP
[0.15±0.05]
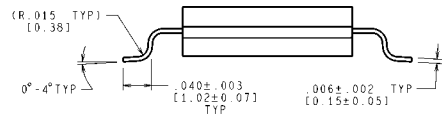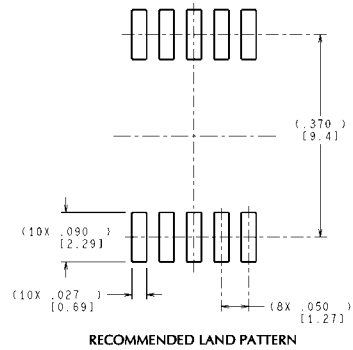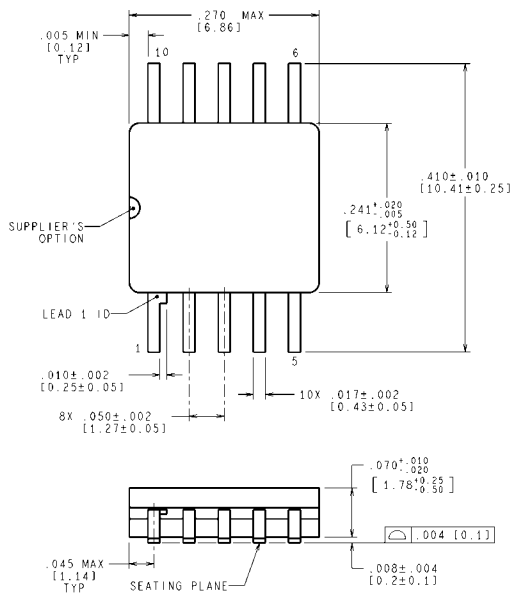
MIL-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

WG10A (Rev F)

10 Lead Ceramic SOIC (WG))
NS Package Number WG10A

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:
www.national.com

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH® Tools	www.national.com/webench
Audio	www.national.com/audio	App Notes	www.national.com/appnotes
Clock and Timing	www.national.com/timing	Reference Designs	www.national.com/refdesigns
Data Converters	www.national.com/adc	Samples	www.national.com/samples
Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
PLL/VCO	www.national.com/wireless	PowerWise® Design University	www.national.com/training

IMPORTANT NOTICE