# Low Charge Injection, 8-Channel High Voltage Analog Switch with Bleed Resistors 

## Features

- HVCMOS technology for high performance
- Integrated bleed resistors on the outputs
- 3.3 V or 5.0 V CMOS input logic level
- 20 MHz data shift clock frequency
- Very low quiescent power dissipation - 10رA
- Low parasitic capacitance
- DC to 50 MHz small signal frequency response
- -60dB typical off-isolation at 5.0 MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches
- Flexible operating supply voltages


## Applications

- Medical ultrasound imaging
- NDT metal flaw detection
- Piezoelectric transducer drivers
- Inkjet printer heads
- Optical MEMS modules


## General Description

The Supertex HV2303 is a low charge injection 8-channel high voltage analog switch integrated circuit (IC) with bleed resistors. The device can be used in applications requiring high voltage switching controlled by low voltage signals, such as medical ultrasound imaging, piezoelectric transducer driver, and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Data is input into an 8 -bit shift register that can then be retained in an 8 -bit latch. To reduce any possible clock feedthrough noise, the latch enable bar should be left high until all bits are clocked in. Data is clocked in during the rising edge of the clock.

Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., $\mathrm{V}_{\mathrm{PP}} / \mathrm{V}_{\mathrm{NN}}$ : $+40 \mathrm{~V} /-160 \mathrm{~V}$, $+100 \mathrm{~V} /-100 \mathrm{~V}$, and $+160 \mathrm{~V} /-40 \mathrm{~V}$.


## Ordering Information

| Device | Package Options |  |
| :---: | :---: | :---: |
|  | 48-Lead LQFP <br> $7.00 \times 7.00 \mathrm{~mm}$ body 1.60 mm height ( max ) 0.50 mm pitch | 28-Lead PLCC <br> .453x.453in body .180in height (max) .050in pitch |
| HV2303 | HV2303FG-G | HV2303PJ-G |

-G indicates package is RoHS compliant ('Green’)


## Absolute Maximum Ratings

| Parameter | Value |
| :--- | ---: |
| $\mathrm{V}_{\mathrm{DD}}$ logic supply | -0.5 V to +6.5 V |
| $\mathrm{~V}_{\mathrm{PP}}-\mathrm{V}_{\mathrm{NN}}$ differential supply | +210 V |
| $\mathrm{~V}_{\mathrm{PP}}$ positive supply | -0.5 V to $\mathrm{V}_{\mathrm{NN}}+200 \mathrm{~V}$ |
| $\mathrm{~V}_{\mathrm{NN}}$ negative supply | +0.5 V to -180 V |
| Logic input voltage | -0.5 V to $\mathrm{V}_{\mathrm{DD}}+0.3 \mathrm{~V}$ |
| Analog signal range | $\mathrm{V}_{\mathrm{NN}}$ to $\mathrm{V}_{\mathrm{PP}}$ |
| Peak analog signal current/channel | 1.0 A |
| Storage temperature | $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ |
| Thermal resistance $\left(\theta_{j a}\right):$    <br> $48-L e a d ~ L Q F P ~$    <br> $\mathrm{FG})$    | $61^{\circ} \mathrm{C} / \mathrm{W}$ |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Operating Conditions

| Sym | Para | Value |
| :---: | :---: | :---: |
| $V_{\text {D }}$ | Logic power supply voltage | 3.0 V to 5.5 V |
| $V_{\text {PP }}$ | Positive high voltage supply | 40 V to $\mathrm{V}_{\text {NN }}+2$ |
| $\mathrm{V}_{\text {NN }}$ | Negative high voltage supply | -40 V to -160V |
| $\mathrm{V}_{\text {IH }}$ | High level input voltage | $0.9 \mathrm{~V}_{\text {DD }}$ to |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage | 0 V to 0.1 V |
| $\mathrm{V}_{\text {SIG }}$ | Analog signal voltage peak-to-peak | $\mathrm{V}_{\mathrm{NN}}+10 \mathrm{~V}$ to $\mathrm{V}_{\text {PP }}-10 \mathrm{~V}$ |
| T ${ }_{\text {A }}$ | Operating free air temperature | $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$ |
| Notes: <br> 1. $P$ | Power up/down sequence is arbitrary except GND must be powered-up first and powered down last. <br> $V_{S I G}$ must be $V_{N N} \leq V_{S I G} \leq V_{P P}$ or floating during power up/down transition. <br> Rise and fall times of power supplies $V_{D 0}, V_{P P}$ and $V_{N N}$ should not be less than 1.0msec. |  |
| $\begin{array}{ll} 2 . & V \\ 3 . & R \\ & 1 . \\ \hline \end{array}$ |  |  |

## Pin Configurations



48-Lead LQFP (FG)


28-Lead PLCC (PJ)

## Product Marking


$Y Y=$ Year Sealed WW = Week Sealed L = Lot Number C = Country of Origin* A = Assembler ID* cccccccc AAA
$\qquad$ = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or (1D
48-Lead LQFP (FG)


Bottom Marking


C = Country of Origin*
$\qquad$ = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or 41
28-Lead PLCC (PJ)

DC Electrical Characteristics
(Over operating conditions unless otherwise specified )

| Sym | Parameter | $0^{\circ} \mathrm{C}$ |  | $+25^{\circ} \mathrm{C}$ |  |  | $+70^{\circ} \mathrm{C}$ |  | Units | Conditions |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Typ | Max | Min | Max |  |  |  |
| $\mathrm{R}_{\text {ONS }}$ | Small signal switch on-resistance | - | - | - | 50 | - | - | - | $\Omega$ | $\mathrm{I}_{\text {SIG }}=5.0 \mathrm{~mA}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+40 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NN}}=-160 \mathrm{~V} \end{aligned}$ |
|  |  | - | - | - | 42 | - | - | - |  | $\mathrm{I}_{\text {SIG }}=200 \mathrm{~mA}$ |  |
|  |  | - | - | - | 40 | - | - | - |  | $\mathrm{I}_{\text {SIG }}=5.0 \mathrm{~mA}$ | $\begin{aligned} & V_{\text {PP }}=+100 \mathrm{~V} \\ & V_{\mathrm{NN}}=-100 \mathrm{~V} \end{aligned}$ |
|  |  | - | - | - | 32 | - | - | - |  | $\mathrm{I}_{\text {SIG }}=200 \mathrm{~mA}$ |  |
|  |  | - | - | - | 38 | - | - | - |  | $\mathrm{I}_{\text {SIG }}=5.0 \mathrm{~mA}$ | $\begin{aligned} & V_{P \mathrm{P}}=+160 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NN}}=-40 \mathrm{~V} \end{aligned}$ |
|  |  | - | - | - | 29 | - | - | - |  | $\mathrm{I}_{\text {SIG }}=200 \mathrm{~mA}$ |  |
| $\Delta R_{\text {ONS }}$ | Small signal switch on-resistance matching | - | - | - | 5.0 | - | - | - | \% | $\begin{aligned} & \mathrm{I}_{\mathrm{SIG}}=5.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{PP}}=+100 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{NN}}=-100 \mathrm{~V} \end{aligned}$ |  |
| $\mathrm{R}_{\text {ONL }}$ | Large signal switch on-resistance | - | - | - | 30 | - | - | - | $\Omega$ | $\mathrm{V}_{\text {SIG }}=\mathrm{V}_{\text {PP }}-10 \mathrm{~V}, \mathrm{I}_{\text {SIG }}=0.5 \mathrm{~A}$ |  |
| $\mathrm{R}_{\text {INT }}$ | Value of output bleed resistance | - | - | 20 | 35 | 50 | - | - | K $\Omega$ | Output switch to RGND $\mathrm{I}_{\text {RINT }}=0.5 \mathrm{~mA}$ |  |
| $\mathrm{I}_{\text {sol }}$ | Switch off leakage per switch | - | 5.0 | - | 1.0 | 10 | - | 15 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {SIG }}=\mathrm{V}_{\text {PP }}-10 \mathrm{~V}, \mathrm{~V}_{\text {NN }}+10 \mathrm{~V}$ |  |
|  | DC offset switch off | - | 300 | - | 100 | 300 | - | 300 | mV | No load |  |
| $\mathrm{V}_{\text {os }}$ | DC offset switch on | - | 500 | - | 100 | 500 | - | 500 | mV |  |  |  |
| $\mathrm{I}_{\text {PPQ }}$ | Quiescent $\mathrm{V}_{\text {PP }}$ supply current | - | - | - | 10 | 50 | - | - | $\mu \mathrm{A}$ | All switches off |  |
| $\mathrm{I}_{\text {NNQ }}$ | Quiescent $\mathrm{V}_{\text {NN }}$ supply current | - | - | - | -10 | -50 | - | - | $\mu \mathrm{A}$ | All switches off |  |
| $\mathrm{I}_{\text {PPQ }}$ | Quiescent $\mathrm{V}_{\text {PP }}$ supply current | - | - | - | 10 | 50 | - | - | $\mu \mathrm{A}$ | All switches on, $\mathrm{I}_{\mathrm{sw}}=5.0 \mathrm{~mA}$ |  |
| $\mathrm{I}_{\text {NNQ }}$ | Quiescent $\mathrm{V}_{\text {NN }}$ supply current | - | - | - | -10 | -50 | - | - | $\mu \mathrm{A}$ | All switches on, $\mathrm{I}_{\text {sw }}=5.0 \mathrm{~mA}$ |  |
| $\mathrm{I}_{\text {sw }}$ | Switch output peak current | - | - | - | - | 1.0 | - | - | A | $\begin{aligned} & \mathrm{V}_{\text {sIG }} \text { duty cycle }<0.1 \%, \\ & 1.0 \mu \mathrm{~s} \end{aligned}$ |  |
| $\mathrm{f}_{\text {sw }}$ | Output switching frequency | - | - | - | - | 50 | - | - | kHz | Duty cycle $=50 \%$ |  |
|  |  | - | 4.0 | - | - | 5.0 | - | 5.5 | mA | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+40 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NN}}=-160 \mathrm{~V} \\ & \hline \end{aligned}$ | All output switches are turning on and off at 50 kHz with no load |
| $\mathrm{I}_{\text {PP }}$ | Average $\mathrm{V}_{\text {Pp }}$ supply current |  | 3.5 | - | - | 3.5 | - | 3.5 |  | $\begin{aligned} & V_{P P}=+100 \mathrm{~V} \\ & V_{\mathrm{NN}}=-100 \mathrm{~V} \end{aligned}$ |  |
|  |  | - | 3.5 | - | - | 3.5 | - | 4.0 |  | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+160 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NN}}=-40 \mathrm{~V} \end{aligned}$ |  |
| $\mathrm{I}_{\text {NN }}$ | Average $\mathrm{V}_{\mathrm{NN}}$ supply current | - | 4.5 | - | - | 5.0 | - | 5.5 | mA | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+40 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NN}}=-160 \mathrm{~V} \end{aligned}$ |  |
|  |  | - | 3.5 | - | - | 3.5 | - | 3.5 |  | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+100 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NN}}=-100 \mathrm{~V} \end{aligned}$ |  |
|  |  | - | 3.5 | - | - | 3.5 | - | 4.0 |  | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+160 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{NN}}=-40 \mathrm{~V} \end{aligned}$ |  |
| $\mathrm{I}_{\mathrm{D}}$ | Average $\mathrm{V}_{\mathrm{DD}}$ supply current | - | 4.0 | - | - | 4.0 | - | 4.0 | mA | $\mathrm{f}_{\text {CLK }}=5.0 \mathrm{MHz}, \mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$ |  |
| $\mathrm{I}_{\text {DDQ }}$ | Quiescent $\mathrm{V}_{\text {D }}$ supply current | - | 10 | - | - | 10 | - | 10 | $\mu \mathrm{A}$ | All logic inputs are static |  |
| $\mathrm{I}_{\text {Sor }}$ | Data out source current | 0.45 | - | 0.45 | 0.70 | - | 0.40 | - | mA | $\mathrm{V}_{\text {OUT }}=\mathrm{V}_{\text {DD }}-0.7 \mathrm{~V}$ |  |
| $\mathrm{I}_{\text {SINK }}$ | Data out sink current | 0.45 | - | 0.45 | 0.70 | - | 0.40 | - | mA | $\mathrm{V}_{\text {OUT }}=0.7 \mathrm{~V}$ |  |
| $\mathrm{C}_{\text {IN }}$ | Logic input capacitance | - | 10 | - | - | 10 | - | 10 | pF | --- |  |

## AC Electrical Characteristics

(Over recommended operating conditions: $V_{D D}=5.0 \mathrm{~V}, t_{R}=t_{F} \leq 5 n s, 50 \%$ duty cycle, $C_{\text {LOAD }}=20 \mathrm{pF}$ unless otherwise specified)

| Sym | Parameter | $0^{\circ} \mathrm{C}$ |  | $+25^{\circ} \mathrm{C}$ |  |  | $+70^{\circ} \mathrm{C}$ |  | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Typ | Max | Min | Max |  |  |
| $\mathrm{t}_{\text {SD }}$ | Set up time before LEE rises | 25 | - | 25 | - | - | 25 | - | ns | --- |
| $\mathrm{t}_{\text {wLe }}$ | Time width of $\overline{\mathrm{LE}}$ | 56 | - | - | 56 | - | 56 | - | ns | $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$ |
|  |  | 12 | - | - | 12 | - | 12 | - |  | $\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$ |
| $\mathrm{t}_{\mathrm{D}}$ | Clock delay time to data out | 50 | 100 | 50 | 78 | 100 | 50 | 100 | ns | $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$ |
|  |  | 15 | 40 | 15 | 30 | 40 | 15 | 40 |  | $\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$ |
| $\mathrm{t}_{\text {wCL }}$ | Time width of CLR | 55 | - | 55 | - | - | 55 | - | ns | --- |
| $\mathrm{t}_{\text {su }}$ | Set up time data to clock | 21 | - | 21 | - | - | 21 | - | ns | $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$ |
|  |  | 7.0 | - | 7.0 | - | - | 7.0 | - |  | $\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$ |
| $\mathrm{t}_{\mathrm{H}}$ | Hold time data from clock | 2.0 | - | 2.0 | - | - | 2.0 | - | ns | $V_{D D}=3.0$ or 5.0 V |
| $\mathrm{f}_{\text {cLK }}$ | Clock frequency | - | 8.0 | - | - | 8.0 | - | 8.0 | MHz | $\mathrm{V}_{\mathrm{DD}}=3.0 \mathrm{~V}$ |
|  |  | - | 20 | - | - | 20 | - | 20 |  | $\mathrm{V}_{\mathrm{DD}}=5.0 \mathrm{~V}$ |
| $\mathrm{t}_{\mathrm{R}}, \mathrm{t}_{\mathrm{F}}$ | Clock rise and fall times | - | 50 |  | - | 50 | - | 50 | ns | --- |
| $\mathrm{t}_{\mathrm{ON}}$ | Turn on time | - | 5.0 | - | - | 5.0 | - | 5.0 | $\mu \mathrm{s}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{SIG}}=\mathrm{V}_{\mathrm{PP}}-10 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{LIADD}}=10 \mathrm{k} \Omega \\ & \hline \end{aligned}$ |
| $\mathrm{t}_{\text {off }}$ | Turn off time | - | 5.0 | - | - | 5.0 | - | 5.0 | $\mu \mathrm{s}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{SIG}}=\mathrm{V}_{\mathrm{PP}}-10 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{LOAD}}=10 \mathrm{k} \Omega \end{aligned}$ |
| dv/dt | Maximum $\mathrm{V}_{\text {SIG }}$ slew rate | - | 20 | - | - | 20 | - | 20 | V/ns | $\mathrm{V}_{\mathrm{PP}}=+40 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-160 \mathrm{~V}$ |
|  |  | - | 20 | - | - | 20 | - | 20 |  | $\mathrm{V}_{\mathrm{PP}}=+100 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-100 \mathrm{~V}$ |
|  |  | - | 20 | - | - | 20 | - | 20 |  | $\mathrm{V}_{\mathrm{PP}}=+160 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-40 \mathrm{~V}$ |
| K | Off isolation | -30 | - | -30 | -33 | - | -30 | - | dB | $\begin{aligned} & \mathrm{f}=5.0 \mathrm{MHz}, \\ & 1.0 \mathrm{k} \Omega / 15 \mathrm{pF} \text { load } \end{aligned}$ |
|  |  | -58 | - | -58 | - | - | -58 | - |  | $\mathrm{f}=5.0 \mathrm{MHz}, 50 \Omega$ load |
| $\mathrm{K}_{\mathrm{CR}}$ | Switch crosstalk | -60 | - | -60 | -70 | - | -60 | - | dB | $\mathrm{f}=5.0 \mathrm{MHz}, 50 \Omega$ load |
| $1{ }_{10}$ | Output switch isolation diode current | - | 300 | - | - | 300 | - | 300 | mA | 300 ns pulse width, 2.0\% duty cycle |
| $\mathrm{C}_{\text {SG(OFF) }}$ | Off capacitance SW to GND | - | - | - | 6.5 | - | - | - | pF | $0 \mathrm{~V}, \mathrm{f}=1.0 \mathrm{MHz}$ |
| $\mathrm{C}_{\text {SGION) }}$ | On capacitance SW to GND | - | - | - | 21.7 | - | - | - | pF | $0 \mathrm{~V}, \mathrm{f}=1.0 \mathrm{MHz}$ |
| $+\mathrm{V}_{\text {SPK }}$ | Output voltage spike | - | - | - | 18 | - | - | - | mV | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+40 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-160 \mathrm{~V}, \\ & \mathrm{R}_{\mathrm{LOAD}}=50 \Omega \end{aligned}$ |
| $-V_{\text {sPK }}$ |  | - | - | - | 60 | - | - | - |  |  |
| $+\mathrm{V}_{\text {SPK }}$ |  | - | - | - | 30 | - | - | - |  | $\mathrm{V}_{\mathrm{PP}}=+100 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-100 \mathrm{~V}$, |
| - $\mathrm{V}_{\text {SPK }}$ |  | - | - | - | 60 | - | - | - |  | $R_{\text {LOAD }}^{p}=50 \Omega$ |
| $+\mathrm{V}_{\text {SPK }}$ |  | - | - | - | 33 | - | - | - |  | $\mathrm{V}_{\mathrm{PP}}=+160 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-40 \mathrm{~V}$, |
| $-V_{\text {SPK }}$ |  | - | - | - | 60 | - | - | - |  | $R_{\text {LOAD }}^{P}=50 \Omega$ |
| QC | Charge injection | - | - | - | 270 | - | - | - | pC | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+40 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-160 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{SIG}}=0 \mathrm{~V} \end{aligned}$ |
|  |  | - | - | - | 220 | - | - | - |  | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+100 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-100 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{SIG}}=0 \mathrm{~V} \end{aligned}$ |
|  |  | - | - | - | 152 | - | - | - |  | $\begin{aligned} & \mathrm{V}_{\mathrm{PP}}=+160 \mathrm{~V}, \mathrm{~V}_{\mathrm{NN}}=-40 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{SIG}}=0 \mathrm{~V} \end{aligned}$ |

## Truth Table

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | LE | CLR | SW0 | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| L |  |  |  |  |  |  |  | L | L | Off |  |  |  |  |  |  |  |  |
| H |  |  |  |  |  |  |  | L | L | On |  |  |  |  |  |  |  |  |
|  | L |  |  |  |  |  |  | L | L |  | Off |  |  |  |  |  |  |  |
|  | H |  |  |  |  |  |  | L | L |  | On |  |  |  |  |  |  |  |
|  |  | L |  |  |  |  |  | L | L |  |  | Off |  |  |  |  |  |  |
|  |  | H |  |  |  |  |  | L | L |  |  | On |  |  |  |  |  |  |
|  |  |  | L |  |  |  |  | L | L |  |  |  | Off |  |  |  |  |  |
|  |  |  | H |  |  |  |  | L | L |  |  |  | On |  |  |  |  |  |
|  |  |  |  | L |  |  |  | L | L |  |  |  |  | Off |  |  |  |  |
|  |  |  |  | H |  |  |  | L | L |  |  |  |  | On |  |  |  |  |
|  |  |  |  |  | L |  |  | L | L |  |  |  |  |  | Off |  |  |  |
|  |  |  |  |  | H |  |  | L | L |  |  |  |  |  | On |  |  |  |
|  |  |  |  |  |  | L |  | L | L |  |  |  |  |  |  | Off |  |  |
|  |  |  |  |  |  | H |  | L | L |  |  |  |  |  |  | On |  |  |
|  |  |  |  |  |  |  | L | L | L |  |  |  |  |  |  |  | Off |  |
|  |  |  |  |  |  |  | H | L | L |  |  |  |  |  |  |  | On |  |
| X | X | X | X | X | X | X | X | H | L |  |  |  | Hold Previous State |  |  |  |  |  |
| X | X | X | X | X | X | X | X | X | H |  |  |  | All Switches Off |  |  |  |  |  |

## Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the $L$ to $H$ transition of the CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{L E}$. When $\overline{L E}$ is low the shift register data flow through the latch.
4. $D_{\text {out }}$ is high when data in the shift register 7 is high.
5. Shift register clocking has no effect on the switch states if $\overline{L E}$ is high.
6. The CLR clear input overrides all other inputs.

## Test Circuits




OFF Isolation


Isolation Diode Current


Crosstalk


Output Voltage Spike

Pin Configuration - 48-Lead LQFP (FG)

| Pin \# | Pin Name | Pin \# | Pin Name |
| :---: | :---: | :---: | :---: |
| 1 | SW5 | 25 | VNN |
| 2 | NC | 26 | NC |
| 3 | SW4 | 27 | RGND |
| 4 | NC | 28 | GND |
| 5 | SW4 | 29 | VDD |
| 6 | NC | 30 | NC |
| 7 | NC | 31 | NC |
| 8 | SW3 | 32 | NC |
| 9 | NC | 33 | DIN |
| 10 | SW3 | 34 | CLK |
| 11 | NC | 35 | LE |
| 12 | SW2 | 36 | CLR |
| 13 | NC | 37 | DOUT |
| 14 | SW2 | 38 | NC |
| 15 | NC | 39 | SW7 |
| 16 | SW1 | 40 | NC |
| 17 | NC | 41 | SW7 |
| 18 | SW1 | 42 | NC |
| 19 | NC | 43 | SW6 |
| 20 | SW0 | 44 | NC |
| 21 | NC | 45 | SW6 |
| 22 | SW0 | 46 | NC |
| 23 | NC | 47 | SW5 |
| 24 | VPP | 48 | NC |

Pin Configuration - 28-Lead PLCC (PJ)

| Pin \# | Pin Name | Pin \# | Pin Name |
| :---: | :---: | :---: | :---: |
| 1 | SW3 | 15 | NC |
| 2 | SW3 | 16 | DIN |
| 3 | SW2 | 17 | CLK |
| 4 | SW2 | 18 | $\overline{\text { LE }}$ |
| 5 | SW1 | 19 | CLR |
| 6 | SW1 | 20 | DOUT |
| 7 | SW0 | 21 | SW7 |
| 8 | SW0 | 22 | SW7 |
| 9 | NC | 23 | SW6 |
| 10 | VPP | 24 | SW6 |
| 11 | RGND | 25 | SW5 |
| 12 | VNN | 26 | SW5 |
| 13 | GND | 27 | SW4 |
| 14 | VDD | 28 | SW4 |

## Typical Waveforms



## 48-Lead LQFP Package Outline (FG)

## $7.00 \times 7.00 \mathrm{~mm}$ body, 1.60 mm height (max), 0.50 mm pitch



Note:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol |  | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | $\theta$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \text { Dimension } \\ (\mathrm{mm}) \end{gathered}$ | MIN | 1.40* | 0.05 | 1.35 | 0.17 | 8.80* | 6.80* | 8.80* | 6.80* | $\begin{aligned} & 0.50 \\ & \text { BSC } \end{aligned}$ | 0.45 | $\begin{aligned} & 1.00 \\ & \text { REF } \end{aligned}$ | $\begin{aligned} & 0.25 \\ & \text { BSC } \end{aligned}$ | $0^{\circ}$ |
|  | NOM | - | - | 1.40 | 0.22 | 9.00 | 7.00 | 9.00 | 7.00 |  | 0.60 |  |  | 3.50 |
|  | MAX | 1.60 | 0.15 | 1.45 | 0.27 | 9.20* | 7.20* | 9.20* | 7.20* |  | 0.75 |  |  | $7^{\circ}$ |

[^0]
## Drawings are not to scale.

Supertex Doc. \#: DSPD-48LQFPFG Version, D041309.

## 28-Lead PLCC Package Outline (PJ)

## .453x.453in. body, .180in. height (max), .050in. pitch



Vertical Side View


Horizontal Side View
View A

## Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

| Symbol |  | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Dimension (inches) | MIN | . 165 | . 090 | . 062 | . 013 | . 026 | . 485 | . 450 | . 485 | . 450 | $\begin{aligned} & .050 \\ & \text { BSC } \end{aligned}$ |
|  | NOM | . 172 | . 105 | - | - | - | . 490 | . 453 | . 490 | . 453 |  |
|  | MAX | . 180 | . 120 | . 083 | . 021 | . 032 | . 495 | . 456 | . 495 | . 456 |  |

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.

## Drawings not to scale.

Supertex Doc. \#: DSPD-28PLCCPJ, Version A092408.
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

[^1]
[^0]:    JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

    * This dimension is not specified in the JEDEC drawing.

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