

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4001B

gates

Quadruple 2-input NOR gate

Product specification
File under Integrated Circuits, IC04

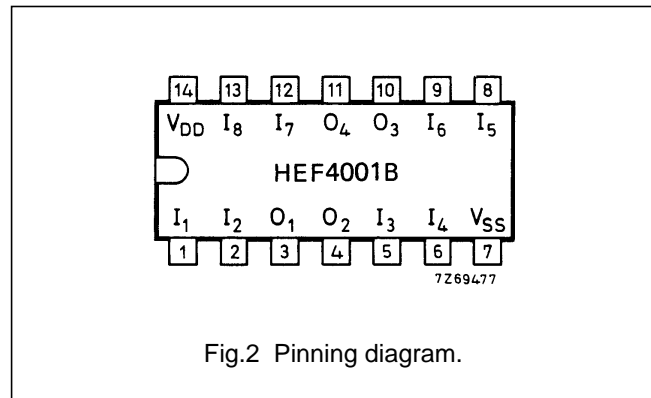
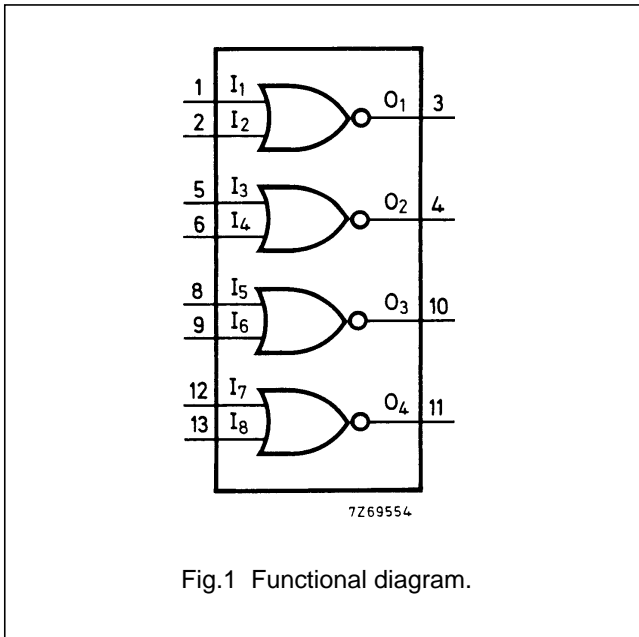
January 1995

Quadruple 2-input NOR gate

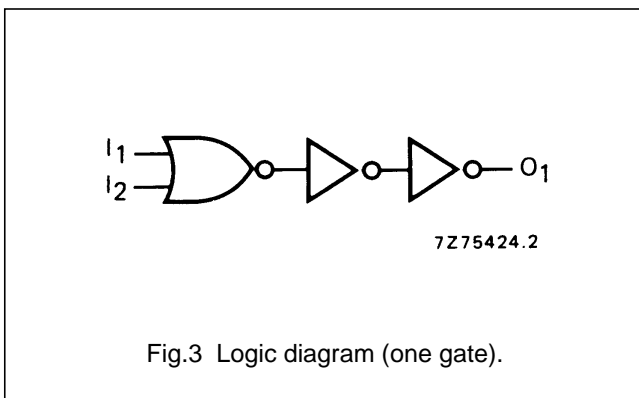
HEF4001B gates

DESCRIPTION

The HEF4001B provides the positive quadruple 2-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



- HEF4001BP(N): 14-lead DIL; plastic (SOT27-1)
 - HEF4001BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
 - HEF4001BT(D): 14-lead SO; plastic (SOT108-1)
- () : Package Designator North America



FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

Quadruple 2-input NOR gate

HEF4001B gates

AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

| | V_{DD} V | SYMBOL | TYP | MAX | | TYPICAL EXTRAPOLATION FORMULA |
|--|---------------|-----------|-----|-----|----|----------------------------------|
| Propagation delays $I_n \rightarrow O_n$ HIGH to LOW | 5 | t_{PHL} | 60 | 120 | ns | 33 ns + (0,55 ns/pF) C_L |
| | 10 | | 25 | 50 | ns | 14 ns + (0,23 ns/pF) C_L |
| | 15 | | 20 | 40 | ns | 12 ns + (0,16 ns/pF) C_L |
| LOW to HIGH | 5 | t_{PLH} | 50 | 100 | ns | 23 ns + (0,55 ns/pF) C_L |
| | 10 | | 25 | 45 | ns | 14 ns + (0,23 ns/pF) C_L |
| | 15 | | 20 | 35 | ns | 12 ns + (0,16 ns/pF) C_L |
| Output transition times HIGH to LOW | 5 | t_{THL} | 60 | 120 | ns | 10 ns + (1,0 ns/pF) C_L |
| | 10 | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) C_L |
| | 15 | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) C_L |
| LOW to HIGH | 5 | t_{TLH} | 60 | 120 | ns | 10 ns + (1,0 ns/pF) C_L |
| | 10 | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) C_L |
| | 15 | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) C_L |

| | V_{DD} V | TYPICAL FORMULA FOR P (μ W) | |
|---|---------------|--|---|
| Dynamic power dissipation per package (P) | 5 | $1100 f_i + \sum (f_o C_L) \times V_{DD}^2$ | where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V) |
| | 10 | $5000 f_i + \sum (f_o C_L) \times V_{DD}^2$ | |
| | 15 | $14\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$ | |