

Dual, High Voltage, Isolated MOSFET Driver

Features

- ▶ $\pm 400\text{V}$ input to output isolation
- ▶ $\pm 700\text{V}$ isolation between outputs
- ▶ No external voltage supply required
- ▶ Dual isolated output drivers
- ▶ Option of internal or external clock

Applications

- ▶ Telecommunications
- ▶ Modems
- ▶ Solid state relays
- ▶ High side switches
- ▶ High end audio switches
- ▶ Avionics
- ▶ ATE

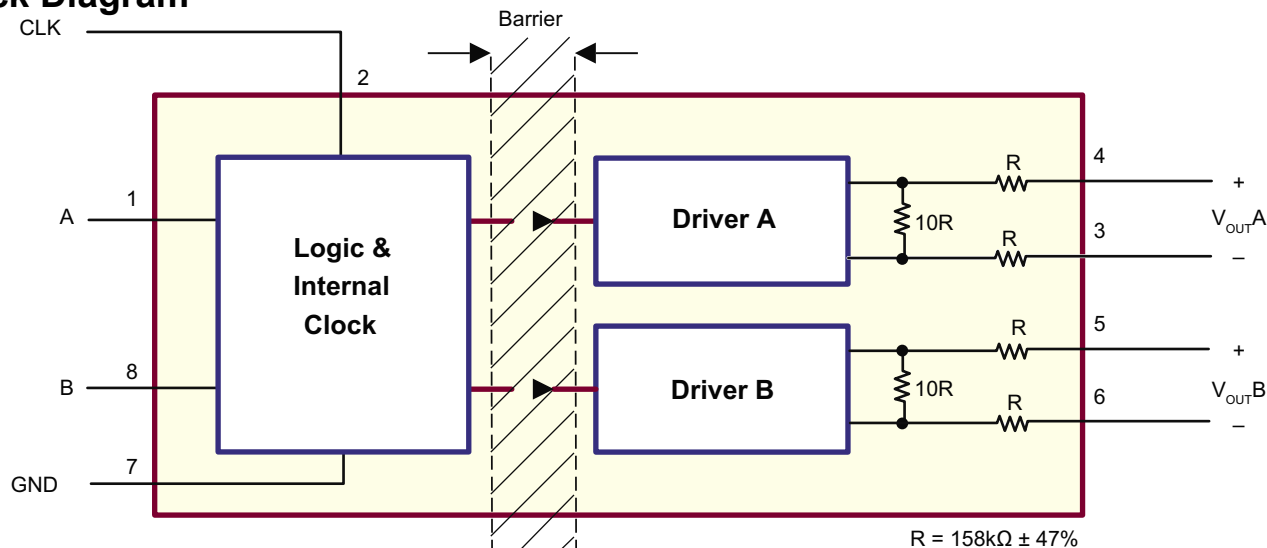
General Description

The Supertex HT0440 is a dual, high voltage, isolated MOSFET driver utilizing Supertex's proprietary HVCMOS® technology. It is designed to drive discrete MOSFETs configured as bi-directional or unidirectional switches. It can drive N-channel MOSFETs as high-side switches up to 400V. The HT0440 generates two independent DC isolated voltages to the outputs, $V_{\text{OUT}A}$ and $V_{\text{OUT}B}$ when logic inputs A and B are at logic high.

The internal clock of the HT0440 can be disabled by applying an external clock signal to the CLK pin. This allows the power dissipation and AC characteristics to be tailored to meet specific needs. The CLK pin should be connected to ground when not in use. The HT0440 does not require any external power supplies, the internal supply voltage is supplied by either of the two logic inputs, A or B, when they are at logic high.

For detailed circuit application information, please refer to application note AN-D26.

Block Diagram



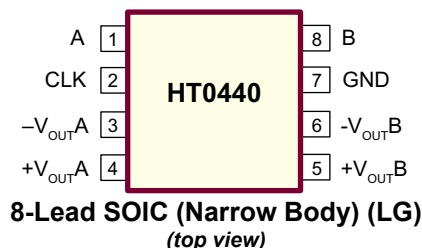
Ordering Information

| Device | Package Option |
|--------|--|
| | 8-Lead SOIC (Narrow Body) 4.90x3.90mm body 1.75mm height (max) 1.27mm pitch |
| HT0440 | HT0440LG-G |

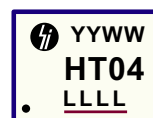
-G indicates package is RoHS compliant ('Green')



Pin Configuration



Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (Narrow Body) (LG)

Absolute Maximum Ratings

| Parameter | Value |
|--|-----------------|
| Input to output isolation voltage, V_{ISO} | $\pm 400V$ |
| Logic input voltage, V_A, V_B | -0.5 to +7.0V |
| Operating temperature | -40°C to +85°C |
| Storage temperature | -55°C to +150°C |
| Soldering temperature* | 300°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Recommended Operating Conditions

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-------------|--------------------------|------|-----|-----|-------|------------|
| CLK | External clock frequency | 0.5 | - | 2.0 | MHz | --- |
| V_{IHCLK} | Clock input high voltage | 3.15 | - | 5.5 | V | --- |
| V_{ILCLK} | Clock input low voltage | 0 | - | 0.5 | V | --- |
| V_{IH} | Logic input high voltage | 3.15 | - | 5.5 | V | --- |
| V_{IL} | Logic input low voltage | 0 | - | 0.5 | V | --- |
| T_A | Operating temperature | -40 | - | +85 | °C | --- |





AC Electrical Characteristics ($T_A = 25^\circ C$ unless otherwise specified)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|--------------|---------------------|-----|-----|-----|---------|---|
| $t_{d(ON)}$ | Turn-on delay time | - | - | 50 | μs | See timing diagram and test circuit CLK = 0V, CL = 600pF |
| t_r | Rise time | - | - | 650 | μs | |
| $t_{d(OFF)}$ | Turn-off delay time | - | - | 150 | μs | |
| t_f | Fall time | - | - | 3.0 | ms | |

DC Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

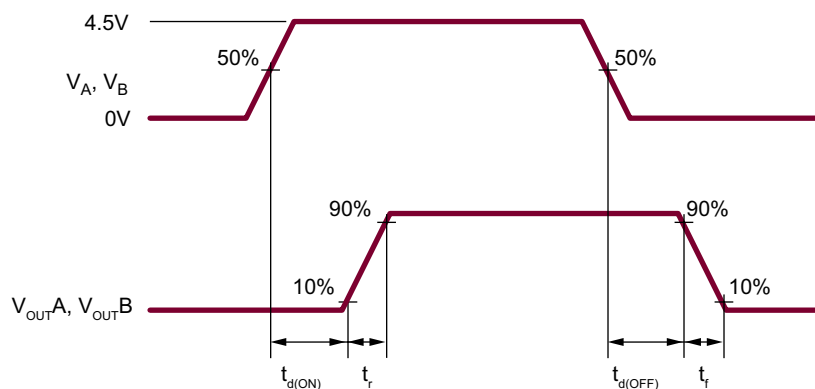
| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|----------------------|------------------------------------|-----------|-----|-----|---------------|--|
| $I_{HA} + I_{HB}$ | Total logic high input current | - | - | 300 | μA | $V_A = 3.5\text{V}, V_B = 3.5\text{V}, \text{CLK} = 0\text{V}$ |
| | | - | - | 500 | μA | $V_A = 3.5\text{V}, V_B = 3.5\text{V}, \text{CLK} = 500\text{KHz}$ |
| | | - | - | 2.0 | mA | $V_A = 3.5\text{V}, V_B = 3.5\text{V}, \text{CLK} = 2.0\text{MHz}$ |
| | | - | - | 1.0 | mA | $V_A = 5.5\text{V}, V_B = 5.5\text{V}, \text{CLK} = 0\text{V}$ |
| | | - | - | 2.0 | mA | $V_A = 5.5\text{V}, V_B = 5.5\text{V}, \text{CLK} = 500\text{KHz}$ |
| V_{OUTA}, V_{OUTB} | Output voltage | 6.0 | - | - | V | $V_A = 3.15\text{V}, V_B = 3.15\text{V}, \text{CLK} = 0\text{V}, \text{no load}$ |
| | | 5.0 | - | - | V | $V_A = 3.15\text{V}, V_B = 3.15\text{V}, \text{CLK} = 500\text{KHz}, \text{no load}$ |
| | | 6.0 | - | - | V | $V_A = 3.15\text{V}, V_B = 3.15\text{V}, \text{CLK} = 2.0\text{MHz}, \text{no load}$ |
| | | 10.0 | - | - | V | $V_A = 4.5\text{V}, V_B = 4.5\text{V}, \text{CLK} = 0\text{V}, \text{no load}$ |
| | | 8.0 | - | - | V | $V_A = 4.5\text{V}, V_B = 4.5\text{V}, \text{CLK} = 500\text{KHz}, \text{no load}$ |
| I_{ILA} | Logic low input A current | - | - | 10 | μA | $V_A = 0.5\text{V}, V_B = \text{high}$ |
| I_{ILB} | Logic low input B current | - | - | 10 | μA | $V_A = \text{high}, V_B = 0.5\text{V}$ |
| I_{ILQ} | Quiescent current | - | - | 10 | μA | $V_A = 0.5\text{V}, V_B = 0.5\text{V}$ |
| V_{ISO} | Input to output isolation voltage | ± 400 | - | - | V | --- |
| V_{CISO} | Output to output isolation voltage | ± 700 | - | - | V | --- |

Truth Table

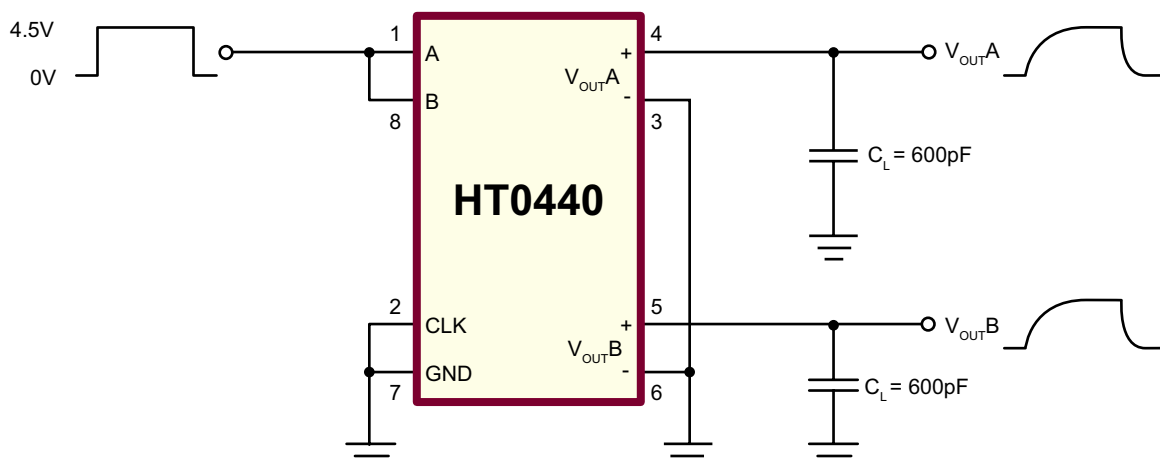
| A | B | CLK | V_{OUTA} | V_{OUTB} | Internal Clock |
|---|---|-----|------------|------------|----------------|
| 0 | 0 | 0 | Off | Off | Off |
| 0 |  | 0 | Off | On | On |
|  | 0 | 0 | On | Off | On |
| 1 | 1* | 0 | On | On | On |
| 0 | 0 | CLK | Off | Off | Off |
| 0 |  | CLK | Off | On | Off |
|  | 0 | CLK | On | Off | Off |
| 1 | 1* | CLK | On | On | Off |

* When both A and B are high, the inputs are internally connected. Both inputs must go low to turn off an output. The logic input for the output that needs to remain on must go back high.

Timing Diagram

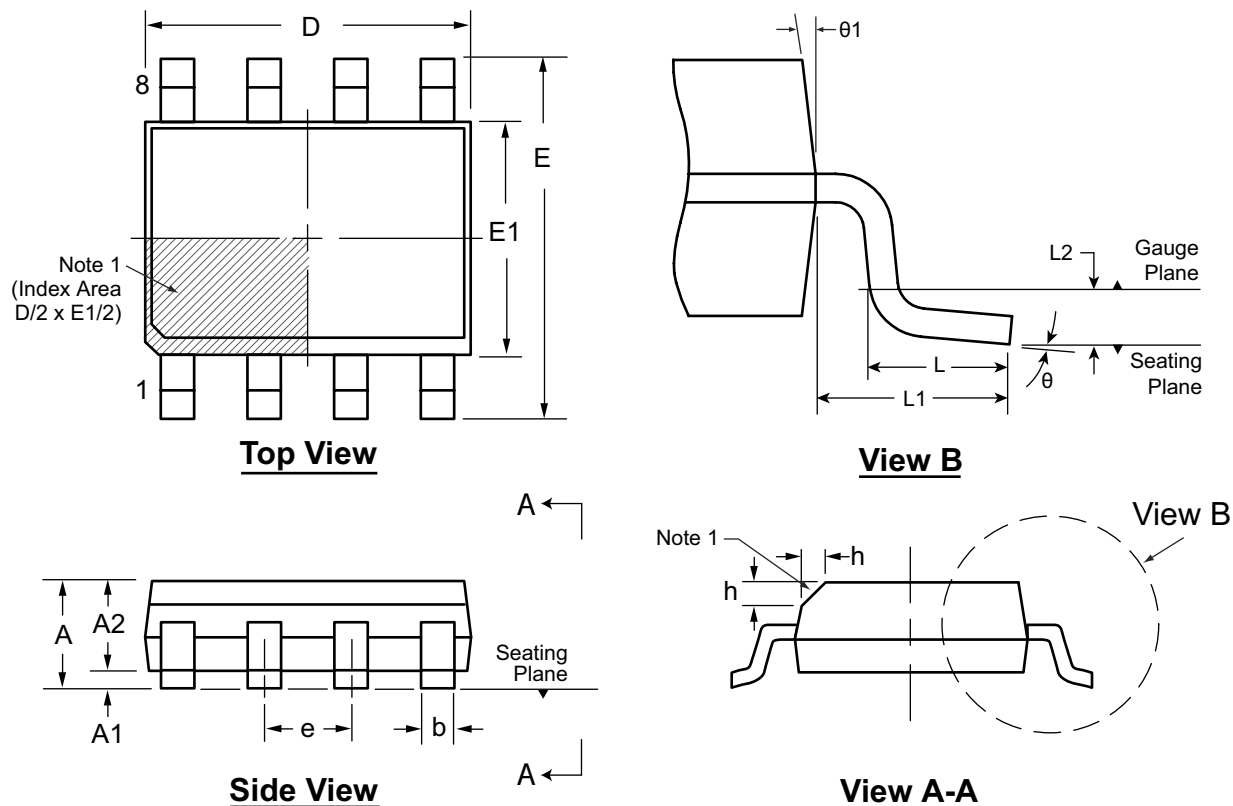


Test Circuit



8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | | A | A1 | A2 | b | D | E | E1 | e | h | L | L1 | L2 | θ | θ1 |
|-------------------|-----|-------|------|-------|------|-------|-------|-------|-------------|------|------|-------------|-------------|----|-----|
| Dimension (mm) | MIN | 1.35* | 0.10 | 1.25 | 0.31 | 4.80* | 5.80* | 3.80* | 1.27 BSC | 0.25 | 0.40 | 1.04 REF | 0.25 BSC | 0° | 5° |
| | NOM | - | - | - | - | 4.90 | 6.00 | 3.90 | | - | - | | | - | - |
| | MAX | 1.75 | 0.25 | 1.65* | 0.51 | 5.00* | 6.20* | 4.00* | | 0.50 | 1.27 | | | 8° | 15° |

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version I041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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