SLLS213A - JANUARY 1996 - REVISED JUNE 1999

- Single Chip With Easy Interface Between **UART and Serial-Port Connector of an External Modem or Other Computer** Peripheral
- **Five Drivers and Three Receivers Meet or Exceed the Requirements of ANSI Standard** TIA/EIA-232-F and ITU Recommendation V.28 Standards
- Supports Data Rates up to 120 kbit/s
- Complement to the GD75232
- Provides Pin-to-Pin Replacement for the Goldstar GD75323
- **Pin-Out Compatible With SN75196**
- **Functional Replacement for the MC145405**

### DW OR N PACKAGE (TOP VIEW) Vcc L 20 🛮 V<sub>DD</sub> 1DA **∏** 2 19 1DY 2DA **∏** 3 18 2DY 3DA **∏** 4 17 **∏** 3DY 1RY **[**] 5 2RY [ 6 15 2RA 4DA **∏** 7 14**∏** 4DY 13 T 3RA 3RY [ 8 5DA **∏** 9 12 5DY GND **1** 10 11 [] V<sub>SS</sub>

### description

The GD75323 combines five drivers and three receivers from the trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The flow-through design of the GD75323 decreases the part count, reduces the board space required, and allows easy interconnection of the UART and serial-port connector. The all-bipolar circuits and processing of the GD75323 provide a rugged, low-cost solution for this function.

The GD75323 complies with the requirements of the ANSI TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signal rates up to 20 kbit/s. The switching speeds of the GD75323 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of ANSI Standard TIA/EIA-423-B and TIA/EIA-422-B and ITU Recommendations V.10 and V.11 are recommended.

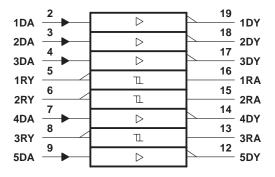
The GD75323 is characterized for operation over a temperature range of 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



### logic symbol†

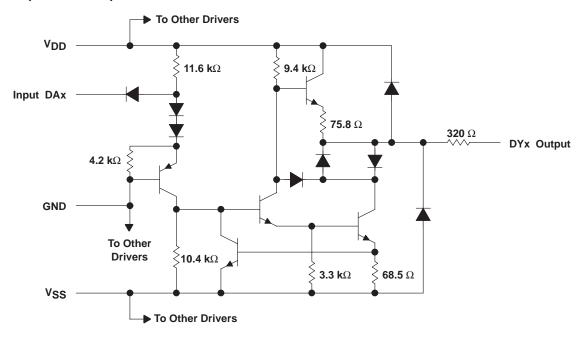


<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)

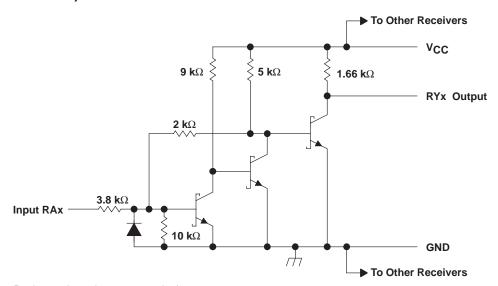


### schematic (each driver)



Resistor values shown are nominal.

## schematic (each receiver)



Resistor values shown are nominal.

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub> (see Note 1)	10 V
Supply voltage, V <sub>DD</sub> (see Note 1)	15 V
Supply voltage, V <sub>SS</sub> (see Note 1)	
Input voltage range, V <sub>I</sub> : Driver	–15 V to 7 V
Receiver	30 V to 30 V
Output voltage range, VO (Driver)	– 15 V to 15 V
Low-level output current, IOL (Receiver)	20 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): [	DW package 97°C/W
1	N package 67°C/W
Lead temperature 1,6 mm (1/16 inch) from case for	or 10 seconds
Storage temperature range, T <sub>stg</sub>	– 65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
	$V_{DD}$	7.5	9	13.5	
Supply voltage	V <sub>SS</sub>	-7.5	-9	-13.5	V
	Vcc	4.5	5	5.5	
High-level input voltage, VIH	Driver	1.9			V
Low-level input voltage, V <sub>IL</sub>	Driver			0.8	V
High lovel output ourrent love	Driver			-6	mA
High-level output current, IOH	Receiver			-0.5	ША
High lovel output ourrent les	Driver			6	mA
High-level output current, IOL	Receiver			16	IIIA
Operating free-air temperature,TA		0		70	°C

### supply currents over operating free-air temperature range

	PARAMETER		TEST CONDITIONS					UNIT
		All inputs at 1.9 V,	No load	$V_{DD} = 9 V$ ,	$V_{SS} = -9 V$		25	mA
,	Supply current from VDD	All inputs at 1.9 v,	140 1084	V <sub>DD</sub> = 12 V,	$V_{SS} = -12 \text{ V}$		32	IIIA
IDD	Supply current from VDD	All inputs at 0.8 V,	No load	V <sub>DD</sub> = 9 V,	$V_{SS} = -9 V$		7.5	mA
	All inputs at 0.6 V, No load	V <sub>DD</sub> = 12 V,	$V_{SS} = -12 \text{ V}$		9.5	IIIA		
		All inputs at 1.9 V,	No load	$V_{DD} = 9 V$ ,	$V_{SS} = -9 V$		-25	mA
las	Cupply ourront from Vaa	All inputs at 1.9 v,	110 10au	V <sub>DD</sub> = 12 V,	$V_{SS} = -12 \text{ V}$		-32	IIIA
ISS	Supply current from VSS	All inputs at 0.8 V,	No load	$V_{DD} = 9 V$ ,	V <sub>SS</sub> = -9 V		-5.3	m A
		All inputs at 0.6 v,	NO IOAU	V <sub>DD</sub> = 12 V,	$V_{SS} = -12 \text{ V}$		-5.3	mA
ICC	Supply current from V <sub>CC</sub>	V <sub>CC</sub> = 5 V,	All inputs at 5 V,	No load			20	mA



NOTES: 1. All voltages are with respect to the network ground terminal.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

### **DRIVER SECTION**

# electrical characteristics over operating free-air temperature range, $V_{DD}$ = 9 V, $V_{SS}$ = -9 V, $V_{CC}$ = 5 V (unless otherwise noted)

	PARAMETER		TEST CONDITIO	ONS	MIN	TYP	MAX	UNIT
Vон	High-level output voltage	V <sub>IL</sub> = 0.8 V,	$R_L = 3 k\Omega$ ,	See Figure 1	6	7.5		V
V <sub>OL</sub>	Low-level output voltage (see Note 3)	V <sub>IH</sub> = 1.9 V,	$R_L = 3 k\Omega$ ,	See Figure 1		-7.5	-6	V
lн	High-level input current	V <sub>I</sub> = 5 V,	See Figure 2				10	μΑ
Ι <sub>Ι</sub> L	Low-level input current	$V_{I} = 0,$	See Figure 2				-1.6	mA
IOS(H)	High-level short-circuit output current (see Note 4)	V <sub>IL</sub> = 0.8 V,	V <sub>O</sub> = 0,	See Figure 1	-4.5	-9	-19.5	mA
IOS(L)	Low-level short-circuit output current	V <sub>IH</sub> = 2 V,	$V_{O} = 0$ ,	See Figure 1	4.5	9	19	mA
ro	Output resistance (see Note 5)	$V_{CC} = V_{DD} = V_{SS} = 0,$		$V_0 = -2 \text{ V to } 2 \text{ V}$	300			Ω

- NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is maximum, the typical value is a more negative voltage.
  - 4. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
  - 5. Test conditions are those specified by TIA/EIA-232-F and as listed above.

## switching characteristics, $V_{DD}$ = 12 V, $V_{SS}$ = -12 V, $V_{CC}$ = 5 V $\pm 10\%$ , $T_A$ = 25°C

	PARAMETER	TEST CONDITI	ONS	MIN	TYP	MAX	UNIT
<sup>t</sup> PLH	Propagation delay time, low- to high-level output	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega,$	C <sub>L</sub> = 15 pF,		315	500	ns
tPHL	Propagation delay time, high- to low-level output	See Figure 3	_		75	175	ns
Transition time law to high level output		$R_L$ = 3 kΩ to 7 kΩ, See Figure 3	C <sub>L</sub> = 15 pF,		60	100	ns
t <sub>TLH</sub> Transition time, low- to high-level output	rransition time, low- to high-level output	$R_L$ = 3 kΩ to 7 kΩ, See Figure 3 and Note 6	$C_L = 2500 \text{ pF},$		1.7	2.5	μs
<u></u>	Transition time, high- to low-level output (see	$R_L$ = 3 kΩ to 7 kΩ, See Figure 3	C <sub>L</sub> = 15 pF,		40	75	ns
<sup>t</sup> THL	Note 5)	$R_L$ = 3 kΩ to 7 kΩ, See Figure 3 and Note 7	$C_L = 2500 \text{ pF},$		1.5	2.5	μs

- NOTES: 6. Measured between 3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.
  - 7. Measured between 3-V and -3-V points of the output waveform (TIA/EIA-232-F conditions), all unused inputs are tied either high or low.



### **RECEIVER SECTION**

### electrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST C	ONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT	
\/	Positive-going input threshold voltage	See Figure 5	T <sub>A</sub> = 25°C	1.75	1.9	2.3		
VIT+	Fositive-going input tilleshold voltage	See Figure 5	$T_A = 0$ °C to 70 °C	1.55		2.3	V	
V <sub>IT</sub> –	Negative-going input threshold voltage	See Figure 5		0.75	0.97	1.25	V	
V <sub>hys</sub>	Input hysteresis voltage (V <sub>IT+</sub> – V <sub>IT-</sub> )	See Figure 5		0.5				
Vou	High-level output voltage	I <sub>OH</sub> = -0.5 mA	V <sub>IH</sub> = 0.75 V	2.6	4	5	V	
VOH	nigri-level output voltage		Inputs open	2.6				
VOL	Low-level output voltage	$I_{OL} = 10 \text{ mA},$	V <sub>I</sub> = 3 V		0.2	0.45	V	
	High-level input current	V <sub>I</sub> = 25 V,	See Figure 5	3.6		8.3	mA	
ΊΗ	riigir-ieveriiiput current	V <sub>I</sub> = 3 V,	See Figure 5	0.43			IIIA	
1	Low-level input current	$V_{I} = -25 \text{ V},$	See Figure 5	-3.6		-8.3	mA	
¹IL	Low-level input current	$V_{I} = -3 V$ ,	See Figure 5	-0.43				
los	Short-circuit output current	See Figure 4			-3.4	-12	mA	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $T_A = 25^{\circ}C$ ,  $V_{CC} = 5$  V,  $V_{DD} = 9$  V, and  $V_{SS} = -9$  V.

## switching characteristics, $V_{CC}$ = 5 V, $V_{DD}$ = 12 V, $V_{SS}$ = -12 V, $T_A$ = 25°C

	PARAMETER	TEST CO	MIN	TYP	MAX	UNIT	
tPLH	Propagation delay time, low- to high-level output				107	500	ns
tPHL	Propagation delay time, high- to low-level output	$C_L = 50 \text{ pF},$	$R_L = 5 k\Omega$ ,		42	150	ns
<sup>t</sup> TLH	Transition time, low- to high-level output	See Figure 6			175	525	ns
tTHL	Transition time, high- to low-level output				16	60	ns

### PARAMETER MEASUREMENT INFORMATION

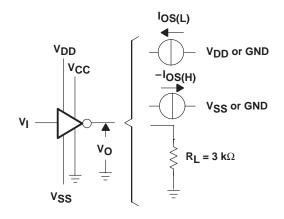


Figure 1. Driver Test Circuit for  $V_{OH}$ ,  $V_{OL}$ ,  $I_{OS(H)}$ , and  $I_{OS(L)}$ 

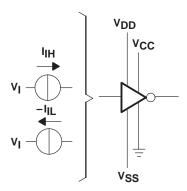
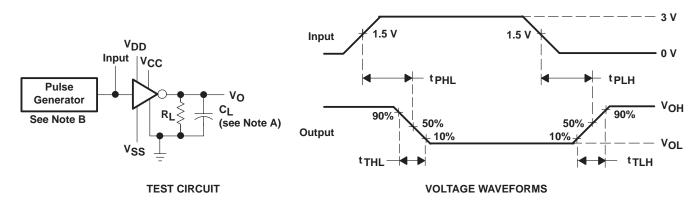


Figure 2. Driver Test Circuit for  $I_{\mbox{\scriptsize IH}}$  and  $I_{\mbox{\scriptsize IL}}$ 



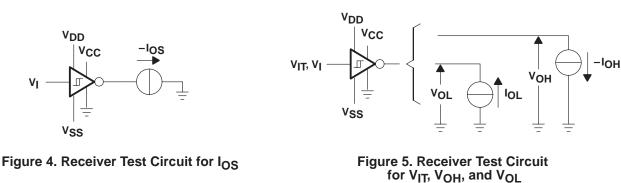
### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $t_W$  = 25  $\mu$ s, PRR = 20 kHz,  $Z_O$  = 50  $\Omega$ ,  $t_r$  =  $t_f$  < 50 ns.

Figure 3. Driver Test Circuit and Voltage Waveforms



50% 50% Input -5 V <sup>t</sup>PHL <sup>t</sup>PLH Vон 90% 50% 50% Output 10% 10% Vol tTHLtTLH

**VOLTAGE WAVEFORMS** 

Input **Pulse** ۷o Generator See Note B (see Note A) VSS

NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

**TEST CIRCUIT** 

 $V_{DD}$ 

B. The pulse generator has the following characteristics:  $t_W = 25 \,\mu s$ , PRR = 20 kHz,  $Z_O = 50 \,\Omega$ ,  $t_T = t_f < 50 \,ns$ .

Figure 6. Receiver Propagation and Transition Times

# TYPICAL CHARACTERISTICS DRIVER SECTION

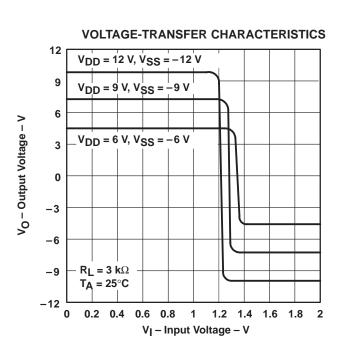
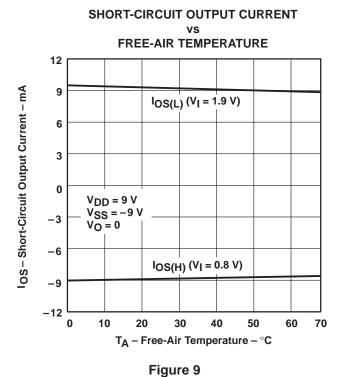
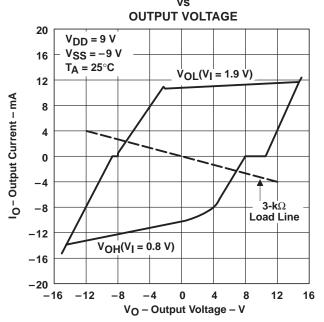


Figure 7





**OUTPUT CURRENT** 

Figure 8

### SLEW RATE vs LOAD CAPACITANCE

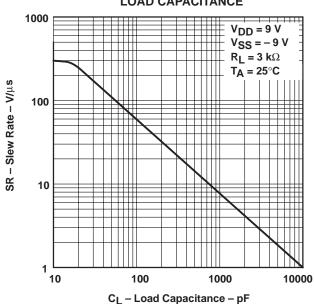


Figure 10



## TYPICAL CHARACTERISTICS **RECEIVER SECTION**

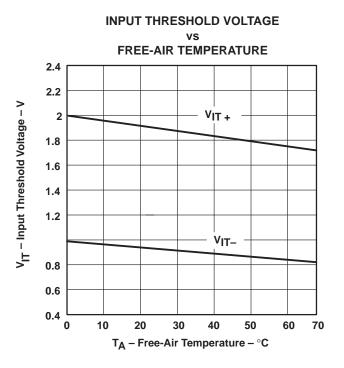
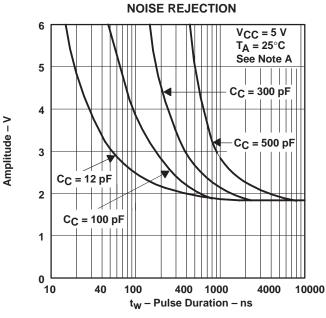


Figure 11



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

Figure 13

### **INPUT THRESHOLD VOLTAGE SUPPLY VOLTAGE** 2 $V_{\text{IT+}}$ 1.8 V<sub>IT</sub> - Input Threshold Voltage - V 1.6 1.4 1.2 1 V<sub>IT</sub>-0.8 0.6 0.4 0.2 0 2 3 5 8 9 10 V<sub>CC</sub> - Supply Voltage - V

Figure 12

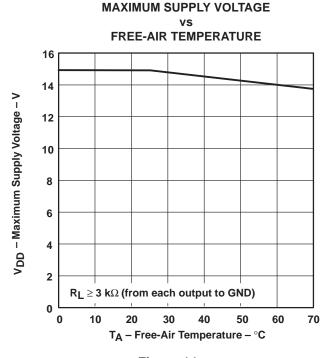


Figure 14



### **APPLICATION INFORMATION**

Diodes placed in series with the  $V_{DD}$  and  $V_{SS}$  leads protect the GD75323 in the fault condition in which the device outputs are shorted to  $V_{DD}$  or  $V_{SS}$ , and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

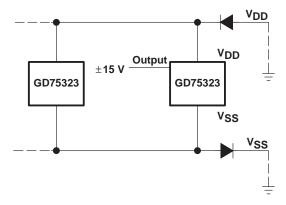
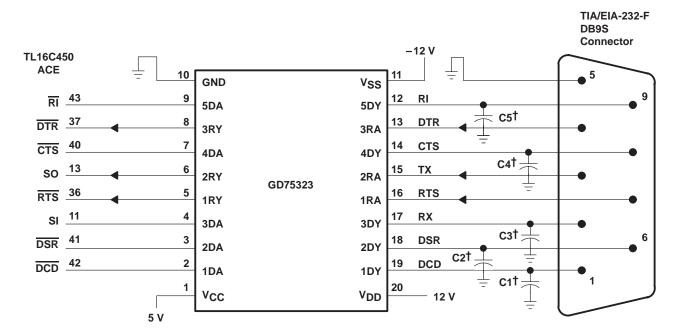


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



<sup>&</sup>lt;sup>†</sup> See Figure 10 to select the correct values for the loading capacitors (C1, C2, C3, C4, and C5), which may be required to meet the RS-232 maximum slew-rate requirement of 30 V/μs. The value of the loading capacitors required depends upon the line length and desired slew rate, but is typically 330 pF.

NOTE C: To use the receivers only, VDD and VSS both must be powered or tied to ground.

**Figure 16. Typical Connection** 







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### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
GD75323DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
GD75323DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
GD75323DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
GD75323DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
GD75323DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
GD75323DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
GD75323N	OBSOLETE	PDIP	N	20	•	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

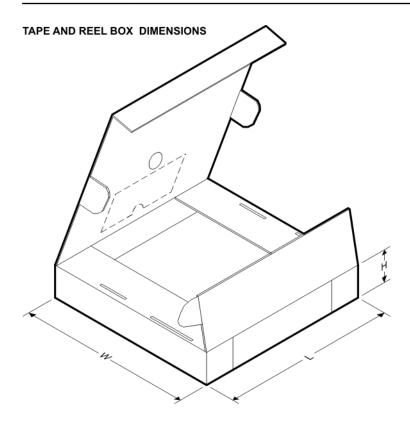
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
GD75323DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
GD75323DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1





### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
GD75323DWR	SOIC	DW	20	2000	346.0	346.0	41.0
GD75323DWR	SOIC	DW	20	2000	346.0	346.0	41.0

## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



## N (R-PDIP-T\*\*)

### PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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