

CD74HCT4067-Q1 HIGH-SPEED CMOS LOGIC 16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

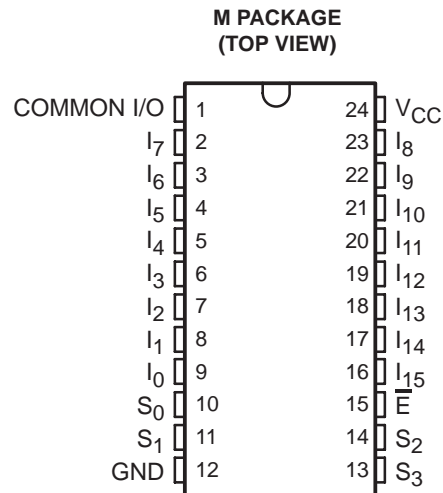
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- Qualified for Automotive Applications
- Wide Analog Input Voltage Range
- Low ON Resistance
 - 70 Ω Typical ($V_{CC} = 4.5\text{ V}$)
- Fast Switching and Propagation Speeds
- “Break-Before-Make” Switching
 - 6 ns Typical ($V_{CC} = 4.5\text{ V}$)
- Fanout (Over Temperature Range)
 - Standard Outputs: 10 LSTTL Loads
 - Bus Driver Outputs: 15 LSTTL Loads
- Wide Operating Temperature Range: -40°C to 85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 4.5-V to 5.5-V Operation
- Direct LSTTL Input Logic Compatibility: $V_{IL} = 0.8\text{ V Max}$, $V_{IH} = 2\text{ V Min}$
- CMOS Input Compatibility: $I_I \leq 1\ \mu\text{A}$ at V_{OL} , V_{OH}

description/ordering information

The CD74HCT4067 device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer/demultiplexer controls analog voltages that may vary across the voltage supply range. It is a bidirectional switch, thus allowing any analog input to be used as an output and vice-versa. The switch has low “on” resistance and low “off” leakages. In addition, the device has an enable control that, when high, disables all switches to their “off” state.



ORDERING INFORMATION†

T _A	PACKAGE‡	ORDERABLE PART NUMBER§	TOP-SIDE MARKING
-40°C to 85°C	SOIC – M Reel of 2000	CD74HCT4067IM96Q1	HCT40671

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

§ The suffix 96 denotes tape and reel.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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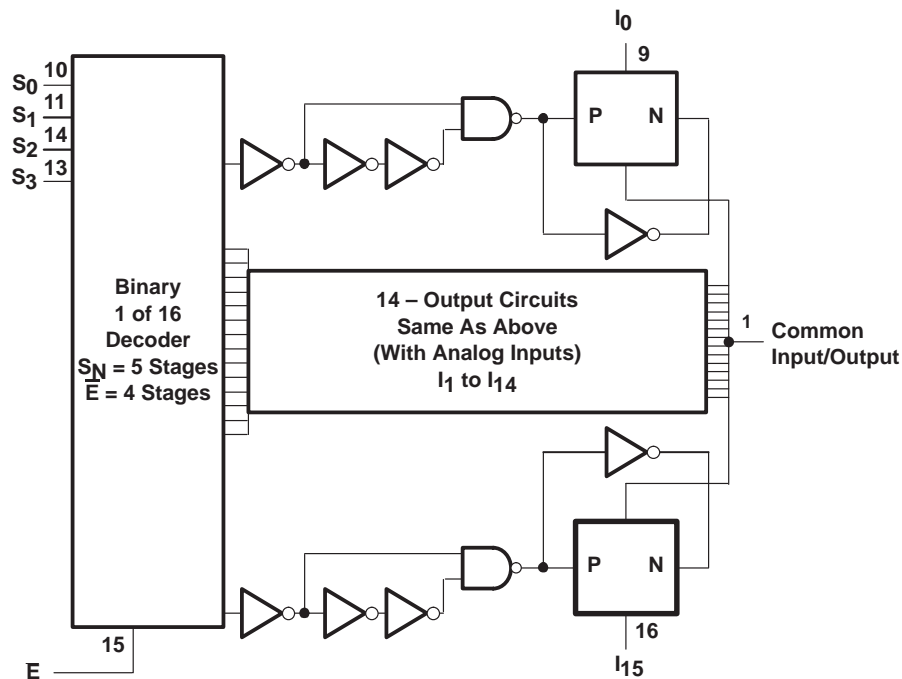
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FUNCTION TABLE

S0	S1	S2	S3	\bar{E}	SELECTED CHANNEL
X	X	X	X	H	None
L	L	L	L	L	0
H	L	L	L	L	1
L	H	L	L	L	2
H	H	L	L	L	3
L	L	H	L	L	4
H	L	H	L	L	5
L	H	H	L	L	6
H	H	H	L	L	7
L	L	L	H	L	8
H	L	L	H	L	9
L	H	L	H	L	10
H	H	L	H	L	11
L	L	H	H	L	12
H	L	H	H	L	13
L	H	H	H	L	14
H	H	H	H	L	15

H = High level
 L = Low level
 X = Don't Care

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to +7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
Output clamp current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
Switch current, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
Output source or sink current per output pin, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2)	46°C/W
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{Stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are referenced to GND, unless otherwise specified.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
t_t	Input transition (rise and fall) time		$V_{CC} = 4.5$ V	ns
T_A	Operating free-air temperature	–40	85	°C

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _I	V _{CC}	T _A = 25°C			T _A = -40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
I _I	Logic input	V _{CC} or GND	5.5 V			±0.1		±1	μA
I _{Iz}	V _{IS} = V _{CC} or GND, $\bar{E} = V_{CC}$		5.5 V			±0.8		±8	μA
r _{on}	I _O = 1 mA	V _{IS} = V _{CC} or GND	V _{CC} or GND	4.5 V		70 160		200	Ω
		V _{IS} = V _{CC} to GND	V _{CC} to GND	4.5 V		90 180		225	
Δr _{on}	Between any two switches		4.5 V			10			Ω
I _{CC}		V _{CC} or GND	5.5 V				8	80	μA
ΔI _{CC}	Per input pin: 1 unit load, See Note 4	V _{CC} - 2.1 V	4.5 V to 5.5 V			100 360		450	μA
C _I	Control inputs							10	pF

NOTE 4: For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT input loading

INPUT	UNIT LOADS†
S ₀ - S ₃	0.5
\bar{E}	0.3

† Unit load is ΔI_{CC} limit specified in the electrical characteristics table, e.g., 360 μA max at 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -40°C TO 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t _{pd}	I _n	Common I/O	C _L = 15 pF	5 V		6			ns	
			C _L = 50 pF	4.5 V		15	19			
t _{en}	\bar{E}	Common I/O	C _L = 15 pF	5 V		25			ns	
			C _L = 50 pF	4.5 V		60	75			
t _{en}	S _n	Common I/O	C _L = 15 pF	5 V		25			ns	
			C _L = 50 pF	4.5 V		60	75			
t _{dis}	\bar{E}	Common I/O	C _L = 15 pF	5 V		23			ns	
			C _L = 50 pF	4.5 V		55	69			
t _{dis}	S _n	Common I/O	C _L = 15 pF	5 V		21			ns	
			C _L = 50 pF	4.5 V		58	73			



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operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, input $t_r, t_f = 6\text{ ns}$

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 5)	96	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption (P_D), per package.

$$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + \sum (C_L + C_S) \times V_{CC}^2 \times f_O$$

f_O = output frequency

f_i = input frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage

analog channel characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
f_{max}	Switch frequency response bandwidth at -3 dB	4.5 V	89	MHz
	Sine-wave distortion	4.5 V	0.051	%
	Switch OFF signal feedthrough	4.5 V	-75	dB
C_S	Switch input capacitance		5	pF
C_{COM}	Common capacitance		50	pF

NOTES: 6. Adjust input voltage to obtain 0 dBm at output, $f = 1\text{ MHz}$.

7. V_{IS} is centered at $V_{CC}/2$.

PARAMETER MEASUREMENT INFORMATION

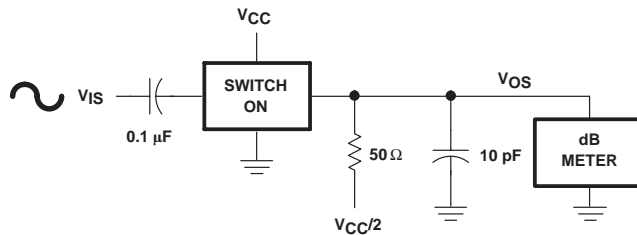


Figure 1. Frequency-Response Test Circuit

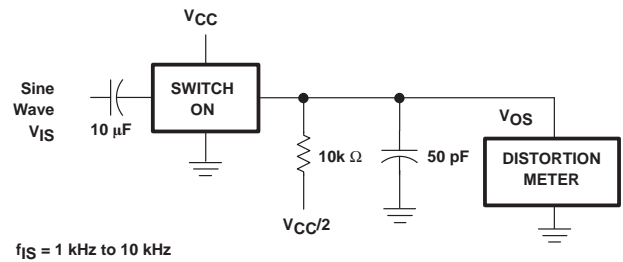


Figure 2. Sine-Wave Distortion Test Circuit

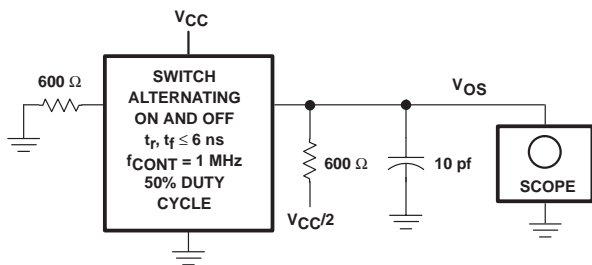


Figure 3. Control-to-Switch Feedthrough Noise Test Circuit

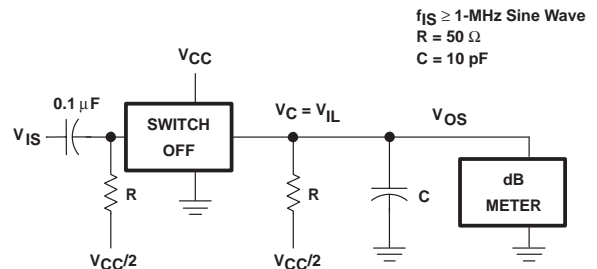
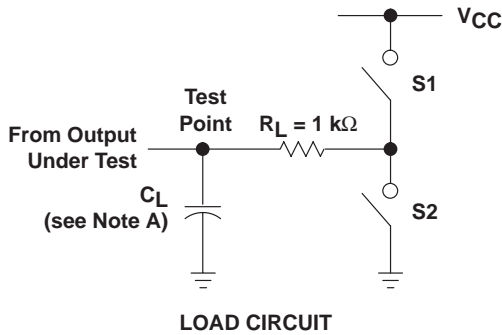


Figure 4. Switch OFF Signal Feedthrough Test Circuit

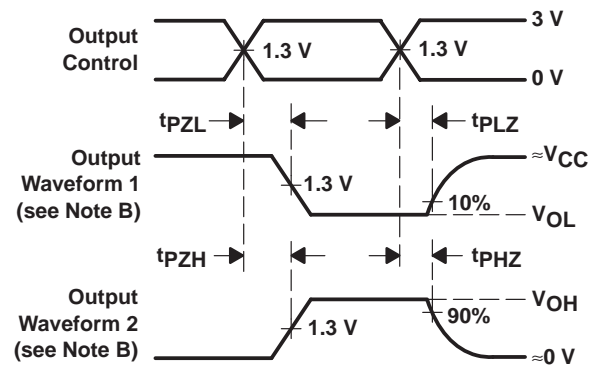
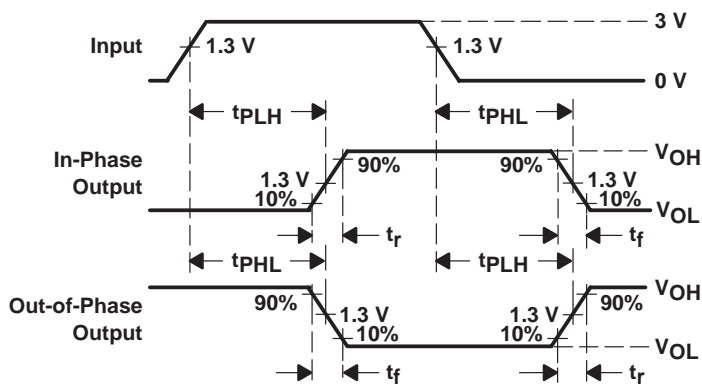
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PARAMETER MEASUREMENT INFORMATION



PARAMETER	S1	S2	
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}	Open	Open	



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time, with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 5. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

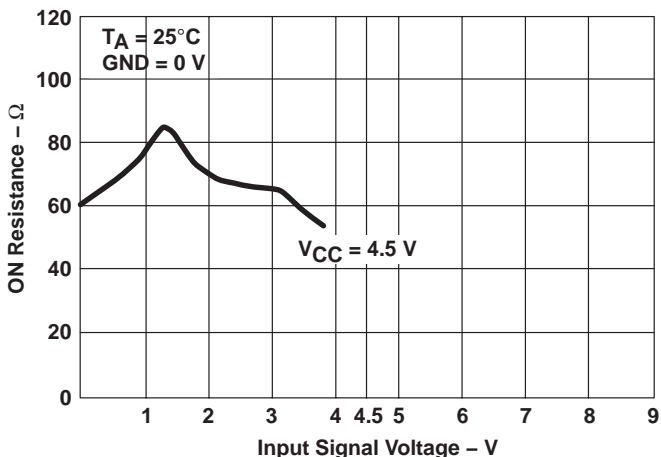


Figure 6. ON Resistance vs Input Signal Voltage

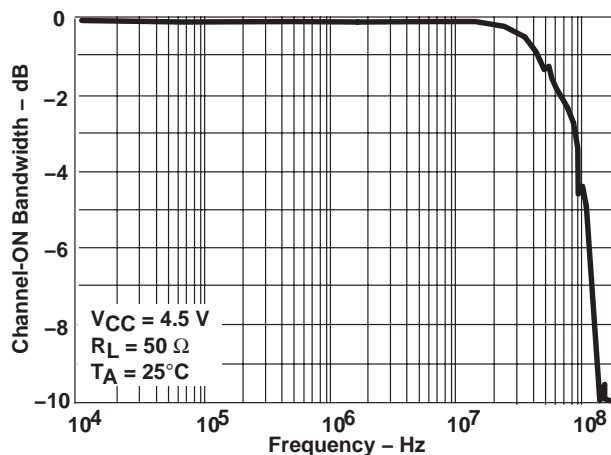


Figure 7. Switch Frequency Response

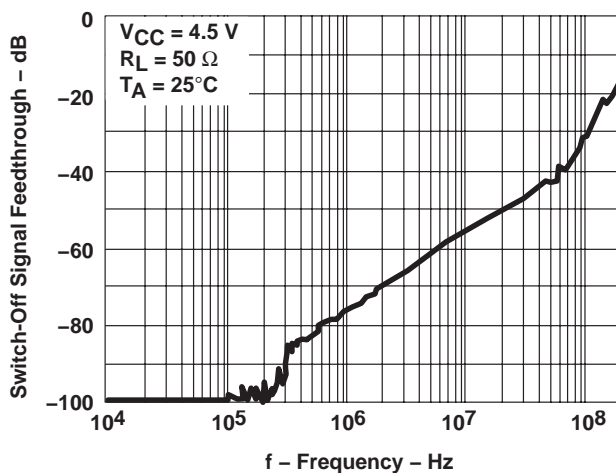


Figure 8. Switch-OFF Signal Feedthrough vs Frequency

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74HCT4067IM96Q1	ACTIVE	SOIC	DW	24	2000	TBD	Call TI	Call TI
D24067IM96G4Q1	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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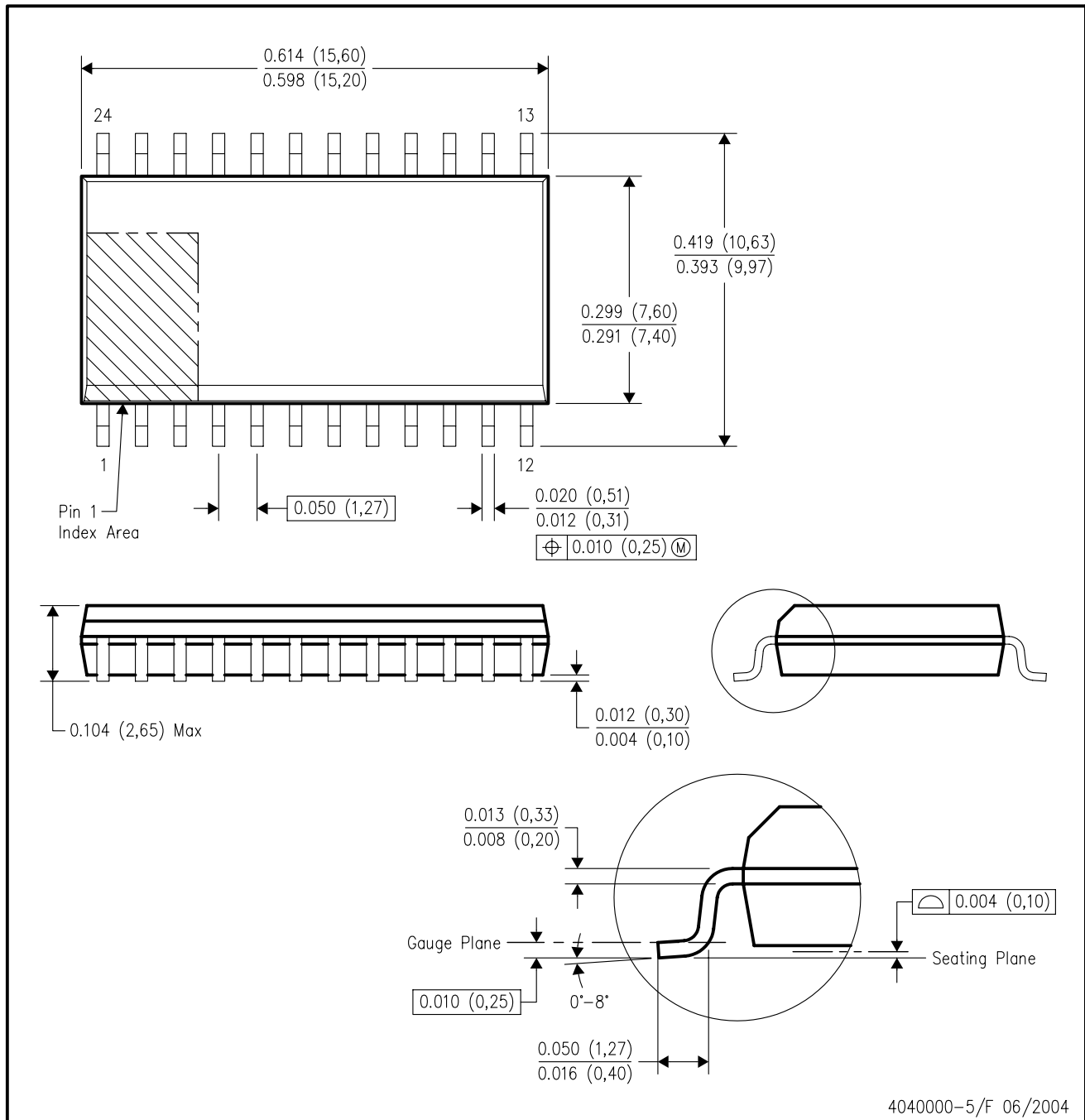
- Catalog: [CD74HCT4067](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

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