DAC102S085

DAC102S085 10-Bit Micro Power DUAL Digital-to-Analog Converter with Rail-to-Rail Output

Literature Number: SNAS364D

National Semiconductor

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DAC102S085
10-Bit Micro Power DUAL Digital-to-Analog Converter with Rail-to-Rail Output

General Description

The DAC102S085 is a full-featured, general purpose DUAL 10-bit voltage-output digital-to-analog converter (DAC) that can operate from a single +2.7V to 5.5V supply and consumes 0.6 mW at 3V and 1.6 mW at 5V. The DAC102S085 is packaged in 10-lead LLP and MSOP packages. The 10-lead LLP package makes the DAC102S085 the smallest DUAL DAC in its class. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range. Competitive devices are limited to 25 MHz clock rates at supply voltages in the 2.7V to 3.6V range. The serial interface is compatible with standard SPI™, QSPI, MICROWIRE and DSP interfaces.

The reference for the DAC102S085 serves both channels and can vary in voltage between 1V and V_A, providing the widest possible output dynamic range. The DAC102S085 has a 16-bit input shift register that controls the outputs to be updated, the mode of operation, the powerdown condition, and the binary input data. Both outputs can be updated simultaneously or individually depending on the setting of the two mode of operation bits.

A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt with three different termination options.

The low power consumption and small packages of the DAC102S085 make it an excellent choice for use in battery operated equipment.

The DAC102S085 is one of a family of pin compatible DACs, including the 8-bit DAC084S085 and the 12-bit DAC122S085. The DAC102S085 operates over the extended industrial temperature range of –40°C to +105°C.

Features

- Guaranteed Monotonicity
- Low Power Operation
- Rail-to-Rail Voltage Output
- Power-on Reset to 0V
- Simultaneous Output Updating
- Wide power supply range (+2.7V to +5.5V)
- Industry's Smallest Package
- Power Down Modes

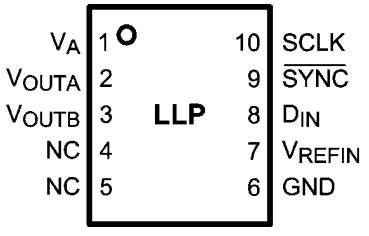
Key Specifications

■ Resolution	10 bits
■ INL	±2 LSB (max)
■ DNL	+0.35 / –0.25 LSB (max)
■ Settling Time	6 µs (max)
■ Zero Code Error	+15 mV (max)
■ Full-Scale Error	–0.75 %FS (max)
■ Supply Power	
■ — Normal	0.6 mW (3V) / 1.6 mW (5V) typ
— Power Down	0.3 µW (3V) / 0.8 µW (5V) typ

Applications

- Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage & Current Sources
- Programmable Attenuators

Pin Configuration



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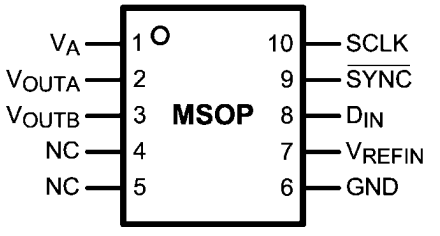

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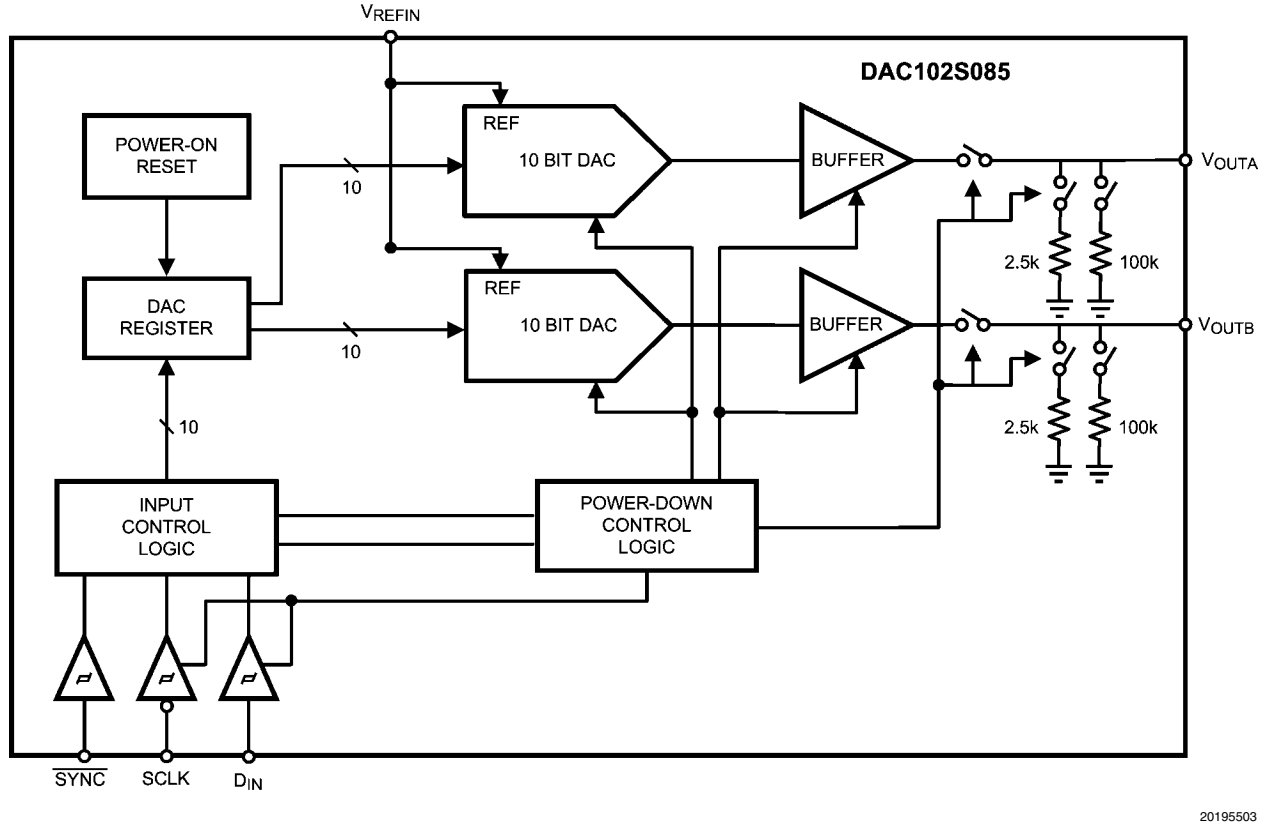
Ordering Information

Order Numbers	Temperature Range	Package	Top Mark
DAC102S085CISD	$-40°C \leq T_A \leq +105°C$	LLP	X75C
DAC102S085CISDX	$-40°C \leq T_A \leq +105°C$	LLP Tape-and-Reel	X75C
DAC102S085CIMM	$-40°C \leq T_A \leq +105°C$	MSOP	X74C
DAC102S085CIMMX	$-40°C \leq T_A \leq +105°C$	MSOP Tape-and-Reel	X74C
DAC102S085EVAL		Evaluation Board (MSOP)	

Block Diagram



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Pin Descriptions

LLP MSOP Pin No.	Symbol	Type	Description
1	V_A	Supply	Power supply input. Must be decoupled to GND.
2	V_{OUTA}	Analog Output	Channel A Analog Output Voltage.
3	V_{OUTB}	Analog Output	Channel B Analog Output Voltage.
4	NC		Not Connected
5	NC		Not Connected
6	GND	Ground	Ground reference for all on-chip circuitry.
7	V_{REFIN}	Analog Input	Unbuffered reference voltage shared by all channels. Must be decoupled to GND.
8	D_{IN}	Digital Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
9	$\overline{SYNC}$	Digital Input	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
10	SCLK	Digital Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
11	PAD (LLP only)	Ground	Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_A	6.5V
Voltage on any Input Pin	−0.3V to 6.5V
Input Current at Any Pin (Note 3)	10 mA
Package Input Current (Note 3)	20 mA
Power Consumption at T_A = 25°C	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2500V
Machine Model	250V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C

Operating Ratings (Notes 1, 2)

Operating Temperature Range	−40°C ≤ T_A ≤ +105°C
Supply Voltage, V_A	+2.7V to 5.5V
Reference Voltage, V_{REFIN}	+1.0V to V_A
Digital Input Voltage (Note 7)	0.0V to 5.5V
Output Load	0 to 1500 pF
SCLK Frequency	Up to 40 MHz

Package Thermal Resistances

Package	θ_{JA}
10-Lead MSOP	240°C/W
10-Lead LLP	250°C/W

Soldering process must comply with National Semiconductor's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 6)

Electrical Characteristics

The following specifications apply for V_A = +2.7V to +5.5V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 12 to 1011. **Boldface limits apply for T_{MIN} ≤ T_A ≤ T_{MAX}** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
STATIC PERFORMANCE					
	Resolution			**10**	Bits (min)
	Monotonicity			**10**	Bits (min)
INL	Integral Non-Linearity		±0.7	**±2**	LSB (max)
DNL	Differential Non-Linearity	V_A = 2.7V to 5.5V	+0.08	**+0.35**	LSB (max)
			−0.03	**−0.25**	LSB (min)
ZE	Zero Code Error	I_{OUT} = 0	+5	**+15**	mV (max)
FSE	Full-Scale Error	I_{OUT} = 0	−0.1	**−0.75**	%FSR (max)
GE	Gain Error	All ones Loaded to DAC register	−0.2	**−1.0**	%FSR
ZCED	Zero Code Error Drift		−20		µV/°C
TC GE	Gain Error Tempco	V_A = 3V	−0.7		ppm/°C
		V_A = 5V	−1.0		ppm/°C
OUTPUT CHARACTERISTICS					
	Output Voltage Range	(Note 10)		**0** **V_{REFIN}**	V (min) V (max)
I_{OZ}	High-Impedance Output Leakage Current (Note 10)			**±1**	µA (max)
ZCO	Zero Code Output	V_A = 3V, I_{OUT} = 200 µA	1.3		mV
		V_A = 3V, I_{OUT} = 1 mA	6.0		mV
		V_A = 5V, I_{OUT} = 200 µA	7.0		mV
		V_A = 5V, I_{OUT} = 1 mA	10.0		mV
FSO	Full Scale Output	V_A = 3V, I_{OUT} = 200 µA	2.984		V
		V_A = 3V, I_{OUT} = 1 mA	2.934		V
		V_A = 5V, I_{OUT} = 200 µA	4.989		V
		V_A = 5V, I_{OUT} = 1 mA	4.958		V
I_{OS}	Output Short Circuit Current (source)	V_A = 3V, V_{OUT} = 0V, Input Code = 3FFh	-56		mA
		V_A = 5V, V_{OUT} = 0V, Input Code = 3FFh	-69		mA

Symbol	Parameter	Conditions		Typical (Note 9)	Limits (Note 9)	Units (Limits)
I_{OS}	Output Short Circuit Current (sink)	V_A = 3V, V_{OUT} = 3V, Input Code = 000h		52		mA
		V_A = 5V, V_{OUT} = 5V, Input Code = 000h		75		mA
				75		mA
I_O	Continuous Output Current (Note 10)	Available on each DAC output			**11**	mA (max)
C_L	Maximum Load Capacitance	$R_L = \infty$		1500		pF
		R_L = 2kΩ		1500		pF
Z_{OUT}	DC Output Impedance			7.5		Ω
REFERENCE INPUT CHARACTERISTICS						
VREFIN	Input Range Minimum			0.2	**1.0**	V (min)
	Input Range Maximum				**V_A**	V (max)
	Input Impedance			60		kΩ
LOGIC INPUT CHARACTERISTICS						
I_{IN}	Input Current (Note 10)				**±1**	µA (max)
V_{IL}	Input Low Voltage (Note 10)	V_A = 3V		0.9	**0.6**	V (max)
		V_A = 5V		1.5	**0.8**	V (max)
V_{IH}	Input High Voltage (Note 10)	V_A = 3V		1.4	**2.1**	V (min)
		V_A = 5V		2.1	**2.4**	V (min)
C_{IN}	Input Capacitance (Note 10)				**3**	pF (max)
POWER REQUIREMENTS						
V_A	Supply Voltage Minimum				**2.7**	V (min)
	Supply Voltage Maximum				**5.5**	V (max)
I_N	Normal Supply Current (output unloaded)	f_{SCLK} = 30 MHz	V_A = 2.7V to 3.6V	210	**270**	µA (max)
			V_A = 4.5V to 5.5V	320	**410**	µA (max)
		f_{SCLK} = 0	V_A = 2.7V to 3.6V	190		µA
			V_A = 4.5V to 5.5V	290		µA
I_{PD}	Power Down Supply Current (output unloaded, SYNC = DIN = 0V after PD mode loaded)	All PD Modes, (Note 10)	V_A = 2.7V to 3.6V	0.10	**1.0**	µA (max)
			V_A = 4.5V to 5.5V	0.15	**1.0**	µA (max)
P_N	Normal Supply Power (output unloaded)	f_{SCLK} = 30 MHz	V_A = 2.7V to 3.6V	0.6	**1.0**	mW (max)
			V_A = 4.5V to 5.5V	1.6	**2.3**	mW (max)
		f_{SCLK} = 0	V_A = 2.7V to 3.6V	0.6		mW
			V_A = 4.5V to 5.5V	1.5		mW
P_{PD}	Power Down Supply Current (output unloaded, SYNC = DIN = 0V after PD mode loaded)	All PD Modes, (Note 10)	V_A = 2.7V to 3.6V	0.3	**3.6**	µW (max)
			V_A = 4.5V to 5.5V	0.8	**5.5**	µW (max)

A.C. and Timing Characteristics

Values shown in this table are design targets and are subject to change before product release.

The following specifications apply for V_A = +2.7V to +5.5V, $V_{REFIN} = V_A$, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 12 to 1011. **Boldface limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$** and all other limits are at T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conductions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
f_{SCLK}	SCLK Frequency		40	**30**	MHz (max)
t_s	Output Voltage Settling Time (Note 10)	100h to 300h code change R_L = 2 kΩ, C_L = 200 pF	4.5	**6**	µs (max)
SR	Output Slew Rate		1		V/µs
	Glitch Impulse	Code change from 200h to 1FFh	12		nV-sec
	Digital Feedthrough		0.5		nV-sec
	Digital Crosstalk		1		nV-sec
	DAC-to-DAC Crosstalk		3		nV-sec
	Multiplying Bandwidth	V_{REFIN} = 2.5V ± 0.1Vpp	160		kHz
	Total Harmonic Distortion	V_{REFIN} = 2.5V ± 1.0Vpp input frequency = 10kHz	70		dB
t_{WU}	Wake-Up Time	V_A = 3V	6		µsec
		V_A = 5V	39		µsec
$1/f_{SCLK}$	SCLK Cycle Time		25	**33**	ns (min)
t_{CH}	SCLK High time		7	**10**	ns (min)
t_{CL}	SCLK Low Time		7	**10**	ns (min)
t_{SS}	$\overline{SYNC}$ Set-up Time prior to SCLK Falling Edge		4	**10**	ns (min)
t_{DS}	Data Set-Up Time prior to SCLK Falling Edge		1.5	**3.5**	ns (min)
t_{DH}	Data Hold Time after SCLK Falling Edge		1.5	**3.5**	ns (min)
t_{CFSR}	SCLK fall prior to rise of $\overline{SYNC}$		0	**3**	ns (min)
t_{SYNC}	$\overline{SYNC}$ High Time		6	**10**	ns (min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

Note 2: All voltages are measured with respect to GND = 0V, unless otherwise specified.

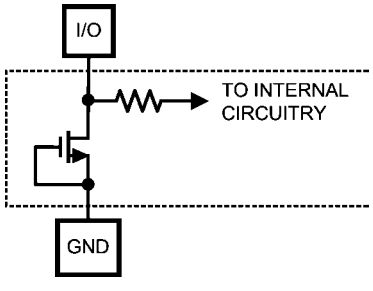
Note 3: When the input voltage at any pin exceeds 5.5V or is less than GND, the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed).

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Note 6: Reflow temperature profiles are different for lead-free packages.

Note 7: The inputs are protected as shown below. Input voltage magnitudes up to 5.5V, regardless of V_A, will not cause errors in the conversion result. For example, if V_A is 3V, the digital input pins can be driven with a 5V logic device.



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Note 8: To guarantee accuracy, it is required that V_A and V_{REFIN} be well bypassed.

Note 9: Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: This parameter is guaranteed by design and/or characterization and is not tested in production.

Specification Definitions

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB, which is V_{REF} / 1024 = V_A / 1024.

DAC-to-DAC CROSSTALK is the glitch impulse transferred to a DAC output in response to a full-scale change in the output of another DAC.

DIGITAL CROSSTALK is the glitch impulse transferred to a DAC output at mid-scale in response to a full-scale change in the input register of another DAC.

DIGITAL FEEDTHROUGH is a measure of the energy injected into the analog output of the DAC from the digital inputs when the DAC outputs are not updated. It is measured with a full-scale code change on the data bus.

FULL-SCALE ERROR is the difference between the actual output voltage with a full scale code (3FFh) loaded into the DAC and the value of V_A x 1023 / 1024.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Zero and Full-Scale Errors as GE = FSE - ZE, where GE is Gain error, FSE is Full-Scale Error and ZE is Zero Error.

GLITCH IMPULSE is the energy injected into the analog output when the input code to the DAC register changes. It is specified as the area of the glitch in nanovolt-seconds.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point method is used. INL for this product is specified over a limited range, per the Electrical Tables.

LEAST SIGNIFICANT BIT (LSB) is the bit that has the smallest value or weight of all bits in a word. This value is

$$LSB = V_{REF} / 2^n$$

where V_{REF} is the supply voltage for this product, and "n" is the DAC resolution in bits, which is 10 for the DAC102S085.

MAXIMUM LOAD CAPACITANCE is the maximum capacitance that can be driven by the DAC with output stability maintained.

MONOTONICITY is the condition of being monotonic, where the DAC has an output that never decreases when the input code increases.

MOST SIGNIFICANT BIT (MSB) is the bit that has the largest value or weight of all bits in a word. Its value is 1/2 of V_A.

MULTIPLYING BANDWIDTH is the frequency at which the output amplitude falls 3dB below the input sine wave on V_{REFIN} with a full-scale code loaded into the DAC.

POWER EFFICIENCY is the ratio of the output current to the total supply current. The output current comes from the power supply. The difference between the supply and output currents is the power consumed by the device without a load.

SETTLING TIME is the time for the output to settle to within 1/2 LSB of the final value after the input code is updated.

TOTAL HARMONIC DISTORTION (THD) is the measure of the harmonics present at the output of the DACs with an ideal sine wave applied to V_{REFIN}. THD is measured in dB.

WAKE-UP TIME is the time for the output to exit power-down mode. This is the time from the falling edge of the 16th SCLK pulse to when the output voltage deviates from the power-down voltage of 0V.

ZERO CODE ERROR is the output error, or voltage, present at the DAC output after a code of 000h has been entered.

Transfer Characteristic

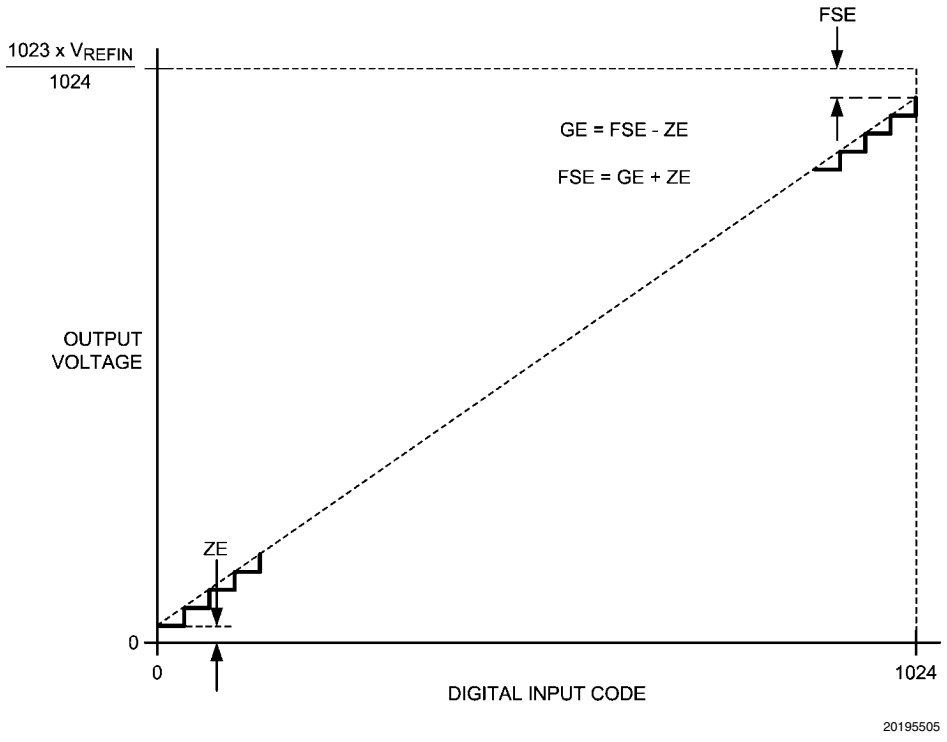


FIGURE 1. Input / Output Transfer Characteristic

Timing Diagrams

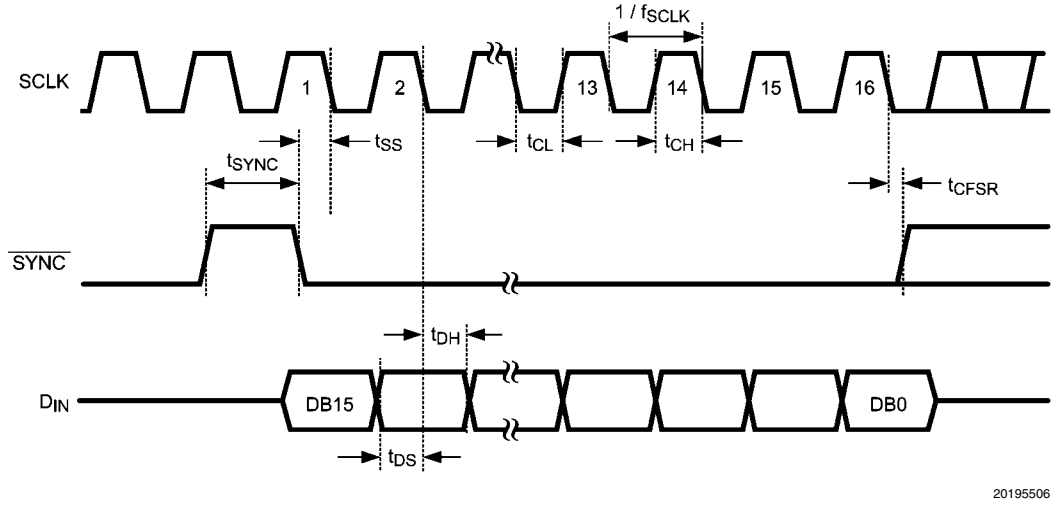
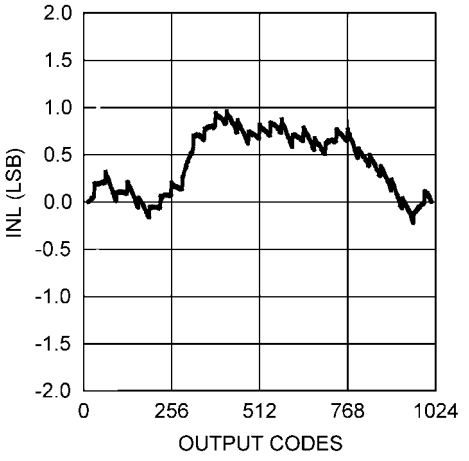


FIGURE 2. Serial Timing Diagram

Typical Performance Characteristics

$V_{REF} = V_A$, f_{SCLK} = 30 MHz, T_A = 25C, Input Code Range 12 to 1011, unless otherwise stated

INL at V_A = 3.0V



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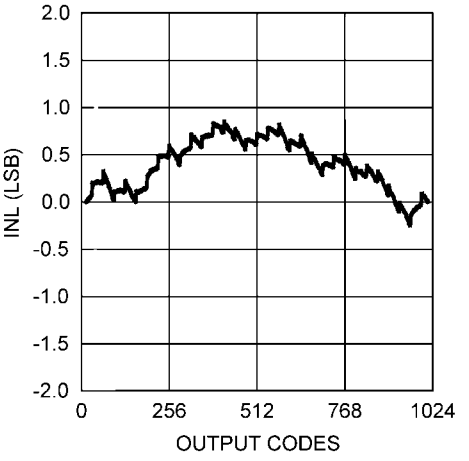
INL at V_A = 5.0V



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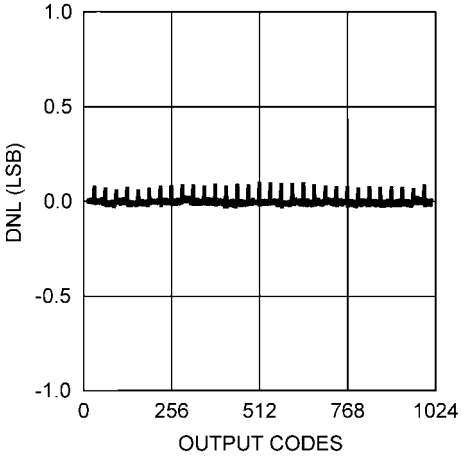
DNL at V_A = 3.0V



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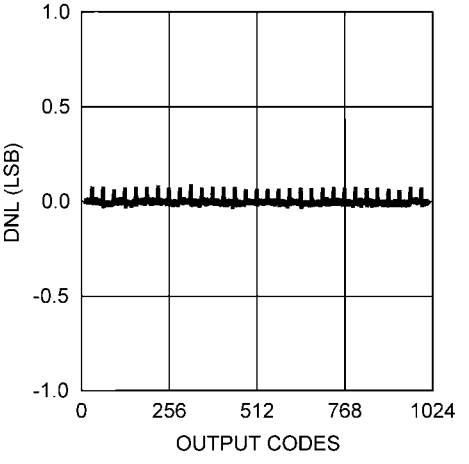
DNL at V_A = 5.0V



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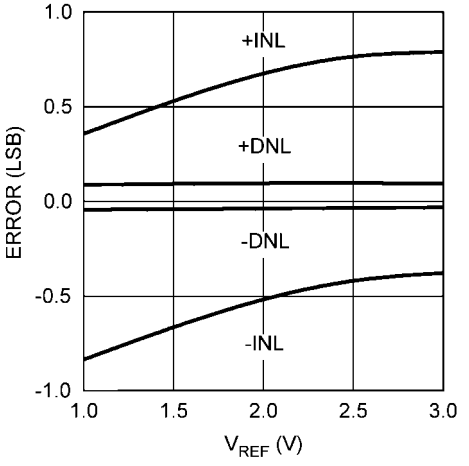
INL/DNL vs V_{REFIN} at V_A = 3.0V



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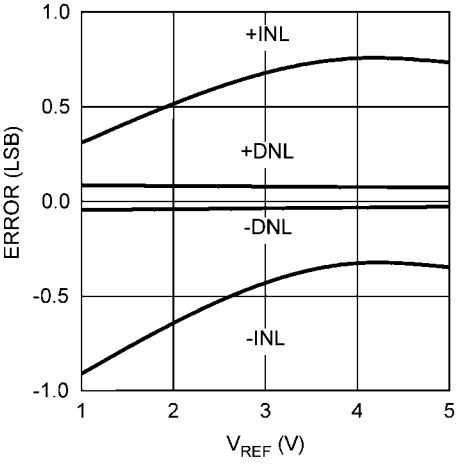
INL/DNL vs V_{REFIN} at V_A = 5.0V



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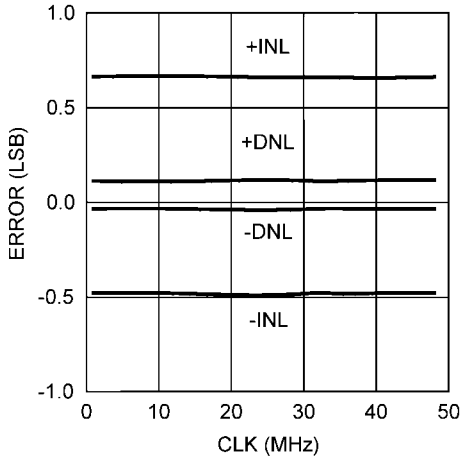
INL/DNL vs f_{SCLK} at V_A = 2.7V



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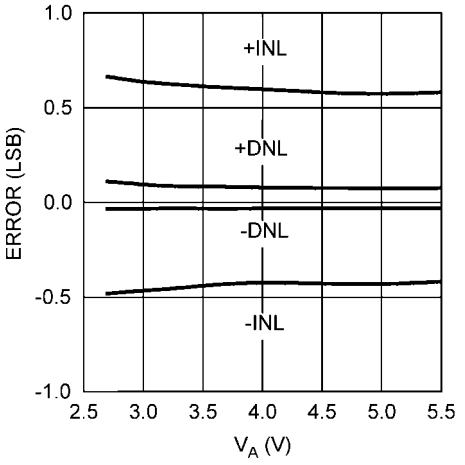
INL/DNL vs V_A



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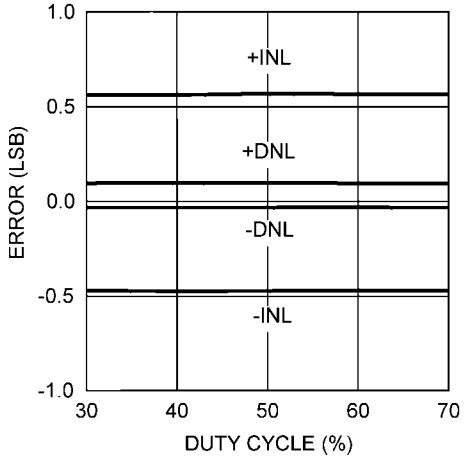
INL/DNL vs Clock Duty Cycle at V_A = 3.0V



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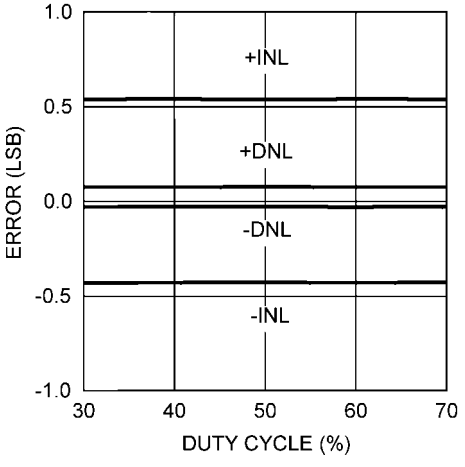
INL/DNL vs Clock Duty Cycle at V_A = 5.0V



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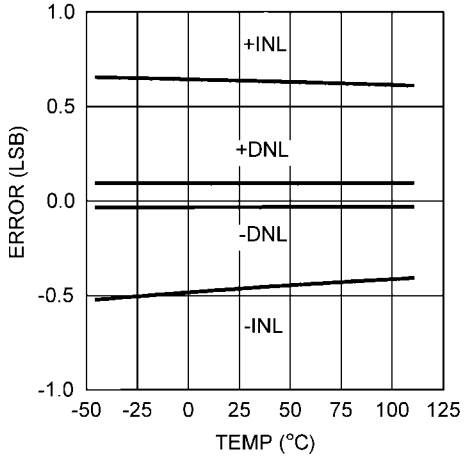
INL/DNL vs Temperature at V_A = 3.0V



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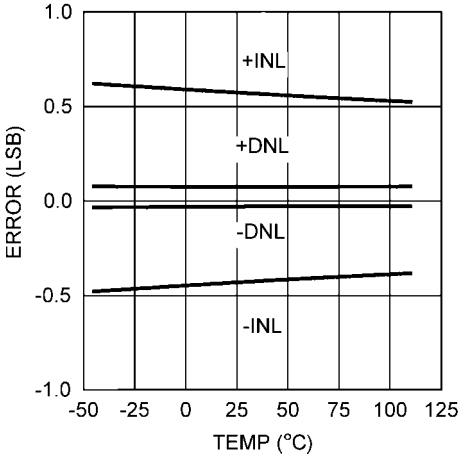
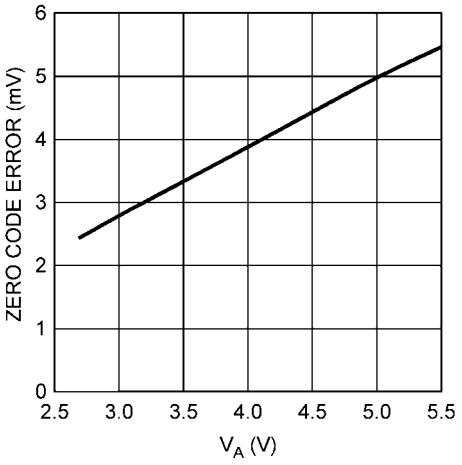
INL/DNL vs Temperature at V_A = 5.0V



20195527

Zero Code Error vs. V_A



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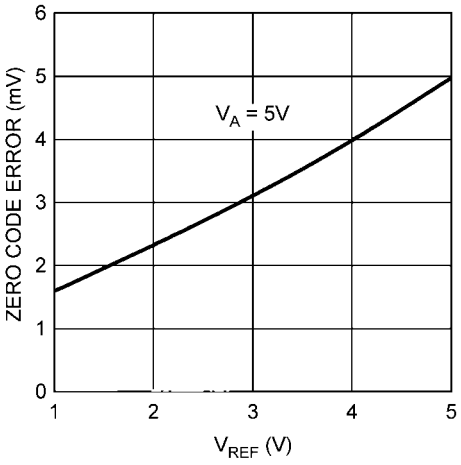
Zero Code Error vs. V_{REFIN}



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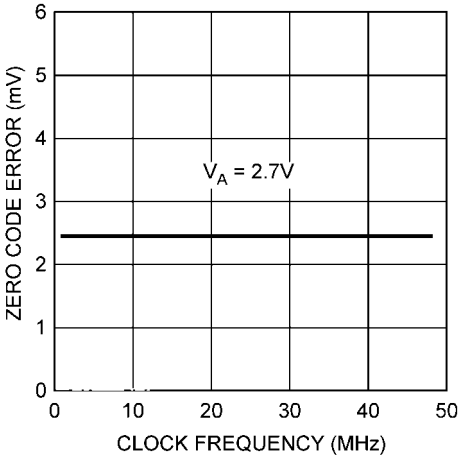
Zero Code Error vs. f_{SCLK}



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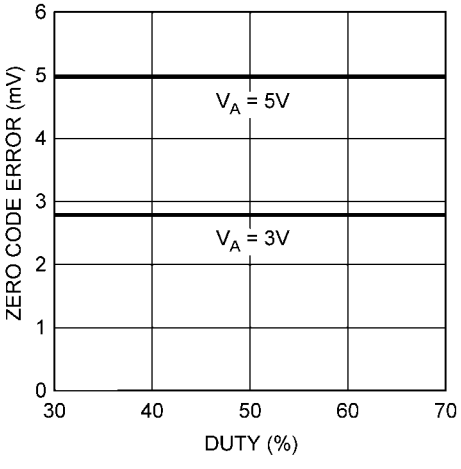
Zero Code Error vs. Clock Duty Cycle



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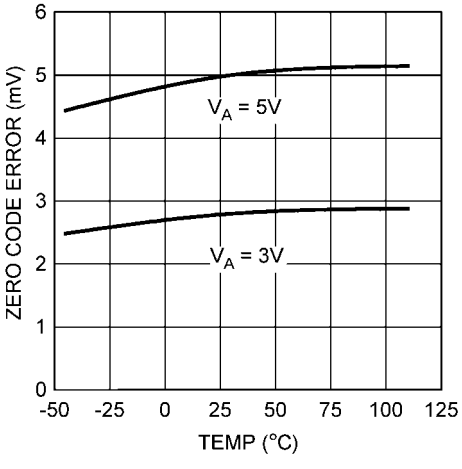
Zero Code Error vs. Temperature



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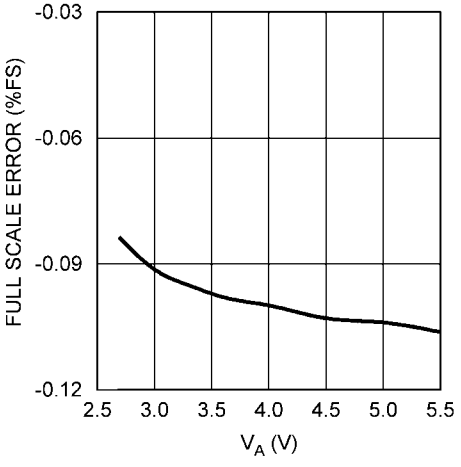
Full-Scale Error vs. V_A



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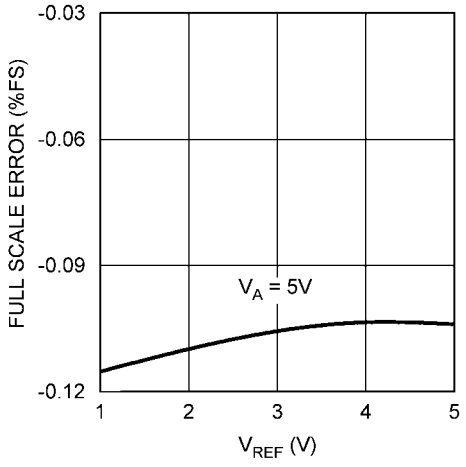
Full-Scale Error vs. V_{REFIN}



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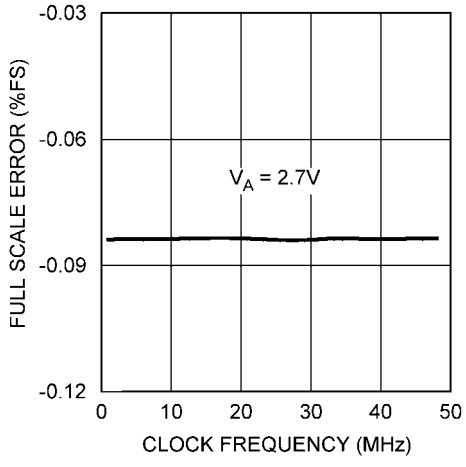
Full-Scale Error vs. f_{SCLK}



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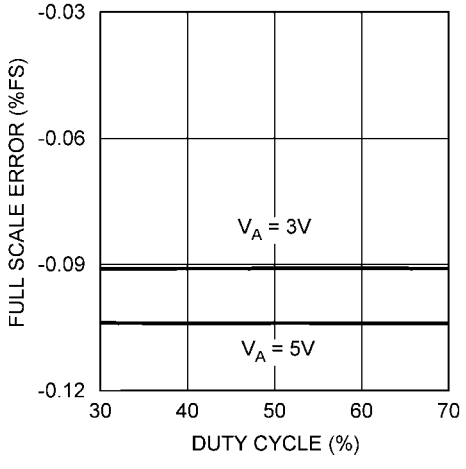
Full-Scale Error vs. Clock Duty Cycle



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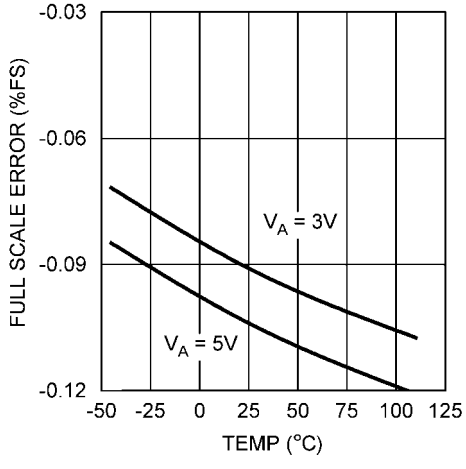
Full-Scale Error vs. Temperature



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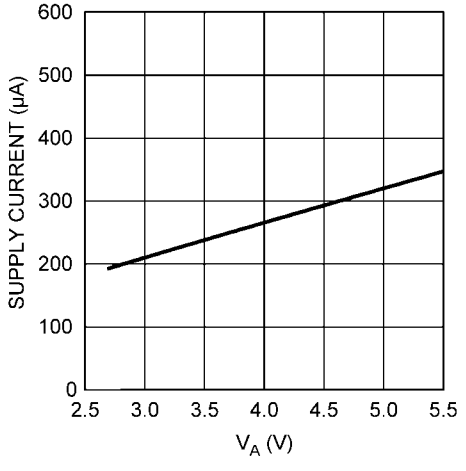
Supply Current vs. V_A



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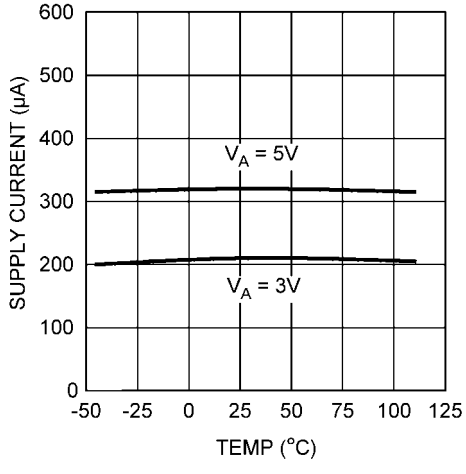
Supply Current vs. Temperature



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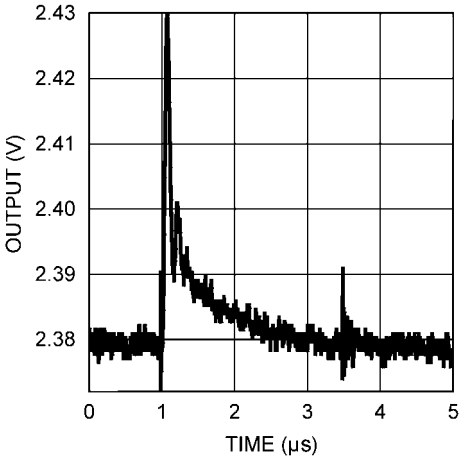
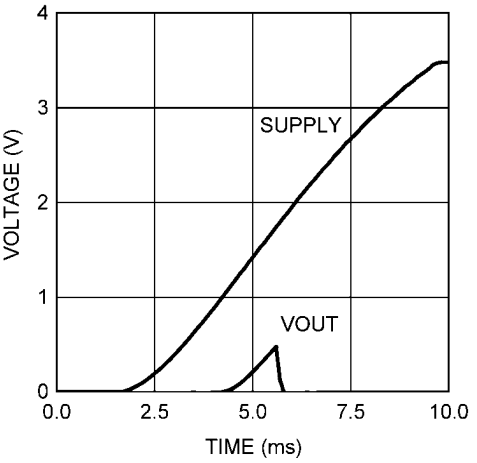
5V Glitch Response



20195546

Power-On Reset



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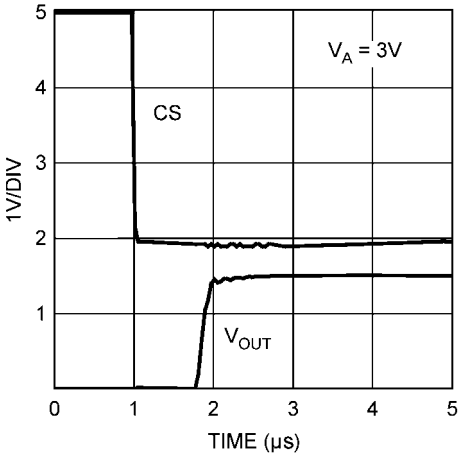
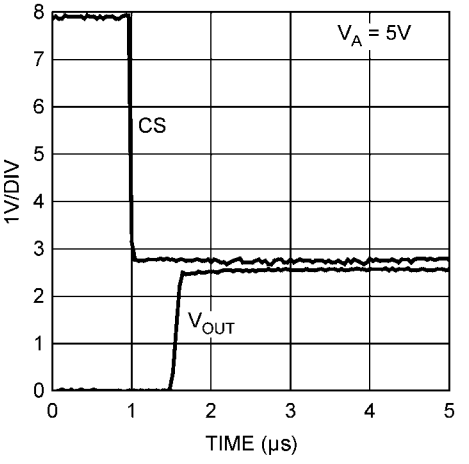
3V Wake-Up Time



20195548

5V Wake-Up Time



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1.0 Functional Description

1.1 DAC SECTION

The DAC102S085 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer. The reference voltage is externally applied at V_{REFIN} and is shared by both DACs.

For simplicity, a single resistor string is shown in *Figure 3*. This string consists of 1024 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{OUTA,B} = V_{REFIN} \times (D / 1024)$$

where *D* is the decimal equivalent of the binary code that is loaded into the DAC register. D can take on any value between 0 and 1023. This configuration guarantees that the DAC is monotonic.

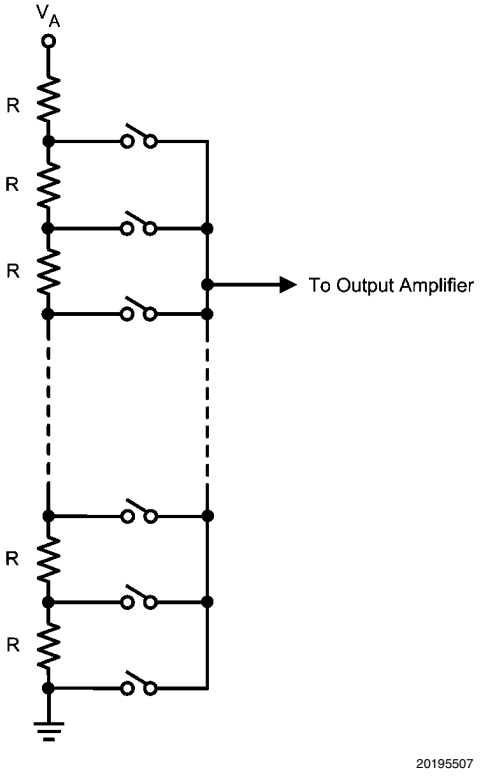


FIGURE 3. DAC Resistor String

1.2 OUTPUT AMPLIFIERS

The output amplifiers are rail-to-rail, providing an output voltage range of 0V to V_A when the reference is V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, there is only a loss in linearity in the lowest codes. The output capabilities of the amplifier are described in the Electrical Tables.

The output amplifiers are capable of driving a load of 2 kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in the Electrical Characterisics Table.

1.3 RERENCE VOLTAGE

The DAC102S085 uses a single external reference that is shared by both channels. The reference pin, V_{REFIN}, is not buffered and has an input impedance of 60 kΩ. It is recommended that V_{REFIN} be driven by a voltage source with low output impedance. The reference voltage range is 1.0V to V_A, providing the widest possible output dynamic range.

1.4 SERIAL INTERFACE

The three-wire interface is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs and operates at clock rates up to 40 MHz. See the Timing Diagram for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. Once $\overline{SYNC}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid misclocking data into the shift register, it is critical that $\overline{SYNC}$ not be brought low simultaneously with a falling edge of SCLK (see Serial Timing Diagram, *Figure 2*). On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the DAC channel address, mode of operation and/or register contents) is executed. At this point the $\overline{SYNC}$ line may be kept low or brought high. Any data and clock pusles after the 16th falling clock edge will be ignored. In either case, $\overline{SYNC}$ must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of $\overline{SYNC}$.

Since the $\overline{SYNC}$ and D_{IN} buffers draw more current when they are high, they should be idled low between write sequences to minimize power consumption.

1.5 INPUT SHIFT REGISTER

The input shift register, *Figure 4*, has sixteen bits. The first bit must be set to "0" and the second bit is an address bit. The address bit determines whether the register data is for DAC A or DAC B. This bit is followed by two bits that determine the mode of operation (writing to a DAC register without updating the outputs of both DACs, writing to a DAC register and updating the outputs of both DACs, writing to the register of both DACs and updating their outputs, or powering down both outputs). The final twelve bits of the shift register are the data bits. The data format is straight binary (MSB first, LSB last), with all 0's corresponding to an output of 0V and all 1's corresponding to a full-scale output of V_{REFIN} - 1 LSB. The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See Timing Diagram, *Figure 2*.

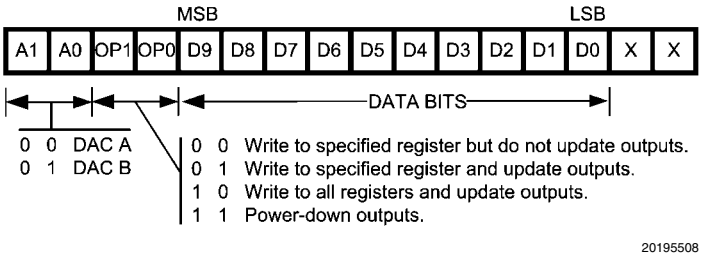


FIGURE 4. Input Register Contents

Normally, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, the data transfer to the shift register is aborted and the write sequence is invalid. Under this condition, the DAC register is not updated and there is no change in the mode of operation or in the DAC output voltages.

1.6 POWER-ON RESET

The power-on reset circuit controls the output voltages of both DACs during power-up. Upon application of power, the DAC registers are filled with zeros and the output voltages are 0V. The outputs remain at 0V until a valid write sequence is made to the DAC.

1.7 POWER-DOWN MODES

The DAC102S085 has four power-down modes, two of which are identical. In power-down mode, the supply current drops to 20 µA at 3V and 30 µA at 5V. The DAC102S085 is set in power-down mode by setting OP1 and OP0 to 11. Since this mode powers down both DACs, the first two bits of the shift register are used to select different output terminations for the DAC outputs. Setting A1 and A0 to 00 or 11 causes the outputs to be tri-stated (a high impedance state). While setting A1 and A0 to 01 or 10 causes the outputs to be terminated by 2.5 kΩ or 100 kΩ to ground respectively (see *Table 1*).

TABLE 1. Power-Down Modes

A1	A0	OP1	OP0	Operating Mode
0	0	1	1	High-Z outputs
0	1	1	1	2.5 kΩ to GND
1	0	1	1	100 kΩ to GND
1	1	1	1	High-Z outputs

The bias generator, output amplifiers, resistor strings, and other linear circuitry are all shut down in any of the power-down modes. However, the contents of the DAC registers are unaffected when in power-down. Each DAC register maintains its value prior to the DAC102S085 being powered down unless it is changed during the write sequence which instructed it to recover from power down. Minimum power consumption is achieved in the power-down mode with $\overline{\text{SYNC}}$ and D_{IN} idled low and SCLK disabled. The time to exit power-down (Wake-Up Time) is typically t_{WU} µsec as stated in the A.C. and Timing Characteristics table.

2.0 Applications Information

2.1 USING REFERENCES AS POWER SUPPLIES

While the simplicity of the DAC102S085 implies ease of use, it is important to recognize that the path from the reference input (V_{REFIN}) to the VOUTs will have essentially zero Power Supply Rejection Ratio (PSRR). Therefore, it is necessary to provide a noise-free supply voltage to V_{REFIN}. In order to utilize the full dynamic range of the DAC102S085, the supply pin (V_A) and V_{REFIN} can be connected together and share the same supply voltage. Since the DAC102S085 consumes very little power, a reference source may be used as the reference input and/or the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used. Listed below are a few reference and power supply options for the DAC102S085.

2.1.1 LM4130

The LM4130, with its 0.05% accuracy over temperature, is a good choice as a reference source for the DAC102S085. The 4.096V version is useful if a 0 to 4.095V output range is desirable or acceptable. Bypassing the LM4130 VIN pin with a 0.1µF capacitor and the VOUT pin with a 2.2µF capacitor will improve stability and reduce output noise. The LM4130 comes in a space-saving 5-pin SOT23.

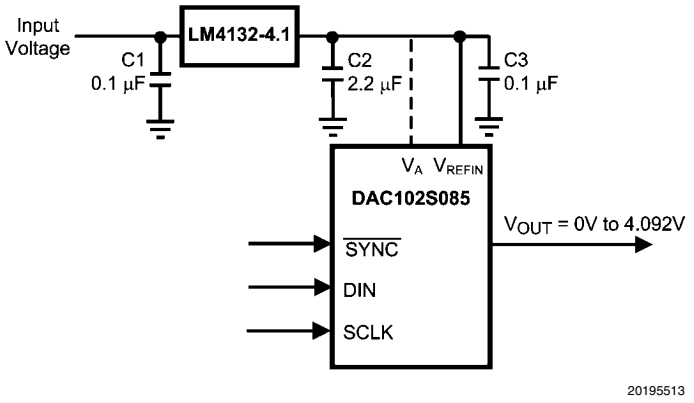


FIGURE 5. The LM4130 as a power supply

2.1.2 LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a reference for the DAC102S085. It is available in 4.096V and 5V versions and comes in a space-saving 3-pin SOT23.

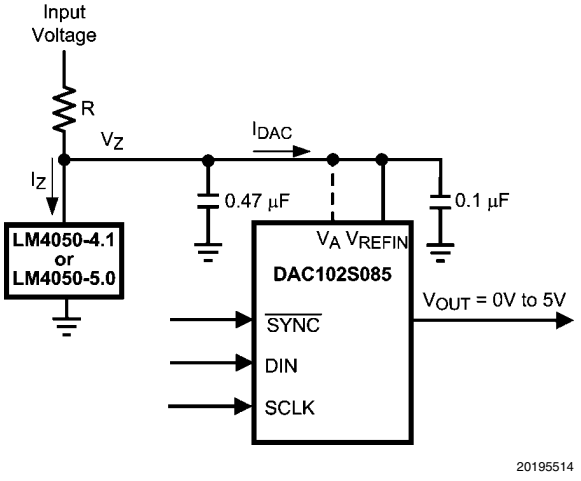


FIGURE 6. The LM4050 as a power supply

The minimum resistor value in the circuit of *Figure 6* must be chosen such that the maximum current through the LM4050 does not exceed its 15 mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, and the DAC102S085 drawing zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC102S085 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC102S085 draws its maximum current. These conditions can be summarized as

$$R(min) = (V_{IN}(max) - V_Z(min)) / I_Z(max)$$

and

$$R(max) = (V_{IN}(min) - V_Z(max)) / ((I_{DAC}(max) + I_Z(min))$$

where $V_Z(min)$ and $V_Z(max)$ are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature, $I_Z(max)$ is the maximum allowable current through the LM4050, $I_Z(min)$ is the minimum current required by the LM4050 for proper regulation, and $I_{DAC}(max)$ is the maximum DAC102S085 supply current.

2.1.3 LP3985

The LP3985 is a low noise, ultra low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC102S085. It comes in 3.0V, 3.3V and 5V versions, among others, and sports a low 30 µV noise specification at low frequencies. Since low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT23 and 5-bump micro SMD packages.

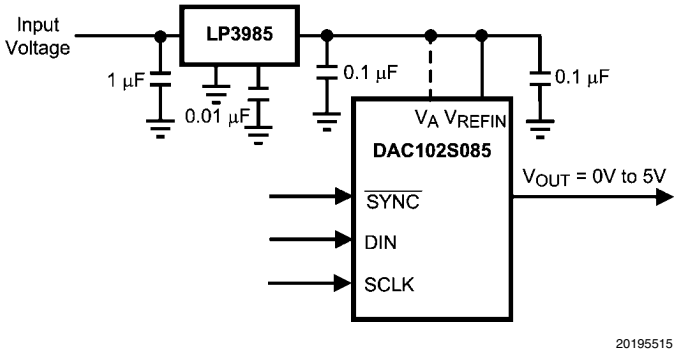


FIGURE 7. Using the LP3985 regulator

An input capacitance of 1.0µF without any ESR requirement is required at the LP3985 input, while a 1.0µF ceramic capacitor with an ESR requirement of 5mΩ to 500mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

2.1.4 LP2980

The LP2980 is an ultra low dropout regulator with a 0.5% or 1.0% accuracy over temperature, depending upon grade. It is available in 3.0V, 3.3V and 5V versions, among others.

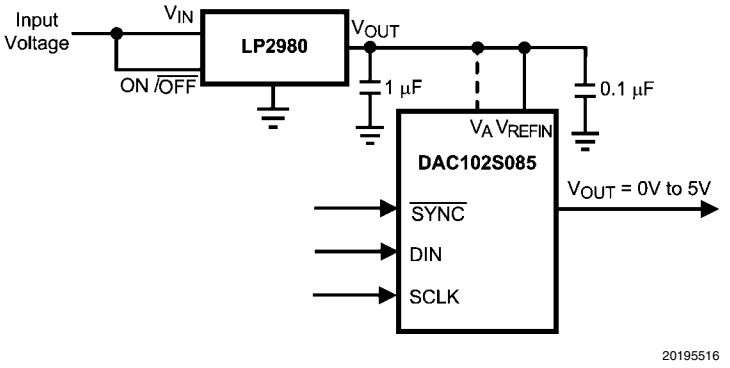


FIGURE 8. Using the LP2980 regulator

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1.0µF over temperature, but values of 2.2µF or more will provide even better performance. The ESR of this capacitor should be within the range specified in the LP2980 data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

2.2 BIPOLAR OPERATION

The DAC102S085 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in *Figure 9*. This circuit will provide an output voltage range of ±5 Volts. A rail-to-rail amplifier should be used if the amplifier supplies are limited to ±5V.

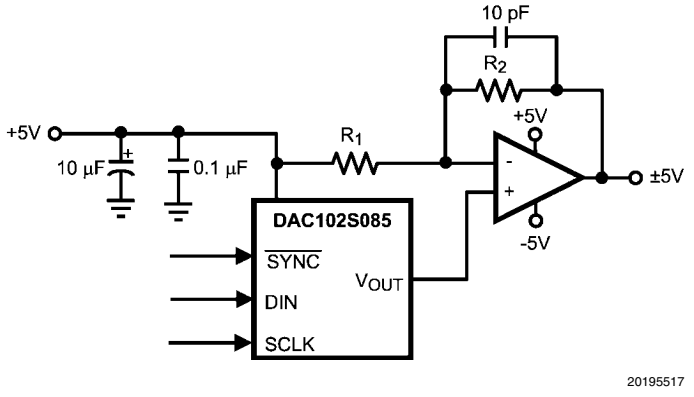


FIGURE 9. Bipolar Operation

The output voltage of this circuit for any code is found to be

$$V_O = (V_A \times (D / 1024) \times ((R1 + R2) / R1) - V_A \times R2 / R1)$$

where D is the input code in decimal form. With V_A = 5V and R1 = R2,

$$V_O = (10 \times D / 1024) - 5V$$

A list of rail-to-rail amplifiers suitable for this application are indicated in *Table 2*.

TABLE 2. Some Rail-to-Rail Amplifiers

AMP	PKGS	Typ V_{OS}	Typ I_{SUPPLY}
LMC7111	DIP-8 SOT23-5	0.9 mV	25 µA
LM7301	SO-8 SOT23-5	0.03 mV	620 µA
LM8261	SOT23-5	0.7 mV	1 mA

2.3 DSP/MICROPROCESSOR INTERFACING

Interfacing the DAC102S085 to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

2.3.1 ADSP-2101/ADSP2103 Interfacing

Figure 10 shows a serial interface between the DAC102S085 and the ADSP-2101/ADSP2103. The DSP should be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and should be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the Tx register after the SPORT mode has been enabled.

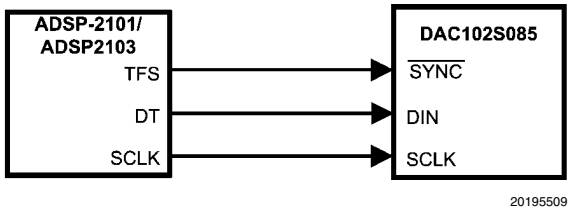


FIGURE 10. ADSP-2101/2103 Interface

2.3.2 80C51/80L51 Interface

A serial interface between the DAC102S085 and the 80C51/80L51 microcontroller is shown in *Figure 11*. The $\overline{\text{SYNC}}$ signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is transmitted to the DAC102S085. Since the 80C51/80L51 transmits 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51/80L51 transmit routine must recognize that the 80C51/80L51 transmits data with the LSB first while the DAC102S085 requires data with the MSB first.

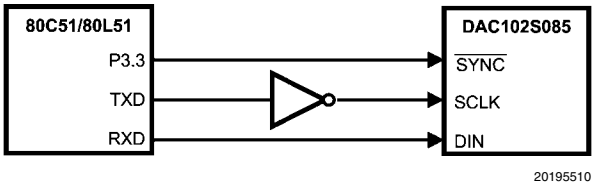


FIGURE 11. 80C51/80L51 Interface

2.3.3 68HC11 Interface

A serial interface between the DAC102S085 and the 68HC11 microcontroller is shown in *Figure 12*. The $\overline{\text{SYNC}}$ line of the DAC102S085 is driven from a port line (PC7 in the figure), similar to the 80C51/80L51.

The 68HC11 should be configured with its CPOL bit as a zero and its CPHA bit as a one. This configuration causes data on the MOSI output to be valid on the falling edge of SCLK. PC7 is taken low to transmit data to the DAC. The 68HC11 transmits data in 8-bit bytes with eight falling clock edges. Data is transmitted with the MSB first. PC7 must remain low after the first eight bits are transferred. A second write cycle is initiated to transmit the second byte of data to the DAC, after which PC7 should be raised to end the write sequence.

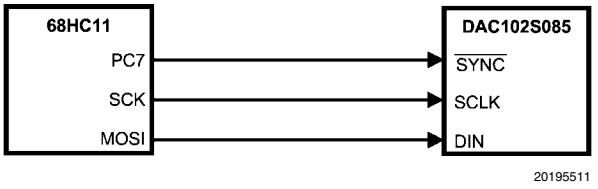


FIGURE 12. 68HC11 Interface

2.3.4 Microwire Interface

Figure 13 shows an interface between a Microwire compatible device and the DAC102S085. Data is clocked out on the rising edges of the SK signal. As a result, the SK of the Microwire device needs to be inverted before driving the SCLK of the DAC102S085.

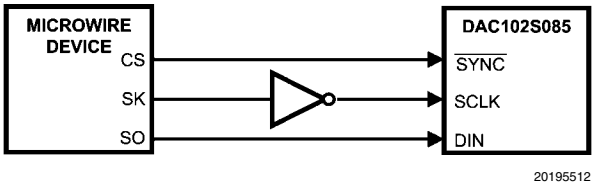


FIGURE 13. Microwire Interface

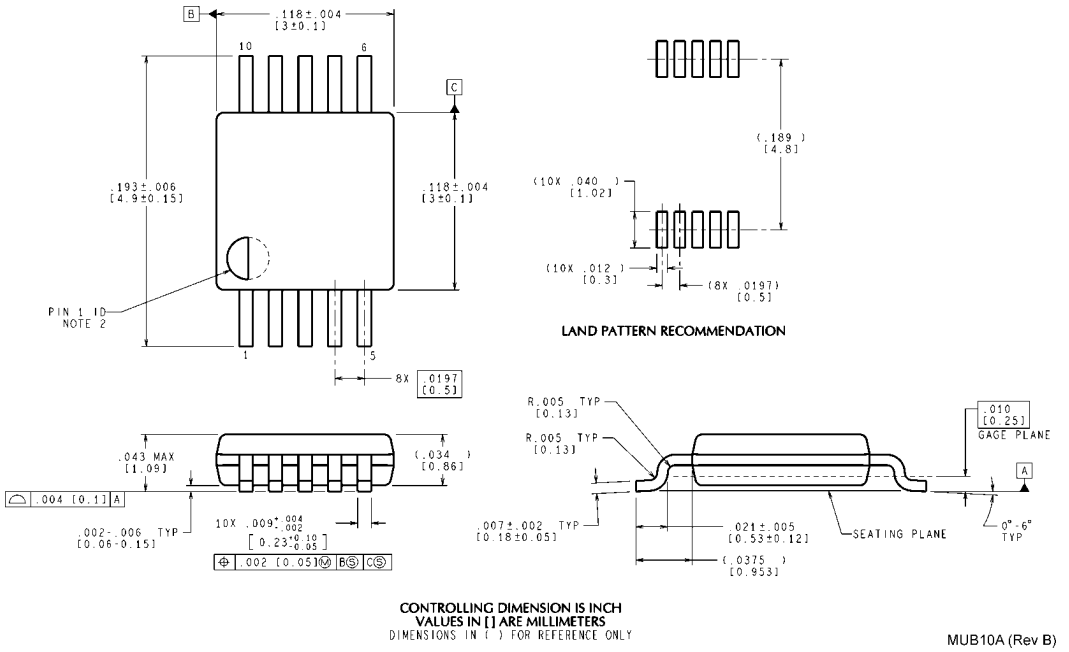
2.4 LAYOUT, GROUNDING, AND BYPASSING

For best accuracy and minimum noise, the printed circuit board containing the DAC102S085 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located in the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will utilize a "fencing" technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC102S085. Special care is required to guarantee that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

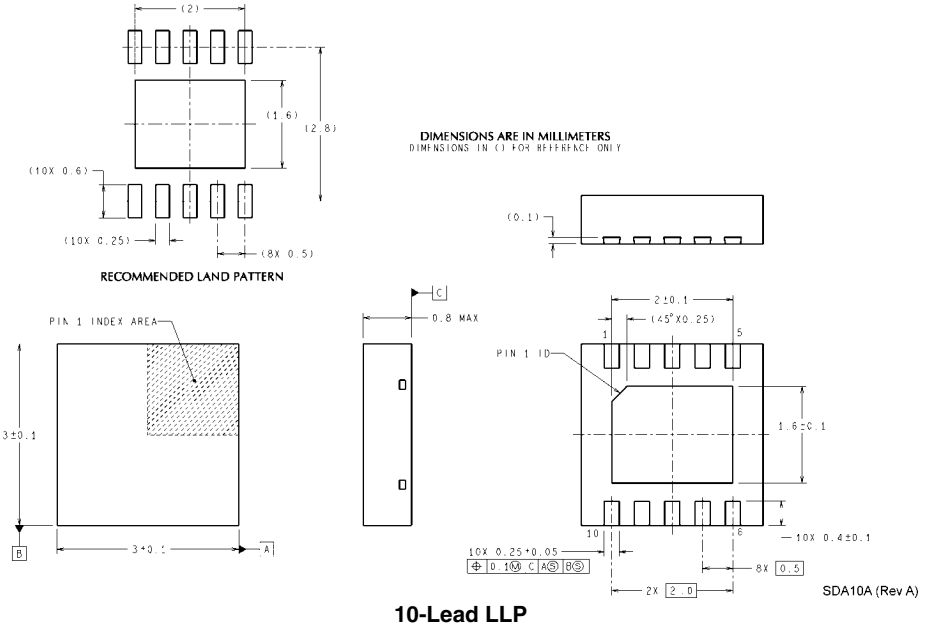
The DAC102S085 power supply should be bypassed with a 10µF and a 0.1µF capacitor as close as possible to the device with the 0.1µF right at the device supply pin. The 10µF capacitor should be a tantalum type and the 0.1µF capacitor should be a low ESL, low ESR type. The power supply for the DAC102S085 should only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines should have controlled impedances.

Physical Dimensions inches (millimeters) unless otherwise noted



10-Lead MSOP
Order Numbers DAC102S085CIMM
NS Package Number MUB10A



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