

CMOS QUAD LOW-TO-HIGH VOLTAGE SHIFTER

Check for Samples: [CD40109B-Q1](#)

FEATURES

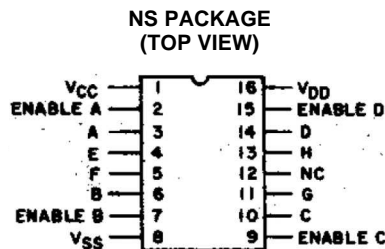
- Qualified for Automotive Applications
- Independent of Power Supply Sequence Considerations
 - V_{CC} Can Exceed V_{DD}
 - Input Signals can Exceed Both V_{CC} and V_{DD}
- Up and Down Level-Shifting Capability
- Three-State Outputs With Separate Enable Controls
- Standardized Symmetrical Output Characteristics
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current:
 - 1 μ A at 18 V Over Full Package-Temperature Range
 - 100 nA at 18 V and 25°C
- Noise Margin (Full Package-Temperature Range):
 - 1 V at $V_{CC} = 5$ V, $V_{DD} = 10$ V
 - 2 V at $V_{CC} = 10$ V, $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V Parametric Ratings
- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard specifications for

Description of 'B' Series CMOS Devices"

- Latch-Up Performance Meets 50 mA per JESD 78, Class I

APPLICATIONS

- High-or-Low Level-Shifting With Three-State Outputs for Unidirectional or Bidirectional Bussing
- Isolation of Logic Subsystem Using Separate Power Supplies from Supply Sequencing, Supply Loss, and Supply Regulation Considerations



DESCRIPTION

CD40109B contains four low-to-high-voltage level-shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 = V_{CC} and logical 0 = V_{SS} to a high-voltage output signal (E, F, G, H) with logical 1 = V_{DD} and logical 0 = V_{SS} .

The RCA-CD40109, unlike other low-to-high level-shifting circuits, does not require the presence of the high-voltage supply (V_{DD}) before the application of either the low-voltage supply (V_{CC}) or the input signals. There are no restrictions on the sequence of application of V_{DD} , V_{CC} , or the input signals. In addition, with one exception there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings, provided that the input signal swings between V_{SS} and at least 0.7 V_{CC} ; V_{CC} may exceed V_{DD} , and input signals may exceed V_{CC} and V_{DD} . When operated in the mode $V_{CC} > V_{DD}$, the CD40109 will operate as a high-to-low level-shifter.

The CD40109 also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

ORDERING INFORMATION⁽¹⁾

| T_A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 125°C | SOIC – NS | Reel of 2000 | CD40109BQNSRQ1 | CD40109BQ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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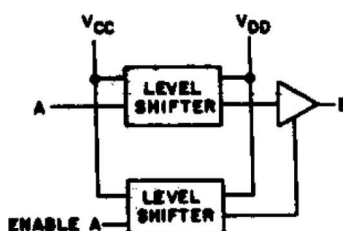
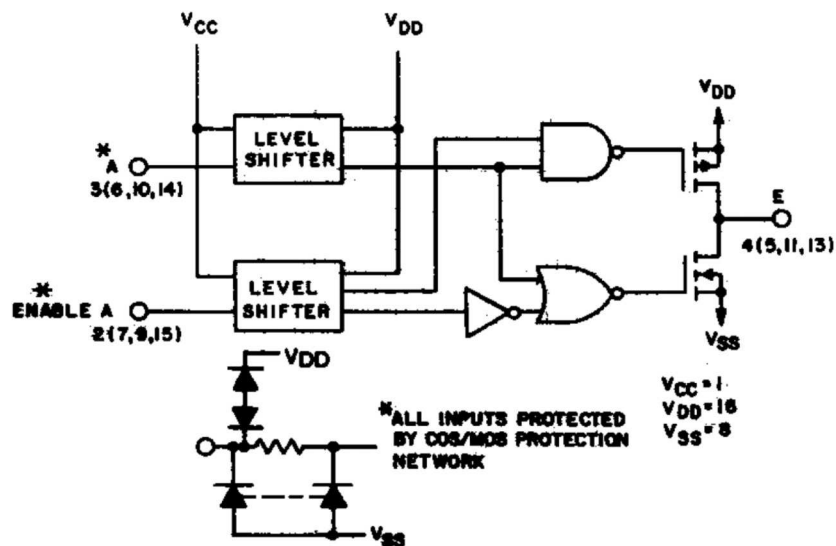
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TRUTH TABLE⁽¹⁾

| INPUTS | | OUTPUTS |
|------------|----------------------|------------|
| A, B, C, D | ENABLE A, B, C, D | E, F, G, H |
| 0 | 1 | 0 |
| 1 | 1 | 1 |
| X | 0 | Z |

(1) 0 = V_{SS} , 1 = V_{CC} at inputs and V_{DD} at outputs, X = Don't care, Z = High impedance

Functional Diagram (1 of 4 Units)**Logic Diagram (1 of 4 Units)**

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | VALUE | UNIT |
|------------------|--|---|--|------|
| V _{DD} | DC supply voltage range | Voltages referenced to V _{SS} terminal | –0.5 to +20 | V |
| | Output voltage range | All outputs | –0.5 to V _{DD} + 0.5 | V |
| | DC input current | Any one input | ±10 | mA |
| P _D | Power dissipation per package | T _A = –40°C to + 100°C | 500 | mW |
| | | T _A = 100°C to + 125°C | Derate linearly at 12 mW/°C to 200 mW | |
| | Device dissipation per output transistor (for T _A = full package-temperature range, all package types) | | 100 | mW |
| T _A | Operating-temperature range | | –40 to +125 | °C |
| T _{stg} | Storage temperature range | | –65 to +150 | °C |
| | Latch-Up Performance per JESD 78, Class I | | 50 | mA |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| V _{DD} Supply-voltage range (for T _A = full package-temperature range) | 3 | 18 | V |

STATIC ELECTRICAL CHARACTERISTICS

| PARAMETER | | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | |
|----------------------|------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------------------|------|-----|------|
| | | V _O (V) | V _{IN} (V) | V _{DD} (V) | −40 | +85 | +125 | +25 | | | UNIT |
| | | | | | | | | MIN | TYP | MAX | |
| I _{DD} Max | Quiescent device current | | 0, 5 | 5 | 1 | 30 | 30 | 0.02 | 1 | μA | |
| | | | 0, 10 | 10 | 2 | 60 | 60 | 0.02 | 2 | | |
| | | | 0, 15 | 15 | 4 | 120 | 120 | 0.02 | 4 | | |
| | | | 0, 20 | 20 | 20 | 600 | 600 | 0.04 | 20 | | |
| I _{OL} Min | Output low (sink) current | 0.4 | 0, 5 | 5 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | mA | |
| | | 0.5 | 0, 10 | 10 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | | |
| | | 1.5 | 0, 15 | 15 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | | |
| I _{OH} Min | Output high (source) current | 4.6 | 0, 5 | 5 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | | |
| | | 2.5 | 0, 5 | 5 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | | |
| | | 9.5 | 0, 10 | 10 | −1.5 | −1.1 | −0.9 | −1.3 | −2.6 | | |
| | | 13.5 | 0, 15 | 15 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | | |
| V _{OL} Max | Output voltage: low-level | | 0, 5 | 5 | 0.05 | | | 0 | 0.05 | V | |
| | | | 0, 10 | 10 | 0.05 | | | 0 | 0.05 | | |
| | | | 0, 15 | 15 | 0.05 | | | 0 | 0.05 | | |
| V _{OH} Min | Output voltage: high-level | | 0, 5 | 5 | 4.95 | | | 4.95 | 5 | | |
| | | | 0, 10 | 10 | 9.95 | | | 9.95 | 10 | | |
| | | | 0, 15 | 15 | 14.95 | | | 14.95 | 15 | | |
| I _{IN} Max | Input current | | 0, 18 | 18 | ±0.1 | ±1 | ±1 | ±10 ^{−5} | ±0.1 | μA | |
| I _{OUT} Max | | | 0, 18 | 18 | ±0.4 | ±12 | ±12 | ±10 ^{−4} | ±0.4 | μA | |
| V _{IL} Max | Input low voltage | 1, 9 | 5 | 10 | 1.5 | | | 1.5 | | V | |
| | | 1.5, 13.5 | 10 | 15 | 3 | | | 3 | | | |
| V _{IH} Min | Input high voltage | 1, 9 | 5 | 10 | 3.5 | | | 3.5 | | | |
| | | 1.5, 13.5 | 10 | 15 | 7 | | | 7 | | | |

DYNAMIC ELECTRICAL CHARACTERISTICS
 $T_A = 25^\circ\text{C}$, Input $t_r/t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SHIFTING MODE | V_{CC} (V) | V_{DD} (V) | MIN | MAX | UNIT |
|---|--------------------------|---------------|-----------------|-----------------|-----|-----|------|
| t_{PHL} Propagation delay time, high-to-low level, data input to output | | L – H | 5 | 10 | 300 | 600 | ns |
| | | | 5 | 15 | 220 | 440 | |
| | | | 10 | 15 | 180 | 360 | |
| | | H – L | 10 | 5 | 250 | 500 | |
| | | | 15 | 5 | 250 | 500 | |
| | | | 15 | 10 | 120 | 240 | |
| t_{PLH} Propagation delay time, low-to-high level, data input to output | | L – H | 5 | 10 | 130 | 260 | ns |
| | | | 5 | 15 | 120 | 240 | |
| | | | 10 | 15 | 70 | 140 | |
| | | H – L | 10 | 5 | 230 | 460 | |
| | | | 15 | 5 | 230 | 460 | |
| | | | 15 | 10 | 80 | 160 | |
| t_{PHZ} Propagation delay time, 3-state disable, delay, output high to high impedance | $R_L = 1\text{ k}\Omega$ | L – H | 5 | 10 | 60 | 120 | ns |
| | | | 5 | 15 | 75 | 150 | |
| | | | 10 | 15 | 35 | 70 | |
| | | H – L | 10 | 5 | 200 | 400 | |
| | | | 15 | 5 | 200 | 400 | |
| | | | 15 | 10 | 40 | 80 | |
| t_{PLZ} Propagation delay time, 3-state disable, delay, output low to high impedance | $R_L = 1\text{ k}\Omega$ | L – H | 5 | 10 | 370 | 740 | ns |
| | | | 5 | 15 | 300 | 600 | |
| | | | 10 | 15 | 250 | 500 | |
| | | H – L | 10 | 5 | 250 | 500 | |
| | | | 15 | 5 | 250 | 500 | |
| | | | 15 | 10 | 130 | 260 | |
| t_{PZH} Propagation delay time, 3-state disable, delay, output high impedance to high | $R_L = 1\text{ k}\Omega$ | L – H | 5 | 10 | 320 | 640 | ns |
| | | | 5 | 15 | 230 | 460 | |
| | | | 10 | 15 | 180 | 360 | |
| | | H – L | 10 | 5 | 300 | 600 | |
| | | | 15 | 5 | 300 | 600 | |
| | | | 15 | 10 | 130 | 260 | |
| t_{PZL} Propagation delay time, 3-state disable, delay, output high impedance to low | $R_L = 1\text{ k}\Omega$ | L – H | 5 | 10 | 100 | 200 | ns |
| | | | 5 | 15 | 80 | 160 | |
| | | | 10 | 15 | 40 | 80 | |
| | | H – L | 10 | 5 | 200 | 400 | |
| | | | 15 | 5 | 200 | 400 | |
| | | | 15 | 10 | 40 | 80 | |
| t_{THL}, t_{TLH} Transition time | | L – H | 5 | 10 | 50 | 100 | ns |
| | | | 5 | 15 | 40 | 80 | |
| | | | 10 | 15 | 40 | 80 | |
| | | H – L | 10 | 5 | 100 | 200 | |
| | | | 15 | 5 | 100 | 200 | |
| | | | 15 | 10 | 50 | 100 | |
| C_i Input capacitance | | | Any input | | 5 | 7.5 | pF |

TYPICAL CHARACTERISTICS

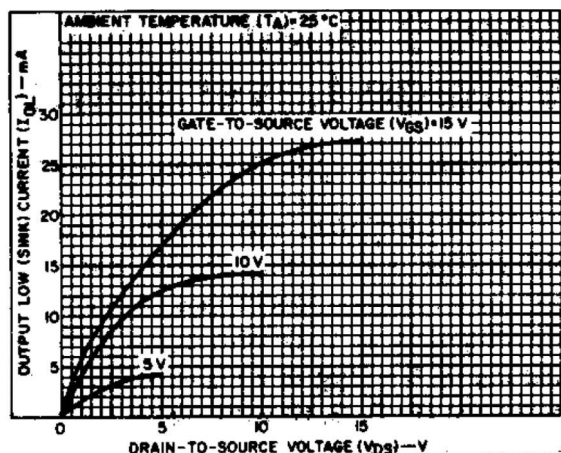


Figure 1. Typical Output Low (Sink) Current Characteristics

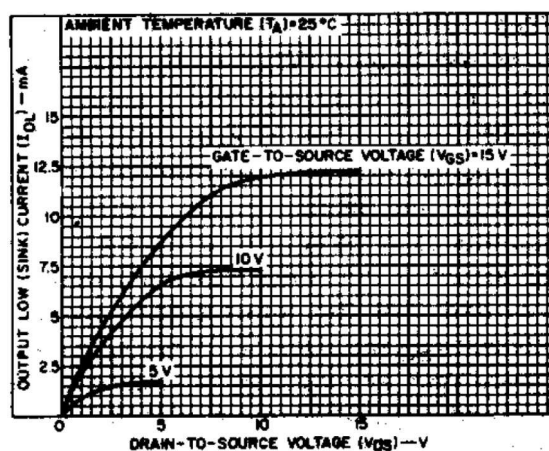


Figure 2. Minimum Output Low (Sink) Current Characteristics

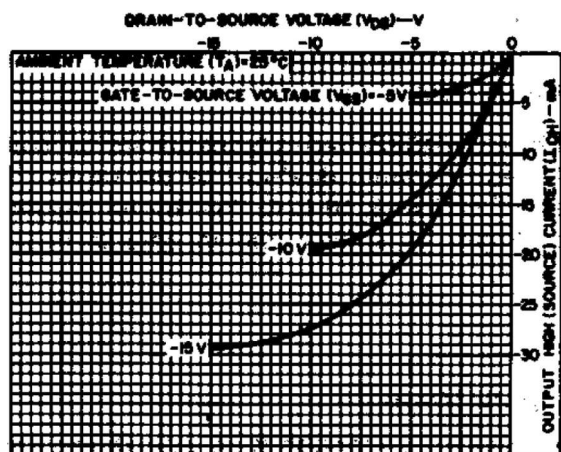


Figure 3. Typical Output High (Source) Current Characteristics

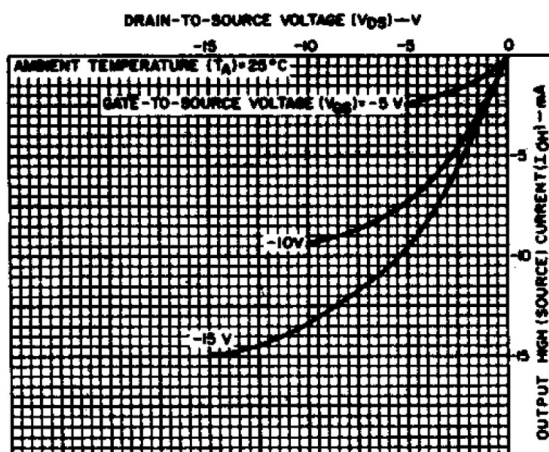


Figure 4. Minimum Output High (Source) Current Characteristics

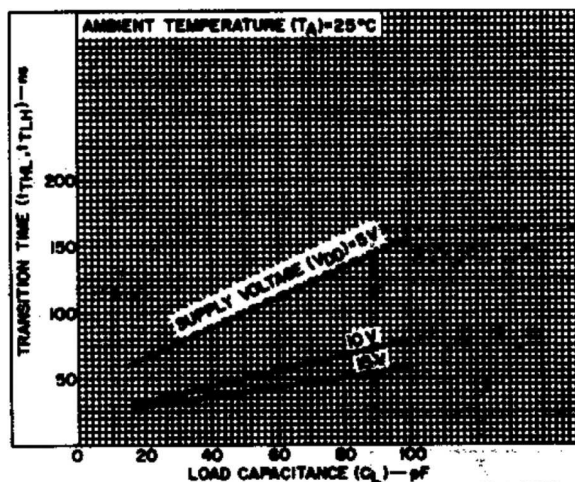


Figure 5. Typical Transition Time as a Function of Load Capacitance

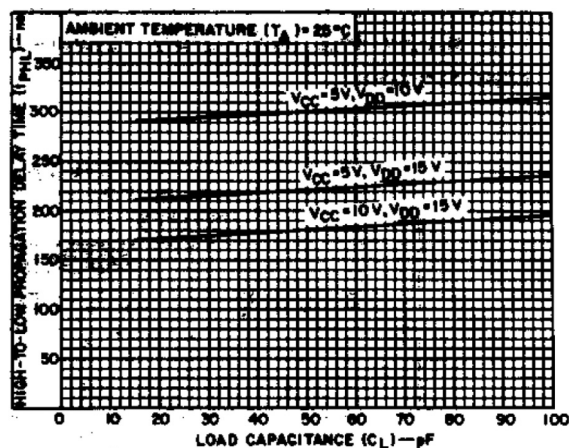


Figure 6. Typical High-to-Low Propagation Delay Time as a Function of Load Capacitance

TYPICAL CHARACTERISTICS (continued)

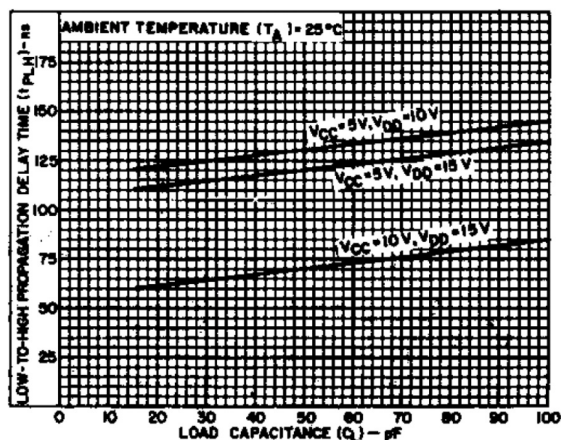


Figure 7. Typical Low-to-High Propagation Delay Time as a Function of Load Capacitance

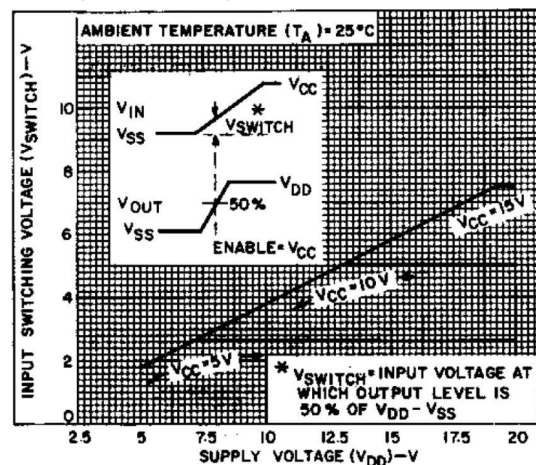


Figure 8. Typical Input Switching as a Function of High-Level Supply Voltage

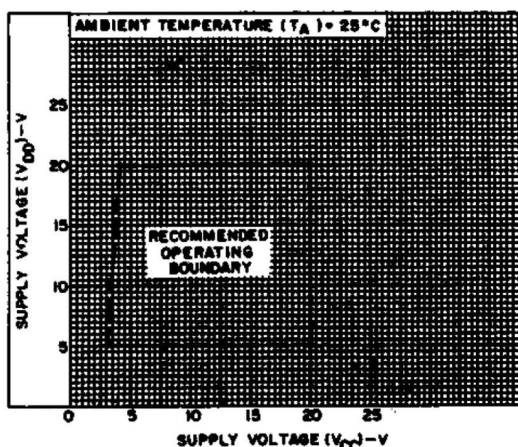


Figure 9. High-Level Supply Voltage vs Low-Level Supply Voltage

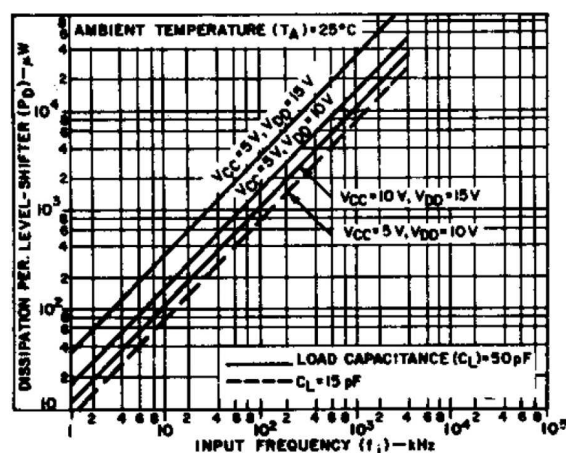


Figure 10. Typical Dynamic Power Dissipation as a Function of Input Frequency

PARAMETER MEASUREMENT INFORMATION

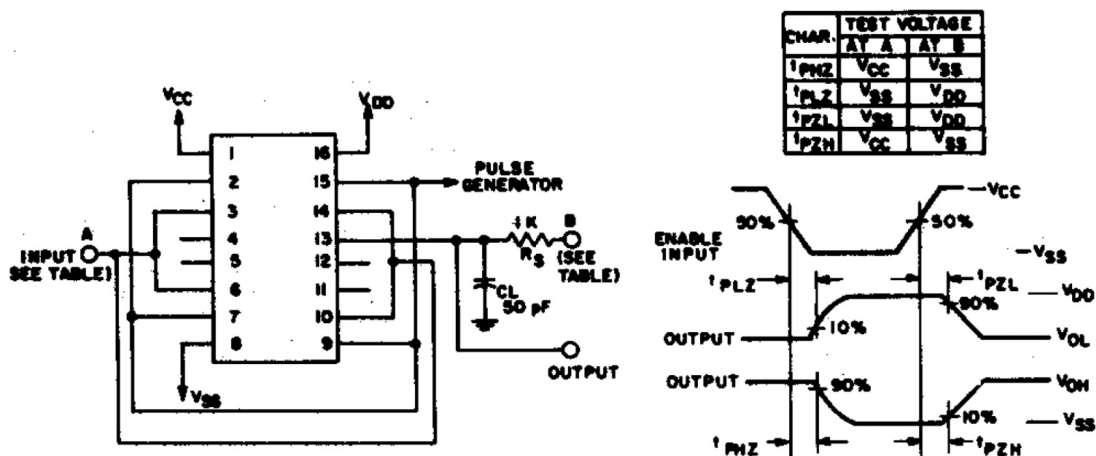


Figure 11. Output Enable Delay Times Test Circuit and Waveforms

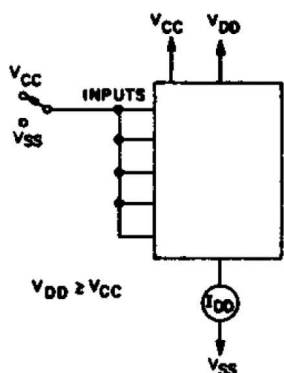


Figure 12. Quiescent Device Current Test Circuit

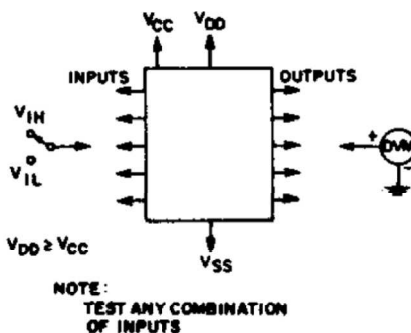


Figure 13. Input Voltage Test Circuit

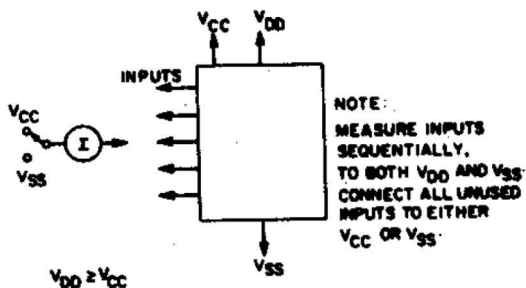


Figure 14. Input Current Test Circuit

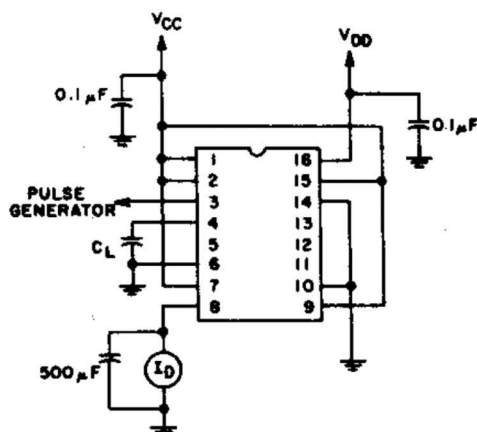
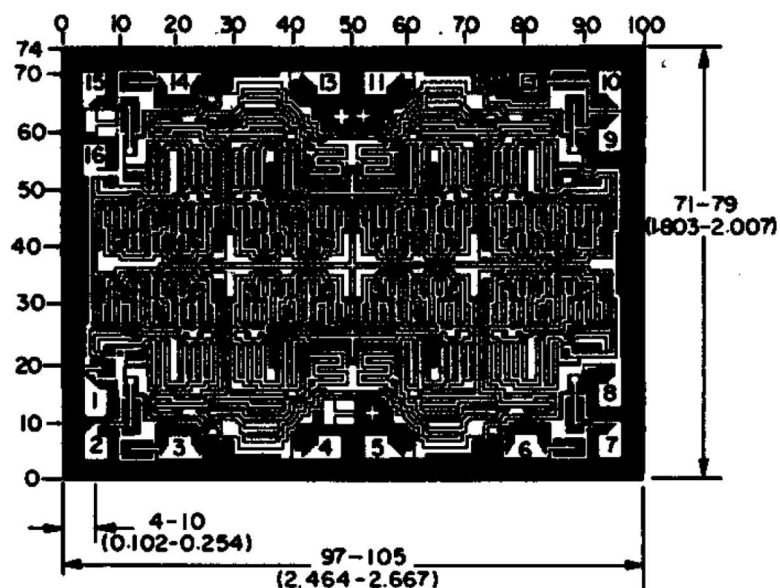


Figure 15. Dynamic Power Dissipation Test Circuit



Note: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Figure 16. Dimensions and Pad Layout

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| CD40109BQNSRQ1 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD40109B-Q1 :

● Catalog: [CD40109B](#)

● Military: [CD40109B-MIL](#)

NOTE: Qualified Version Definitions:

-
- Catalog - TI's standard catalog product
 - Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD40109BQNSRQ1 | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD40109BQNSRQ1 | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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