CS1500

Digital Power Factor Correction IC

Features

- ❑ **Digital EMI Noise Shaping**
- ❑ **Excellent Efficiency Under All Load Conditions**
- ❑ **Minimal External Devices Required**
- ❑ **Optimized Digital Loop Compensation**
- ❑ **Comprehensive Safety Features**
  - Undervoltage Lockout (UVLO)
  - Output Overvoltage Protection
  - Input Current Limiting
  - Open/short Loop Protection for IAC & IFB Pins
  - Thermal Shutdown

Applications

- ❑ **LCD and LED TVs**
- ❑ **Monitor Supplies**
- ❑ **Battery Chargers**

Description

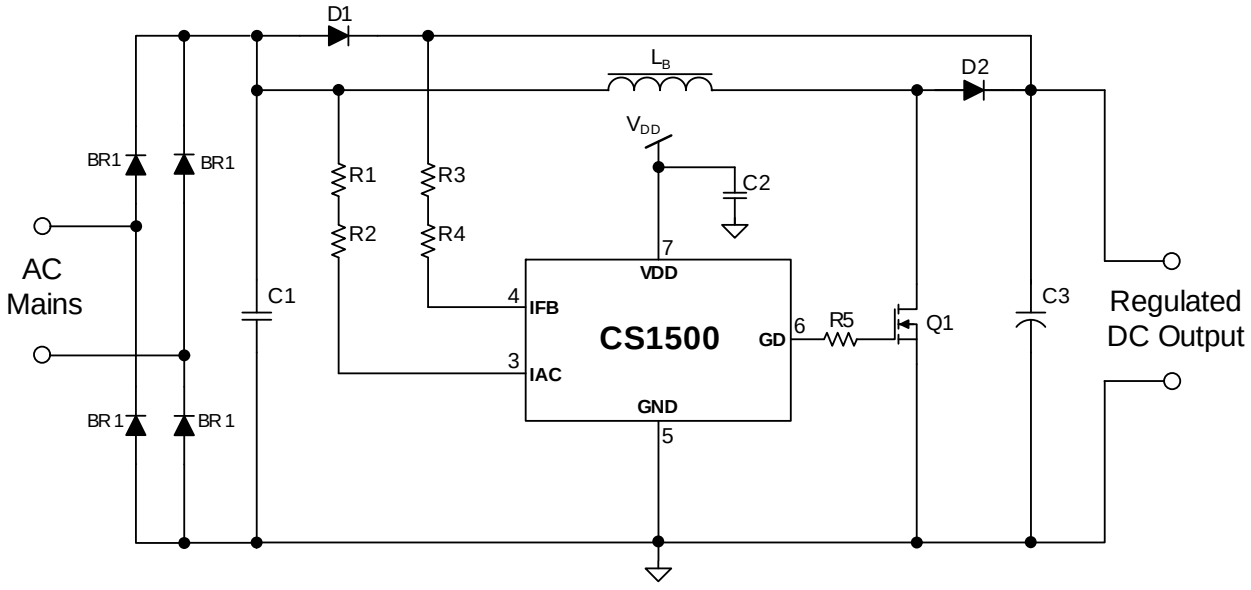
The CS1500 is a high-performance power factor correction (PFC) controller for universal AC input, which uses a proprietary digital algorithm for discontinuous conduction mode (DCM) with variable on-time and variable frequency control, ensuring unity power factor.

The CS1500 incorporates all the safety features necessary for robust and compact PFC stages. In addition, it has burst mode control to lower the light-load/standby losses to a minimum. Protection features such as overvoltage, open- and short-circuit protection, and overtemperature help protect the device during abnormal transient conditions.

The digital controller optimizes the system stability and transient performance, simplifies the PFC design, reduces the external component count and BOM costs. The simple design and minimum cost makes CS1500 the ideal choice for PFC up to 300 watts.

Ordering Information

See **page 13.**



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

1. INTRODUCTION

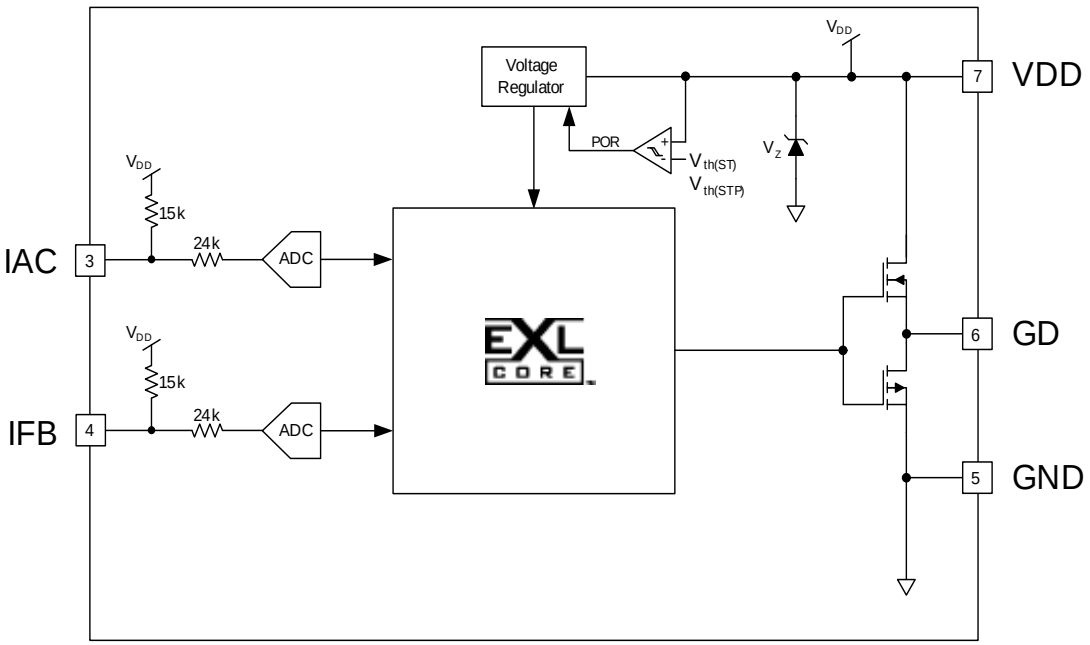


Figure 1. CS1500 Block Diagram

The CS1500 digital power factor controller operates in variable on-time, variable frequency, discontinuous conduction mode (DCM). The CS1500 uses a proprietary digital algorithm to maximize the efficiency and reduce the conductive EMI.

The analog-to-digital converter (ADC) shown in the CS1500 block diagram in Figure 9 is used to sense the PFC output voltage (V_{link}) and the rectified AC line voltage (V_{rect}) by measuring currents through their respective resistors. The magnitudes of these currents are measured as a proportion of a reference current (I_{REF}) that functions as the reference for the ADCs. The digital signal is then processed in a control algorithm which determines the behavior of the CS1500 during start-up, normal operation, and under fault conditions, such as overvoltage, and over-temperature conditions.

The CS1500 PFC switching frequency varies with the V_{rect} on a cycle-by-cycle basis, and its digital algorithm calculates the on-time accordingly for unity power factor. Unlike traditional Critical Conduction Mode (CRM) PFC controller, CS1500 operates at its low switching frequency near the zero-crossing point of the AC input voltage, and it operates at its high switching frequency at the peak of its AC input voltage (this is the opposite of the switching frequency profile for a CRM PFC controller), thus CS1500 reduces switching losses especially under light-load conditions, spreads conducted EMI energy peaks over a wide frequency band and increases overall system efficiency.

The proprietary digital control engine optimizes the feedback error signal using an adaptive control algorithm, improves system stability and transient response. No external feedback error signal compensation components are required.

The CS1500s digital controller algorithm limits the ON time of the Power MOSFET by the following equation:

$$T_{on} \leq \frac{0.001587V\mu S}{V_{rect}}$$

Where T_{on} is the max time that the power MOSFET is turned on and V_{rect} is the rectified line voltage. In the event of a sudden line surge or sporadic, high dv/dt line voltages, this equation may not limit the ON time appropriately. For this type of line disturbance, additional protection mechanisms such as fusible resistors, fast-blow fuses, or other current-limiting devices are recommended.

Under steady-state conditions, the voltage loop keeps PFC output voltage close to its nominal value. Under light load startup or feedback loop open conditions, the output voltage may pass the overvoltage protection threshold. The digital control engine initiates a fast response loop to shut down gate driving signal to reduce the energy delivered to the output for PFC capacitor protection. When the link voltage drop below V_{OVP}-$V_{OVP(Hy)}$, PFC resumes normal operation.

2. PIN DESCRIPTION

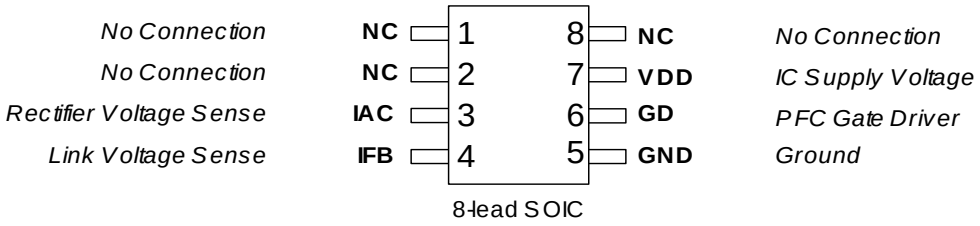


Figure 2. CS1501 Pin Assignments

Table 1. Pin Descriptions

Pin Name	Pin #	I/O	Description
NC	1,2,8	-	**NC** — No connections
IAC	3	IN	**Rectifier Voltage Sense** — A current proportional to the rectified line voltage (V_{rect}) is fed into this pin. The current is measured with an A/D converter.
IFB	4	IN	**Link Voltage Sense** — A current proportional to the output link voltage (V_{link}) of the PFC is fed into this pin. The current is measured with an A/D converter.
GND	5	PWR	**Ground** — Current return for both the input signal portion of the IC and the gate driver.
GD	6	OUT	**Gate Driver Output** — The totem pole stage is able to drive the power MOSFET with a peak current of 0.5 A source and 1.0 A sink. The high-level voltage of this pin is clamped at V_Z to avoid excessive gate voltages.
VDD	7	PWR	**IC Supply Voltage** — Supply voltage of both the input signal portion of the IC and the gate driver.

3. CHARACTERISTICS AND SPECIFICATIONS

3.1 Electrical Characteristics

Typical characteristics conditions:
T_A = 25º C, V_{DD} = 13 V, GND = 0 V
All voltages are measured with respect to GND.
Unless otherwise specified, all currents are positive when flowing into the IC.

Minimum/Maximum characteristics conditions:
T_J = -40º to +125º C, V_{DD} = 10 V to 15 V, GND = 0 V

Parameter	Condition	Symbol	Min	Typ	Max	Unit
VDD Supply Voltage						
Turn-on Threshold Voltage	V_{DD} Increasing	$V_{DD(on)}$	8.4	8.8	9.3	V
Turn-off Threshold Voltage (UVLO)	V_{DD} Decreasing	$V_{DD(off)}$	7.1	7.4	7.9	V
UVLO Hysteresis		V_{Hys}	-	1.3	-	V
Zener Voltage	I_{DD} = 20 mA	V_Z	17.0	17.9	18.5	V
VDD Supply Current						
Start-up Supply Current	$V_{DD} = V_{DD(on)}$	I_{ST}	-	68	80	µA
Operating Supply Current	C_L=1nF, fsw=70kHz	I_{DD}	-	1.7	1.9	mA
PFC Gate Drive						
Output Source Resistance	I_{GD} = 100mA,V_{DD} = 13V	R_{OH}	-	9	-	Ω
Output Sink Resistance	I_{GD} = -200mA,V_{DD} = 13V	R_{OL}	-	6	-	Ω
Rising Time	C_L=1nF,V_{DD} = 13V	t_r	-	32	60	ns
Falling Time	C_L=1nF,V_{DD} = 13V	t_f	-	15	30	ns
Output Voltage Low State	I_{GD} = -200mA,V_{DD} = 13V	Vol	-	0.9	1.3	V
Output Voltage High State	I_{GD} = 100mA,V_{DD} = 13V	Voh	11.3	11.8	-	V
Overvoltage Protection (OVP) [2]						
Output Voltage at Startup Mode		$V_{O(startup)}$	-	360	-	V
Output Voltage at Normal Mode		$V_{O(nom)}$	-	400	-	V
OVP Threshold		V_{OVP}	-	418	-	V
OVP Hysteresis		$V_{OVP(Hy)}$	-	4	-	V
Thermal Protection [1]						
Thermal Shutdown Threshold		T_{SD}	130	143	155	ºC
Thermal Shutdown Hysteresis		$T_{SD(Hy)}$	-	9	-	ºC

Notes:
1. Specifications guaranteed by design and are characterized and correlated using statistical process methods.
2. Specification are based upon a PFC system configured for AC input of 90-265 VAC (Sine), 45/65 Hz, V_{link}= 400 V, R_{IAC} = 3.0 MΩ, R_{IFB} = 3.0 MΩ, C3 = 180 µF, L_B = 360 µH, 90 W.
3. Overpower protection is scaled to rated power.
4. Normal operation mode, see 5.2 *Start-up vs. Normal Operation Mode* on page 8.

3.2 Absolute Maximum Ratings

Pin	Symbol	Parameter		Value	Unit
7	V_{DD}	IC Supply Voltage		V_Z	V
1,3,4,5	-	Analog Input Maximum Voltage		-0.5 to V_Z	V
1,3,4,5	-	Analog Input Maximum Current		50	mA
7	V_{GD}	Gate Drive Output Voltage		-0.3 to V_Z	V
7	I_{GD}	Gate Drive Output Current		-1.0 / +0.5	A
-	P_D	Total Power Dissipation @ T_A=50° C		600	mW
-	θ_{JA}	Junction-to-Ambient Thermal Impedance		107	ºC / W
-	T_A	Operating Ambient Temperature Range[1]		-40 to +125	ºC
-	T_J	Junction Temperature Operating Range		-40 to +125	ºC
-	T_{Stg}	Storage Temperature Range		-65 to +150	ºC
All Pins	ESD	Electrostatic Discharge Capability	Human Body Model Machine Model Charged Device Model	2000 200 500	V

Notes:
5. The CS1501 has an internal shunt regulator that controls the voltage on the VDD pin. V_Z, the shunt regulation voltage, can be a maximum of 20 V but may also be as low as 10 V.
6. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation at the rate of 50 mW / ºC for variation over temperature.

WARNING:

Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

4. TYPICAL ELECTRICAL PERFORMANCE

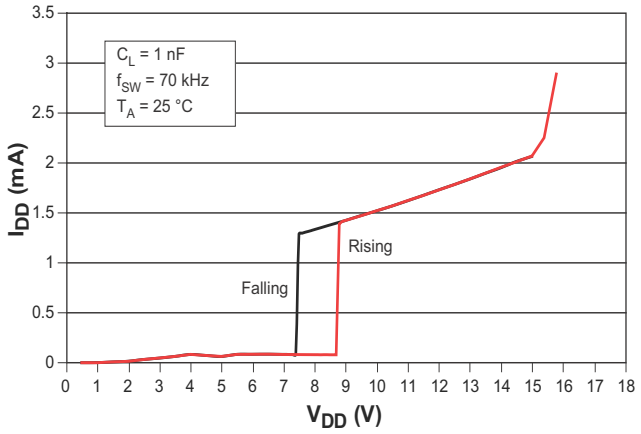


Figure 3. Supply Current vs. Supply Voltage

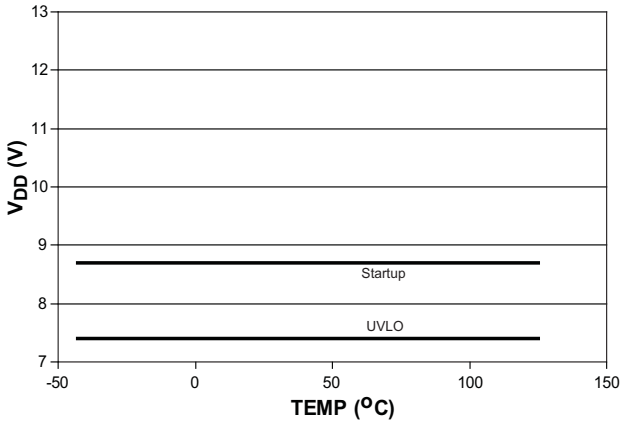


Figure 4. Start-up & UVLO vs. Temp

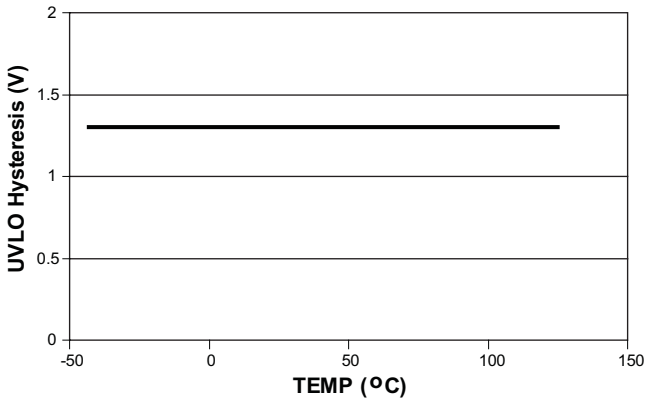


Figure 5. UVLO Hysteresis vs. Temp

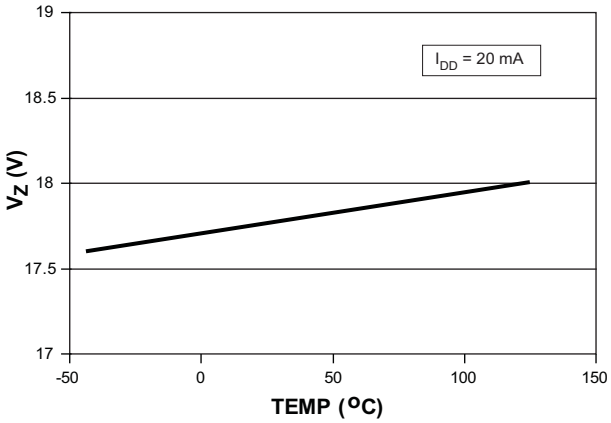


Figure 6. VDD Zener Voltage vs. Temp

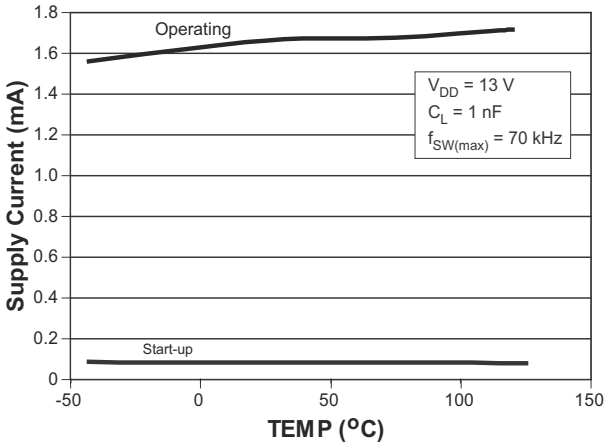


Figure 7. Supply Current (I_{SB}, I_{ST}, I_{DD}) vs. Temp

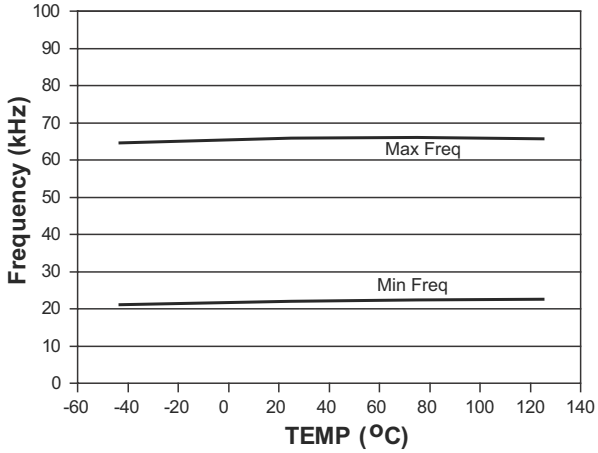


Figure 8. Min/Max Operating Frequency vs. Temp

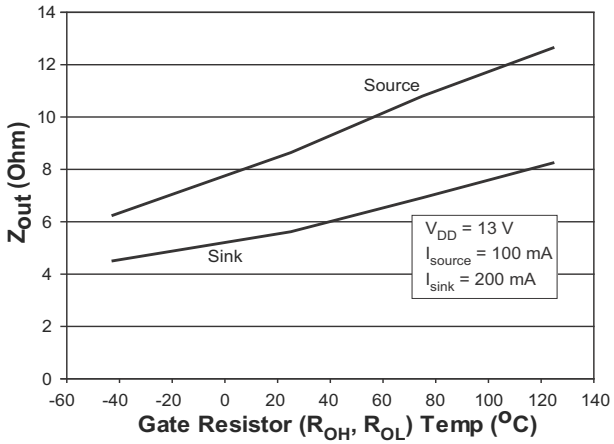


Figure 9. Gate Resistance (R_{OH}, R_{OL}) vs. Temp

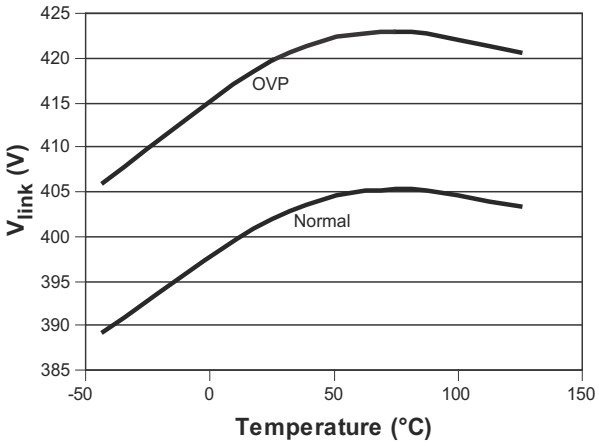


Figure 10. OVP vs. Temp

5. GENERAL DESCRIPTION

The CS1500 offers numerous features, options, and functional capabilities to the designer of switching power converters. This digital PFC control IC is designed to replace legacy analog PFC controllers with minimal design effort.

5.1 PFC Operation

One key feature of the CS1500 is its operating frequency profile. Figure 11 illustrates how the frequency varies over half cycle of the line voltage in steady-state operation. When power is first applied to the CS1500, it examines the line voltage and adapts its operating frequency to the line voltage as shown in Figure 11. The operating frequency is varied from the peak to the trough of the AC input. During start-up the control algorithm uses the current-sense threshold, providing an approximate square-wave envelop current within every half line cycle by adjusting the operating frequency for fast startup behavior.

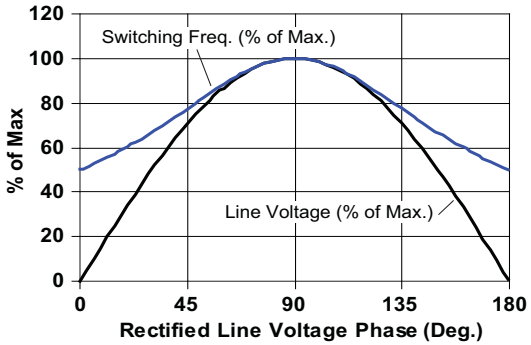


Figure 11. Switching Frequency vs. Phase Angle

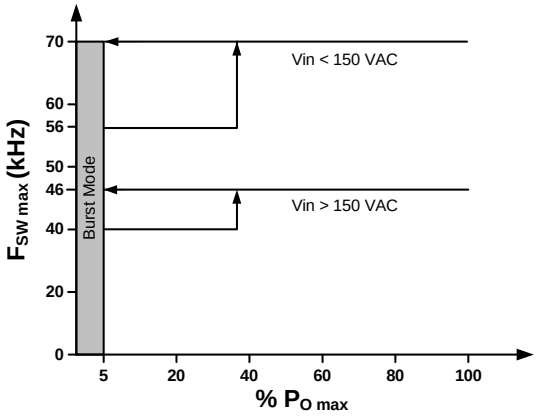


Figure 12. Switching Frequency vs. Output Power

Figure 12 illustrates how the operating frequency (as a percentage of maximum frequency) changes with output power and the peak of the line voltage. When P_O falls below 5% the CS1500 changes to Burst Mode (See 5.3 *Burst Mode* on page 9).

5.2 Start-up vs. Normal Operation Mode

CS1500 has two discrete operation modes: Start-up and Normal. Start-up mode will be activated when V_{link} is less than 90% of nominal value and remains active until V_{link} reaches 100% of nominal value, as shown in Figure 13. Startup mode is activated during initial system power-up. Any V_{link} drop to less than 90% of nominal value, such as load change, can cause the system to enter Start-up mode until V_{link} is brought back into regulation.

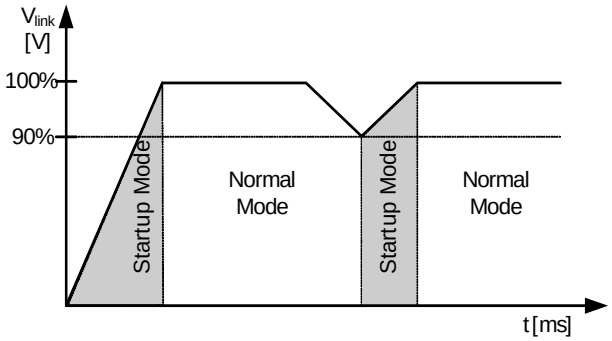


Figure 13. Start-up and Normal Modes

Startup mode is defined as a surge of current delivering approximately 1.4x the maximum power to the output regardless of the load. During startup, the CS1500 controller is in an open loop phase with power factor correction suppressed, causing the current delivered to the output to mimic a square wave instead of a sine wave. During every active switch cycle, the 'ON' time is calculated to drive a constant peak current over the entire line cycle. However, the 'OFF' time is calculated based on the DCM/CCM boundary equation.

5.3 Burst Mode

Burst mode is utilized to improve system efficiency when the system output power (P_o) is < 5% of nominal. Burst mode is implemented by intermittently disabling the PFC over a full half-line period cycle under light load conditions, as shown in Figure 14.

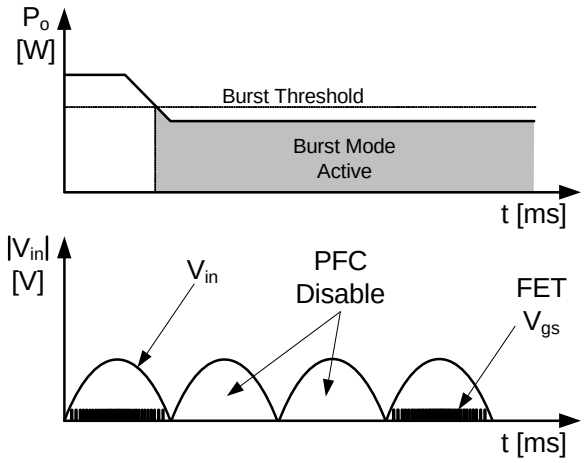


Figure 14. Burst Modes

5.4 Output Power and PFC Boost Inductor

In normal operating mode, the nominal output power is estimated by the following equation.

$$P_o = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times L_B \times V_{link}} \quad \text{[Eq.1]}$$

where:

P_o	rated output power of the system
η	efficiency of the boost converter (estimated as 100% by the PFC algorithm)
$V_{in(min)}$	minimum RMS line voltage is 90V, measured after the rectifier and EMI filter
V_{link}	nominal PFC output voltage must be 400 V
f_{max}	maximum switching frequency is 70 kHz
L_B	boost inductor specified by rated power requirement
α	margin factor to guarantee rated output power (P_o) against boost inductor tolerances.

Equation 1 is provided for explanation purposes only. Using substituted required design values for V_{link} and f_{max} gives the following equation.

$$P_o = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{400V - (V_{in(min)} \times \sqrt{2})}{2 \times 70kHz \times L_B \times 400V} \quad \text{[Eq.2]}$$

Changing values for application-specific devices such as the boost inductor or V_{link} voltage is not recommended and requires changing internal register values.

Solving Equation 2 for the PFC boost inductor L_B gives the following equation.:

$$L_B = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{400V - (V_{in(min)} \times \sqrt{2})}{2 \times 70kHz \times P_o \times 400V} \quad \text{[Eq.3]}$$

If a value of the boost inductor other than that obtained from Equation 3 above is used, the total output power capability as well as the minimum input voltage threshold will differ according to Equation 2.

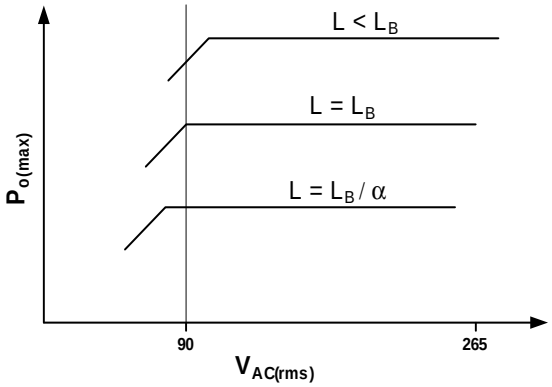


Figure 15. Relative Effects of Varying Boost Inductance

5.5 PFC Output Capacitor

The value of the PFC output capacitor should be chosen based upon voltage ripple and hold-up requirements. To ensure system stability with the digital controller, the recommended value of the capacitor is within the range of 0.5 µF / watt to 2.0 µF / watt.

5.6 Output IFB Sense & Input IAC Sense

A current proportional to the PFC output voltage, V_{link}, is supplied to the IC on pin IFB and is used as a feedback control signal. This current is compared against an internal fixed-value current.

The ADC is used to measure the magnitude of the I_{FB} current through resistor R_{IFB}. The magnitude of the I_{FB} current is then compared to an internal fixed-value current.

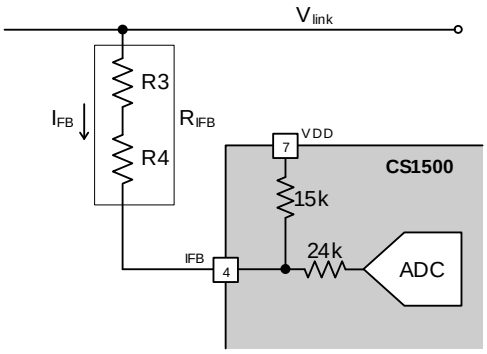


Figure 16. Feedback Input Pin Model

Resistor R_{IFB} sets the feedback current and is calculated as follows:

$$R_{IFB} = \frac{V_{link} - V_{dd}}{I_{fixed}} = \frac{400V - V_{dd}}{129\mu A} \quad \text{[Eq.4]}$$

By using digital loop compensation, the voltage feedback signal does not require an external compensation network.

A current proportional to the AC input voltage is supplied to the IC on pin IAC and is used by the PFC control algorithm.

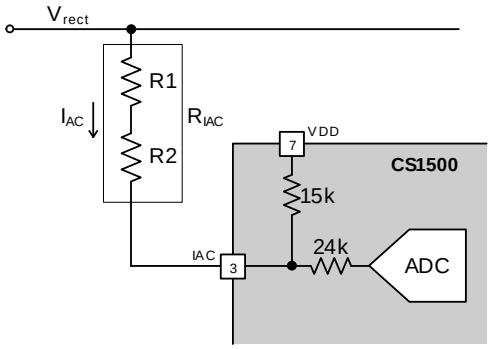


Figure 17. IAC Input Pin Model

Resistor R_{IAC} sets the IAC current and is derived as follows:

$$R_{IAC} = R_{IFB} \quad \text{[Eq.5]}$$

For optimal performance, resistors R_{IAC} & R_{IFB} should use 1% tolerance or better resistors.

5.7 Overvoltage Protection

The overvoltage protection (OVP) will trigger immediately and stop the gate drive when the current into the IFB pin (I_{OVP}) exceeds 105% of the reference current value (I_{ref}). The IC resumes gate drive switching when the link voltage drops below $V_{OVP} - V_{OVP(HY)}$.

5.8 Open/Short Loop Protection

If the PFC output sense resistor R_{IFB} fails (open or short to GND), the measured output voltage decreases at a slew rate of about 2V / µs, which is determined by ADC sampling rate. The IC stops the gate drive when the measured output voltage

6. SUMMARY OF EQUATIONS

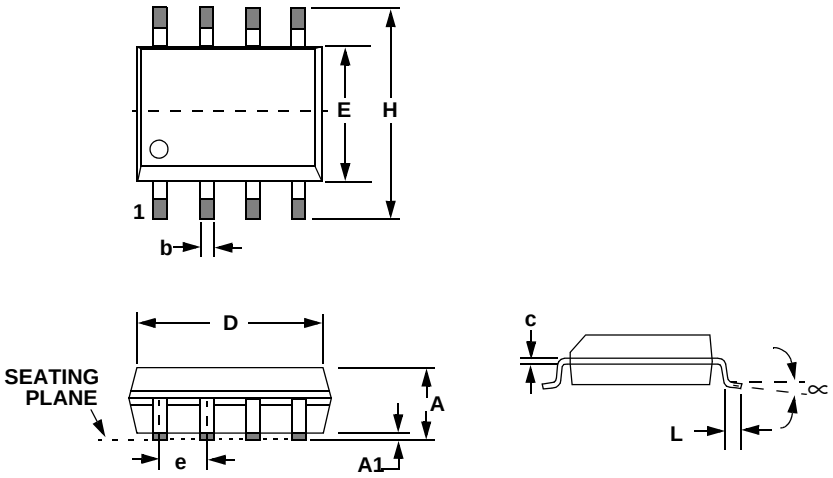
Eq. #	Equation	Variables/Recommended Values
1	**Output Power** (page 9) $P_o = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{V_{link} - (V_{in(min)} \times \sqrt{2})}{2 \times f_{max} \times L_B \times V_{link}}$	P_o rated output power of the system η efficiency of the boost converter (estimated as 100% by the PFC algorithm) $V_{in(min)}$ minimum RMS line voltage is 90V, measured after the rectifier and EMI filter V_{link} nominal PFC output voltage must be 400 V f_{max} maximum switching frequency is 70 kHz L_B boost inductor specified by rated power requirement α margin factor to guarantee rated output power (P_o) against boost inductor tolerances.
2	**Output Power w/ required values** (page 9) $P_o = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{400V - (V_{in(min)} \times \sqrt{2})}{2 \times 70kHz \times L_B \times 400V}$	
3	**Boost Inductor** (page 9) $L_B = \alpha \times \eta \times (V_{in(min)})^2 \times \frac{400V - (V_{in(min)} \times \sqrt{2})}{2 \times 70kHz \times P_o \times 400V}$	
4	**Output IFB Sense Resistor** (page 10) $R_{IFB} = \frac{V_{link} - V_{dd}}{I_{fixed}} = \frac{400V - V_{dd}}{129\mu A}$	
5	**Input IAC Sense Resistor** (page 10) $R_{IAC} = R_{IFB}$	

7. SUMMARY OF TERMS

Variable	Definition
η	The efficiency factor.
α	A margin factor to guarantee rated power against tolerances and transients.
$f_{line(min)}$	The minimum AC line frequency.
I_{AC}	The current generated by V_{rect} that flows into the IAC pin.
I_{FB}	The current generated by V_{link} that flows into the IFB pin.
$I_{FET(pk)}$	The PFC MOSFET peak current, which is equal to the peak current in the PFC boost inductor.
I_{rms}	The magnitude of the RMS current.
I_{sat}	The boost inductor L_B saturation current.
I_{st}	The sum of the current into the IAC and IFB pins.
I_{ST}	The startup current of the chip.
L_B	The PFC boost inductor.
P_o	The nominal output power from the CS1500 PFC circuit.
$P_{o(max)}$	The maximum value of the output power from the CS1500 PFC circuit.
R_{IAC}	The sense resistor used to measure current into the IAC pin.
R_{IFB}	The sense resistor used to measure current into the IFB pin.
$V_{in(min)}$	The minimum specified line voltage for proper operation (volts RMS).
V_{link}	The magnitude of the output voltage from the PFC.
$V_{link(min)}$	The magnitude of the output voltage from the PFC.
$\Delta V_{link(rip)}$	$\Delta V_{link(rip)}$, is the output voltage ripple requirement in volts peak-to-peak
V_{rect}	The instantaneous value of the rectified line voltage (volts).

8. PACKAGE DRAWING

8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC # MS-012

9. ORDERING INFORMATION

Part #	Temperature Range	Package Description
CS1500-FSZ	-40 °C to +125 °C	8-lead SOIC, Lead (Pb) Free

10.ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating[a]	Max Floor Life[b]
CS1500-FSZ	260 °C	2	365 Days

a. MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

b. Stored at 30 °C, 60% relative humidity.

11.REVISION HISTORY

Revision	Date	Changes
A7	JUL 2010	Initial public advance data release.
F1	OCT 2010	First production preliminary data release.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to http://www.cirrus.com