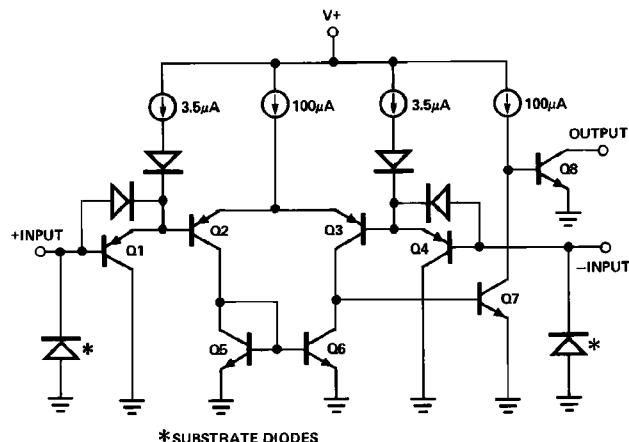


**FEATURES**

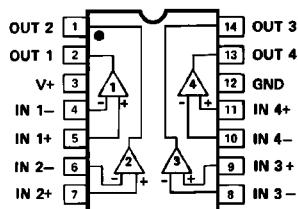
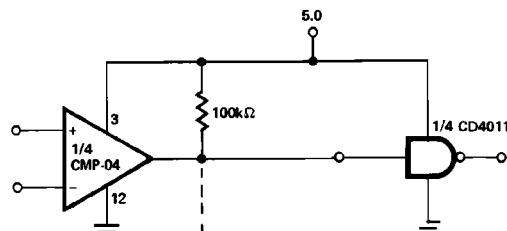
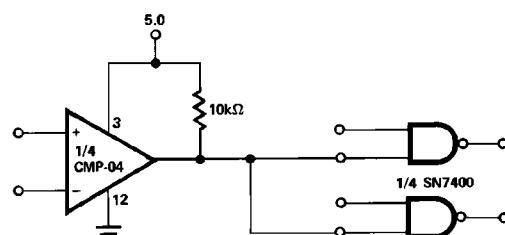
- High Gain:** 200 V/mV typ
- Single or Dual Supply Operation**
- Input Voltage Range Includes Ground**
- Low Power Consumption (1.5 mW/ Comparator)**
- Low Input Bias Current:** 100 nA max
- Low Input Offset Current:** 10 nA max
- Low Offset Voltage:** 1 mV max
- Low Output Saturation Voltage:** 250 mV @ 4 mA
- Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS**
- Directly Replaces LM139/239/339 Comparators**
- Available in Die Form**

**SIMPLIFIED SCHEMATIC (1/4 CMP-04)**

**GENERAL DESCRIPTION**

Four precision independent comparators comprise the CMP04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V<sub>-</sub> for split supplies. A low power supply current of 2 mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

**PIN CONNECTIONS**

- 14-Pin Hermetic DIP (Y Suffix)**
- 14-Pin Epoxy DIP (P Suffix)**
- 14-Pin SO (S Suffix)**


**TYPICAL INTERFACE**
**Driving CMOS**

**Driving TTL**

**REV. B**

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# CMP04-SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS (@ $V_4 = +5\text{ V}$ , $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$V_{OS}$	$R_S = 0\ \Omega$ , $R_L = 5.1\text{ k}\Omega$ , $V_O = 1.4\text{ V}^1$		0.4	1	mV
Input Offset Current	$I_{OS}$	$I_{IN(+)} - I_{IN(-)}$ , $R_L = 5.1\text{ k}\Omega$ $V_O = 1.4\text{ V}$		2	10	nA
Input Bias Current	$I_B$	$I_{IN(+)} \text{ or } I_{IN(-)}$		25	100	nA
Voltage Gain	$A_V$	$R_L \geq 15\text{ k}\Omega$ , $V_+ = 15\text{ V}^5$	80	200		V/mV
Large-Signal Response Time	$t_r$	$V_{IN} = \text{TTL Logic Swing}$ , $V_{REF} = 1.4\text{ V}^4$ $V_{RL} = 5\text{ V}$ , $R_L = 5.1\text{ k}\Omega$		300		ns
Small-Signal Response Time	$t_r$	$V_{IN} = 100\text{ mV Step}^4$ , 5 mV Overdrive $V_{RL} = 5\text{ V}$ , $R_L = 5.1\text{ k}\Omega$		1.3		μs
Input Voltage Range	CMVR	(Note 2)	0		$V_+ - 1.5$	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100		dB
Power Supply Rejection Ratio	PSRR	$V_+ = +5\text{ V}$ to $+18\text{ V}^5$	80	100		dB
Saturation Voltage	$V_{OL}$	$V_{IN(-)} \geq 1\text{ V}$ , $V_{IN(+)} = 0$ , $I_{SINK} \leq 4\text{ mA}$		250	400	mV
Output Sink Current	$I_{SINK}$	$V_{IN(-)} \geq 1\text{ V}$ , $V_{IN(+)} = 0$ , $V_O \leq 1.5\text{ V}$	6	16		mA
Output Leakage Current	$I_{LEAK}$	$V_{IN(+)} \geq 1\text{ V}$ , $V_{IN(-)} = 0$ , $V_O = 30\text{ V}$		0.1	100	nA
Supply Current	$I_+$	$R_L = \infty$ , All Comps, $V_+ = 30\text{ V}$		0.8	2.0	mA

### NOTES

<sup>1</sup>At output switch point,  $V_O = 1.4\text{ V}$ ,  $R_S = 0\ \Omega$  with  $V_+$  from 5 V; and over the full input common-mode range (0 V to  $V_+ - 1.5$  V).

<sup>2</sup>The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is  $V_+ - 1.5$  V, but either or both inputs can go to  $+30$  V without damage.

<sup>3</sup> $R_L \geq 15\text{ k}\Omega$ ,  $V_+ = 15\text{ V}$ ,  $V_{CM} = 1.5\text{ V}$  to  $13.5\text{ V}$ .

<sup>4</sup>Sample tested.

<sup>5</sup>Guaranteed by design.

Specifications subject to change without notice

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Supply Voltage .....	36 V or $\pm 18\text{ V}$
Differential Input Voltage .....	36 Vdc
Input Voltage .....	-0.3 V to $+36\text{ V}$
Operating Temperature Range	
CMP04FY .....	-40°C to $+85^\circ\text{C}$
CMP04BY .....	-55°C to $+125^\circ\text{C}$
CMP04FP, FS .....	-40°C to $+85^\circ\text{C}$
Junction Temperature ( $T_J$ ) .....	-65°C to $+150^\circ\text{C}$
Storage Temperature Range .....	-65°C to $+150^\circ\text{C}$
(P Suffix) .....	-65°C to $+125^\circ\text{C}$
Input Current ( $V_{IN} < -3.0\text{ V}$ ) .....	50 mA
Output Short-Circuit to GND .....	Continuous
Lead Temperature (Soldering, 60 sec) .....	300°C

Package Type	$\theta_{JA}^2$	$\theta_{JC}$	Units
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

### NOTES

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

<sup>2</sup> $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for Cerdip and Plastic DIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

## ORDERING GUIDE

Model	$T_A = +25^\circ\text{C}$ $V_{OS}$	Temperature Range	Package Descriptions	Package Options
CMP04BY/883C	1 mV	-55°C to $+125^\circ\text{C}$	14-Contact LCC	Q-14
CMP04FP	1 mV	-40°C to $+85^\circ\text{C}$	14-Pin P-DIP	N-14
CMP04FS	1 mV	-40°C to $+85^\circ\text{C}$	14-Pin SO	SO-14

\*Burn-in is available on commercial and industrial temperature range parts in Cerdip and plastic DIP packages.

## ELECTRICAL CHARACTERISTICS

(@ $V_+ = +5\text{ V}$ ,  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  for CMP04BY,  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for CMP04FY/FP/FS, unless otherwise noted.)

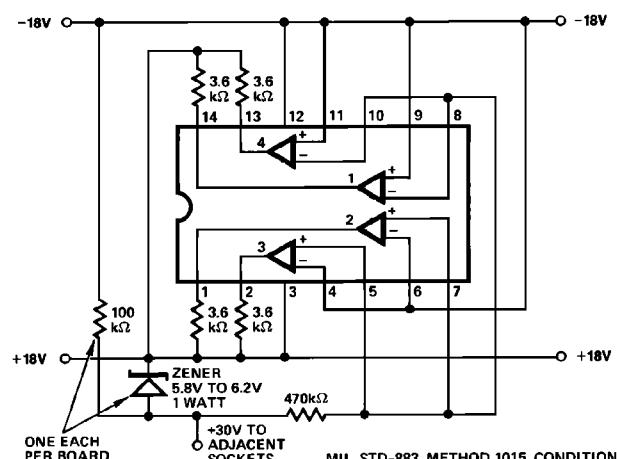
Parameter	Symbol	Conditions	CMP04B/F <sup>1</sup>			Units
			Min	Typ	Max	
Input Offset Voltage	$V_{OS}$	$R_S = 0\ \Omega$ , $R_L = 5.1\text{ k}\Omega$ $V_O = 1.4\text{ V}$ <sup>2</sup>		1	2	mV
				1	2	mV
Input Offset Current	$I_{OS}$	$I_{IN(+)} - I_{IN(-)}$ $R_L = 5.1\text{ k}\Omega$ $V_O = 1.4\text{ V}$		4	20	nA
				4	20	nA
				4	20	nA
Input Bias Current	$I_B$	$I_{IN(+)} \text{ or } I_{IN(-)}$		40	200	nA
Voltage Gain	$A_V$	$R_L \geq 15\text{ k}\Omega$ , $V_+ = 15\text{ V}$ <sup>3</sup>	70	125		V/mV
Large-Signal Response Time	$t_r$	$V_{IN} = \text{TTL Logic Swing}$ $V_{REF} = 1.4\text{ V}$ <sup>4</sup> $V_{RL} = 5\text{ V}$ , $R_L = 5.1\text{ k}\Omega$		300		ns
				300		ns
				300		ns
Small-Signal Response Time	$t_r$	$V_{IN} = 100\text{ mV Step}^4$ 5 mV Overdrive $V_{RL} = 5\text{ V}$ , $R_L = 5.1\text{ k}\Omega$		1.3		$\mu\text{s}$
				1.3		$\mu\text{s}$
				1.3		$\mu\text{s}$
Input Voltage Range	CMVR	(Note 5)	0		$V_+ - 1.5$	V
Common-Mode Rejection Ratio	CMRR	(Notes 1, 3)	60	100		dB
Power Supply Rejection Ratio	PSRR	$V_+ = +5\text{ V}$ to $18\text{ V}$	80	100		dB
Saturation Voltage	$V_{OL}$	$V_{IN(-)} \geq 1\text{ V}$ , $V_{IN(+)} = 0$ , $I_{SINK} \leq 4\text{ mA}$		250	700	mV
				250	700	mV
Output Sink Current	$I_{SINK}$	$V_{IN(-)} \geq 1\text{ V}$ , $V_{IN(+)} = 0$ , $V_O \leq 1.5\text{ V}$	5	16		mA
			5	16		mA
Output Leakage Current	$I_{LEAK}$	$V_{IN(+)} \geq 1\text{ V}$ , $V_{IN(-)} = 0$ , $V_O = 30\text{ V}$		0.1	200	nA
				0.1	200	nA
Supply Current	$I_+$	$R_L = \infty$ , All Comps $V_+ = 30\text{ V}$		1.2	3.0	mA
				1.2	3.0	mA

## NOTES

<sup>1</sup>  $R_L \geq 15\text{ k}\Omega$ ,  $V_+ = 15\text{ V}$ ,  $V_{CM} = 1.5\text{ V}$  to  $13.5\text{ V}$ .<sup>2</sup> At output switch point,  $V_O = 1.4\text{ V}$ ,  $R_S = 0\ \Omega$  with  $V_+$  from  $5\text{ V}$ ; and over the full input common-mode range ( $0\text{ V}$  to  $V_+ - 1.5\text{ V}$ ).<sup>3</sup> Guaranteed by design.<sup>4</sup> Sample tested.<sup>5</sup> The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than  $0.3\text{ V}$ . The upper end of the common-mode voltage range is  $V_+ - 1.5\text{ V}$ , but either or both inputs can go to  $+30\text{ V}$  without damage.

Specifications subject to change without notice.

## BURN-IN CIRCUIT



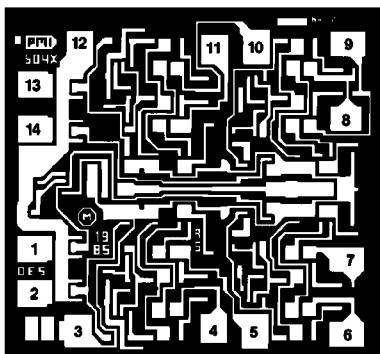
MIL-STD-883, METHOD 1015, CONDITION B

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as  $4000\text{ V}$  readily accumulate on the human body and test equipment and can discharge without detection. Although the CMP04 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## DICE CHARACTERISTICS



- |                           |                            |
|---------------------------|----------------------------|
| 1. OUTPUT (2)             | 8. INVERTING INPUT (3)     |
| 2. OUTPUT (1)             | 9. NONINVERTING INPUT (3)  |
| 3. POSITIVE SUPPLY        | 10. INVERTING INPUT (4)    |
| 4. INVERTING INPUT (1)    | 11. NONINVERTING INPUT (4) |
| 5. NONINVERTING INPUT (1) | 12. GROUND (SUBSTRATE)     |
| 6. INVERTING INPUT (2)    | 13. OUTPUT (4)             |
| 7. NONINVERTING INPUT (2) | 14. OUTPUT (3)             |

DIE SIZE 0.058 X 0.055 inch, 3190 sq. mils  
(1.47 X 1.40 mm, 2.058 sq. mm)

WAFER TEST LIMITS (@V<sub>I</sub> = +5 V, T<sub>A</sub> = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	CMP04N Limit	CMP04G Limit	Units
Input Offset Voltage	V <sub>OS</sub>	R <sub>S</sub> = 0 Ω, R <sub>L</sub> = 5.1 kΩ V <sub>O</sub> = 1.4 V <sup>1</sup>	1	2	mV max
Input Offset Current	I <sub>OS</sub>	I <sub>IN(+)</sub> - I <sub>IN(-)</sub> R <sub>L</sub> = 5.1 kΩ V <sub>O</sub> = 1.4 V	10	25	nA max
Input Bias Current	I <sub>B</sub>	I <sub>IN(+)</sub> or I <sub>IN(-)</sub> <sup>1</sup>	100	100	nA max
Voltage Gain	A <sub>V</sub>	R <sub>L</sub> ≥ 15 kΩ, V <sub>+</sub> = 15 V <sup>3</sup>	80	50	V/mV min
Input Voltage Range	CMVR	(Notes 2, 3)	V <sub>+</sub> -1.5	V <sub>+</sub> -1.5	V max
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB min
Power Supply Rejection Ratio	PSRR	V <sub>+</sub> = 5 V to +18 V	80	80	dB min
Saturation Voltage	V <sub>OL</sub>	V <sub>IN(-)</sub> ≥ 1 V, V <sub>IN(+)</sub> = 0, I <sub>SINK</sub> ≤ 4 mA	400	400	mV max
Output Sink Current	I <sub>SINK</sub>	V <sub>IN(-)</sub> ≥ 1 V, V <sub>IN(+)</sub> = 0, V <sub>O</sub> ≤ 1.5 V	6	6	mA min
Output Leakage Current	I <sub>LEAK</sub>	V <sub>IN(+)</sub> ≥ 1 V, V <sub>IN(-)</sub> = 0, V <sub>O</sub> = 30 V	100	100	nA max
Supply Current	I <sub>+</sub>	R <sub>L</sub> = ∞, All Comps V <sub>+</sub> = 30 V	2	2	mA max

## NOTES

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS (@V<sub>I</sub> = +5 V, unless otherwise noted.)

Parameter	Symbol	Conditions	CMP04N Typical	CMP04G Typical	Units
Large-Signal Response Time	t <sub>r</sub>	V <sub>IN</sub> = TTL Logic Swing V <sub>REF</sub> = 1.4 V <sup>5</sup> V <sub>RL</sub> = 5 V, R <sub>L</sub> = 5.1 kΩ	600	600	ns
Small-Signal Response Time	t <sub>r</sub>	V <sub>IN</sub> = 100 mV Step <sup>5</sup> 5 mV Overdrive V <sub>RL</sub> = 5 V, R <sub>L</sub> = 5.1 kΩ	1.3	1.3	μs

## NOTES

<sup>1</sup>At output switch point, V<sub>O</sub> = 1.4 V, R<sub>S</sub> = 0 Ω with V<sub>+</sub> from 5 V; and over the full input common-mode range (0 V to V<sub>+</sub> - 1.5 V).

<sup>2</sup>The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the

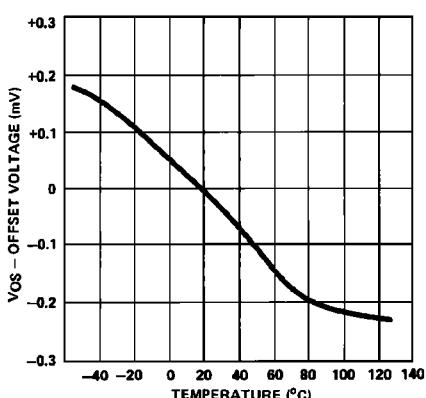
common-mode voltage range is V<sub>+</sub> - 1.5 V, but either or both inputs can go to +30 V without damage.

<sup>3</sup>Guaranteed by design.

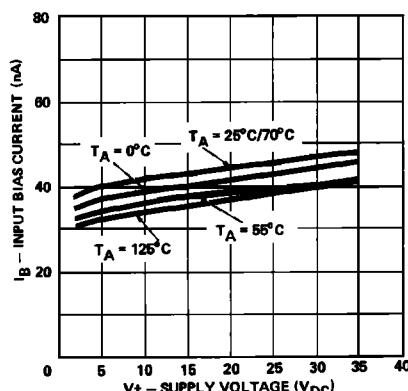
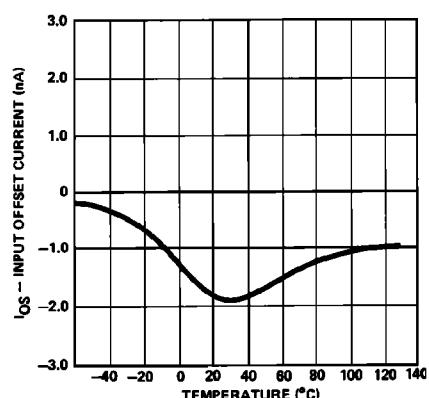
<sup>4</sup>R<sub>L</sub> ≥ 15 kΩ, V<sub>CM</sub> = 1.5 V to 13.5 V.

<sup>5</sup>Sample tested.

## TYPICAL PERFORMANCE CHARACTERISTICS



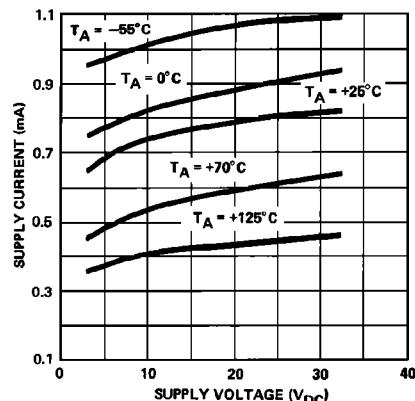
Offset Voltage vs. Temperature

Input Bias Current vs.  $V_+$  and Temperature

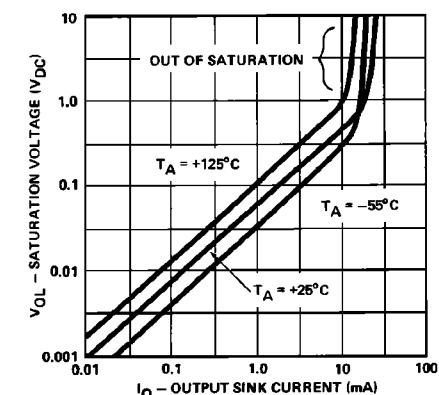
Input Offset Current vs. Temperature



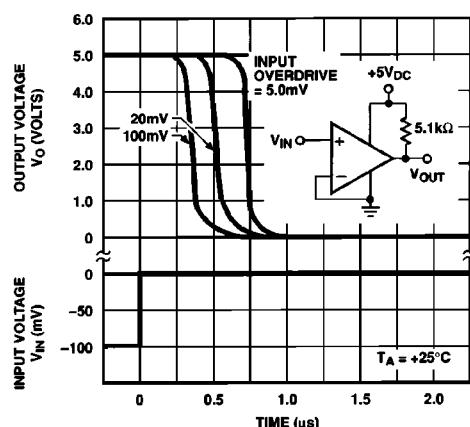
Voltage Gain vs. Temperature



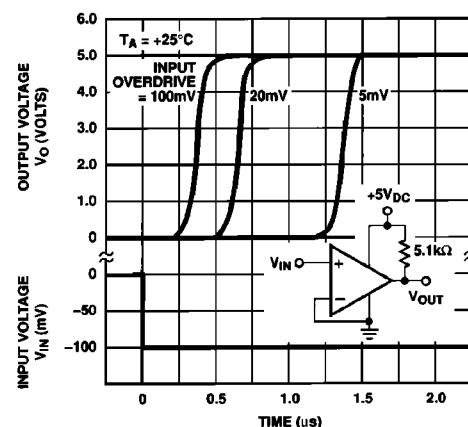
Supply Current vs. Supply Voltage



Output Voltage vs. Output Current and Temperature



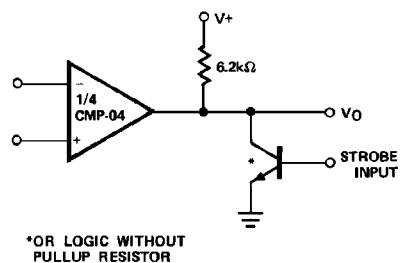
Response Time for Various Input Overdrives—Negative Transition



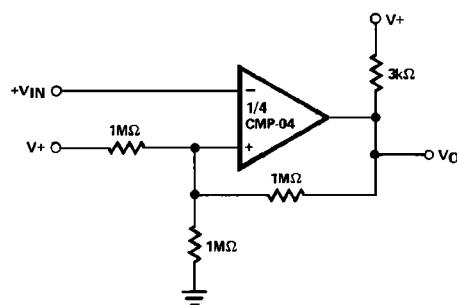
Response Time for Various Input Overdrives—Positive Transition

# CMPO4

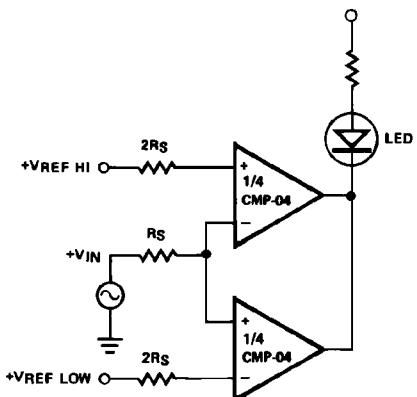
## TYPICAL APPLICATIONS



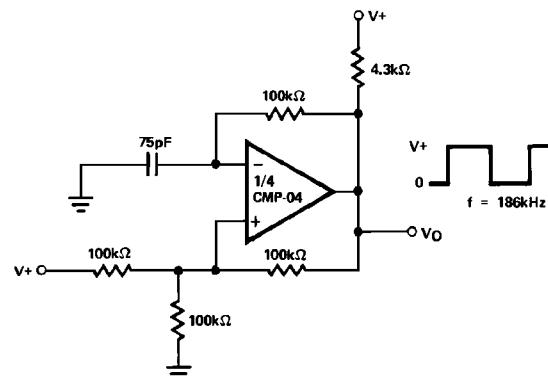
*Output Strobing*



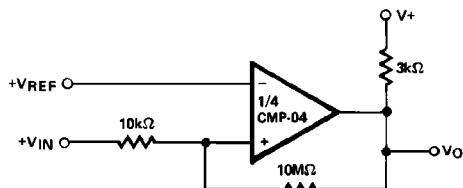
*Inverting Comparator with Hysteresis*



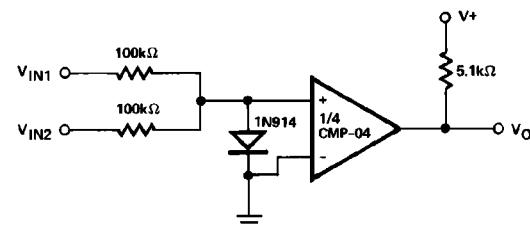
*Limit Comparator*



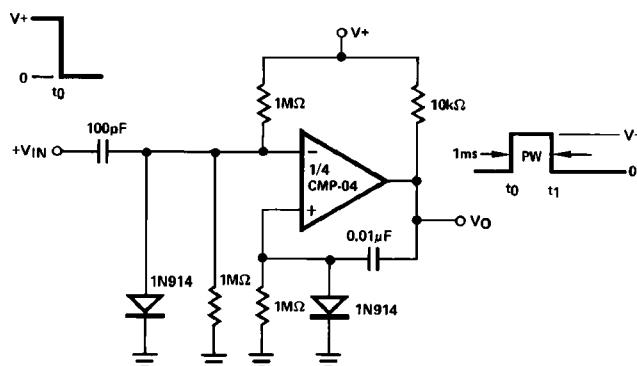
*Squarewave Oscillator*



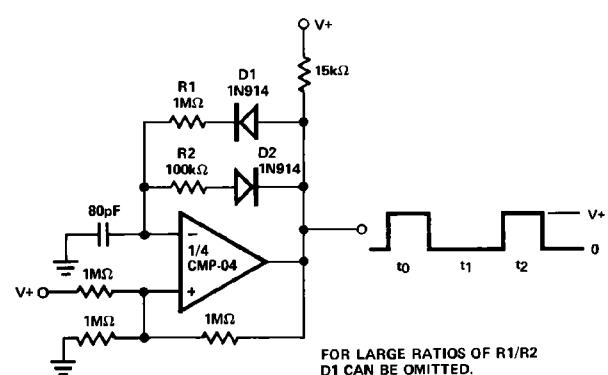
*Noninverting Comparator with Hysteresis*



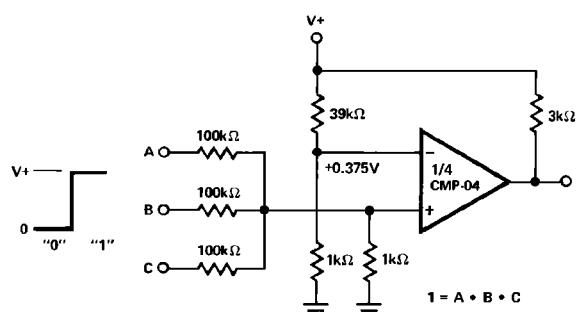
*Comparing Input Voltages of Opposite Polarity*



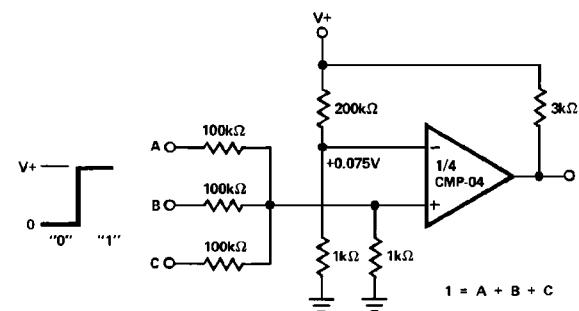
One-Shot Multivibrator



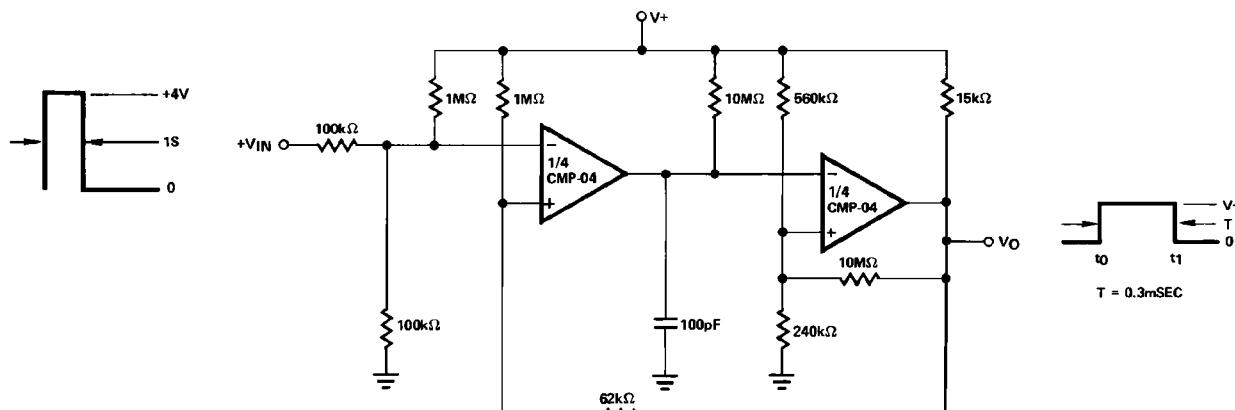
Pulse Generator



And Gate



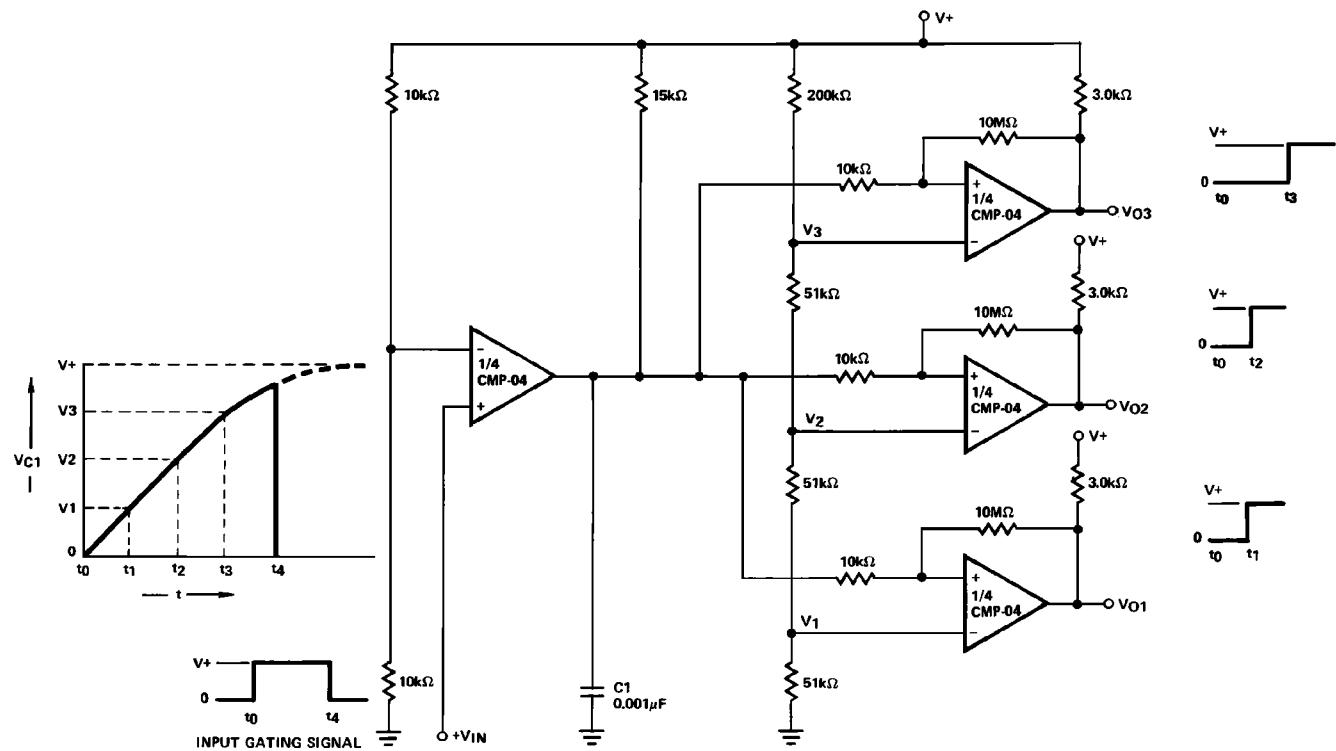
Or Gate



One-Shot Multivibrator with Input Lock Out

AMP04

## TYPICAL APPLICATIONS



## *Time Delay Generator*

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