Very Low Power CMOS SRAM
1M X 16 bit

Green package materials are compliant to RoHS

BS616LV1611

■ FEATURES

- Wide V_{CC} operation voltage : 2.4V ~ 5.5V
- Very low power consumption :
  - V_{CC} = 3.0V Operation current : 46mA (Max.)at 55ns
    2mA (Max.)at 1MHz
    Standby current : 16uA (Max.) at 85 ^{O}C
  - V_{CC} = 5.0V Operation current : 115mA (Max.)at 55ns
    10mA (Max.)at 1MHz
    Standby current : 100uA (Max.) at 85^{O}C
- High speed access time :
  - -55 55ns(Max.) at V_{CC}=3.0~5.5V
  - -70 70ns(Max.) at V_{CC}=2.7~5.5V
- Automatic power down when chip is deselected
- Easy expansion with CE2, $\overline{CE1}$ and $\overline{OE}$ options
- I/O Configuration x8/x16 selectable by $\overline{LB}$ and $\overline{UB}$ pin.
- Three state outputs and TTL compatible
- Fully static operation, no clock, no refresh
- Data retention supply voltage as low as 1.5V

■ DESCRIPTION

The BS616LV1611 is a high performance, very low power CMOS Static Random Access Memory organized as 1,048,576 by 16 bits and operates form a wide range of 2.4V to 5.5V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with maximum CMOS standby current of 16/100uA at Vcc=3/5V at 85^{O}C and maximum access time of 55/70ns.

Easy memory expansion is provided by an active LOW chip enable ($\overline{CE1}$), active HIGH chip enable (CE2) and active LOW output enable ($\overline{OE}$) and three-state output drivers.

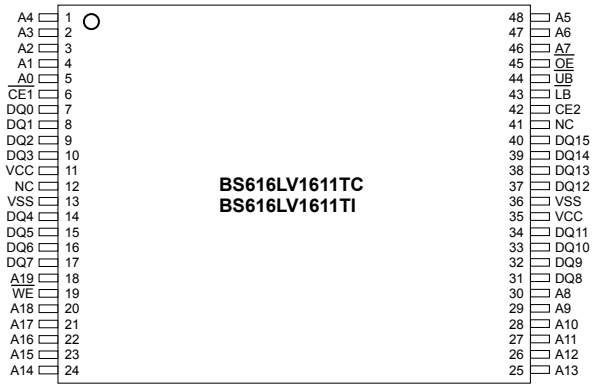
The BS616LV1611 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

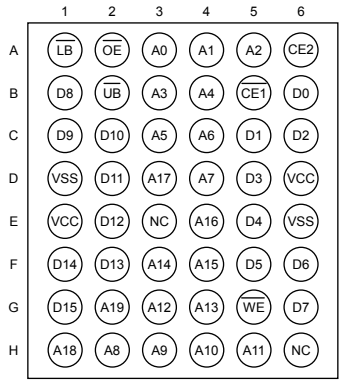
The BS616LV1611 is available in 48-pin TSOP Type I package and 48-ball BGA package.

■ POWER CONSUMPTION

PRODUCT FAMILY	OPERATING TEMPERATURE	POWER DISSIPATION								PKG TYPE
		STANDBY (I_{CCSB1}, Max)		Operating (I_{CC}, Max)						
				V_{CC}=5.0V			V_{CC}=3.0V			
		V_{CC}=5.0V	V_{CC}=3.0V	1MHz	10MHz	$f_{Max.}$	1MHz	10MHz	$f_{Max.}$	
BS616LV1611FI	Industrial -40^{O}C to +85^{O}C	100uA	16uA	10mA	50mA	115mA	2mA	20mA	46mA	BGA-48-0912
BS616LV1611TI										TSOP I-48

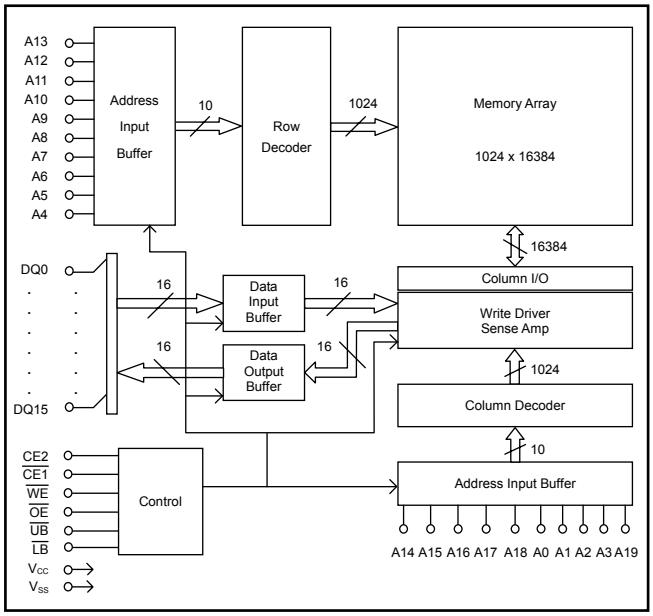
■ PIN CONFIGURATIONS





48-ball BGA top view

■ BLOCK DIAGRAM



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■ PIN DESCRIPTIONS

Name	Function
A0-A19 Address Input	These 20 address inputs select one of the 1,048,576 x 16 bit in the RAM
$\overline{CE1}$ Chip Enable 1 Input **CE2 Chip Enable 2 Input**	$\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read form or write to the device. If either chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impendence state when $\overline{OE}$ is inactive.
$\overline{LB}$ and $\overline{UB}$ Data Byte Control Input	Lower byte and upper byte data input/output control pins.
DQ0-DQ15 Data Input/Output Ports	16 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power Supply
V_{SS}	Ground

■ TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ0~DQ7	DQ8~DQ15	V_{CC} CURRENT
Chip De-selected (Power Down)	H	X	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
	X	L	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
	X	X	X	X	H	H	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	L	X	High Z	High Z	I_{CC}
	L	H	H	H	X	L	High Z	High Z	I_{CC}
Read	L	H	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
					H	L	High Z	D_{OUT}	I_{CC}
					L	H	D_{OUT}	High Z	I_{CC}
Write	L	H	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
					H	L	X	D_{IN}	I_{CC}
					L	H	D_{IN}	X	I_{CC}

NOTES: H means V_{IH}; L means V_{IL}; X means don't care (Must be V_{IH} or V_{IL} state)

■ ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(2) to 7.0	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. –2.0V in case of AC pulse width less than 30 ns.

■ OPERATING RANGE

RANG	AMBIENT TEMPERATURE	V_{CC}
Commercial	$0^{O}C$ to + $70^{O}C$	2.4V ~ 5.5V
Industrial	$-40^{O}C$ to + $85^{O}C$	2.4V ~ 5.5V

■ CAPACITANCE (1) (T_A = 25^{O}C, f = 1.0MHz)

SYMBOL	PAMAMETER	CONDITIONS	MAX.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{IO}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS (T_A = -40^{O}C to +85^{O}C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNITS
V_{CC}	Power Supply			2.4	--	5.5	V
V_{IL}	Input Low Voltage			-0.5(2)	--	0.8	V
V_{IH}	Input High Voltage			2.2	--	V_{CC}+0.3(3)	V
I_{IL}	Input Leakage Current	V_{IN} = 0V to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		--	--	1	uA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH}		--	--	1	uA
V_{OL}	Output Low Voltage	V_{CC} = Max, I_{OL} = 2.0mA		--	--	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1.0mA		2.4	--	--	V
I_{CC}(5)	Operating Power Supply Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH}, I_{DQ} = 0mA, f = F_{MAX}(4)	V_{CC}=3.0V	--	--	46	mA
			V_{CC}=5.0V			115	
I_{CC1}	Operating Power Supply Current	$\overline{CE1}$ = V_{IL} and CE2 = V_{IH}, I_{DQ} = 0mA, f = 1MHz	V_{CC}=3.0V	--	--	2	mA
			V_{CC}=5.0V			10	
I_{CCSB}	Standby Current – TTL	$\overline{CE1}$ = V_{IH}, or CE2 = V_{IL}, I_{DQ} = 0mA	V_{CC}=3.0V	--	--	1.0	mA
			V_{CC}=5.0V			2.0	
I_{CCSB1}(6)	Standby Current – CMOS	$\overline{CE1} \geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V, $V_{IN} \geqq V_{CC}$-0.2V or $V_{IN} \leqq$ 0.2V	V_{CC}=3.0V	--	1.5	16	uA
			V_{CC}=5.0V		6.0	100	

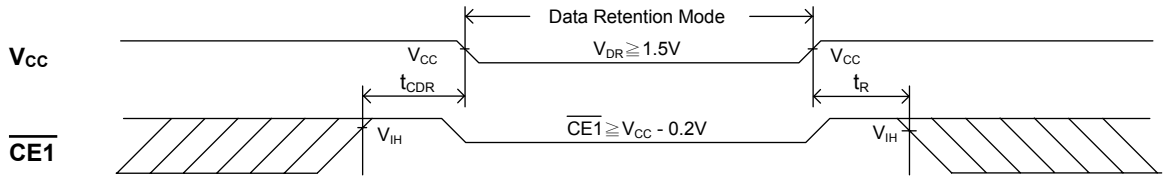
1. Typical characteristics are at T_A=25^{O}C and not 100% tested.
2. Undershoot: -1.0V in case of pulse width less than 20 ns.
3. Overshoot: V_{CC}+1.0V in case of pulse width less than 20 ns.
4. F_{MAX}=1/t_{RC}.
5. $I_{CC\ (MAX.)}$ is 45mA/113mA at V_{CC}=3.0V/5.0V and T_A=70^{O}C.
6. $I_{CCSB1(MAX.)}$ is 8.0uA/50uA at V_{CC}=3.0V/5.0V and T_A=70^{O}C.

■ DATA RETENTION CHARACTERISTICS (T_A = -40°C to +85°C)

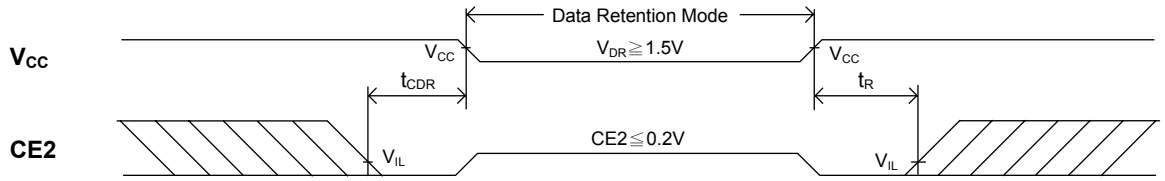
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{CE1} \geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V, $V_{IN} \geqq V_{CC}$-0.2V or $V_{IN} \leqq$ 0.2V	1.5	--	--	V
I_{CCDR} (3)	Data Retention Current	$\overline{CE1} \geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V, $V_{IN} \geqq V_{CC}$-0.2V or $V_{IN} \leqq$ 0.2V	--	0.8	8.0	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		t_{RC} (2)	--	--	ns

1. V_{CC}=1.5V, T_A=25°C and not 100% tested.
2. t_{RC} = Read Cycle Time.
3. $I_{CCDR(Max.)}$ is 4.0uA at T_A=70°C.

■ LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)



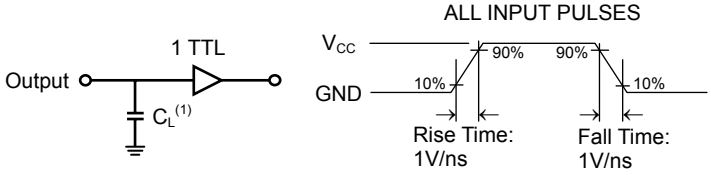
■ LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



■ AC TEST CONDITIONS

(Test Load and Input/Output Reference)

Input Pulse Levels		Vcc / 0V
Input Rise and Fall Times		1V/ns
Input and Output Timing Reference Level		0.5Vcc
Output Load	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}	C_L = 5pF+1TTL
	Others	C_L = 30pF+1TTL



1. Including jig and scope capacitance.

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOW
	DOES NOT APPLY	CENTER LINE IS HIGH INPEDANCE "OFF" STATE

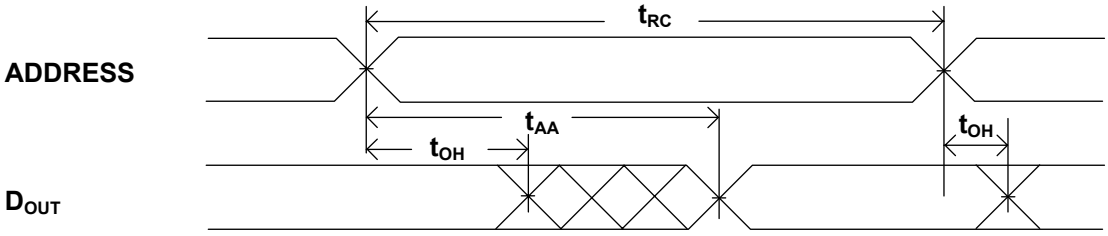
■ AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

READ CYCLE

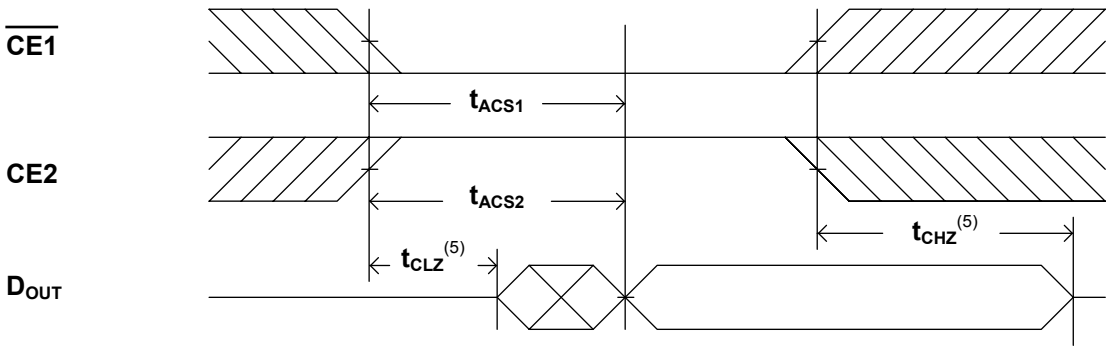
JEDEC PARAMETER NAME	PARANETER NAME	DESCRIPTION	CYCLE TIME : 55ns (V_{CC}=3.0~5.5V)			CYCLE TIME : 70ns (V_{CC}=2.7~5.5V)			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	55	--	--	70	--	--	ns
t_{AVQX}	t_{AA}	Address Access Time	--	--	55	--	--	70	ns
t_{ELQV1}	t_{ACS1}	Chip Select Access Time ($\overline{CE1}$)	--	--	55	--	--	70	ns
t_{ELQV2}	t_{ACS2}	Chip Select Access Time (CE2)	--	--	55	--	--	70	ns
t_{BLQV}	t_{BA}	Data Byte Control Access Time ($\overline{LB}$, $\overline{UB}$)	--	--	55	--	--	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	30	--	--	35	ns
t_{ELQX1}	t_{CLZ1}	Chip Select to Output Low Z ($\overline{CE1}$)	10	--	--	10	--	--	ns
t_{ELQX2}	t_{CLZ2}	Chip Select to Output Low Z (CE2)	10	--	--	10	--	--	ns
t_{BLQX}	t_{BE}	Data Byte Control to Output Low Z ($\overline{LB}$, $\overline{UB}$)	10	--	--	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	5	--	--	5	--	--	ns
t_{EHQZ1}	t_{CHZ1}	Chip Select to Output High Z ($\overline{CE1}$)	--	--	30	--	--	35	ns
t_{EHQZ2}	t_{CHZ2}	Chip Select to Output High Z (CE2)	--	--	30	--	--	35	ns
t_{BHQZ}	t_{BDO}	Data Byte Control to Output High Z ($\overline{LB}$, $\overline{UB}$)	--	--	30	--	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Enable to Output High Z	--	--	25	--	--	30	ns
t_{AVQX}	t_{OH}	Data Hold from Address Change	10	--	--	10	--	--	ns

■ SWITCHING WAVEFORMS (READ CYCLE)

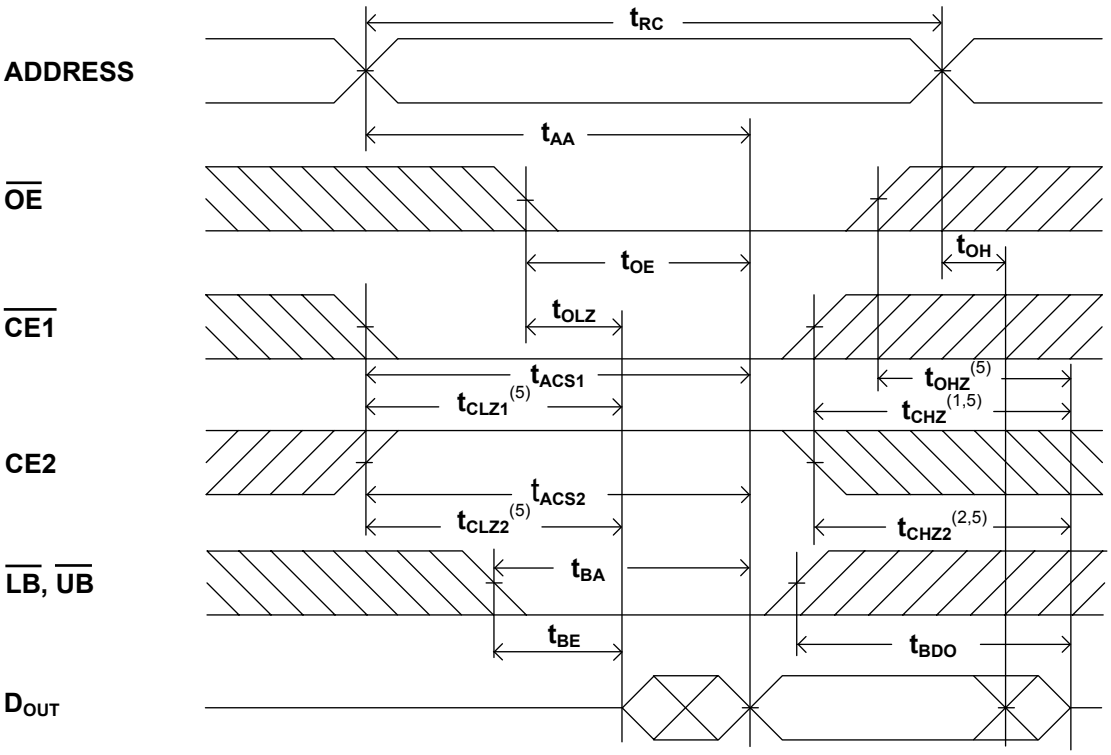
READ CYCLE 1 (1,2,4)



READ CYCLE 2 (1,3,4)



READ CYCLE 3 (1, 4)



NOTES:
1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE1}$ = V_{IL} and CE2= V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and/or CE2 transition high.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ± 500mV from steady state with C_L = 5pF.
   The parameter is guaranteed but not 100% tested.

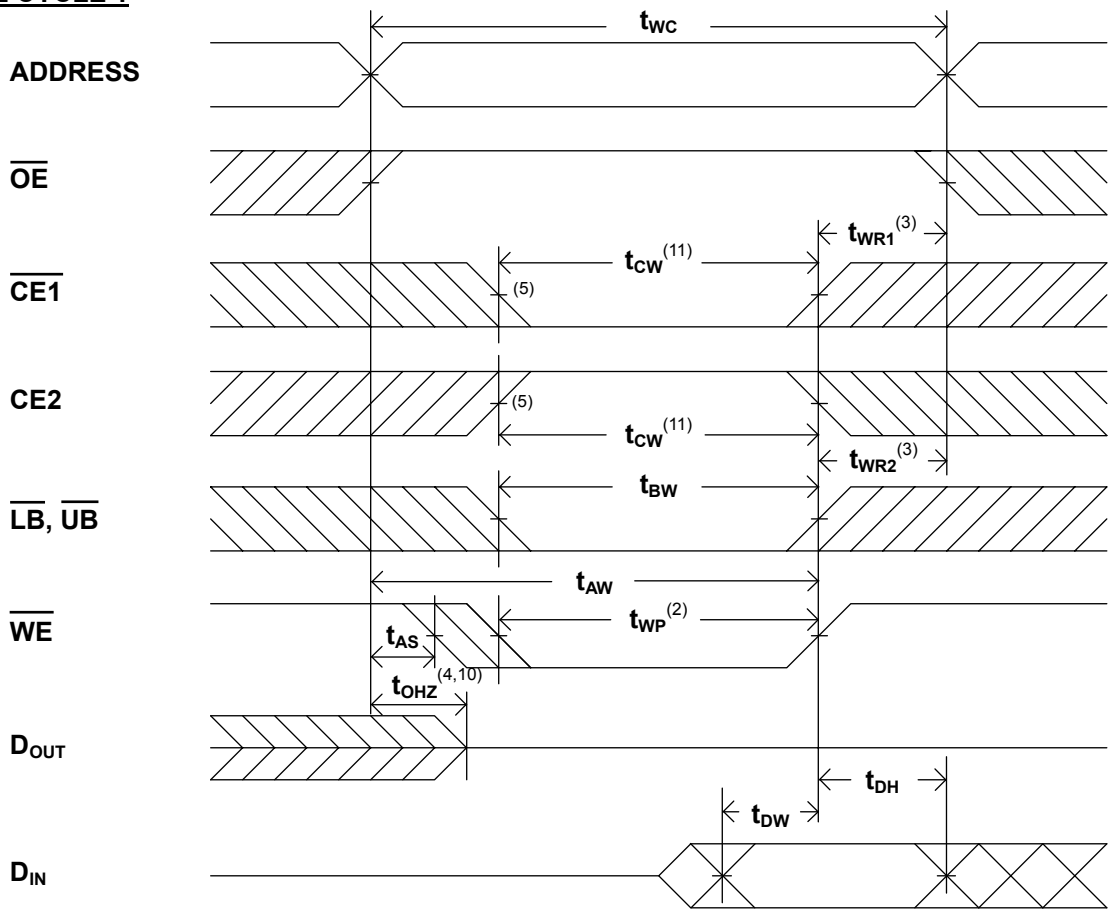
■ AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

WRITE CYCLE

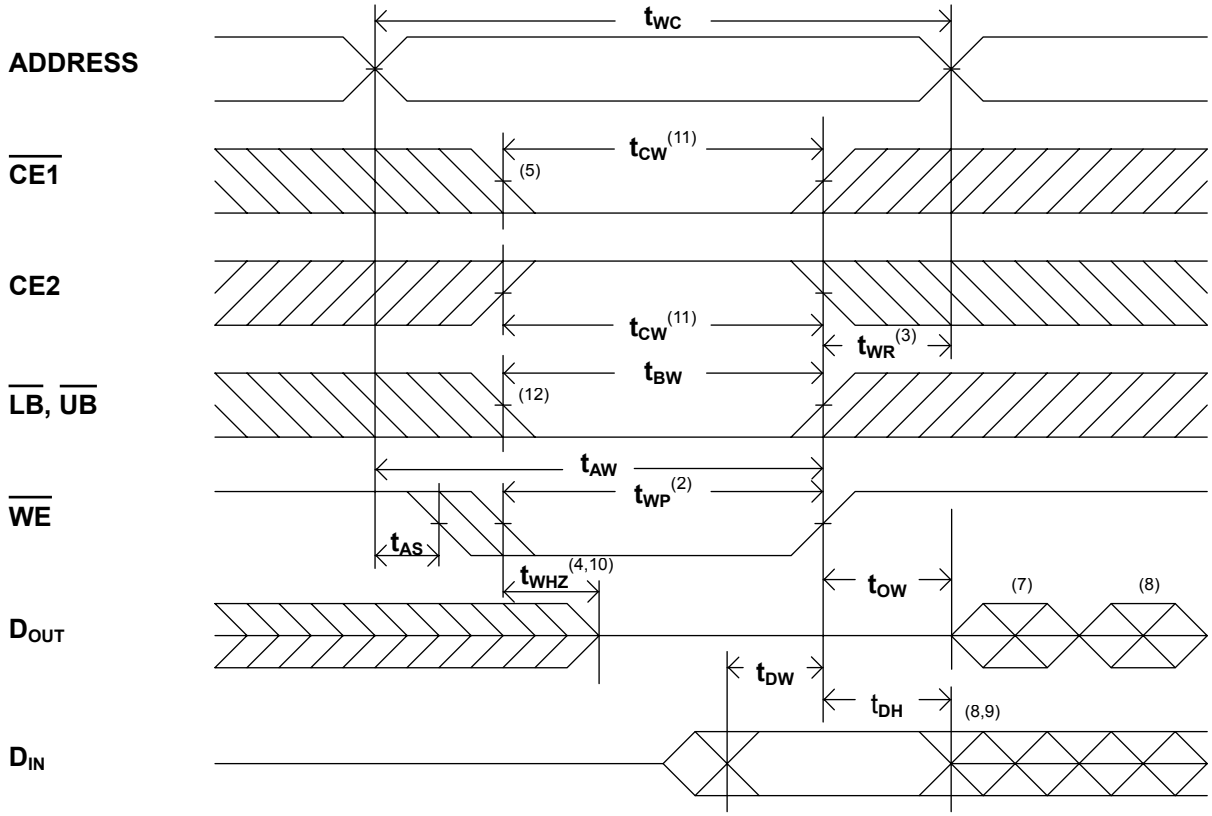
JEDEC PARAMETER NAME	PARANETER NAME	DESCRIPTION	CYCLE TIME : 55ns (V_{CC}=3.0~5.5V)			CYCLE TIME : 70ns (V_{CC}=2.7~5.5V)			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	55	--	--	70	--	--	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	55	--	--	70	--	--	ns
t_{ELWH}	t_{CW}	Chip Select to End of Write	55	--	--	70	--	--	ns
t_{BLWH}	t_{BW}	Data Byte Control to End of Write ($\overline{LB}$, $\overline{UB}$)	25	--	--	30	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	30	--	--	35	--	--	ns
t_{WHAX1}	t_{WR1}	Write Recovery Time ($\overline{CE1}$, $\overline{WE}$)	0	--	--	0	--	--	ns
t_{WHAX2}	t_{WR2}	Write Recovery Time (CE2)	0	--	--	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output High Z	--	--	25	--	--	30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25	--	--	30	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	25	--	--	30	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	--	--	5	--	--	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (1)



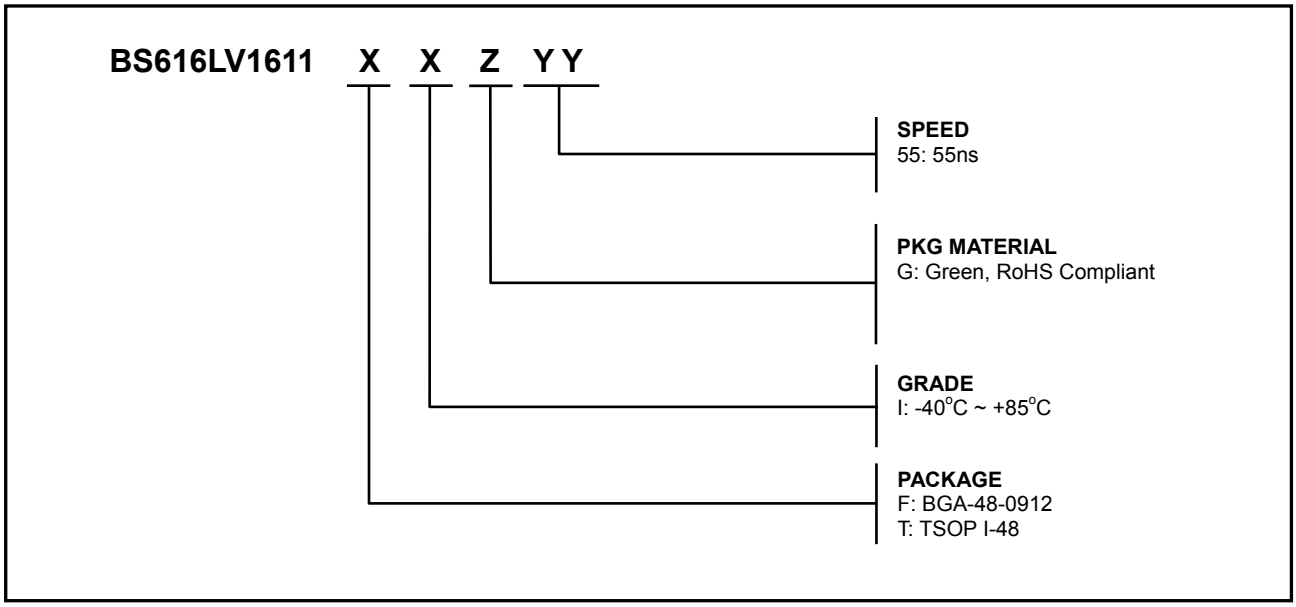
WRITE CYCLE 2 (1,6)



NOTES:

1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{WR} is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE1}$ is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state with C_L = 5pF.
    The parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.
12. The change of Read/Write cycle must accompany with CE or address toggled.

■ ORDERING INFORMATION



Note:
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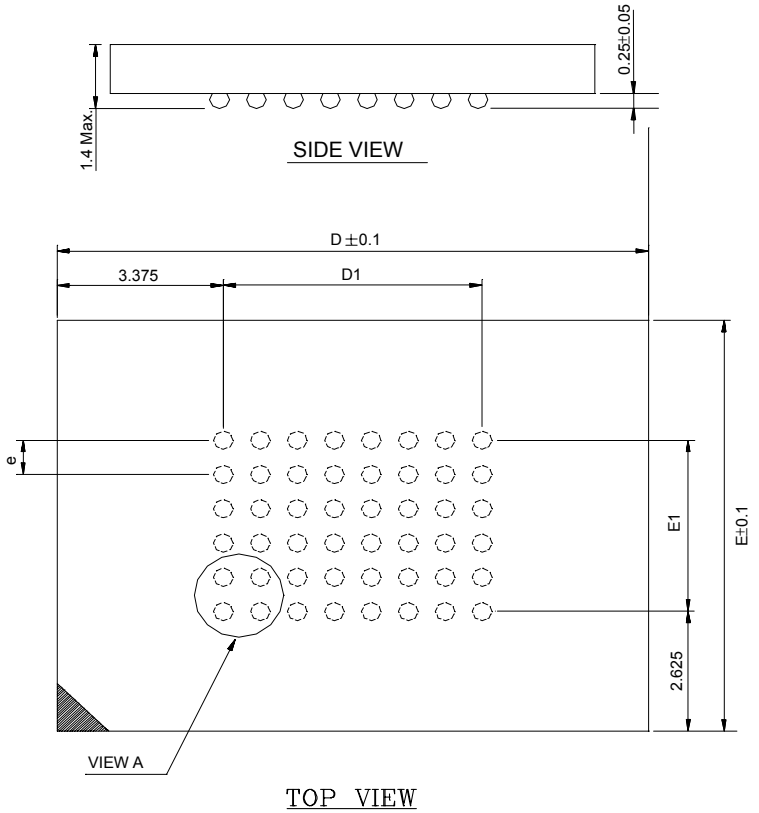
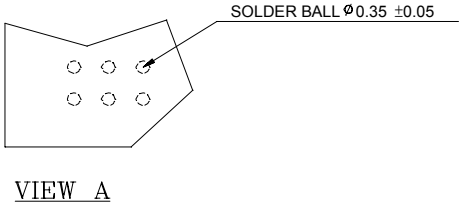
■ PACKAGE DIMENSIONS



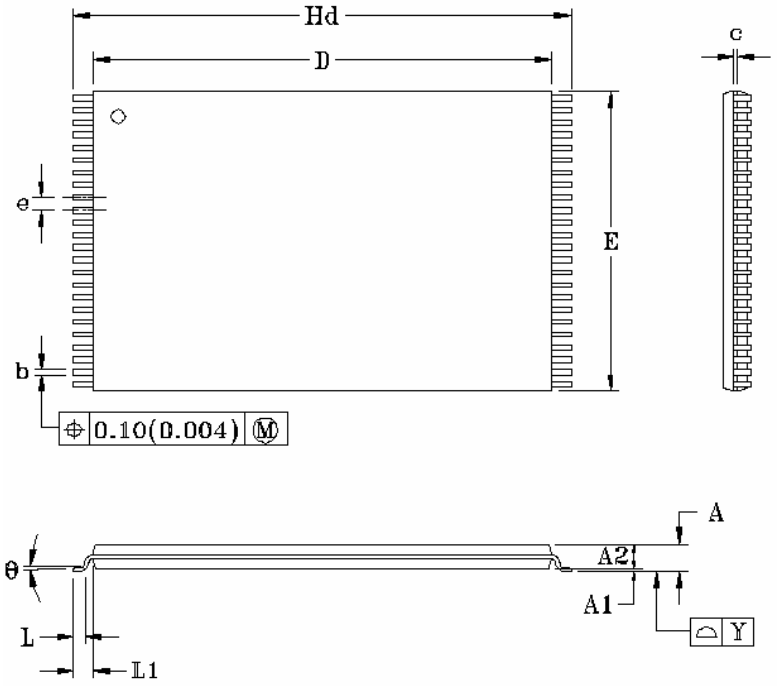
NOTES:
1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

N	D	E	D1	E1	e
48	12.0	9.0	5.25	3.75	0.75



48 mini-BGA (9mm x 12mm)

■ PACKAGE DIMENSIONS



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.23	0.007	0.008	0.009
c	0.10	0.125	0.15	0.004	0.005	0.006
D	18.30	18.40	18.50	0.720	0.724	0.728
E	11.90	12.00	12.10	0.468	0.472	0.476
Hd	19.80	20.00	20.20	0.780	0.787	0.795
e		0.50			0.020	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.80			0.031	
Y	0.00		0.10	0.000		0.004
θ	1°	3°	5°	1°	3°	5°

TSOP I-48 Pin (12mm x 20mm)

■ Revision History

Revision No.	History	Draft Date	Remark
2.2	Add Icc1 characteristic parameter Improve Iccsb1 spec. I-grade from 220uA to 100uA at 5.0V 20uA to 16uA at 3.0V C-grade from 110uA to 50uA at 5.0V 10uA to 8.0uA at 3.0V	Jan. 13, 2006	
2.3	Change I-grade operation temperature range - from –25°C to –40°C	May. 25, 2006	
2.4	Typical value of standby current is replaced by maximum value in Featues and Description section Remove “-: Normal” (Leaded) PKG Material in ordering information	Oct. 31, 2008	