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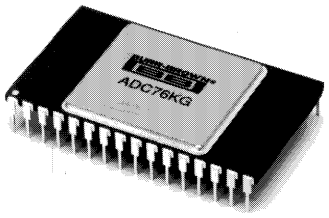


ADC76

16-Bit
ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **16-BIT RESOLUTION**
- **LINEARITY ERROR: ±0.003% max (KG, BG)**
- **NO MISSING CODES GUARANTEED FROM –25°C TO +85°C**
- **17μs CONVERSION TIME (16-Bit)**
- **SERIAL AND PARALLEL OUTPUTS**

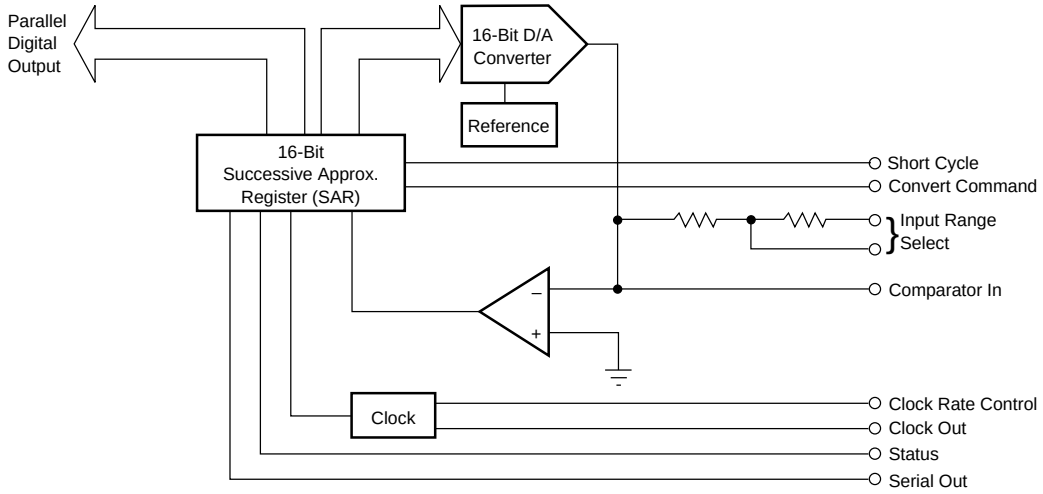
DESCRIPTION

The ADC76 is a high quality, 16-bit successive approximation analog-to-digital converter. The ADC76 uses state-of-the-art laser-trimmed IC thin-film resistors and is packaged in a hermetic 32-pin dual-in-line package. The converter is complete with internal reference, short cycling capabilities, serial output, and thin-film scaling resistors, which allow selection of analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V.

It is specified for operation over two temperature ranges: 0°C to +70°C (J, K) and –25°C to +85°C (A, B).

Data is available in parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL-compatible.

Power supply voltages are ±15VDC and +5VDC.



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SPECIFICATIONS

ELECTRICAL

At +25°C, and rated power supplies, unless otherwise noted.

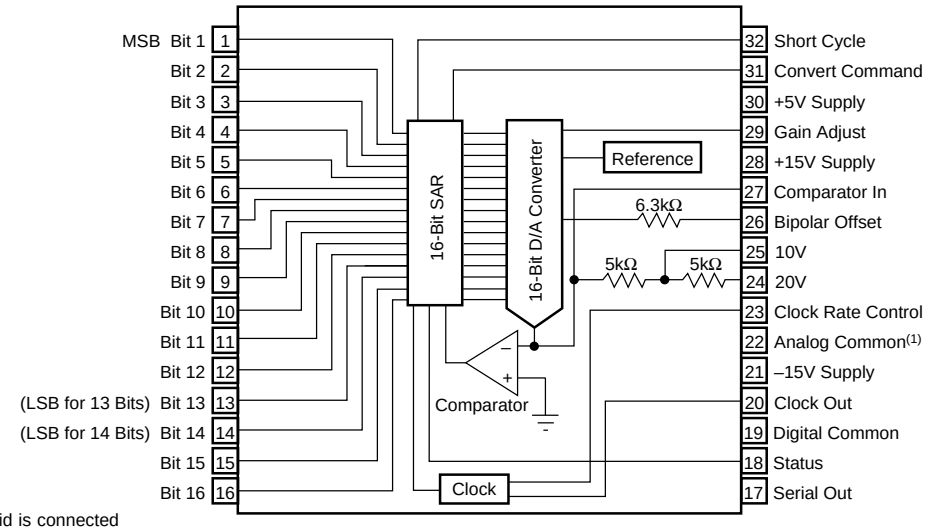
MODEL	ADC76J, K MIN	ADC76J, K TYP	ADC76J, K MAX	ADC76A, B MIN	ADC76A, B TYP	ADC76A, B MAX	UNITS
RESOLUTION			16			*	Bits
ANALOG INPUTS							
Voltage Ranges: Bipolar		±2.5, ±5, ±10			*		V
Unipolar		0 to +5, 0 to +10			*		V
		0 to +20			*		
Impedance (Direct Input)							
0 to +5V, ±2.5V		2.5			*		kΩ
0 to +10V, ±5.0V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
DIGITAL INPUTS(1)							
Convert Command		Positive pulse 50ns wide (min) trailing edge ("1" to "0" initiates conversion)					
Logic Loading			1			*	TTL Load
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(2)		±0.1	±0.2		*	*	%
Offset Error: Unipolar(2)		±0.05	±0.1		*	*	% of FSR(3)
Bipolar(2)		±0.1	±0.2		*	*	% of FSR
Linearity Error: K, B			±0.003			*	% of FSR
J, A			±0.006			*	% of FSR
Inherent Quantization Error		±1/2			*		LSB
Differential Linearity Error		±0.003			*		% of FSR
Noise (3σ, p-p)		±0.001	±0.003		*	*	% of FSR
POWER SUPPLY SENSITIVITY							
±15VDC		0.003			*		% of FSR/%V_S
+5VDC		0.001			*		% of FSR/%V_S
CONVERSION TIME(4)							
14 Bits			15			*	µs
15 Bits			16			*	µs
16 Bits			17			*	µs
WARM-UP TIME	5			*			Min
DRIFT							
Gain			±15			*	ppm/°C
Offset: Unipolar		±2	±4		*	*	ppm of FSR/°C
Bipolar			±10			*	ppm of FSR/°C
Linearity		±2	±3		*	*	ppm of FSR/°C
No Missing Codes Temp Range							
J, A (13-bit)	0		+70	–25		+85	°C
K, B (14-bit)	0		+70	–25		+85	°C
OUTPUT DIGITAL DATA							
(All codes complementary)							
Parallel							
Output Codes(5): Unipolar		CSB			*		
Bipolar		COB, CTC(6)			*		
Output Drive			2			*	TTL Loads
Serial Data Code (NRZ)		CSB, COB			*		
Output Drive			2			*	TTL Loads
Status		Logic "1" during conversion			*		
Status Output Drive			2			*	TTL Loads
Internal Clock: Clock Output Drive			2			*	TTL Loads
Frequency(7)	933		1400	*		*	kHz
POWER SUPPLY REQUIREMENTS							
Power Consumption		0.655			*		W
Rated Voltage: Analog	±11.4	±15	±16	*	*	*	VDC
Digital	+4.75	+5	+5.25	*	*	*	VDC
Supply Drain: +15VDC		+10	+15		*	*	mA
–15VDC		–28	–35		*	*	mA
+5VDC		+17	+20		*	*	mA
TEMPERATURE RANGE							
Specification	0		+70	–25		+85	°C
Storage	–55		+125	*		*	°C

*Specification same as ADC76J, K.

NOTES: (1) CMOS/TTL compatible, i.e., Logic "0" = 0.8V, max, Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = 0.4V, max, Logic "1' = 2.4V, min. (2) Adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full Scale Range. For example, unit connected for ±10V range has 20V FSR. (4) Conversion time may be shortened with "Short Cycle" set for lower resolution and with use of Clock Rate Control. See "Optional Conversion Time Adjustment" section. The Clock Rate Control (pin 23) should be connected to Digital Common for specified conversion time. Short Cycle (pin 32) should be left open for 16-bit resolution or connected to the n + 1 digital output for n-bit resolution. For example, connect Short Cycle to Bit 15 (pin 15) for 14-bit resolution. For resolutions less than 16 bits, pin 32 should also be tied to +5V through a 2kΩ resistor. (5) See Table I. CSB = Complementary Straight Binary, COB = Complementary Offset Binary, CTC = Complementary Two's Complement. (6) CTC coding obtained by inverting MSB (pin 1). (7) Adjustable with Clock Rate Control from approximately 933kHz to 1.4MHz.

PIN CONFIGURATION

Top View **DIP**



NOTE: (1) Metal lid is connected to pin 22 (Analog Common).

ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{CC}$ to Common	0V to +16.5V
$-V_{CC}$ to Common	0V to –16.5V
$+V_{DD}$ to Common	0V to +7V
Analog Common to Digital Common	±0.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	300°C

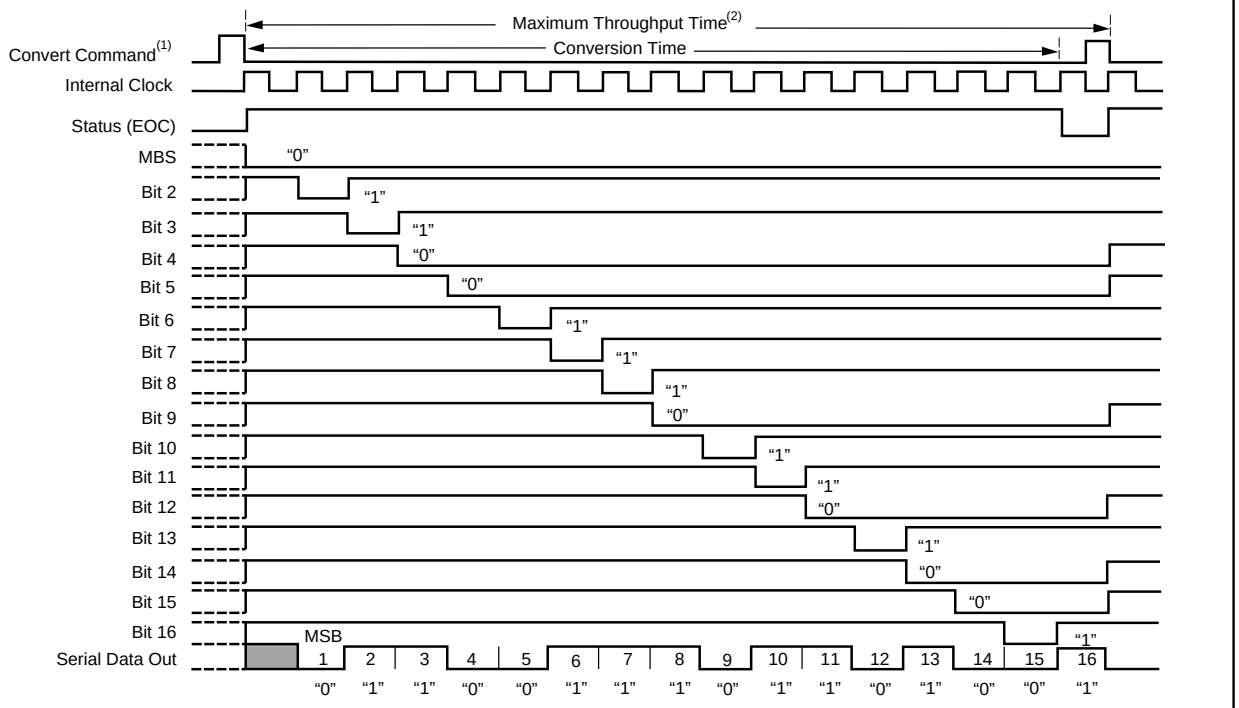
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC76JG	32-Pin Hermetic DIP	172-5
ADC76KG	32-Pin Hermetic DIP	172-5
ADC76AG	32-Pin Hermetic DIP	172-5
ADC76BG	32-Pin Hermetic DIP	172-5

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	LINEARITY ERROR max (% of FSR)	TEMPERATURE RANGE
ADC76AG	±0.006	–25°C to +85°C
ADC76BG	±0.003	–25°C to +85°C
ADC76JG	±0.006	0°C to +70°C
ADC76KG	±0.003	0°C to +70°C



NOTES: (1) The convert command must be at least 50ns wide and must remain low during a conversion. The conversion is initiated by the "trailing edge" of the convert command. (2) 17µs for 16 bits.

FIGURE 1. ADC76 Timing Diagram.

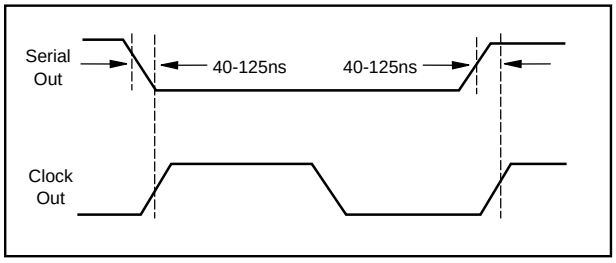


FIGURE 2. Timing Relationship of Serial Data to Clock.

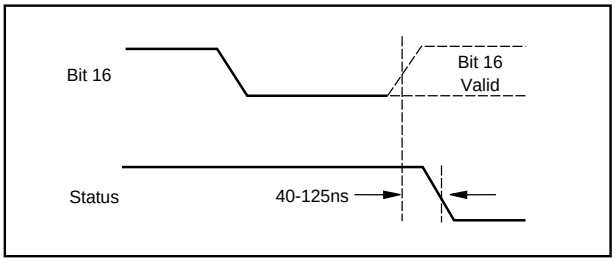


FIGURE 3. Timing Relationship of Valid Data to Status.

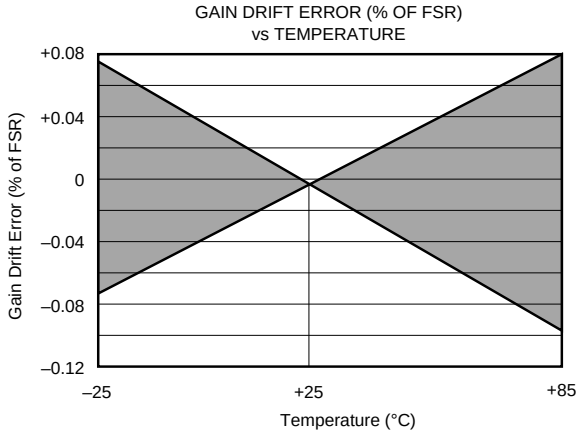
BINARY (BIN) OUTPUT	**INPUT VOLTAGE RANGE AND LSB VALUES**						
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB(1) or CTC(2)	COB(1) or CTC(2)	COB(1) or CTC(2)	CSB(3)	CSB(3)	CSB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{20V}{2^n}$
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610µV	1.22mV	610µV	2.44mV
	n = 14	1.22mV	610µV	305µV	610µV	305µV	1.22mV
Transition Values MSB LSB							
000 ... 000(4)	+Full Scale	+10V–3/2LSB	+5V–3/2LSB	+2.5V–3/2LSB	+10V–3/2LSB	+5V–3/2LSB	+20V–3/2LSB
011 ... 111	Mid Scale	0	0	0	+5V	+2.5V	+10V
111 ... 110	–Full Scale	–10V +1/2LSB	–5V +1/2LSB	–2.5V +1/2LSB	0 +1/2LSB	0 +1/2LSB	0 +1/2LSB

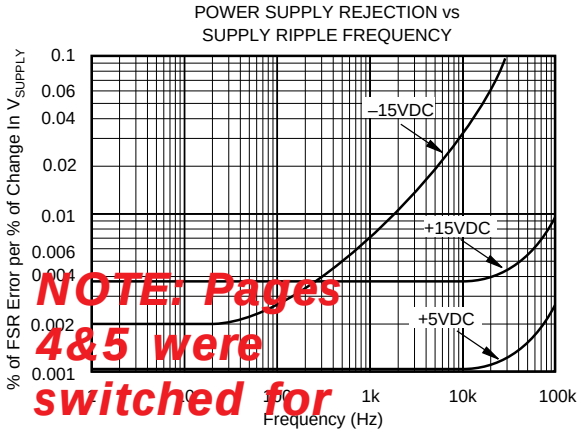
NOTES: (1) COB = Complementary Offset Binary. (2) Complementary Two's Complement—obtained by inverting the most significant bit MSB (pin 1). (3) CSB = Complementary Straight Binary. (4) Voltages given are the nominal value for transition to the code specified.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.





NOTE: Pages 4&5 were switched for abridge version for '96 data book. Be sure to switch back for full PDS.

THEORY OF OPERATION

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent quantization error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure l) about the zero or minus full scale point (all bits Off) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A differential linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB.

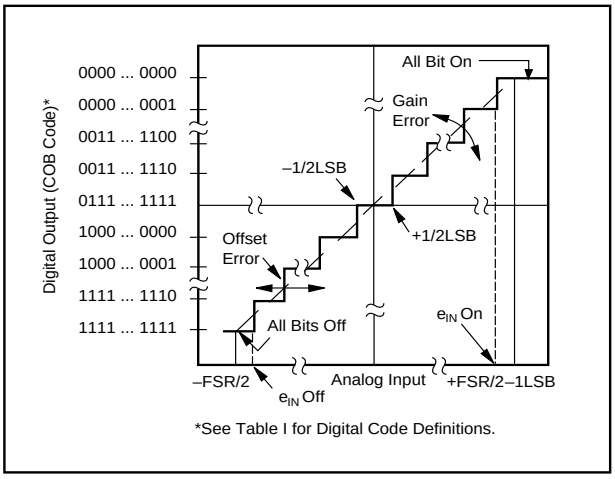


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

The ADC76 is also monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. Burr-Brown, Inc guarantees that this converter will have no missing codes over a specified temperature range when short cycled for 14-bit operation

TIMING CONSIDERATIONS

The timing diagram in Figure 2 assumes an analog input such that the positive true digital word 1001 1000 1001 0110 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110 1001 is the digital output). Figures 3 and 4 are timing diagrams showing the relationship of serial data to clock, and valid data to status.

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC76 parallel output: they are complementary (logic “0” is true) straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) for bipolar input signal ranges. Complementary two’s complement (CTC) may be obtained by inverting the MSB (pin 1).

Table I shows the LSB, transition values, and code definitions for each possible analog input signal range for 12-, 13- and 14-bit resolutions. Figure 5 shows the connections for 14-bit resolution, parallel data output, with ±10V input.

Serial Data

Two straight binary (complementary) codes are available on the serial output line: CSB and COB. The serial data is available only during conversion and appears with MSB occurring first. The serial data is synchronous with the internal clock as shown in the timing diagrams of Figures 2 and 3. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

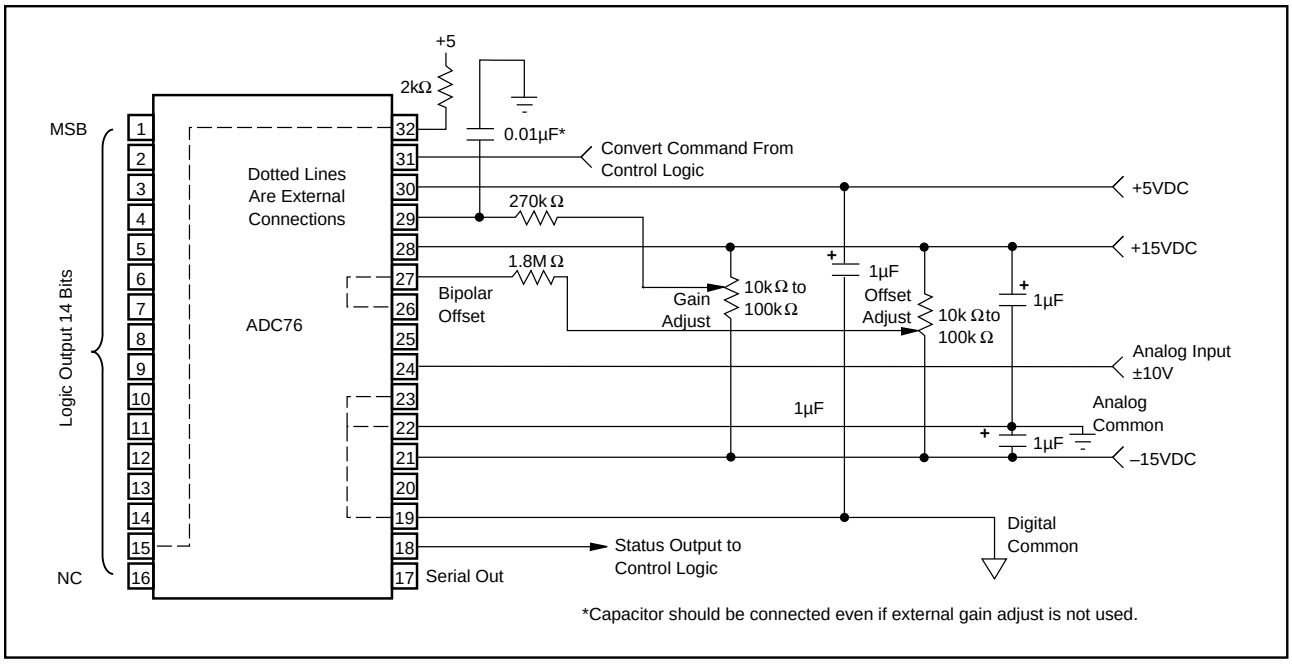


FIGURE 5. ADC76 Connections for: ±10V Analog Input, 14-Bit Resolution (Short-Cycled), Parallel Data Output.

DISCUSSION OF SPECIFICATIONS

The ADC76 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors, and conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10 and 11.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. The ADC76 power supply sensitivity is specified at ±0.003% of FSR/%V_S for the ±15V supplies and ±0.0015% of FSR/%V_S for the +5V supply. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

LINEARITY ERROR

Linearity error is not adjustable and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential linearity describes the step size between transition values. A differential linearity error of ±0.003% of FSR indicates that the size of any step may not vary from the ideal step size by more than 0.003% of Full Scale Range.

ACCURACY VERSUS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC76 are shown in Figure 6.

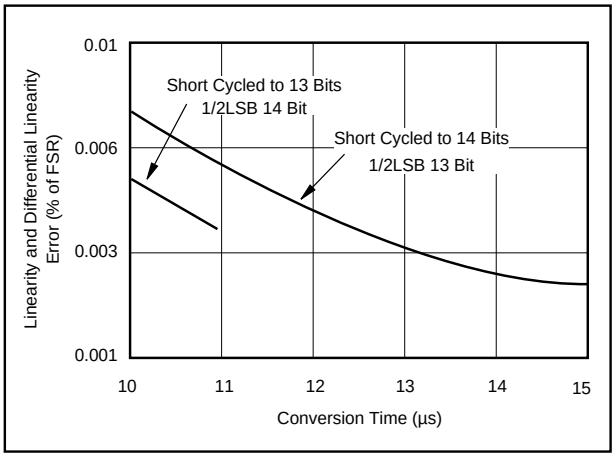


FIGURE 6. Linearity Versus Conversion Time.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital common are not connected internally in the ADC76, but should be connected together as close to the unit as possible, preferably to a large plane under the ADC. If these grounds must be run separately, use a wide conductor pattern and a 0.01µF to 0.1µF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. The comparator input (pin 27) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by Analog Common or ±15VDC supply patterns.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic capacitors as shown in Figure 7 to obtain noise free operation. These capacitors should be located close to the ADC.

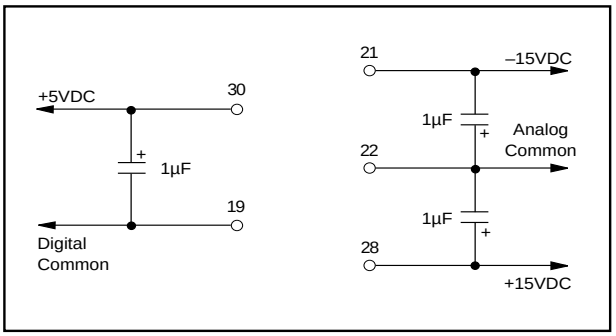


FIGURE 7. Recommended Power Supply Decoupling.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 8 for circuit details.

INPUT SIGNAL RANGE	OUTPUT CODE	CONNECT PIN 26 TO PIN	CONNECT PIN 24 TO	CONNECT INPUT SIGNAL TO PIN
±10V	COB or CTC*	27	Input Signal	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Signal	24

*Obtained by inverting MSB pin 1.

TABLE II. ADC76 Input Scaling Connections.

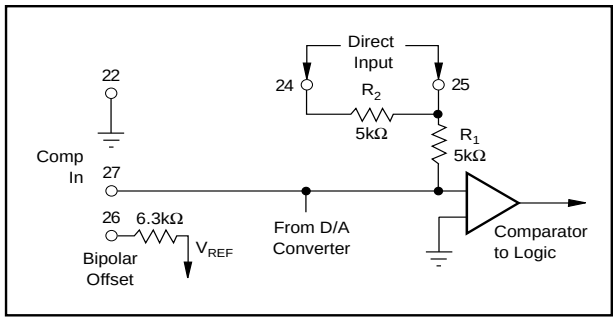


FIGURE 8. ADC76 Input Scaling Circuit.

OUTPUT DRIVE

Normally all ADC76 logic outputs will drive two standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

INPUT IMPEDANCE

The input signal to the ADC76 should be low impedance, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC76.

If this impedance is not low, a buffer amplifier should be added between the input signal and the direct input to the ADC76 as shown in Figure 9.

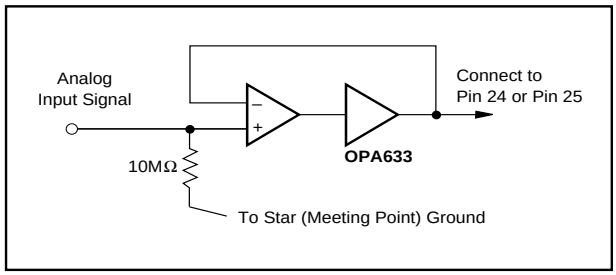


FIGURE 9. Source Impedance Buffering.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC as shown in Figures 10 and 11. Multiturn potentiometers with 100ppm/°C or better TCRs are recommended for minimum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 29 (Gain Adjust) and pin 27 (Offset Adjust) may be left open if no external adjustment is required; however, pin 29 should always be bypassed with 0.01µF to Analog Common.

ADJUSTMENT PROCEDURE

Offset—Connect the Offset potentiometer (make sure R_1 is as close to pin 27 as possible) as shown in Figure 10.

Sweep the input through the end point transition voltage that should cause an output transition to all bits off (E_{IN} Off), Figure 1.

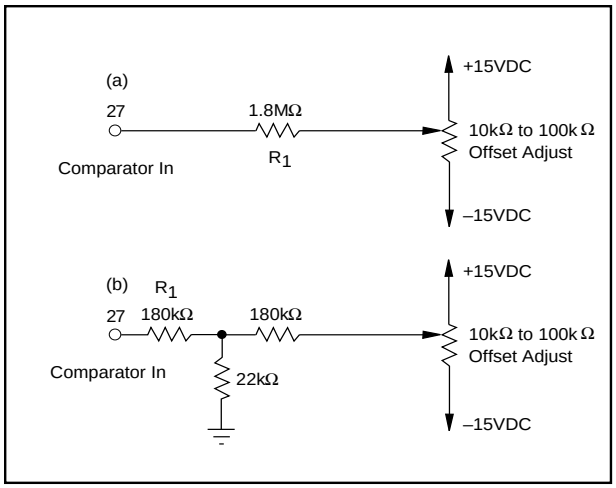


FIGURE 10. Two Methods of Connecting Optional Offset Adjust.

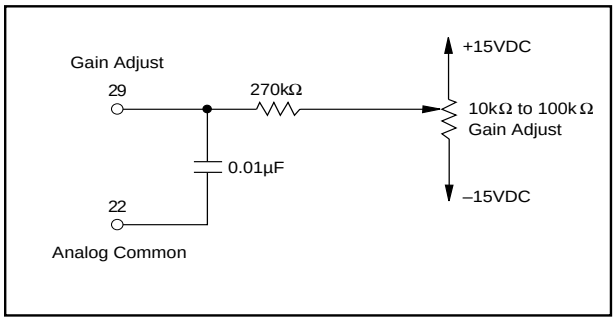


FIGURE 11. Connecting Optional Gain Adjust.

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN} Off. The ideal transition voltage values of the input are given in Table I.

Gain—Connect the Gain adjust potentiometer as shown in Figure 11. Sweep the input through the end point transition voltage; that should cause an output transition to all bits on E_{IN} On. Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN} On.

Table I details the transition voltage levels required.

CONVERT COMMAND CONSIDERATIONS

Convert command resets the converter whenever taken high. This insures a valid conversion on the first conversion after power-up.

Convert command must stay low during a conversion unless it is desired to reset the converter during a conversion.

OPTIONAL CONVERSION TIME ADJUSTMENT

The ADC76 may be operated with faster conversion times for resolutions less than 14 bits by connecting the Short Cycle (pin 32) as shown in Table III. Typical conversion times for the resolution and connections are indicated.

Resolution (Bits)	16	15	14	13	12
Connect Pin 32 to	Open	Pin 16	Pin 15	Pin 14	Pin 13
Typical Conversion Time	17µs	16µs	15µs	13µs	12µs

TABLE III. Short Cycle Connections for 12- to 16-Bit Resolutions.

Clock Rate Control may be connected to an external multi-turn trim potentiometer with a TCR of ±10ppm/°C or less as shown in Figure 12. The typical conversion time versus the Clock Rate Control voltage is shown in Figure 13. The effect of varying the conversion time and the resolution on Linearity Error and Differential Linearity Error is shown in Figure 6.

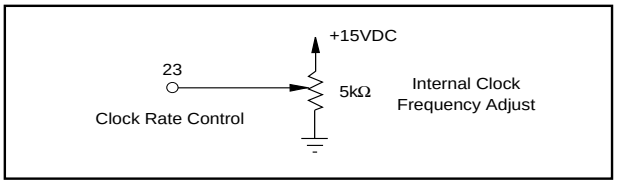


FIGURE 12. Clock Rate Control, Optional Fine Adjust.

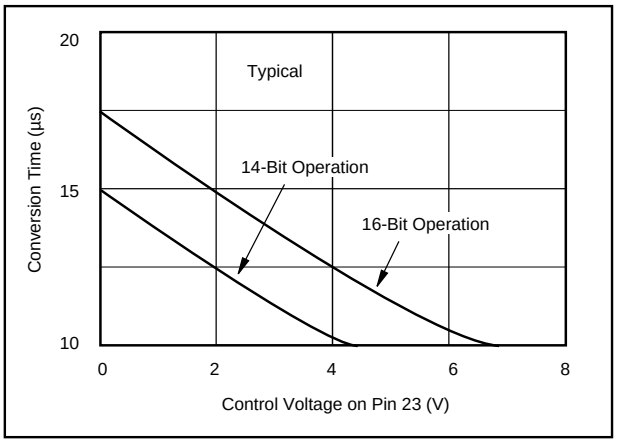


FIGURE 13. Conversion Time vs Clock Rate Control Voltage.