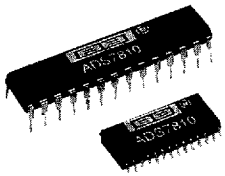
BURR-BROWN®



# ADS7810

DEMO BOARD AVAILABLE
See Appendix A



# 12-Bit 800kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

## FEATURES

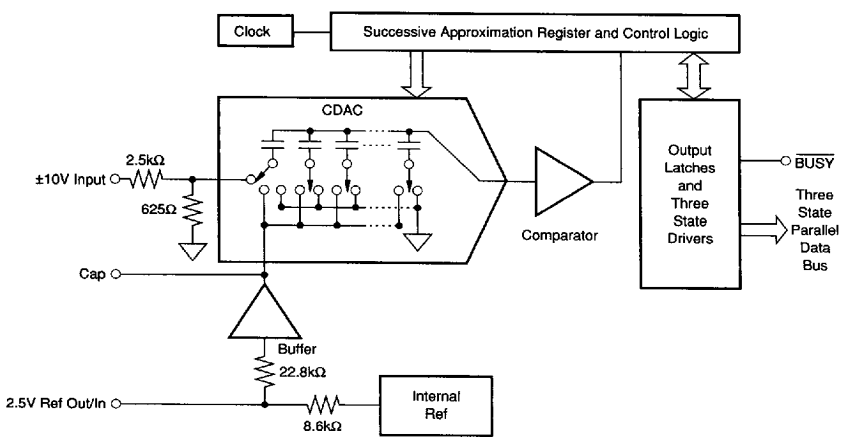
- 1.25µs THROUGHPUT TIME
- STANDARD ±10V INPUT RANGE
- 69dB min SINAD WITH 250kHz INPUT
- ±3/4 LSB max INL AND ±1 LSB max DNL
- INTERNAL REFERENCE
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/LATCHES
- 250mW max POWER DISSIPATION
- 28-PIN 0.3" PDIP AND SOIC

## DESCRIPTION

The ADS7810 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7810 is specified at an 800kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide the industry-standard ±10V input range, while an innovative design allows operation from ±5V supplies, with power dissipation under 250mW.

The 28-pin ADS7810 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

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# SPECIFICATIONS

## ELECTRICAL

At $T_A$ = –40°C, to +85°C, $f_S$ = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7810P, U | | | ADS7810PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | | 12 | | | * | Bits |
| **ANALOG INPUT** | | | | | | | | |
| Voltage Range | | | ±10 | | | * | | V |
| Impedance | | | 3.1 | | | * | | kΩ |
| Capacitance | | | 5 | | | * | | pF |
| **THROUGHPUT SPEED** | | | | | | | | |
| Conversion Time | | | 985 | | | * | | ns |
| Complete Cycle | Acquire & Convert | | | 1240 | | | * | ns |
| Throughput Rate | | 800 | | | * | | | kHz |
| **DC ACCURACY** | | | | | | | | |
| Integral Linearity Error | | | | ±1 | | | ±0.75 | LSB[1] |
| Differential Linearity Error | | | | ±1 | | | ±1 | LSB |
| No Missing Codes | | | Guaranteed | | | * | | |
| Transition Noise[2] | | | 0.1 | | | * | | LSB |
| Full Scale Error[3, 4] | | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | | | ±5 | | | ±3 | | ppm/°C |
| Full Scale Error[3, 4] | Ext. 2.5000V Ref | | | ±0.5 | | | ±0.25 | % |
| Full Scale Error Drift | Ext. 2.5000V Ref | | ±2 | | | * | | ppm/°C |
| Bipolar Zero Error[3] | | | | ±8 | | | ±4 | LSB |
| Bipolar Zero Error Drift | | | ±1 | | | ±0.5 | | ppm/°C |
| Power Supply Sensitivity | | | | | | | | |
| ($+V_{DIG} = +V_{ANA} = V_D$) | +4.75V < $V_D$ < +5.25V | | | ±5 | | | * | LSB |
| | –5.25V < $-V_{ANA}$ < –4.75V | | | ±0.5 | | | * | LSB |
| **AC ACCURACY** | | | | | | | | |
| Spurious-Free Dynamic Range | $f_{IN}$ = 250kHz | 74 | | | 77 | | | dB[5] |
| Total Harmonic Distortion | $f_{IN}$ = 250kHz | | | –74 | | | –77 | dB |
| Signal-to-(Noise+Distortion) | $f_{IN}$ = 250kHz | 67 | | | 69 | | | dB |
| Signal-to-Noise | $f_{IN}$ = 250kHz | 68 | | | 70 | | | dB |
| Full-Power Bandwidth[6] | | | 1.5 | | | * | | MHz |
| **SAMPLING DYNAMICS** | | | | | | | | |
| Aperture Delay | | | 20 | | | * | | ns |
| Aperture Jitter | | | Sufficient to Meet AC Specs | | | * | | |
| Transient Response | FS Step | | 100 | | | * | | ns |
| Overvoltage Recovery[7] | | | 150 | | | * | | ns |
| **REFERENCE** | | | | | | | | |
| Internal Reference Voltage | | 2.48 | 2.5 | 2.52 | * | * | * | V |
| Internal Reference Source Current (Must use external buffer) | | | 100 | | | * | | nA |
| Internal Reference Drift | | | 8 | | | | | ppm/°C |
| External Reference Voltage Range For Specified Linearity | | 2.3 | 2.5 | 2.7 | * | * | * | V |
| External Reference Current Drain | Ext. 2.5000V Ref | | | 100 | | | * | µA |
| **DIGITAL INPUTS** | | | | | | | | |
| Logic Levels | | | | | | | | |
| $V_{IL}$ | | –0.3 | | +0.8 | * | | * | V |
| $V_{IH}$ | | +2.4 | | $V_D$ + 0.3 | * | | * | V |
| $I_{IL}$ | $V_{IL}$ = 0V | | | ±10 | | | * | µA |
| $I_{IH}$ | $V_{IH}$ = 5V | | | ±10 | | | * | µA |
| **DIGITAL OUTPUTS** | | | | | | | | |
| Data Format | | | | Parallel 12-bits | | | | |
| Data Coding | | | | Binary Two's Complement | | | | |
| $V_{OL}$ | $I_{SINK}$ = 1.6mA | | | +0.4 | | | * | V |
| $V_{OH}$ | $I_{SOURCE}$ = 500µA | +2.8 | | | * | | | V |
| Leakage Current | High-Z State, $V_{OUT}$ = 0V to $V_{DIG}$ | | | ±5 | | | * | µA |
| Output Capacitance | High-Z State | | | 15 | | | 15 | pF |
| **DIGITAL TIMING** | | | | | | | | |
| Bus Access Time | | | | 83 | | | * | ns |
| Bus Relinquish Time | | | | 83 | | | * | ns |

# SPECIFICATIONS (CONT)

## ELECTRICAL

At $T_A$ = –40°C, to +85°C, $f_S$ = 800kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference, unless otherwise specified.

| PARAMETER | CONDITIONS | ADS7810P, U | | | ADS7810PB, UB | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **POWER SUPPLIES** | | | | | | | | |
| Specified Performance | | | | | | | | |
| $+V_{DIG} = +V_{ANA}$ | | +4.75 | +5 | +5.25 | * | * | * | V |
| $-V_{ANA}$ | | –5.25 | –5 | –4.75 | * | * | * | V |
| $+I_{DIG}$ | | | +16 | | | * | | mA |
| $+I_{ANA}$ | | | +16 | | | * | | mA |
| $-I_{ANA}$ | | | –13 | | | * | | mA |
| Derated Performance | | | | | | | | |
| $+V_{DIG} = +V_{ANA}$ | | +4.5 | +5 | +5.5 | * | * | * | V |
| $-V_{ANA}$ | | –5.5 | –5 | –4.5 | * | * | * | V |
| Power Dissipation | $f_S$ = 800kHz | | | 250 | | | * | mW |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specified Performance | | –40 | | +85 | * | | * | °C |
| Derated Performance | | –55 | | +125 | | | | °C |
| Storage | | –65 | | +150 | * | | * | °C |
| Thermal Resistance ($\theta_{JA}$) | | | | | | | | |
| Plastic DIP | | | 75 | | | * | | °C/W |
| SOIC | | | 75 | | | * | | °C/W |

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±10V input ADS7810, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input over voltage.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Analog Inputs: $V_{IN}$ | ±25V |
| CAP | $+V_{ANA}$ +0.3V to AGND2 –0.3V |
| REF | Indefinite Short to AGND2, Momentary Short to $+V_{ANA}$ |
| Ground Voltage Differences: DGND, AGND1, AGND2 | ±0.3V |
| $+V_{ANA}$ | +7V |
| $+V_{DIG}$ to $+V_{ANA}$ | +0.3V |
| $+V_{DIG}$ | 7V |
| $-V_{ANA}$ | –7V |
| Digital Inputs | –0.3V to $+V_{DIG}$ +0.3V |
| Maximum Junction Temperature | +165°C |
| Internal Power Dissipation | 825mW |
| Lead Temperature (soldering, 10s) | +300°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

## PACKAGE INFORMATION

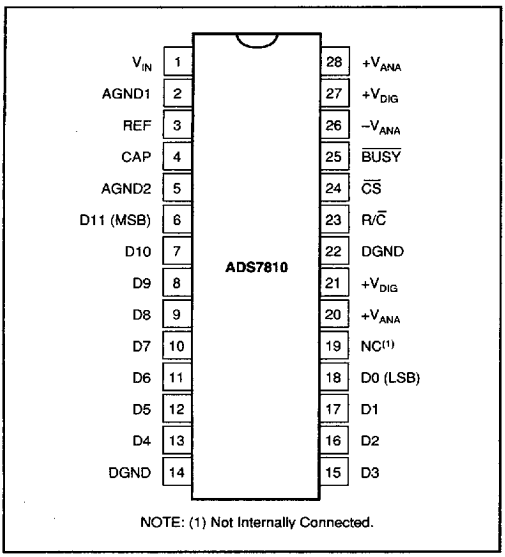
| MODEL | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| ADS7810P | 28-Pin Plastic DIP | 246 |
| ADS7810PB | 28-Pin Plastic DIP | 246 |
| ADS7810U | 28-Pin SOIC | 217 |
| ADS7810UB | 28-Pin SOIC | 217 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## ORDERING INFORMATION

| MODEL | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB) | SPECIFICATION TEMPERATURE RANGE | PACKAGE |
|---|---|---|---|---|
| ADS7810P | ±1 | 67 | –40°C to +85°C | Plastic DIP |
| ADS7810PB | ±0.75 | 69 | –40°C to +85°C | Plastic DIP |
| ADS7810U | ±1 | 67 | –40°C to +85°C | SOIC |
| ADS7810UB | ±0.75 | 69 | –40°C to +85°C | SOIC |

## PIN CONFIGURATION




NOTE: (1) Not Internally Connected.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_1$ | Convert Pulse Width | 40 | | | ns |
| $t_2$ | Data Valid Delay After R/$\overline{C}$ LOW | | 1030 | 1150 | ns |
| $t_3$ | $\overline{BUSY}$ Delay From R/$\overline{C}$ LOW | | 85 | 125 | ns |
| $t_4$ | $\overline{BUSY}$ LOW | | 1000 | 1115 | ns |
| $t_5$ | $\overline{BUSY}$ Delay After End of Conversion | | 80 | | ns |
| $t_6$ | Aperture Delay | | 20 | | ns |
| $t_7$ | Conversion Time | | 985 | 1090 | ns |
| $t_8$ | Acquisition Time | | 100 | 150 | ns |
| $t_7$ & $t_8$ | Throughput Time | | 1085 | 1240 | ns |
| $t_9$ | Bus Relinquish Time | 20 | 50 | 83 | ns |
| $t_{10}$ | $\overline{BUSY}$ Delay After Data Valid | 20 | 55 | 90 | ns |
| $t_{11}$ | R/$\overline{C}$ to $\overline{CS}$ Setup Time | 5 | | | ns |
| $t_{12}$ | Time Between Conversions | 1250 | | | ns |
| $t_{13}$ | Bus Access Time | 10 | 35 | 83 | ns |

TABLE I. Timing Specifications ($T_{MIN}$ to $T_{MAX}$).

## PIN ASSIGNMENTS

| PIN # | NAME | DIGITAL I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{IN}$ | | Analog input. Connect via 50Ω to analog input. Full-scale input range is ±10V. |
| 2 | AGND1 | | Analog Ground. Used internally as ground reference point. Minimal current flow. |
| 3 | REF | | Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor. |
| 4 | CAP | | Reference Buffer Capacitor. 2.2µF tantalum to ground. |
| 5 | AGND2 | | Analog Ground. |
| 6 | D11 (MSB) | O | Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 7 | D10 | O | Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 8 | D9 | O | Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 9 | D8 | O | Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 10 | D7 | O | Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 11 | D6 | O | Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 12 | D5 | O | Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 13 | D4 | O | Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 14 | DGND | | Digital Ground. |
| 15 | D3 | O | Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 16 | D2 | O | Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 17 | D1 | O | Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 18 | D0 (LSB) | O | Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress. |
| 19 | | | Not internally connected. |
| 20 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28, and decouple to ground with 0.1µF ceramic and 10µF tantulum capacitors. |
| 21 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28. |
| 22 | DGND | | Digital ground. |
| 23 | R/$\overline{C}$ | I | Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits. |
| 24 | $\overline{CS}$ | I | Chip Select. Internally OR'd with R/$\overline{C}$. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits. |
| 25 | $\overline{BUSY}$ | O | Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to read the data. |
| 26 | $-V_{ANA}$ | | Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantulum capacitors. |
| 27 | $+V_{DIG}$ | | Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28. |
| 28 | $+V_{ANA}$ | | Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27. |

## BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7810 with a full parallel data output. Taking R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns will initiate a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7810 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal.

### STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 24) and R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7810 in the hold state and starts a conversion. BUSY (pin 25) will go LOW and stay LOW until the conversion is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored.

The ADS7810 will begin tracking the input signal at the end of the conversion. Allowing 1.25µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 through 3 for timing diagrams.

| $\overline{CS}$ | R/$\overline{C}$ | $\overline{BUSY}$ | OPERATION |
|---|---|---|---|
| 1 | X | X | None. Databus in Hi-Z state. |
| ↓ | 0 | 1 | Initiates conversion. Databus remains in Hi-Z state. |
| 0 | ↓ | 1 | Initiates conversion. Databus enters Hi-Z state. |
| 0 | 1 | ↑ | Conversion completed. Valid data from the most recent conversion on the databus. |
| ↓ | 1 | 1 | Enables databus with valid data from the most recent conversion. |
| ↓ | 1 | 0 | Conversion in progress. Databus enabled when conversion is completed. |
| 0 | ↑ | 0 | Conversion in progress. Databus enabled when conversion is completed. |
| 0 | 0 | ↑ | Conversion completed. Valid data from the most recent conversion in the output register, but outputs are still tri-stated. |
| X | X | 0 | New convert commands ignored. Conversion in progress. |

Table II. Control Line Functions for 'read' and 'convert'.

| DESCRIPTION | ANALOG INPUT | DIGITAL OUTPUT BINARY TWO'S COMPLEMENT | |
|---|---|---|---|
| | | BINARY CODE | HEX CODE |
| Full Scale Range | ±10V | | |
| Least Significant Bit (LSB) | 4.88mV | | |
| +Full Scale (10V – 1LSB) | 9.995V | 0111 1111 1111 | 7FF |
| Midscale | 0V | 0000 0000 0000 | 000 |
| One LSB below Midscale | –4.88mV | 1111 1111 1111 | FFF |
| –Full Scale | –10V | 1000 0000 0000 | 800 |

TABLE III. Ideal Input Voltages and Output Codes.

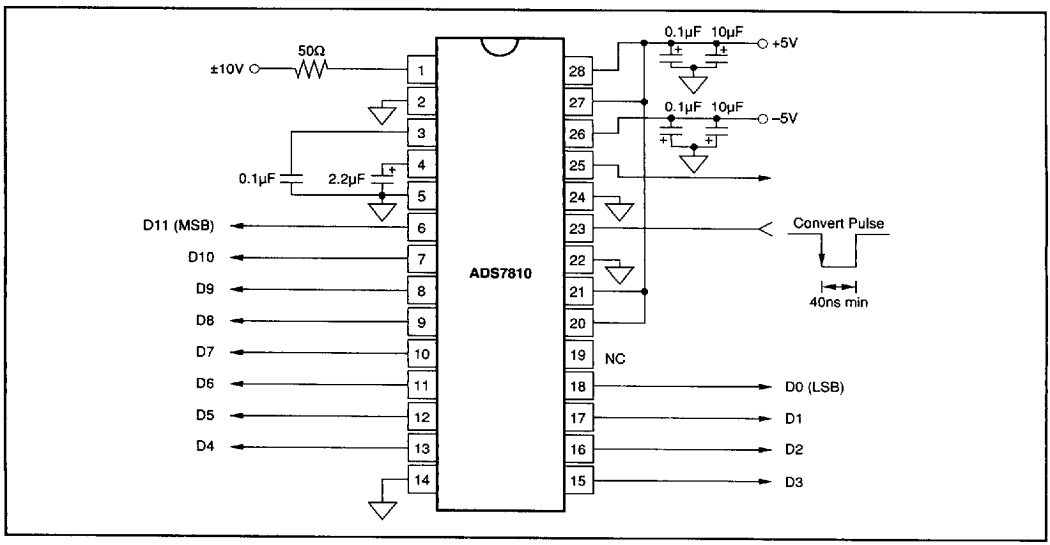



FIGURE 1. Basic Operation

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiate the conversion, be sure the less critical input is LOW at least 5ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. Note that the parallel output will be active whenever R/$\overline{C}$ is HIGH and no conversion is in progress. See the Reading Data section and refer to Table II for control line functions for 'read' and 'convert' modes.

## READING DATA

The ADS7810 outputs full parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 23) is HIGH, $\overline{CS}$ (pin 24) is LOW, and no conversion is in progress. Any other combination will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on pins 6-13 and pins 15-18. Refer to Table III for ideal output codes.

After the conversion is completed and the output registers have been updated, $\overline{BUSY}$ (pin 25) will go HIGH. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table I and Figures 2 and 3.

**Note!** For the best possible performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 2.

## INPUT RANGES

The ADS7810 offers a standard ±10V input range. Figure 4 shows the necessary circuit connections for the ADS7810 with and without external trim. Offset and full scale error(1) specifications are tested and guaranteed with the 50Ω resistor shown in Figure 4. This external resistor makes it possible to trim the offset ±50mV using a trim pot or trim DAC. This resistor may be left out if the offset and gain are negligible or they will be trimmed in software. See the Calibration section of the data sheet for details.

The nominal input impedance of 3.125kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and external 50Ω resistor. The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V. The 50Ω, 1% resistor used for the external offset adjustment circuitry does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

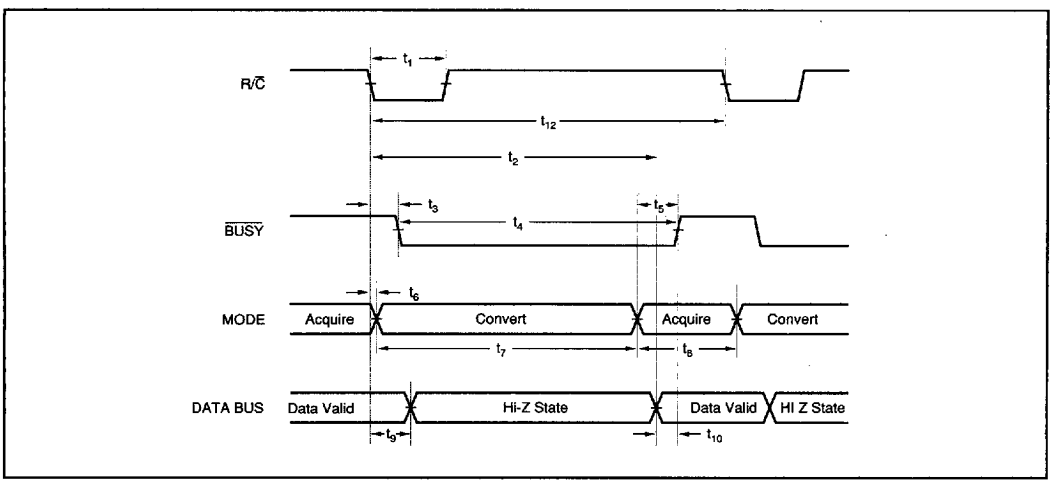



FIGURE 2. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low).

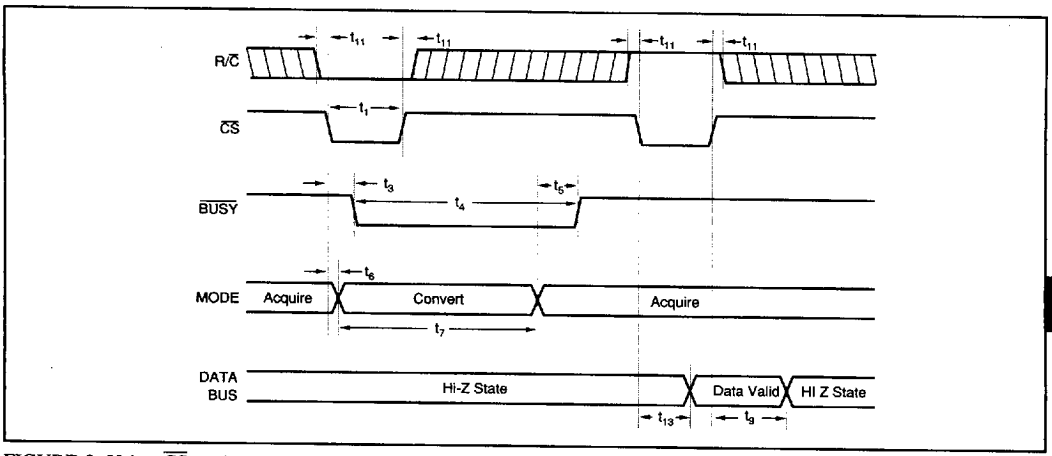



FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing.

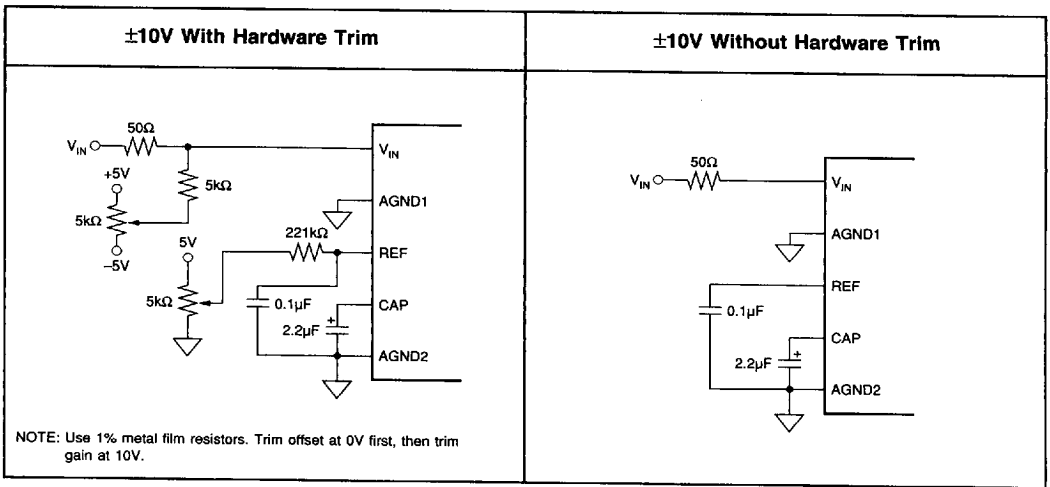



FIGURE 4. Circuit Diagram With and Without External Resistors.

## CALIBRATION

The ADS7810 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

**Hardware Calibration**

To calibrate the offset and gain of the ADS7810, install the proper resistors and potentiometers as shown in Figure 4. The calibration range is ±50mV for the offset and ±135mV for the gain.

**Software Calibration**

To calibrate the offset and gain of the ADS7810, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistor. Refer to Table IV for range of gain errors with and without the external 50Ω resistor.

**No Calibration**

See Figure 4 for circuit connections. The 50Ω external resistor shown in Figure 4 may not be necessary in some applications. This resistor provides trim capability for the gain of the ADS7810. The nominal transfer function of the ADS7810 will be bound by the shaded region seen in Figure 5 with a typical offset of 0mV and a typical gain error of –1.6%. Refer to Table IV for range of offset and gain errors with and without external resistors.

| | WITH EXTERNAL RESISTORS | WITHOUT EXTERNAL RESISTORS | UNITS |
|---|---|---|---|
| BPO | –40 < BPO < 40<br>–8 < BPO < 8 | –40 < BPO < 40<br>–8 < BPO < 8 | mV<br>LSBs |
| Gain Error | –0.5 < error < 0.5 | –2.5 < error < –1 | % of FSR |

TABLE IV. Offset and Gain Errors With and Without External Resistors.

## REFERENCE

The ADS7810 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 3, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output of the buffer accessible on CAP (pin 4).

The internal reference has a 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

### REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 0.1µF capacitor should be connected as close to the REF pin as possible. The capacitor

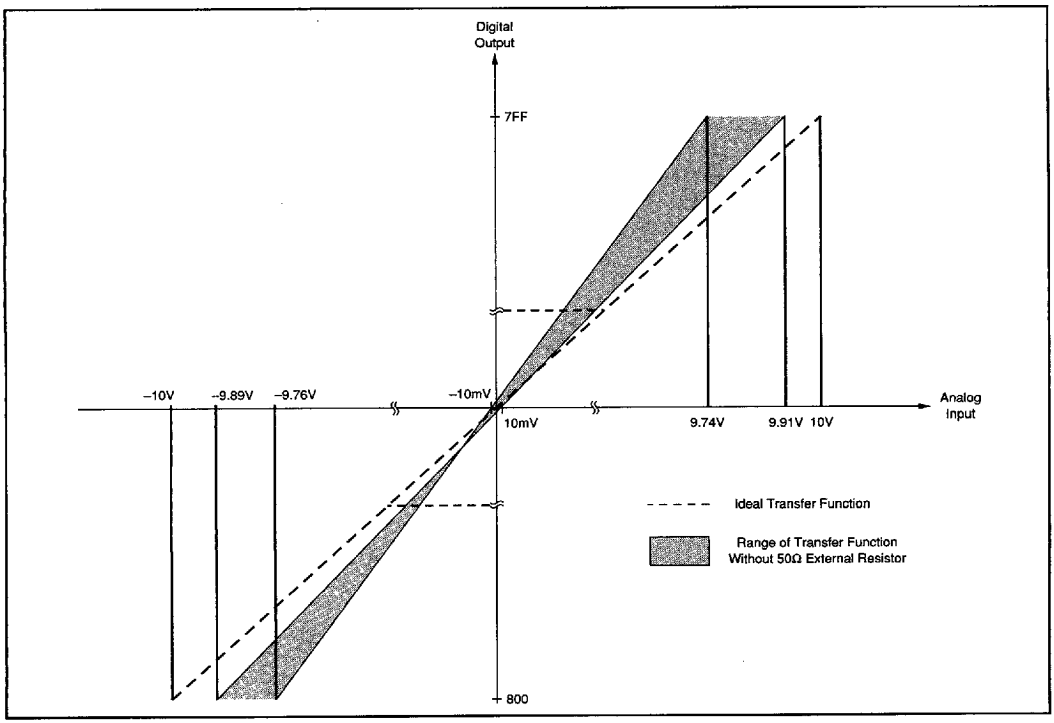



FIGURE 5. Bipolar Transfer Function Without External Resistors.

and the output resistance of REF create a low pass filter to band limit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

### CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little effect on improving performance. The voltage on the CAP pin is approximately 2V when using the internal reference, or 80% of an externally supplied reference.

## LAYOUT

### POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. The ADS7810 uses the majority of its power for analog and static circuitry. The ADS7810 should be considered as an analog component.

The +5V power for the ADS should be separate from the +5V used for the system's digital logic. Connecting $V_{DIG}$ (pin 21 and 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, simple +5V and –5V regulators can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, the $V_{DIG}$ and $V_{ANA}$ pins should be tied to the same +5V source.

### GROUNDING

Three ground pins are present on the ADS7810. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADS should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

### SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7810, compared to FET switches on other CMOS A/D converters, releases 5%—10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the op amp on the front end. Any op amp sufficient for the signal in an application will be sufficient to the drive the ADS7810.

The resistive front end of the ADS7810 also provides a guaranteed ±25V over voltage protection. In most cases, this eliminates the need for external input protection circuitry.

### INTERMEDIATE LATCHES

The ADS7810 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7810 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.