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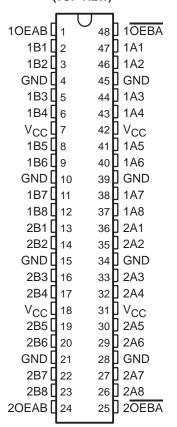
- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at V_{CC} = 5 V, T_A = 25°C
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (-32-mA I_{OH}, 64-mA I_{OI})
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'ABT16623 are 16-bit transceivers designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing. The 'ABT16623 provide true data at the outputs.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable (OEAB and OEBA) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated. The dual-enable configuration gives the transceivers the capability of storing data by simultaneously enabling OEAB and OEBA. Each output reinforces its input in this configuration. When both OEAB and OEBA are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (32 total) remain at their last states.

SN54ABT16623 . . . WD PACKAGE SN74ABT16623 . . . DGG OR DL PACKAGE (TOP VIEW)





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description (continued)

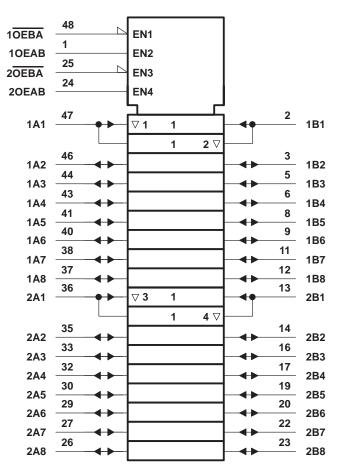
To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The SN54ABT16623 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT16623 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE (each 8-bit section)

INP	UTS	ODED ATION
OEBA	OEAB	OPERATION
L	L	B data to A bus
L	Н	B data to A bus, A data to B bus
Н	L	Isolation
Н	Н	A data to B bus

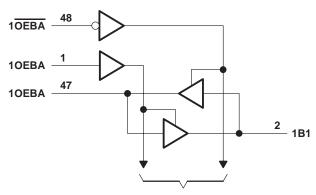
logic symbol†

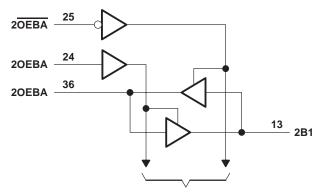


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)





To Seven Other Channels To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, VO	–0.5 V to 5.5 V
Current into any output in the low state, IO: SN54ABT16623	96 mA
SN74ABT16623	128 mA
Input clamp current, I _{IK} (V _I < 0)	–18 mA
Output clamp current, I _{OK} (V _O < 0)	–50 mA
Package thermal impedance, θ _{JA} (see Note 2): DGG package	89°C/W
DL package	94°C/W
Storage temperature range, T _{stg}	. −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 3)

			SN54AB1	16623	SN74AB1	16623	UNIT
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	EN	2		V	
VIL	Low-level input voltage		0.8		0.8	V	
VI	Input voltage		0 0	Vcc	0	VCC	V
ІОН	High-level output current		ζ ₂ ,	-24		-32	mA
l _{OL}	Low-level output current	200	48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled	N.	5		5	ns/V
TA	Operating free-air temperature		– 55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

^{2.} The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

SN54ABT16623, SN74ABT16623 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST 601	Т	A = 25°C	;	SN54AB1	Г16623	SN74AB1	16623	UNIT	
PAR	AWEIER	TEST CON	PILIONS	MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	UNII
VIK		$V_{CC} = 4.5 \text{ V},$	I _I = -18 mA			-1.2		-1.2		-1.2	V
		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
\/a		$V_{CC} = 5 V$	$I_{OH} = -3 \text{ mA}$	3			3		3		V
VOH		V _{CC} = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2				V
		VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
VOL		V _{CC} = 4.5 V	I _{OL} = 48 mA			0.55		0.55			V
VOL		VCC = 4.5 V	I _{OL} = 64 mA			0.55*				0.55	V
V _{hys}					100						mV
l _l	Control inputs	V _{CC} = 5.5 V,	V _I = V _{CC} or GND			±1		±1		±1	μА
	A or B ports					±100		±100		±100	
IOZH [‡]		$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 2.7 \text{ V}$				50		50		50	μΑ
lozL [‡]		$V_{CC} = 5.5 \text{ V},$	V _O = 0.5 V			- 50	4	- 50		– 50	μΑ
l _{off}		$V_{CC} = 0$,	V_I or $V_O \le 4.5 \text{ V}$			±100	7,2			±100	μΑ
ICEX		V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high			50	Ongc	50		50	μА
IO§		$V_{CC} = 5.5 \text{ V},$	V _O = 2.5 V	-50	-100	-180	2 –50	-180	-50	-180	mA
		V _{CC} = 5.5 V,	Outputs high			2		2		2	
Icc	A or B ports	$I_{O} = 0$,	Outputs low			35		35		35	mA
		$V_I = V_{CC}$ or GND	Outputs disabled			2		2		2	
	Data innuta	V _{CC} = 5.5 V, One input at 3.4 V,	Outputs enabled			1		1.5		1	
∆ICC¶	Data inputs	Other inputs at V _{CC} or GND	Outputs disabled			0.05		0.05		0.05	mA
	Control inputs	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				1.5		1.5		1.5	
Ci	Control inputs	V _I = 2.5 V or 0.5 V			3						pF
C _{io}	A or B ports	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$			8						pF

^{*} On products compliant to MIL-PRF-38535, this parameter does not apply.

[†] All typical values are at $V_{CC} = 5 \text{ V}$.

[‡] The parameters I_{OZH} and I_{OZL} include the input leakage current.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[¶] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ABT16623, SN74ABT16623 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

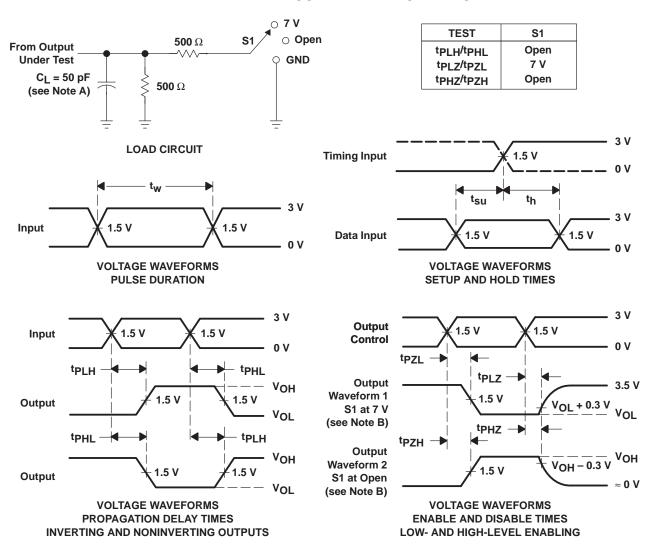
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V ₍	CC = 5 V 4 = 25°C	<u>',</u>	SN54AB1	Г16623	SN74AB	Г16623	UNIT
	(INFOT)	(001F01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
^t PLH	A or B	B or A	1	2	3.2	1	3.7	1	3.6	ns
tPHL	AOIB	BULA	1	2.2	3.4	1 2	4.4	1	4.3	115
^t PZH	<u> </u>	A or B	1.1	3	4	1.1	5	1.1	4.9	ns
tpzL	OEBA or OEAB	AOFB	1.4	3.3	4.9	1.4	6.2	1.4	6	115
t _{PHZ}	OEBA or OEAB	A or B	1	3.5	4.9	0 1	6.2	1	6	no
t _{PLZ}	OEDA UI OEAB		1.4	2.8	4.7	1.4	5.6	1.4	5.4	ns

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50~\Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ABT16623DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ABT16623DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16623DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16623DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16623DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16623DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16623DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16623DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74ABT16623DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT16623DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74ABT16623DLR	SSOP	DL	48	1000	346.0	346.0	49.0

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