SCAS201B - MARCH 1991 - REVISED APRIL 1998



- Free-Running Read and Write Clocks Can Be Asynchronous or Coincident
- Read and Write Operations Synchronized to Independent System Clocks
- Input-Ready Flag Synchronized to Write Clock
- Output-Ready Flag Synchronized to Read Clock
- 256 Words by 18 Bits
- Low-Power Advanced CMOS Technology
- Half-Full Flag and Programmable Almost-Full/Almost-Empty Flag
- Bidirectional Configuration and Width Expansion Without Additional Logic
- Fast Access Times of 12 ns With a 50-pF Load and All Data Outputs Switching Simultaneously
- Data Rates up to 67 MHz
- Pin-to-Pin Compatible With SN74ACT7803 and SN74ACT7813
- Packaged in Shrink Small-Outline 300-mil Package Using 25-mil Center-to-Center Spacing

#### description

The SN74ACT7805 is a 256-word × 18-bit clocked FIFO suited for buffering asynchronous data paths up to 67-MHz clock rates and 12-ns access

times. Two devices can be configured for bidirectional data buffering without additional logic. Multiple distributed  $V_{CC}$  and GND pins, along with Texas Instruments patented output edge control ( $OEC^{TM}$ ) circuit, dampen simultaneous switching noise.

The write clock (WRTCLK) and read clock (RDCLK) are free running and can be asynchronous or coincident. Data is written to memory on the rising edge of WRTCLK when WRTEN1 is high, WRTEN2 is low, and IR is high. Data is read from memory on the rising edge of RDCLK when RDEN, OE1, and OE2 are low and OR is high. The first word written to memory is clocked through to the output buffer, regardless of the RDEN, OE1, and OE2 levels. The OR flag indicates that valid data is present on the output buffer.

The FIFO can be reset asynchronously to WRTCLK and RDCLK. RESET must be asserted while at least four WRTCLK and four RDCLK rising edges occur to clear the synchronizing registers. Resetting the FIFO initializes the input-ready (IR), output-ready (OR), and half-full (HF) flags low and the almost-full/almost-empty (AF/AE) flag high. The FIFO must be reset upon power up.

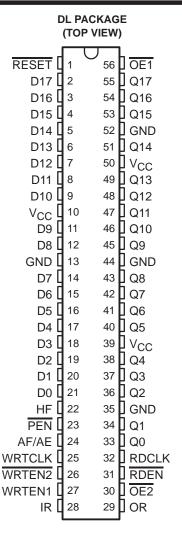
The SN74ACT7805 is characterized for operation from 0°C to 70°C.



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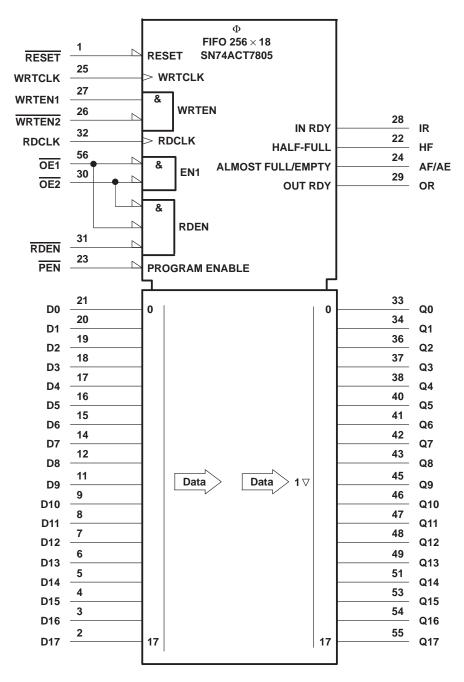
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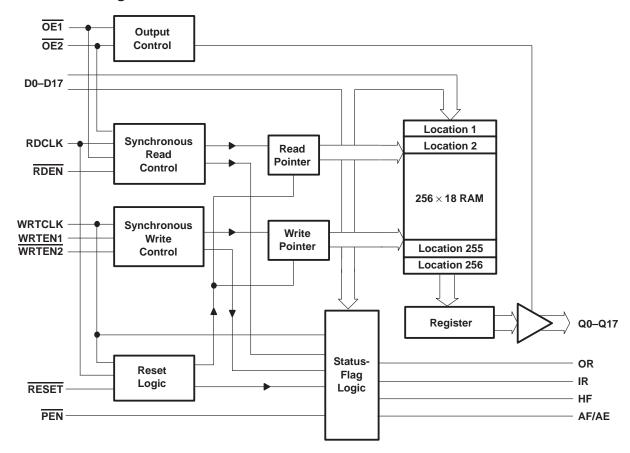
#### logic symbol†



 $<sup>\</sup>dagger$  This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



#### functional block diagram



#### **Terminal Functions**

TEI	RMINAL		PEOPLETION
NAME	NO.	1/0	DESCRIPTION
AF/AE	24	0	Almost-full/almost-empty flag. Depth offset values can be programmed for AF/AE, or the default value of 32 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AE is high when memory contains X or fewer words or (256 – Y) or more words. AF/AE is high after reset.
D0-D17	21–14, 12–11, 9–2	ı	18-bit data input port
HF	22	0	Half-full flag. HF is high when the FIFO memory contains 128 or more words. HF is low after reset.
IR	28	0	Input-ready flag. IR is synchronized to the low-to-high transition of WRTCLK. When IR is low, the FIFO is full and writes are disabled. IR is low during reset and goes high on the second low-to-high transition of WRTCLK after reset.
OE1, OE2	56, 30	ı	Output enables. When OE1, OE2, and RDEN are low and OR is high, data is read from the FIFO on a low-to-high transition of RDCLK. When either OE1 or OE2 is high, reads are disabled and the data outputs are in the high-impedance state.
OR	29	0	Output-ready flag. OR is synchronized to the low-to-high transition of RDCLK. When OR is low, the FIFO is empty and reads are disabled. Ready data is present on Q0–Q17 when OR is high. OR is low during reset and goes high on the third low-to-high transition of RDCLK after the first word is loaded to empty memory.
PEN	23	I	Program enable. After reset and before the first word is written to the FIFO, the binary value on D0–D6 is latched as an AF/AE offset value when PEN is low and WRTCLK is high.
Q0-Q17	33–34, 36–38, 40–43, 45–49, 51, 53–55	0	18-bit data output port. After the first valid write to empty memory, the first word is output on Q0–Q17 on the third rising edge of RDCLK. OR also is asserted high at this time to indicate ready data. When OR is low, the last word read from the FIFO is present on Q0–Q17.
RDCLK	32	ı	Read clock. RDCLK is a continuous clock and can be asynchronous or coincident to WRTCLK. A low-to-high transition of RDCLK reads data from memory when $\overline{OE1}$ , $\overline{OE2}$ , and $\overline{RDEN}$ are low and OR is high. OR is synchronous to the low-to-high transition or RDCLK.
RDEN	31	ı	Read enable. When RDEN, OE1, and OE2 are low and OR is high, data is read from the FIFO on the low-to-high transition of RDCLK.
RESET	1	I	Reset. To reset the FIFO, four low-to-high transitions of RDCLK and four low-to-high transitions of WRTCLK must occur while RESET is low. This sets HF, IR, and OR low and AF/AE high.
WRTCLK	25	I	Write clock. WRTCLK is a continuous clock and can be asynchronous or coincident to RDCLK. A low-to-high transition of WRTCLK writes data to memory when WRTEN2 is low, WRTEN1 is high, and IR is high. IR is synchronous to the low-to-high transition of WRTCLK.
WRTEN1, WRTEN2	27, 26	ı	Write enables. When WRTEN1 is high, WRTEN2 is low, and IR is high, data is written to the FIFO on a low-to-high transition of WRTCLK.



SCAS201B - MARCH 1991 - REVISED APRIL 1998

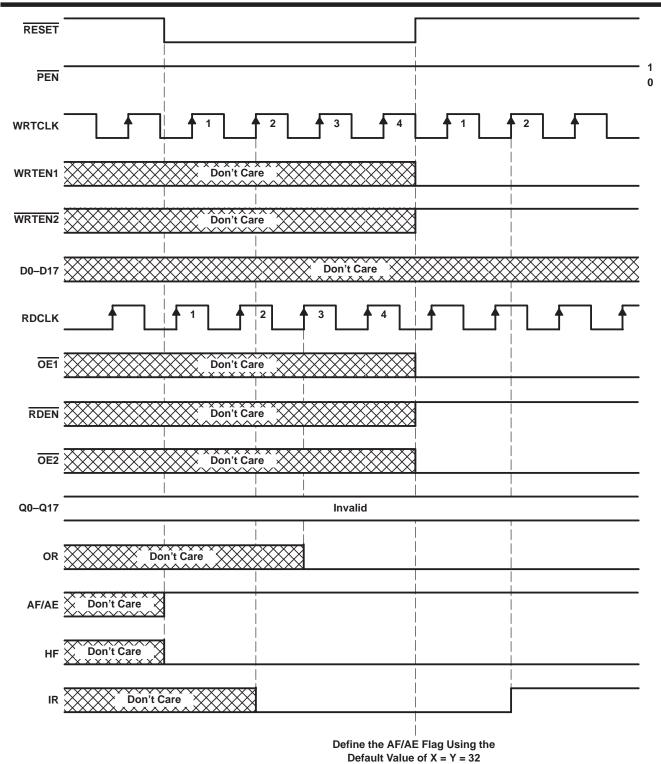


Figure 1. Reset Cycle



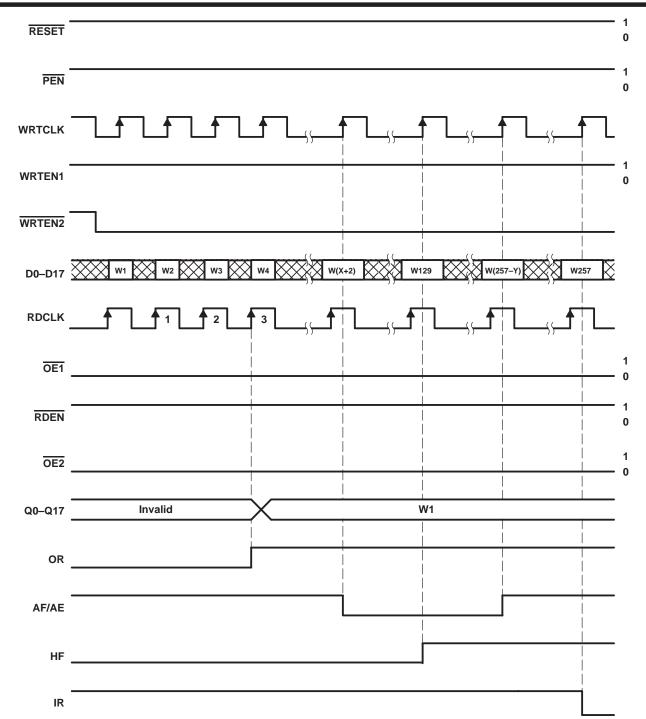


Figure 2. Write



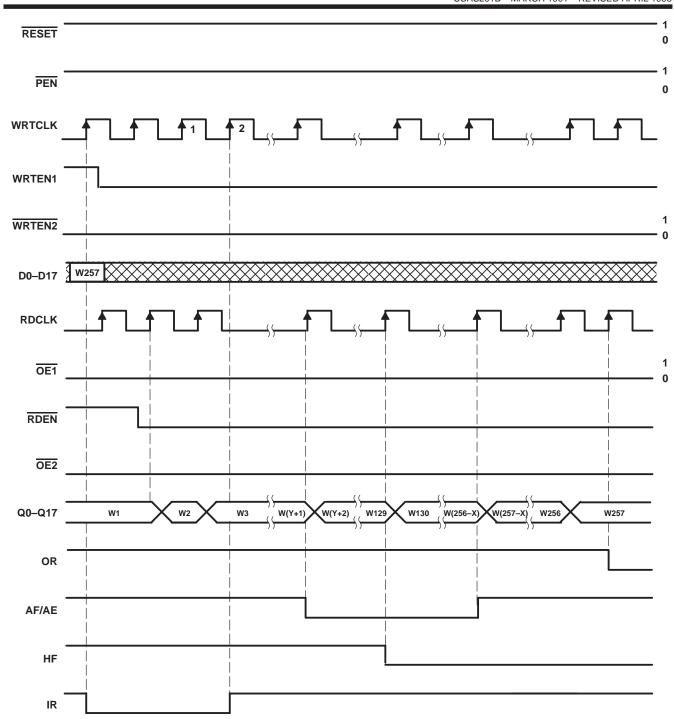


Figure 3. Read

#### offset values for AF/AE

The AF/AE flag has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed after the FIFO is reset and before the first word is written to memory. If the offsets are not programmed, the default values of X = Y = 32 are used. The AF/AE flag is high when the FIFO contains X or fewer words or (256 - Y) or more words.

Program enable (PEN) should be held high throughout the reset cycle. PEN can be brought low only when IR is high and WRTCLK is low. On the following low-to-high transition of WRTCLK, the binary value on D0-D6 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding PEN low for another low-to-high transition of WRTCLK reprograms Y to the binary value on D0-D6 at the time of the second WRTCLK low-to-high transition. When the offsets are being programmed, writes to the FIFO memory are disabled regardless of the state of the write enables (WRTEN1, WRTEN2). A maximum value of 127 can be programmed for either X or Y (see Figure 4). To use the default values of X = Y = 32,  $\overline{PEN}$  must be held high.

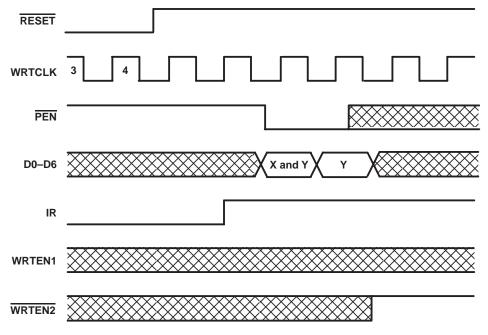


Figure 4. Programming X and Y Separately

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5	$\mbox{V}$ to 7 $\mbox{V}$
Input voltage range, V <sub>I</sub>	0.5	$V \ to \ 7 \ V$
Voltage range applied to a disabled 3-state output	0.5 V	to 5.5 V
Package thermal impedance, θ <sub>JA</sub> (see Note 1)		74°C/W
Storage temperature range, T <sub>stg</sub>	–65°C t	to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.



SCAS201B - MARCH 1991 - REVISED APRIL 1998

#### recommended operating conditions

			'ACT78	305-15	'ACT78	305-20	'ACT78	305-25	'ACT78	05-40	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V	
VIH	High-level input voltage		2		2		2		2		V
VIL	Low-level input voltage			0.8		0.8		0.8		0.8	V
ІОН	High-level output current	Q outputs, flags		-8		-8		-8		-8	mA
la.	Low-level output current	Q outputs		16		16		16		16	mA
IOL Low-level output current		Flags		8		8		8		8	IIIA
TA	Operating free-air temperature		0	70	0	70	0	70	0	70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	ARAMETER		TEST CONDITION	ONS	MIN	TYP <sup>†</sup>	MAX	UNIT
Vон		$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -8 \text{ mA}$		2.4			V
\/a.	Flags	$V_{CC} = 4.5 \text{ V},$	IOL = 8 mA				0.5	V
VOL	Q outputs	V <sub>CC</sub> = 4.5 V,	I <sub>OL</sub> = 16 mA				0.5	V
II		V <sub>CC</sub> = 5.5 V,	VI = VCC or 0				±5	μΑ
loz		V <sub>CC</sub> = 5.5 V,	VO = VCC or 0				±5	μΑ
Icc		$V_{I} = V_{CC} - 0.2 V_{C}$	or 0				400	μΑ
∆l <sub>CC</sub> ‡		$V_{CC} = 5.5 V$ ,	One input at 3.4 V,	Other inputs at V <sub>CC</sub> or GND			1	mA
Ci		V <sub>I</sub> = 0,	f = 1 MHz			4		pF
Co		$V_{O} = 0,$	f = 1 MHz			8		pF

<sup>†</sup> All typical values are at  $V_{CC}$  = 5 V,  $T_A$  = 25°C. ‡ This is the supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

## timing requirements over recommended operating conditions (unless otherwise noted) (see Figures 1 through 5)

			'ACT78	305-15	'ACT78	305-20	'ACT78	305-25	'ACT78	05-40	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency			67		50		40		25	MHz
		WRTCLK high or low	6		7		8		12		
t <sub>W</sub>	Pulse duration	RDCLK high or low	6		7		8		12		ns
		PEN low	8		9		9		12		
		D0-D17 before WRTCLK↑	4		5		5		5		
		WRTEN1, WRTEN2 before WRTCLK1	4		5		5		5		
t <sub>SU</sub> Setup time	OE1, OE2 before RDCLK↑	5		5		6		6			
	RDEN before RDCLK↑	4		5		5		5		ns	
t <sub>su</sub>	Octup time	Reset: RESET low before first WRTCLK↑ and RDCLK↑†	5		6		6		6		113
		PEN before WRTCLK↑	5		6		6		6		
		Define AF/AE: PEN before WRTCLK↑	5		6		6		6		
		D0–D17) after WRTCLK↑	0		0		0		0		
		WRTEN1, WRTEN2 after WRTCLK↑	0		0		0		0		
t <sub>h</sub>	th Hold time	OE1, OE2, RDEN after RDCLK↑	0		0		0		0		ns
qı Hold illic	Reset: RESET low after fourth WRTCLK↑ and RDCLK↑†	2		2		2		2		110	
		Define AF/AE: PEN after WRTCLK↑	2		2		2		2		

<sup>&</sup>lt;sup>†</sup> To permit the clock pulse to be utilized for reset purposes

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM	то	'A	CT7805-1	15	'ACT78	305-20	'ACT78	805-25	'ACT78	305-40	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP†	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f <sub>max</sub>	WRTCLK or RDCLK		67			50		40		25		MHz
t <sub>pd</sub>	RDCLK↑	Any Q	4	9.5	12	4	13	4	15	4	20	ns
t <sub>pd</sub> ‡	RDCLK↑	Any Q		8.5								ns
	WRTCLK↑	IR	3		8.5	3	11	3	13	3	15	
l	RDCLK↑	OR	3		8.5	3	11	3	13	3	15	no
<sup>t</sup> pd	WRTCLK↑	AF/AE	7		16.5	7	19	7	21	7	23	ns
	RDCLK↑	AF/AE	7		17	7	19	7	21	7	23	
t <sub>PLH</sub>	WRTCLK↑	HF	7		15	7	17	7	19	7	21	ns
t <sub>PHL</sub>	RDCLK↑	HF	7		15.5	7	18	7	20	7	22	ns
t <sub>PLH</sub>	RESET low	AF/AE	2		9	2	11	2	13	2	15	ns
t <sub>PHL</sub>	RESET low	HF	2		10	2	12	2	14	2	16	ns
t <sub>en</sub>	OE1, OE2	Any Q	2		8.5	2	11	2	11	2	11	ns
<sup>t</sup> dis	OE1, OE2	Any Q	2		9.5	2	11	2	14	2	14	ns

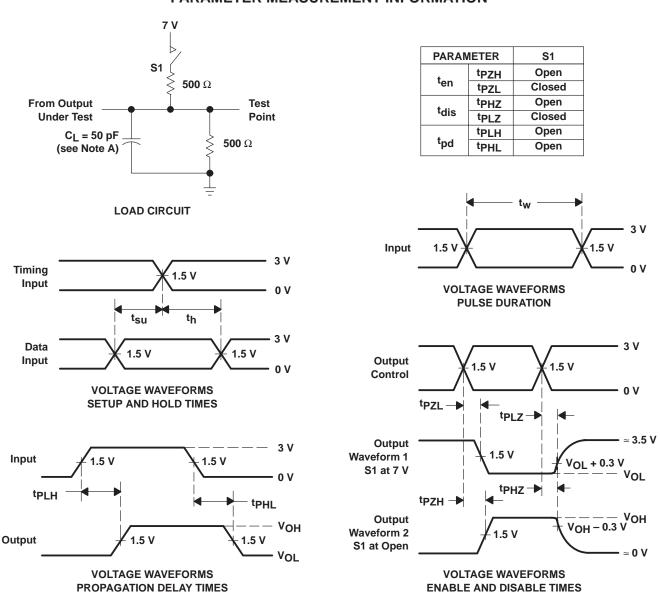
<sup>&</sup>lt;sup>‡</sup> This parameter is measured with a 30-pF load (see Figure 6).



## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER		TEST CON	TYP	UNIT	
Ср	Power dissipation capacitance per FIFO channel Ou	utputs enabled	$C_L = 50 pF$ ,	f = 5 MHz	53	pF

#### PARAMETER MEASUREMENT INFORMATION

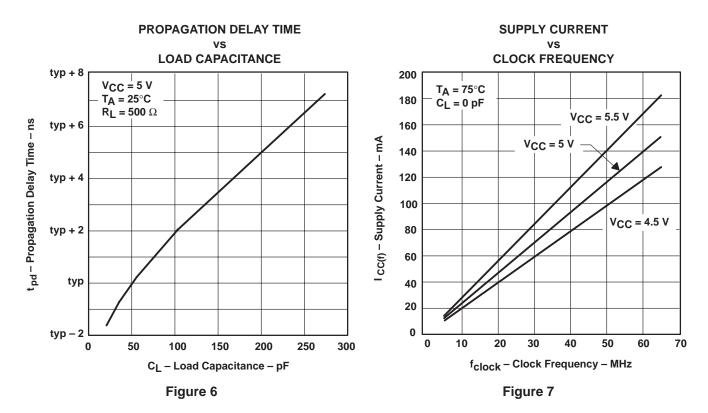


NOTE A: C<sub>L</sub> includes probe and jig capacitance.

Figure 5. Load Circuit and Voltage Waveforms



#### TYPICAL CHARACTERISTICS



#### **APPLICATION INFORMATION**

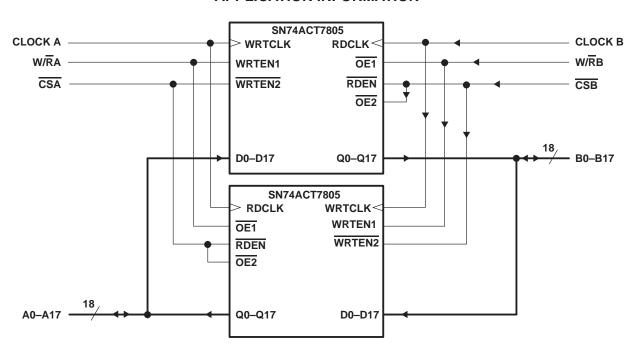


Figure 8. Bidirectional Configuration

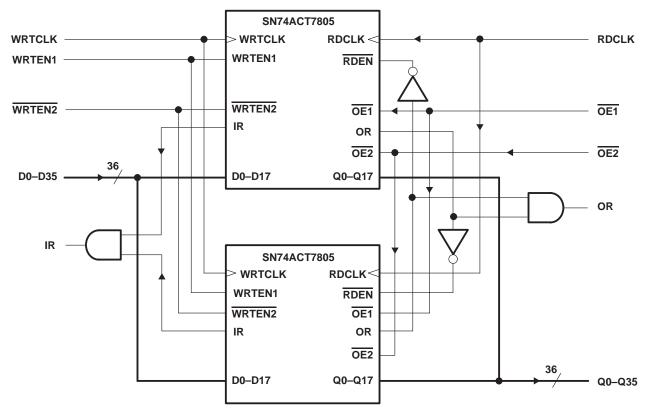


Figure 9. Word-Width Expansion: 256 × 36 Bits



#### PACKAGE OPTION ADDENDUM

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#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
1M7805-15DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT7805-15DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT7805-15DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT7805-25DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT7805-40DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>&</sup>lt;sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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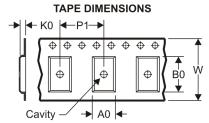
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### **PACKAGE MATERIALS INFORMATION**

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#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT7805-15DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT7805-15DLR	SSOP	DL	56	1000	346.0	346.0	49.0

#### DL (R-PDSO-G\*\*)

#### **48 PINS SHOWN**

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118

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