XIO2001

XIO2001 PCI Express™ to PCI Bus Translation Bridge

Data Manual

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1 Introduction

1.1 Features

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- **Fully Compliant with *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0**
- **Fully Compliant with *PCI Express Base Specification*, Revision 2.0**
- **Fully Compliant with *PCI Local Bus Specification*, Revision 2.3**
- **PCI Express Advanced Error Reporting Capability Including ECRC Support**
- **Support for D1, D2, $D3_{hot}$, and $D3_{cold}$**
- **Active-State Link Power Management Saves Power When Packet Activity on the PCI Express Link is Idle, Using Both L0s and L1 States**
- **Wake Event and Beacon Support**
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- **Five 3.3-V, Multifunction, General-Purpose I/O Terminals**
- **Memory-Mapped EEPROM Serial-Bus Controller Supporting PCI Express Power Budget/Limit Extensions for Add-In Cards**
- **Compact Footprint, Lead-Free 144-Ball, ZAJ MicroStar™ BGA, Lead-Free 169-Ball ZGU MicroStar BGA, and PowerPad™ HTQFP 128-Pin PNP Package**

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2 Overview

The Texas Instruments XIO2001 is a PCI Express to PCI local bus translation bridge that provides full PCI Express and PCI local bus functionality and performance.

2.1 Description

The XIO2001 is a single-function PCI Express to PCI translation bridge that is fully compliant to the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. For downstream traffic, the bridge simultaneously supports up to eight posted and four non-posted transactions. For upstream traffic, up to six posted and and four non-posted transactions are simultaneously supported.

The PCI Express interface is fully compliant to the *PCI Express Base Specification*, Revision 2.0.

The PCI Express interface supports a ×1 link operating at full 250 MB/s packet throughput in each direction simultaneously. Also, the bridge supports the advanced error reporting including extended CRC (ECRC) as defined in the *PCI Express Base Specification*. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency across the bridge. If parity errors are detected, then packet poisoning is supported for both upstream and downstream operations.

The PCI local bus is fully compliant with the *PCI Local Bus Specification* (Revision 2.3) and associated programming model. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The PCI bus interface is 32-bit and can operate at either 25 MHz, 33 MHz, 50 MHz, or 66 MHz. Also, the PCI interface provides fair arbitration and buffered clock outputs for up to 6 subordinate devices.

Power management (PM) features include active state link PM, PME mechanisms, the beacon and wake protocols, and all conventional PCI D-states. If the active state link PM is enabled, then the link automatically saves power when idle using the L0s and L1 states. PM active state NAK, PM PME, and PME-to-ACK messages are supported. Standard PCI bus power management features provide several low power modes, which enable the host system to further reduce power consumption.

The bridge has additional capabilities including, but not limited to, serial IRQ with MSI messages, serial EEPROM, power override, clock run, PCI Express clock request and PCI bus $\overline{\text{LOCK}}$. Also, five general-purpose inputs and outputs (GPIOs) are provided for further system control and customization.

2.2 Related Documents

- *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0
- *PCI Express Base Specification*, Revision 2.0
- *PCI Express Card Electromechanical Specification*, Revision 2.0
- *PCI Local Bus Specification*, Revision 2.3
- *PCI-to-PCI Bridge Architecture Specification*, Revision 1.2
- *PCI Bus Power Management Interface Specification*, Revision 1.2
- *PCI Mobile Design Guide*, Revision 1.1
- *Serialized IRQ Support for PCI Systems*, Revision 6.0

2.3 Documents Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are listed below:

1. To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
2. To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
3. All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
4. If the signal or terminal name has a bar above the name (for example, $\overline{\text{GRST}}$), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
5. Differential signal names end with P, N, +, or – designators. The P or + designators signify the positive signal associated with the differential pair. The N or – designators signify the negative signal associated with the differential pair.
6. RSVD indicates that the referenced item is reserved.
7. In Sections 4 through 6, the configuration space for the bridge is defined. For each register bit, the software access method is identified in an access column. The legend for this access column includes the following entries:
   - r – read access by software
   - u – updates by the bridge internal hardware
   - w – write access by software
   - c – clear an asserted bit with a write-back of 1b by software. Write of zero to the field has no effect
   - s – the field may be set by a write of one. Write of zero to the field has no effect
   - na – not accessible or not applicable

2.4 Document History

REVISION DATE	REVISION NUMBER	REVISION COMMENTS
5/2009	–	Initial release
5/2009	A	Corrected typos
9/2009	B	
10/2009	C	Added PNP package and ESD ratings Removed terminal assignment tables for all packages
1/2010	D	Corrected PNP pinout, replaced Ordering Information with Package Option Addendum

2.5 Terminal Assignments

The XIO2001 is available in either a 169-ball ZGU MicroStar BGA or a 144−ball ZAJ MicroStar BGA package.

Figure 2-1 shows a terminal diagram of the ZGU package.

Figure 2-2 shows a terminal diagram of the ZAJ package.

Figure 2-3 shows a terminal diagram of the PNP package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	
N	C/BE[3]	AD25	AD27	AD30	AD31	INTB	PRST	SERIRQ	GPIO0//CLKRUN	GPIO2	GPIO3//SDA	JTAG_TDI	GRST	**N**
M	AD20	AD22	AD24	AD26	AD28	INTA	INTC	LOCK	GPIO1//PWR_OVRD	GPIO4//SCL	JTAG_TDO	JTAG_TCK	WAKE	**M**
L	AD18	AD19	AD21	AD23	AD29	M66EN	INTD	VDD_33	JTAG_TRST#	JTAG_TMS	VSS	PME	VDD_15_COMB	**L**
K	AD16	AD17	PCIR	VSS	VSS	VSS	VDD_15	VSS	VDD_33	VSSA	VDD_33_COMB_IO	REF0_PCIE	REF1_PCIE	**K**
J	IRDY	FRAME	C/BE[2]	VDD_33	VSS	VSS	VSS	VSS	VSS	VSS	VDD_33_AUX	VDD_33	VDD_33_COMB	**J**
H	TRDY	DEVSEL	VDD_33	VSS	VSS	VSS	VSS	VSS	VSS	VDD_15	PERST	VSSA	VDDA_15	**H**
G	STOP	PERR	SERR#	VDD_15	VSS	VSS	VSS	VSS	VSS	VDD_15	VSSA	TXN	TXP	**G**
F	PAR	C/BE[1]	CLK	VSS	VSS	VSS	VSS	VSS	VSS	VDD_15	VSS	VSS	VDDA_15	**F**
E	AD15	AD14	AD13	VDD_33	VSS	VSS	VSS	VSS	VSS	VSSA	VSSA	RXN	RXP	**E**
D	AD12	AD11	AD8	VSS	VDD_33	VSS	VDD_15	VSS	VDD_33	VSS	CLKREQ	VREG_PD33	VDDA_33	**D**
C	AD10	AD9	AD7	AD5	AD0	GNT1	VDD_33	REQ3	REQ4	EXT_ARB_EN	VSSA	REFCLK–	REFCLK+	**C**
B	C/BE[0]	AD6	AD3	AD2	CLKOUT0	CLKOUT1	CLKOUT3	GNT2	GNT3	GNT5	CLKOUT6	PCLK66_SEL	REFCLK125_SEL	**B**
A	PCIR	AD4	AD1	REQ0	GNT0	REQ1	CLKOUT2	REQ2	CLKOUT4	CLKOUT5	GNT4	REQ5	CLKRUN_EN	**A**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	

Figure 2-1. XIO2001 ZGU MicroStar BGA Package (Bottom View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
N	AD21	AD24	AD27	AD28	AD31	$\overline{\text{INTA}}$	$\overline{\text{INTD}}$	$\overline{\text{LOCK}}$	GPIO0// $\overline{\text{CLKRUN}}$	GPIO2	JTAG_TDO	JTAG_TCK	VDD_15_ COMB	**N**
M	AD18	AD22	$\overline{\text{C/BE[3]}}$	AD25	AD29	M66EN	$\overline{\text{INTC}}$	SERIRQ	GPIO1// PWR_OVRD	GPIO4_ SCL	$\overline{\text{GRST}}$	$\overline{\text{PME}}$	REF0_PCIE	**M**
L	AD16	AD20	AD23	AD26	AD30	$\overline{\text{INTB}}$	$\overline{\text{PRST}}$	GPIO3//SDA	JTAG_ $\overline{\text{TRST}}$	JTAG_TDI	JTAG_TMS	$\overline{\text{WAKE}}$	REF1_PCIE	**L**
K	$\overline{\text{C/BE[2]}}$	AD19	AD17								VDD_33_ COMB_IO	VDD_33_ COMB	VDD_15	**K**
J	$\overline{\text{FRAME}}$	$\overline{\text{TRDY}}$	PCIR		VSS	VSS	VDD_15	VDD_15	VSS		VDD_33	VDD_33_ AUX	VSSA	**J**
H	$\overline{\text{STOP}}$	$\overline{\text{DEVSEL}}$	$\overline{\text{IRDY}}$		VSS	VDD_33	VDD_33	VDD_15	VSS		$\overline{\text{PERST}}$	VDDA_15	TXP	**H**
G	PAR	$\overline{\text{SERR}}$	$\overline{\text{PERR}}$		VSS	VDD_33	VDD_33	VDD_15	VSSA		VDD_15	VSSA	TXN	**G**
F	CLK	AD15	$\overline{\text{C/BE[1]}}$		VSS	VDD_33	VDD_33	VDD_33	VSS		VDD_15	VSS	VSSA	**F**
E	AD13	AD12	AD14		VDD_33	VSS	VSS	VSS	VSS		VREG_PD33	VDDA_15	RXP	**E**
D	AD11	AD9	PCIR								$\overline{\text{CLKREQ}}$	VSSA	RXN	**D**
C	AD10	$\overline{\text{C/BE[0]}}$	AD5	AD2	AD1	$\overline{\text{REQ1}}$	$\overline{\text{REQ2}}$	$\overline{\text{REQ3}}$	$\overline{\text{REQ5}}$	CLKOUT6	CLKRUN_EN	VDDA_33	REFCLK+	**C**
B	AD8		AD6	AD0	CLKOUT0	CLKOUT1	CLKOUT2	$\overline{\text{GNT2}}$	$\overline{\text{GNT3}}$	$\overline{\text{GNT4}}$	$\overline{\text{GNT5}}$	VSSA	REFCLK-	**B**
A	AD7	AD4	AD3	$\overline{\text{REQ0}}$	$\overline{\text{GNT0}}$	$\overline{\text{GNT1}}$	CLKOUT3	CLKOUT4	$\overline{\text{REQ4}}$	CLKOUT5	PCLK66_ SEL	EXT_ARB_ EN	REFCLK125 _SEL	**A**
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 2-2. XIO2001 ZAJ MicroStar BGA Package (Bottom View)

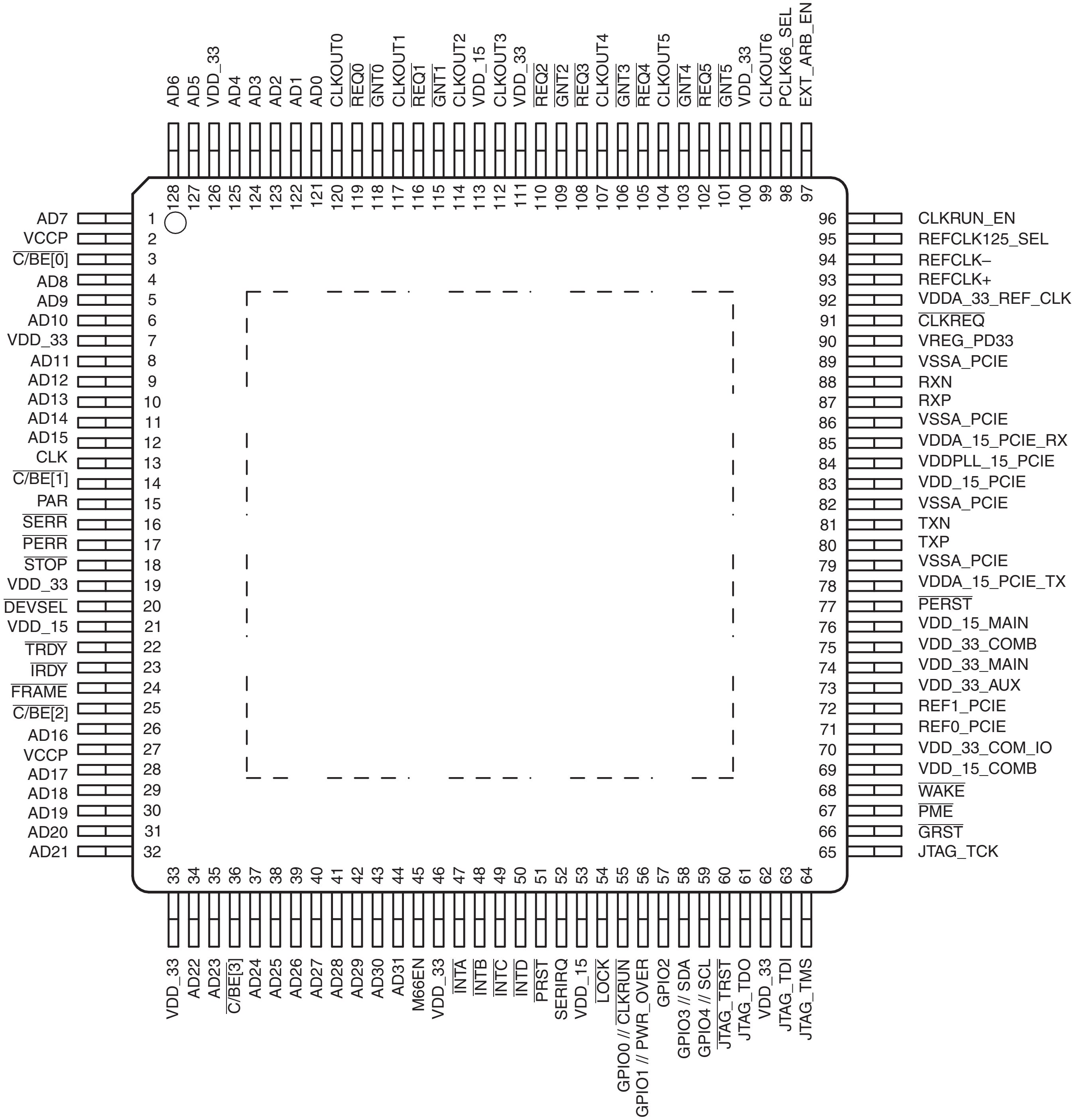


Figure 2-3. XIO2001 PNP PowerPad™ HTQFP Package (Top View)

2.6 Terminal Descriptions

The following tables give a description of the terminals. These terminals are grouped in tables by functionality. Each table includes the terminal name, terminal number, I/O type, and terminal description.

The following list describes the different input/output cell types that appear in the terminal description tables:

- HS DIFF IN = High speed differential input
- HS DIFF OUT = High speed differential output
- PCI BUS = PCI bus 3-state bidirectional buffer with 3.3-V or 5.0-V clamp rail.
- LV CMOS = 3.3-V low voltage CMOS input or output with 3.3-V clamp rail
- BIAS = Input/output terminals that generate a bias voltage to determine a driver's operating current
- Feed through = these terminals connect directly to macros within the part and not through an input or output cell.
- PWR = Power terminal
- GND = Ground terminal

Table 2-1. Power Supply Terminals

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	EXTERNAL PARTS	DESCRIPTION
PCIR	A01, K03	D03, J03		I/O	Resistor	PCI Rail. 5.0-V or 3.3-V PCI bus clamp voltage to set maximum I/O voltage tolerance of the secondary PCI bus signals. Connect this terminal to the secondary PCI bus I/O clamp rail through a 1kΩ resistor.
V_{DD_15}	G04, K07, D07, H10, G10, F10	J08, H08, J07, G08, N13, K13, G11, F11	21, 53, 113	PWR	Bypass capacitors	1.5-V digital core power terminals
V_{DDA_15}	F13, H13	E12, H12		PWR	Pi filter	1.5-V analog power terminal
V_{DD_33}	E04, H03, J04, L08, K09, D09, C07, D05, J12	E05, G06, H07, G07, H06, F08, F07, F06, J11	7, 19, 33, 46, 62, 100, 111, 126	PWR	Bypass capacitors	3.3-V digital I/O power terminal
$V_{DD\_33\_AUX}$	J11	J12	73	PWR	Bypass capacitors	3.3-V auxiliary power terminal **Note:** This terminal is connected to V_{SS} through a pulldown resistor if no auxiliary supply is present.
V_{DDA_33}	D13	C12		PWR	Pi filter	3.3-V analog power terminal

Table 2-2. Ground Terminals

SIGNAL	ZGU BALL #	ZAJ BALL #	I/O TYPE	DESCRIPTION
V_{SS}	D04, F04, H04, K04, K05, K06, K08, L11, J10, D10, D08, D06, F11, F12	E06, F05, G05, H05, J05, J06, J09, H09, E09, E08, E07, F12 ,F09	GND	Digital ground terminals
V_{SS}	E05, E06, E07, E08, E09, F05, F06, F07, F08, F09, G05, G06, G07, G08, G09, H05, H06, H07, H08, H09, J05, J06, J07, J08, J09		GND	Ground terminals for thermally-enhanced package
V_{SSA}	K10, C11, H12, G11, E11, E10	G09, B12, J13, G12, F13, D12	GND	Analog ground terminal

Table 2-3. Combined Power Output Terminals

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	EXTERNAL PARTS	DESCRIPTION
$V_{DD\_15\_COMB}$	L13	N13	69	Feed through	Bypass capacitors	Internally-combined 1.5-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 1.5-V circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power to other devices.
$V_{DD\_33\_COMB}$	J13	K12	75	Feed through	Bypass capacitors	Internally-combined 3.3-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 3.3-V circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power to other devices.
$V_{DD\_33\_COMBIO}$	K11	K11	70	Feed through	Bypass capacitors	Internally-combined 3.3-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 3.3-V input/output circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power to other devices.

Table 2-4. PCI Express Terminals

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
$\overline{\text{CLKREQ}}$	D11	D11	91	0	LV CMOS	$V_{DD\_33\_COMBIO}$	–	Clock request. When asserted low, requests upstream device start clock in cases where clock may be removed in L1. **Note:** Since $\overline{\text{CLKREQ}}$ is an open-drain output buffer, a system side pullup resistor is required.
$\overline{\text{PERST}}$	H11	H11	77	I	LV CMOS	$V_{DD\_33\_COMBIO}$	–	PCI Express reset input. The $\overline{\text{PERST}}$ signal identifies when the system power is stable and generates an internal power on reset. **Note:** The $\overline{\text{PERST}}$ input buffer has hysteresis.
REFCLK125_SEL	B13	A13	95	I	LV CMOS	V_{DD_33}	Pullup or pulldown resistor	Reference clock select. This terminal selects the reference clock input. 0 = 100-MHz differential common reference clock used. 1 = 125-MHz single-ended, reference clock used.

Table 2-4. PCI Express Terminals (continued)

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
REFCLK+	C13	C13	93	DI	HS DIFF IN	V_{DD_33}	–	Reference clock. REFCLK+ and REFCLK– comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, use the REFCLK+ input.
REFCLK–	C12	B13	94	DI	HS DIFF IN	V_{DD_33}	Capacitor for V_{SS} for single-ended node	Reference clock. REFCLK+ and REFCLK– comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, attach a capacitor from REFCLK– to V_{SS}.
REF0_PCIE REF1_PCIE	K12 K13	M13 L13	71 72	I/O	BIAS	–	External resistor	External reference resistor + and – terminals for setting TX driver current. An external resistance of 14,532-Ω is connected between REF0_PCIE and REF1_PCIE terminals. To eliminate the need for a custom resistor, two series resistors are recommended: a 14.3-kΩ, 1% resistor and a 232-Ω, 1% resistor.
RXP RXN	E13 E12	E13 D13	87 88	DI	HS DIFF IN	V_{SS}	–	High-speed receive pair. RXP and RXN comprise the differential receive pair for the single PCI Express lane supported.
TXP TXN	G13 G12	H13 G13	80 81	DO	HS DIFF OUT	V_{DD_15}	Series capacitor	High-speed transmit pair. TXP and TXN comprise the differential transmit pair for the single PCI Express lane supported.
$\overline{\text{WAKE}}$	M13	L12	68	O	LV CMOS	$V_{DD\_33\_COMBIO}$	–	Wake is an active low signal that is driven low to reactivate the PCI Express link hierarchy's main power rails and reference clocks. **Note**: Since $\overline{\text{WAKE}}$ is an open-drain output buffer, a system side pullup resistor is required.

Table 2-5. PCI System Terminals

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
AD31	N05	N05	44	I/O	PCI Bus	PCIR	–	PCI address data lines
AD30	N04	L05	43					
AD29	L05	M05	42					
AD28	M05	N04	41					
AD27	N03	N03	40					
AD26	M04	L04	39					
AD25	N02	M04	38					
AD24	M03	N02	37					
AD23	L04	L03	35					
AD22	M02	M02	34					
AD21	L03	N01	32					
AD20	M01	L02	31					
AD19	L02	K02	30					
AD18	L01	M01	29					
AD17	K02	K03	28					
AD16	K01	L01	26					
AD15	E01	F02	12					
AD14	E02	E03	11					
AD13	E03	E01	10					
AD12	D01	E02	9					
AD11	D02	D01	8					
AD10	C01	C01	6					
AD9	C02	D02	5					
AD8	D03	B01	4					
AD7	C03	A01	1					
AD6	B02	B03	128					
AD5	C04	C03	127					
AD4	A02	A02	125					
AD3	B03	A03	124					
AD2	B04	C04	123					
AD1	A03	C05	122					
AD0	C05	B04	121					

Table 2-5. PCI System Terminals (continued)

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
C/BE[3] C/BE[2] C/BE[1] C/BE[0]	N01 J03 F02 B01	M03 K01 F03 C02	36 25 14 3	I/O	PCI Bus	PCIR	–	PCI command byte enables
CLK	F03	F01	13	I	PCI Bus	PCIR	–	PCI clock input. This is the clock input to the PCI bus core.
CLKOUT0 CLKOUT1 CLKOUT2 CLKOUT3 CLKOUT4 CLKOUT5 CLKOUT6	B05 B06 A07 B07 A09 A10 B11	B05 B06 B07 A07 A08 A10 C10	120 117 114 112 107 104 99	O	PCI Bus	PCIR	–	PCI clock outputs. These clock outputs are used to clock the PCI bus. If the bridge PCI bus clock outputs are used, then CLKOUT6 must be connected to the CLK input.
DEVSEL	H02	H02	20	I/O	PCI Bus	PCIR	Pullup resistor per PCI spec	PCI device select
FRAME	J02	J01	24	I/O	PCI Bus	PCIR	Pullup resistor per PCI spec	PCI frame
GNT5 GNT4 GNT3 GNT2 GNT1 GNT0	B10 A11 B09 B08 C06 A05	B11 B10 B09 B08 A06 A05	101 103 106 109 115 118	O	PCI Bus	PCIR	–	PCI grant outputs. These signals are used for arbitration when the PCI bus is the secondary bus and an external arbiter is not used. GNT0 is used as the REQ for the bridge when an external arbiter is used.
INTA INTB INTC INTD	M06 N06 M07 L07	N06 L06 M07 N07	47 48 49 50	I	PCI Bus	PCIR	Pullup resistor per PCI spec	PCI interrupts A–D. These signals are interrupt inputs to the bridge on the secondary PCI bus.
IRDY	J01	H03	23	I/O	PCI Bus	PCIR	Pullup resistor per PCI spec	PCI initiator ready
LOCK	M08	N08	54	I/O	PCI Bus	PCIR	Pullup resistor per PCI spec	This terminal functions as PCI LOCK when bit 12 (LOCK_EN) is set in the general control register (see Section 4.65). **Note**: In lock mode, an external pullup resistor is required to prevent the LOCK signal from floating.
M66EN	L06	M06	45	I	PCI Bus	PCIR	Pullup resistor per PCI spec	66-MHz mode enable 0 = Secondary PCI bus and clock outputs operate at 33 MHz. If PCLK66_SEL is low then the frequency will be 25 MHz. 1 = Secondary PCI bus and clock outputs operate at 66 MHz. If PCLK66_SEL is low then the frequency will be 50 MHz.
PAR	F01	G01	15	I/O	PCI Bus	PCIR	–	PCI bus parity
PERR	G02	G03	17	I/O	PCI Bus	PCIR	Pullup resistor per PCI spec	PCI parity error
PME	L12	M12	67	I	LV CMOS	$V_{DD\_33\_COMBIO}$	Pullup resistor per PCI spec	Pullup resistor per PCI spec PCI power management event. This terminal may be used to detect PME events from a PCI device on the secondary bus. **Note:** The PME input buffer has hysteresis.

Table 2-5. PCI System Terminals (continued)

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
$\overline{\text{REQ5}}$ $\overline{\text{REQ4}}$ $\overline{\text{REQ3}}$ $\overline{\text{REQ2}}$ $\overline{\text{REQ1}}$ $\overline{\text{REQ0}}$	A12 C09 C08 A08 A06 A04	C09 A09 C08 C07 C06 A04	102 105 108 110 116 119	I	PCI Bus	PCIR	If unused, a weak pullup resistor per PCI spec	PCI request inputs. These signals are used for arbitration on the secondary PCI bus when an external arbiter is not used. $\overline{\text{REQ0}}$ is used as the $\overline{\text{GNT}}$ for the bridge when an external arbiter is used.
$\overline{\text{PRST}}$	N07	L07	51	O	PCI Bus	PCIR	–	PCI reset. This terminal is an output to the secondary PCI bus.
$\overline{\text{SERR}}$	G03	G02	16	I/O	PCI Bus	PCIR	Pullup resistor per PCI spec	PCI system error
$\overline{\text{STOP}}$	G01	H01	18	I/O	PCI Bus	PCIR	Pullup resistor per PCI spec	PCI stop
$\overline{\text{TRDY}}$	H01	J02	22	I/O	PCI Bus	PCIR	Pullup resistor per PCI spec	PCI target ready

Table 2-6. JTAG Terminals

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
JTAG_TCK	M12	N12	65	I	LV CMOS	V_{DD_33}	Optional pullup resistor	JTAG test clock input. This signal provides the clock for the internal TAP controller. **Note**: This terminal has an internal active pullup resistor. The pullup is active at all times. **Note**: This terminal should be tied to ground or pulled low if JTAG is not required.
JTAG_TDI	N12	L10	63	I	LV CMOS	V_{DD_33}	Optional pullup resistor	JTAG test data input. Serial test instructions and data are received on this terminal. **Note**: This terminal has an internal active pullup resistor. The pullup is active at all times. **Note**: This terminal can be left unconnected if JTAG is not required.
JTAG_TDO	M11	N11	61	O	LV CMOS	V_{DD_33}	–	JTAG test data output. This terminal the serial output for test instructions and data. **Note**: This terminal can be left unconnected if JTAG is not required.
JTAG_TMS	L10	L11	64	I	LV CMOS	V_{DD_33}	Optional pullup resistor	JTAG test mode select. The signal received at JTAG_TMS is decoded by the internal TAP controller to control test operations. **Note**: This terminal has an internal active pullup resistor. The pullup is active at all times. **Note**: This terminal can be left unconnected if JTAG is not required.

Table 2-6. JTAG Terminals (continued)

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
JTAG_TRST	L09	L09	60	I	LV CMOS	V_{DD_33}	Optional pullup resistor	JTAG test reset. This terminal provides Optional for asynchronous initialization of the TAP controller. **Note**: This terminal has an internal active pullup resistor. The pullup is active at all times. **Note**: This terminal should be tied to ground or pulled low if JTAG is not required.

Table 2-7. Miscellaneous Terminals

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
CLKRUN_EN	A13	C11	96	I	LV CMOS	V_{DD_33}	Optional pullup resistor	Clock run enable 0 = Clock run support disabled 1 = Clock run support enabled **Note**: The CLKRUN_EN input buffer has an internal active pulldown. This pulldown is active at all times.
EXT_ARB_EN	C10	A12	97	I	LV CMOS	V_{DD_33}	Optional pullup resistor	External arbiter enable 0 = Internal arbiter enabled 1 = External arbiter enabled **Note**: The EXT_ARB_EN input buffer has an internal active pulldown. This pulldown is active at all times.
GPIO0 // CLKRUN	N09	N09	55	I/O	LV CMOS	V_{DD_33}	Optional pullup resistor	General-purpose I/O 0/clock run. This terminal functions as a GPIO controlled by bit 0 (GPIO0_DIR) in the GPIO control register (see Section 4.59) or the clock run terminal. This terminal is used as clock run input when the bridge is placed in clock run mode. **Note**: In clock run mode, an external pullup resistor is required to prevent the CLKRUN signal from floating. **Note**: This terminal has an internal active pullup resistor. The pullup is only active when reset is asserted or when the GPIO is configured as an input.
GPIO1 // PWR_OVRD	M09	M09	56	I/O	LV CMOS	V_{DD_33}	–	General-purpose I/O 1/power override. This terminal functions as a GPIO controlled by bit 1 (GPIO1_DIR) in the GPIO control register (see Section 4.59) or the power override output terminal. GPIO1 becomes PWR_OVRD when bits 22:20 (POWER_OVRD) in the general control register are set to 001b or 011b (see Section 4.65). **Note**: This terminal has an internal active pullup resistor. The pullup is only active when reset is asserted or when the GPIO is configured as an input.
GPIO2	N10	N10	57	I/O	LV CMOS	V_{DD_33}	–	General-purpose I/O 2. This terminal functions as a GPIO controlled by bit 2 (GPIO2_DIR) in the GPIO control register (see Section 4.59). **Note**: This terminal has an internal active pullup resistor. The pullup is only active when reset is asserted or when the GPIO is configured as an input.

Table 2-7. Miscellaneous Terminals (continued)

SIGNAL	ZGU BALL #	ZAJ BALL #	PNP PIN #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
GPIO3 // SDA	N11	L08	58	I/O	LV CMOS	V_{DD_33}	Optional pullup resistor	GPIO3 or serial-bus data. This terminal functions as serial-bus data if a pullup resistor is detected on SCL or when the SBDETECT bit is set in the Serial Bus Control and Status Register (see Section 4.58). If no pullup is detected then this terminal functions as GPIO3. **Note**: In serial-bus mode, an external pullup resistor is required to prevent the SDA signal from floating.
GPIO4 // SCL	M10	M10	59	I/O	LV CMOS	V_{DD_33}	Optional pullup resistor	GPIO4 or serial-bus clock. This terminal functions as serial-bus clock if a pullup resistor is detected on SCL or when the SBDETECT bit is set in the Serial Bus Control and Status Register (see Section 4.58). If no pullup is detected then this terminal functions as GPIO4. **Note**: In serial-bus mode, an external pullup resistor is required to prevent the SCL signal from floating. **Note**: This terminal has an internal active pullup resistor. The pullup is only active when reset is asserted or when the GPIO is configured as an input.
$\overline{\text{GRST}}$	N13	M11	66	I	LV CMOS	$V_{DD\_33\_COMBIO}$	–	Global reset input. Asynchronously resets all logic in device, including sticky bits and power management state machines. **Note**: The GRST input buffer has both hysteresis and an internal active pullup. The pullup is active at all times.
PCLK66_SEL	B12	A11	98	I	LV CMOS	V_{DD_33}	Optional pulldown resistor	PCI clock select. This terminal determines the default PCI clock frequency driven out the CLKOUTx terminals. 0 = 50 MHz PCI Clock 1 = 66 MHz PCI Clock **Note**: This terminal has an internal active pullup resistor. This pullup is active at all times. **Note**: M66EN terminal also has an affect of PCI clock frequency.
SERIRQ	N08	M08	52	I/O	PCI Bus	PCIR	Pullup or pulldown resistor	Serial IRQ interface. This terminal functions as a serial $\overline{\text{IRQ}}$ interface if a pullup is detected when $\overline{\text{PERST}}$ is deasserted. If a pulldown is detected, then the serial IRQ interface is disabled.
VREG_PD33	D12	E11	90	I	LV CMOS	$V_{DD\_33\_COMBIO}$	Pulldown resistor	3.3-V voltage regulator powerdown. This terminal should always be tied directly to ground or an optional pulldown resistor can be used.

3 Feature/Protocol Descriptions

This chapter provides a high-level overview of all significant device features. Figure 3-1 shows a simplified block diagram of the basic architecture of the PCI-Express to PCI Bridge. The top of the diagram is the PCI Express interface and the PCI bus interface is located at the bottom of the diagram.

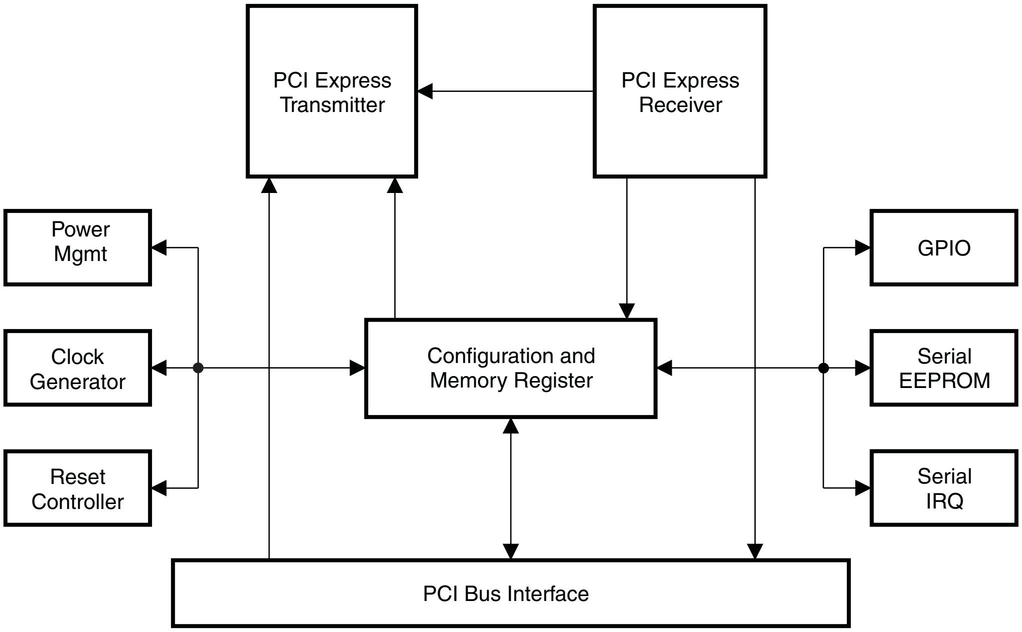


Figure 3-1. XIO2001 Block Diagram

3.1 Power-Up/-Down Sequencing

The bridge contains both 1.5-V and 3.3-V power terminals. The following power-up and power-down sequences describe how power is applied to these terminals.

In addition, the bridge has three resets: $\overline{\text{PERST}}$, $\overline{\text{GRST}}$ and an internal power-on reset. These resets are fully described in Section 3.2. The following power-up and power-down sequences describe how $\overline{\text{PERST}}$ is applied to the bridge.

The application of the PCI Express reference clock (REFCLK) is important to the power-up/-down sequence and is included in the following power-up and power-down descriptions.

3.1.1 Power-Up Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Apply 1.5-V and 3.3-V voltages.
3. Apply PCIR clamp voltage.
4. Apply a stable PCI Express reference clock.
5. To meet PCI Express specification requirements, $\overline{\text{PERST}}$ cannot be deasserted until the following two delay requirements are satisfied:
   - Wait a minimum of 100 μs after applying a stable PCI Express reference clock. The 100-μs limit satisfies the requirement for stable device clocks by the deassertion of $\overline{\text{PERST}}$.
   - Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the deassertion of $\overline{\text{PERST}}$.

See the power-up sequencing diagram in Figure 3-2.

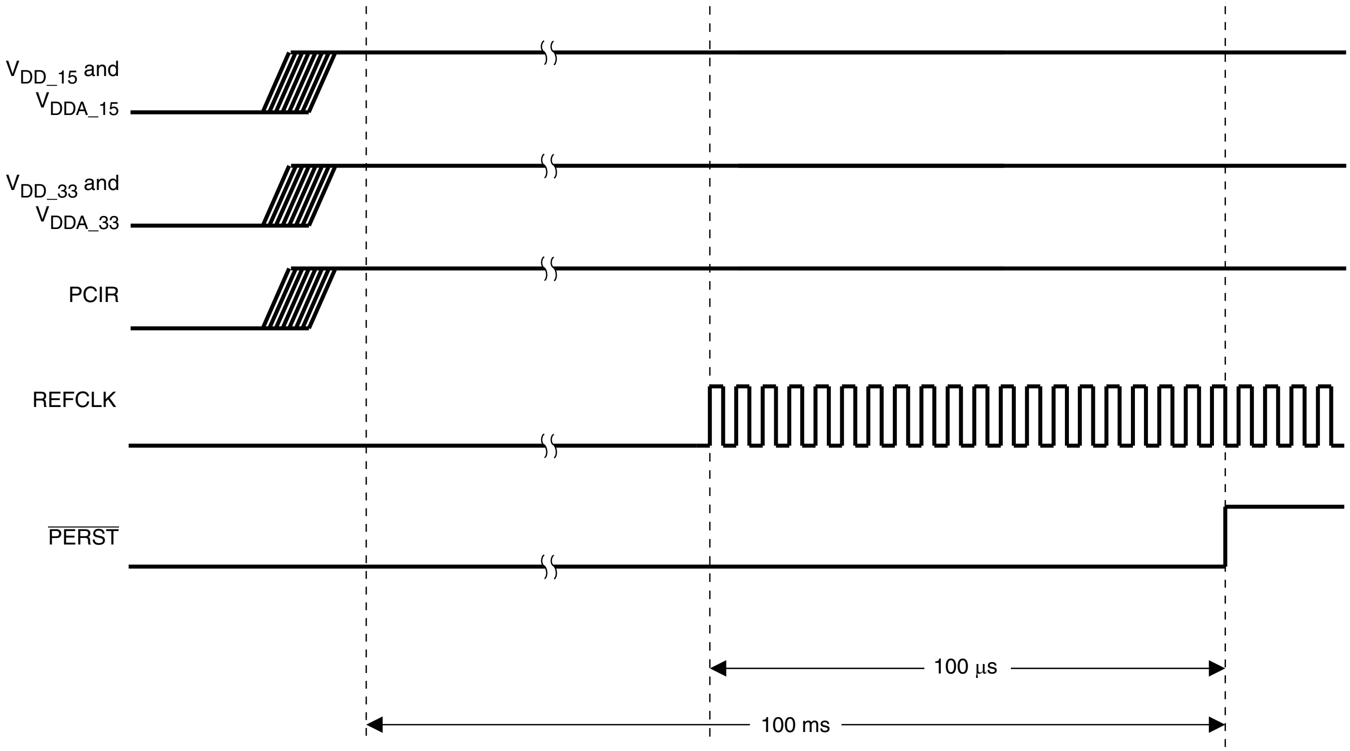


Figure 3-2. Power-Up Sequence

3.1.2 Power-Down Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Remove the reference clock.
3. Remove PCIR clamp voltage.
4. Remove 3.3-V and 1.5-V voltages.

See the power-down sequencing diagram in Figure 3-3. If the $V_{DD\_33\_AUX}$ terminal is to remain powered after a system shutdown, then the bridge power-down sequence is exactly the same as shown in Figure 3-3.

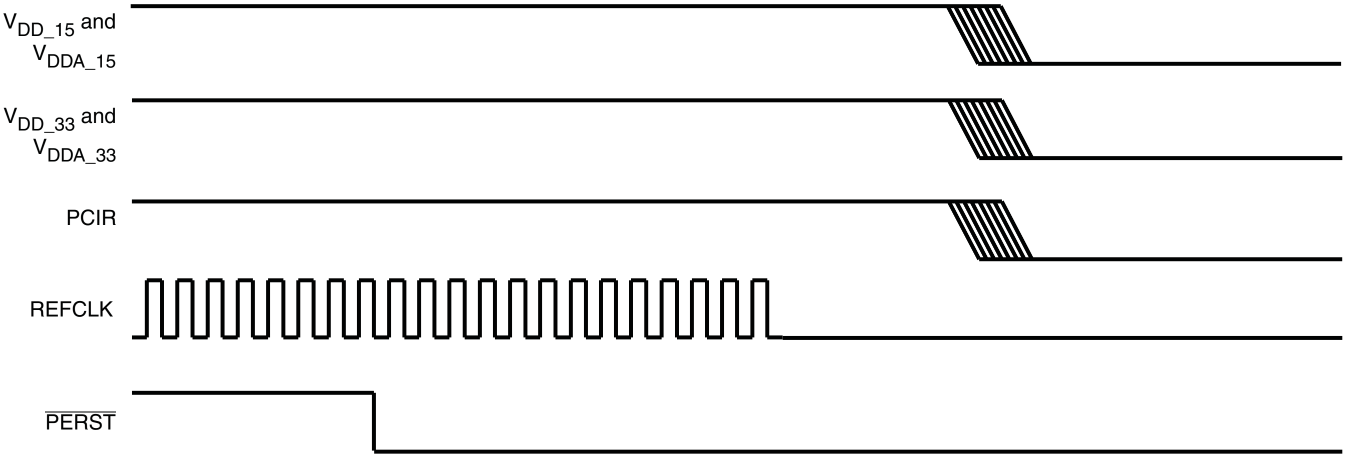


Figure 3-3. Power-Down Sequence

3.2 Bridge Reset Features

There are five bridge reset options that include internally-generated power-on reset, resets generated by asserting input terminals, and software-initiated resets that are controlled by sending a PCI Express hot reset or setting a configuration register bit. Table 3-1 identifies these reset sources and describes how the bridge responds to each reset.

Table 3-1. XIO2001 Reset Options

RESET OPTION	XIO2001 FEATURE	RESET RESPONSE
Bridge internally-generated power-on reset	During a power-on cycle, the bridge asserts an internal reset and monitors the $V_{DD\_15\_COMB}$ terminal. When this terminal reaches 90% of the nominal input voltage specification, power is considered stable. After stable power, the bridge monitors the PCI Express reference clock (REFCLK) and waits 10 μs after active clocks are detected. Then, internal power-on reset is deasserted.	When the internal power-on reset is asserted, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. In addition, the XIO2001 asserts the internal PCI bus reset.
Global reset input $\overline{\text{GRST}}$	When $\overline{\text{GRST}}$ is asserted low, an internal power-on reset occurs. This reset is asynchronous and functions during both normal power states and V_{AUX} power states.	When $\overline{\text{GRST}}$ is asserted low, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. In addition, the bridge asserts PCI bus reset ($\overline{\text{PRST}}$). When the rising edge of $\overline{\text{GRST}}$ occurs, the bridge samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The bridge starts link training within 80 ms after $\overline{\text{GRST}}$ is deasserted.

Table 3-1. XIO2001 Reset Options (continued)

RESET OPTION	XIO2001 FEATURE	RESET RESPONSE
PCI Express reset input $\overline{\text{PERST}}$	This XIO2001 input terminal is used by an upstream PCI Express device to generate a PCI Express reset and to signal a system power good condition. When $\overline{\text{PERST}}$ is asserted low, the XIO2001 generates an internal PCI Express reset as defined in the PCI Express specification. When $\overline{\text{PERST}}$ transitions from low to high, a system power good condition is assumed by the XIO2001. **Note:** The system must assert $\overline{\text{PERST}}$ before power is removed, before REFCLK is removed or before REFCLK becomes unstable.	When $\overline{\text{PERST}}$ is asserted low, all control register bits that are not sticky are reset. Within the configuration register maps, the sticky bits are indicated by the ┤ symbol. Also, all state machines that are not associated with sticky functionality are reset. In addition, the XIO2001 asserts the internal PCI bus reset. When the rising edge of $\overline{\text{PERST}}$ occurs, the XIO2001 samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The XIO2001 starts link training within 80 ms after $\overline{\text{PERST}}$ is deasserted.
PCI Express training control hot reset	The XIO2001 responds to a training control hot reset received on the PCI Express interface. After a training control hot reset, the PCI Express interface enters the DL_DOWN state.	In the DL_DOWN state, all remaining configuration register bits and state machines are reset. All remaining bits exclude sticky bits and EEPROM loadable bits. All remaining state machines exclude sticky functionality and EEPROM functionality. Within the configuration register maps, the sticky bits are indicated by the ┤ symbol and the EEPROM loadable bits are indicated by the † symbol. In addition, the XIO2001 asserts the internal PCI bus reset.
PCI bus reset $\overline{\text{PRST}}$	System software has the ability to assert and deassert the $\overline{\text{PRST}}$ terminal on the secondary PCI bus interface. This terminal is the PCI bus reset.	When bit 6 (SRST) in the bridge control register at offset 3Eh (see Section 4.29) is asserted, the bridge asserts the $\overline{\text{PRST}}$ terminal. A 0 in the SRST bit deasserts the $\overline{\text{PRST}}$ terminal.

3.3 PCI Express Interface

3.3.1 External Reference Clock

The bridge requires either a differential, 100-MHz common clock reference or a single-ended, 125-MHz clock reference. The selected clock reference must meet all *PCI Express Electrical Specification* requirements for frequency tolerance, spread spectrum clocking, and signal electrical characteristics. Spread Spectrum is an optional feature of the *PCI Express Electrical Specification* that is supported by this bridge.

If the REFCLK125_SEL input is connected to V_{SS}, then a differential, 100-MHz common clock reference is expected by the XIO2001. If the REFCLK125_SEL terminal is connected to V_{DD_33}, then a single-ended, 125-MHz clock reference is expected by the bridge

When the single-ended, 125-MHz clock reference option is enabled, the single-ended clock signal is connected to the REFCLK+ terminal. The REFCLK– terminal is connected to one side of an external capacitor with the other side of the capacitor connected to V_{SS}.

When using a single-ended reference clock, care must be taken to ensure interoperability from a system jitter standpoint. The *PCI Express Base Specification* does not ensure interoperability when using a differential reference clock commonly used in PC applications along with a single-ended clock in a non-common clock architecture. System jitter budgets will have to be verified to ensure interoperability. See the *PCI Express Jitter and BER White Paper* from the PCI-SIG.

3.3.2 Beacon

The bridge supports the PCI Express in-band beacon feature. Beacon is driven on the upstream PCI Express link by the bridge to request the reapplication of main power when in the L2 link state. To enable the beacon feature, bit 10 (BEACON_ENABLE) in the general control register at offset D4h is asserted. See Section 4.65, General Control Register, for details.

If the bridge is in the L2 link state and beacon is enabled, when a secondary PCI bus device asserts PME, then the bridge outputs the beacon signal on the upstream PCI Express link. The beacon signal frequency is approximately 500 kHz ± 50% with a differential peak-to-peak amplitude of 500 mV and no de-emphasis. Once the beacon is activated, the bridge continues to send the beacon signal until main power is restored as indicated by PERST going inactive. At this time, the beacon signal is deactivated.

3.3.3 Wake

The bridge supports the PCI Express sideband WAKE feature. WAKE is an active low signal driven by the bridge to request the reapplication of main power when in the L2 link state. Since WAKE is an open-collector output, a system-side pullup resistor is required to prevent the signal from floating.

When the bridge is in the L2 link state and PME is received from a device on the secondary PCI bus, the WAKE signal is asserted low as a wakeup mechanism. Once WAKE is asserted, the bridge drives the signal low until main power is restored as indicated by PERST going inactive. At this time, WAKE is deasserted.

3.3.4 Initial Flow Control Credits

The bridge flow control credits are initialized using the rules defined in the *PCI Express Base Specification*. Table 3-2 identifies the initial flow control credit advertisement for the bridge.

Table 3-2. Initial Flow Control Credit Advertisements

CREDIT TYPE	INITIAL ADVERTISEMENT
Posted request headers (PH)	8
Posted request data (PD)	128
Non-posted header (NPH)	4
Non-posted data (NPD)	4
Completion header (CPLH)	0 (infinite)
Completion data (CPLD)	0 (infinite)

3.3.5 PCI Express Message Transactions

PCI Express messages are both initiated and received by the bridge. Table 3-3 outlines message support within the bridge.

Table 3-3. Messages Supported by the Bridge

MESSAGE	SUPPORTED	BRIDGE ACTION
Assert_INTx	Yes	Transmitted upstream
Deassert_INTx	Yes	Transmitted upstream
PM_Active_State_Nak	Yes	Received and processed
PM_PME	Yes	Transmitted upstream
PME_Turn_Off	Yes	Received and processed
PME_TO_Ack	Yes	Transmitted upstream
ERR_COR	Yes	Transmitted upstream
ERR_NONFATAL	Yes	Transmitted upstream

Table 3-3. Messages Supported by the Bridge (continued)

MESSAGE	SUPPORTED	BRIDGE ACTION
ERR_FATAL	Yes	Transmitted upstream
Set_Slot_Power_Limit	Yes	Received and processed
Unlock	No	Discarded
Hot plug messages	No	Discarded
Advanced switching messages	No	Discarded
Vendor defined type 0	No	Unsupported request
Vendor defined type 1	No	Discarded

All supported message transactions are processed per the *PCI Express Base Specification*.

3.4 PCI Bus Interface

3.4.1 I/O Characteristics

Figure 3-4 shows a 3-state bi-directional buffer that represents the I/O cell design for the PCI bus. Section 7.7, *Electrical Characteristics over Recommended Operating Conditions*, provides the electrical characteristics of the PCI bus I/O cell.

NOTE

The PCI bus interface on the bridge meets the ac specifications of the *PCI Local Bus Specification*. Additionally, PCI bus terminals (input or I/O) must be held high or low to prevent them from floating.

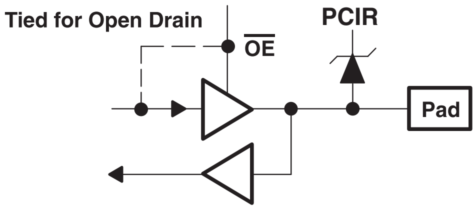


Figure 3-4. 3-State Bidirectional Buffer

3.4.2 Clamping Voltage

In the bridge, the PCI bus I/O drivers are powered from the V_{DD_33} power rail. Plus, the I/O driver cell is tolerant to input signals with 5-V peak-to-peak amplitudes.

For PCI bus interfaces operating at 50MHz or 66 MHz, all devices are required to output only 3.3-V peak-to-peak signal amplitudes. For PCI bus interfaces operating at 25-MHz or 33-MHz, devices may output either 3.3-V or 5-V peak-to-peak signal amplitudes. The bridge accommodates both signal amplitudes.

Each PCI bus I/O driver cell has a clamping diode connected to the internal V_{CCP} voltage rail that protects the cell from excessive input voltage. The internal V_{CCP} rail is connected to two PCIR terminals. If the PCI signaling is 3.3-V, then PCIR terminals are connected to a 3.3-V power supply via a 1kΩ resistor. If the PCI signaling is 5-V, then the PCIR terminals are connected to a 5-V power supply via a 1kΩ resistor.

The PCI bus signals attached to the V_{CCP} clamping voltage are identified as follows

- Table 2-5, PCI System Terminals, all terminal names except for $\overline{\text{PME}}$
- Table 2-7, Miscellaneous Terminals, the terminal name SERIRQ.

3.4.3 PCI Bus Clock Run

The bridge supports the clock run protocol as specified in the PCI Mobile Design Guide. When the clock run protocol is enabled, the bridge assumes the role of the central resource master.

To enable the clock run function, terminal CLKRUN_EN is asserted high. Then, terminal GPIO0 is enabled as the CLKRUN signal. An external pullup resistor must be provided to prevent the CLKRUN signal from floating To verify the operational status of the PCI bus clocks, bit 0 (SEC_CLK_STATUS) in the clock run status register at offset DAh (see Section 4.68) is read.

Since the bridge has several unique features associated with the PCI bus interface, the system designer must consider the following interdependencies between these features and the CLKRUN feature:

1. If the system designer chooses to generate the PCI bus clock externally, then the CLKRUN mode of the bridge must be disabled. The central resource function within the bridge only operates as a CLKRUN master and does not support the CLKRUN slave mode.
2. If the central resource function has stopped the PCI bus clocks, then the bridge still detects INTx state changes and will generate and send PCI Express messages upstream.
3. If the serial IRQ interface is enabled and the central resource function has stopped the PCI bus clocks, then any PCI bus device that needs to report an IRQ interrupt asserts CLKRUN to start the bus clocks.
4. When a PCI bus device asserts CLKRUN, the central resource function turns on PCI bus clocks for a minimum of 512 cycles.
5. If the serial IRQ function detects an IRQ interrupt, then the central resource function keeps the PCI bus clocks running until the IRQ interrupt is cleared by software.
6. If the central resource function has stopped the PCI bus clocks and the bridge receives a downstream transaction that is forwarded to the PCI bus interface, then the bridge asserts CLKRUN to start the bus clocks.
7. The central resource function is reset by PCI bus reset (PRST) assuring that clocks are present during PCI bus resets.

3.4.4 PCI Bus External Arbiter

The bridge supports an external arbiter for the PCI bus. Terminal (EXT_ARB_EN), when asserted high, enables the use of an external arbiter.

When an external arbiter is enabled, GNT0 is connected to the external arbiter as the REQ for the bridge. Likewise, REQ0 is connected to the external arbiter as the GNT for the bridge.

3.4.5 MSI Messages Generated from the Serial IRQ Interface

When properly configured, the bridge converts PCI bus serial IRQ interrupts into PCI Express message signaled interrupts (MSI). classic PCI configuration register space is provided to enable this feature. The following list identifies the involved configuration registers:

1. Command register at offset 04h, bit 2 (MASTER_ENB) is asserted (see Table 4-2).
2. MSI message control register at offset 52h, bits 0 (MSI_EN) and 6:4 (MM_EN) enable single and multiple MSI messages, respectively (see Section 4.42).
3. MSI message address register at offsets 54h and 58h specifies the message memory address. A nonzero address value in offset 58h initiates 64-bit addressing (see Section 4.37 and Section 4.44).
4. MSI message data register at offset 5Ch specifies the system interrupt message (see Section 4.45).
5. Serial IRQ mode control register at offset E0h specifies the serial IRQ bus format (see Section 4.72).
6. Serial IRQ edge control register at offset E2h selects either level or edge mode interrupts (see Section 4.73).
7. Serial IRQ status register at offset E4h reports level mode interrupt status (see Section 4.74).

A PCI Express MSI is generated based on the settings in the serial IRQ edge control register. If the system is configured for edge mode, then an MSI message is sent when the corresponding serial IRQ interface sample phase transitions from low to high. If the system is configured for level mode, then an MSI message is sent when the corresponding IRQ status bit in the serial IRQ status register changes from low to high.

The bridge has a dedicated SERIRQ terminal for all PCI bus devices that support serialized interrupts. This SERIRQ interface is synchronous to the PCI bus clock input (CLK) frequency. The bridge always generates a 17-phase serial IRQ stream. Internally, the bridge detects only 16 IRQ interrupts, IRQ0 frame through IRQ15 frame. The IOCHCK frame is not monitored by the serial IRQ state machine and never generates an IRQ interrupt or MSI message.

The multiple message enable (MM_EN) field determines the number of unique MSI messages that are sent upstream on the PCI Express link. From 1 message to 16 messages, in powers of 2, are selectable. If fewer than 16 messages are selected, then the mapping from IRQ interrupts to MSI messages is aliased. Table 3-4 illustrates the IRQ interrupt to MSI message mapping based on the number of enabling messages.

Table 3-4. IRQ Interrupt to MSI Message Mapping

IRQ INTERRUPT	1 MESSAGE ENABLED	2 MESSAGES ENABLED	4 MESSAGES ENABLED	8 MESSAGES ENABLED	16 MESSAGES ENABLED
IRQ0	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #0
IRQ1	MSI MSG #0	MSI MSG #1	MSI MSG #1	MSI MSG #1	MSI MSG #1
IRQ2	MSI MSG #0	MSI MSG #0	MSI MSG #2	MSI MSG #2	MSI MSG #2
IRQ3	MSI MSG #0	MSI MSG #1	MSI MSG #3	MSI MSG #3	MSI MSG #3
IRQ4	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #4	MSI MSG #4
IRQ5	MSI MSG #0	MSI MSG #1	MSI MSG #1	MSI MSG #5	MSI MSG #5
IRQ6	MSI MSG #0	MSI MSG #0	MSI MSG #2	MSI MSG #6	MSI MSG #6
IRQ7	MSI MSG #0	MSI MSG #1	MSI MSG #3	MSI MSG #7	MSI MSG #7
IRQ8	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #8
IRQ9	MSI MSG #0	MSI MSG #1	MSI MSG #1	MSI MSG #1	MSI MSG #9
IRQ10	MSI MSG #0	MSI MSG #0	MSI MSG #2	MSI MSG #2	MSI MSG #10
IRQ11	MSI MSG #0	MSI MSG #1	MSI MSG #3	MSI MSG #3	MSI MSG #11
IRQ12	MSI MSG #0	MSI MSG #0	MSI MSG #0	MSI MSG #4	MSI MSG #12
IRQ13	MSI MSG #0	MSI MSG #1	MSI MSG #1	MSI MSG #5	MSI MSG #13
IRQ14	MSI MSG #0	MSI MSG #0	MSI MSG #2	MSI MSG #6	MSI MSG #14
IRQ15	MSI MSG #0	MSI MSG #1	MSI MSG #3	MSI MSG #7	MSI MSG #15

The MSI message format is compatible with the PCI Express request header format for 32-bit and 64-bit memory write transactions. The system message and message number fields are included in bytes 0 and 1 of the data payload.

3.4.6 PCI Bus Clocks

The bridge has seven PCI bus clock outputs and one PCI bus clock input. Up to six PCI bus devices are supported by the bridge.

Terminal PCLK66_SEL selects the default operating frequency. This signal works in conjunction with terminal M66EN to determine the final output frequency. When PCLK66_SEL is asserted high then the clock frequency will be either 66-MHz or 33-MHz depending on the state of M66EN. When M66EN is asserted high then the clock frequency will be 66-MHz, when M66EN is de-asserted the clock frequency will be 33-MHz. When PCLK66_SEL is de-asserted then the clock frequency will be either 50-MHz or 25-MHz. When M66EN is asserted high then the clock frequency will be 50-MHz, when M66EN is de-asserted the clock frequency will be 25-MHz. The clock control register at offset D8h provides 7 control bits to individually enable or disable each PCI bus clock output (see Section 4.66). The register default is enabled for all 7 outputs.

The PCI bus clock (CLK) input provides the clock to the internal PCI bus core and serial IRQ core. When the internal PCI bus clock source is selected, PCI bus clock output 6 (CLKOUT6) is connected to the PCI bus clock input (CLK). When an external PCI bus clock source is selected, the external clock source is connected to the PCI bus clock input (CLK). For external clock mode, all seven CLKOUT6:0 terminals must be disabled using the clock control register at offset D8h (see Section 4.66).

3.5 PCI Port Arbitration

The internal PCI port arbitration logic supports up to six external PCI bus devices plus the bridge. This bridge supports a classic PCI arbiter.

3.5.1 Classic PCI Arbiter

The classic PCI arbiter is configured through the classic PCI configuration space at offset DCh. Table 3-5 identifies and describes the registers associated with classic PCI arbitration mode.

Table 3-5. Classic PCI Arbiter Registers

PCI OFFSET	REGISTER NAME	DESCRIPTION
Classic PCI configuration register DCh	Arbiter control (see Section 4.69)	Contains a two-tier priority scheme for the bridge and six PCI bus devices. The bridge defaults to the high priority tier. The six PCI bus devices default to the low priority tier. A bus parking control bit (bit 7, PARK) is provided.
Classic PCI configuration register DDh	Arbiter request mask (see Section 4.70)	Six mask bits provide individual control to block each PCI Bus REQ input. Bit 7 (ARB_TIMEOUT) in the arbiter request mask register enables generating timeout status if a PCI device does not respond within 16 PCI bus clocks. Bit 6 (AUTO_MASK) in the arbiter request mask register automatically masks a PCI bus REQ if the device does not respond after GNT is issued. The AUTO_MASK bit is cleared to disable any automatically generated mask.
Classic PCI configuration register DEh	Arbiter time-out status (see Section 4.71)	When bit 7 (ARB_TIMEOUT) in the arbiter request mask register is asserted, timeout status for each PCI bus device is reported in this register.

3.6 Configuration Register Translation

PCI Express configuration register transactions received by the bridge are decoded based on the transaction's destination ID. These configuration transactions can be broken into three subcategories: type 0 transactions, type 1 transactions that target the secondary bus, and type 1 transactions that target a downstream bus other than the secondary bus.

PCI Express type 0 configuration register transactions always target the configuration space and are never passed on to the secondary interface.

Type 1 configuration register transactions that target a device on the secondary bus are converted to type 0 configuration register transactions on the PCI bus. Figure 3-5 shows the address phase of a type 0 configuration transaction on the PCI bus as defined by the PCI specification.

31 16	15 11	10 8	7 2	1	0
IDSEL	**Reserved**	**Function Number**	**Register Number**	**0**	**0**

Figure 3-5. Type 0 Configuration Transaction Address Phase Encoding

In addition, the bridge converts the destination ID device number to one of the AD[31:16] lines as the IDSEL signal. The implemented IDSEL signal mapping is shown in Table 3-6.

Table 3-6. Type 0 Configuration Transaction IDSEL Mapping

DEVICE NUMBER	AD[31:16]
00000	0000 0000 0000 0001
00001	0000 0000 0000 0010
00010	0000 0000 0000 0100
00011	0000 0000 0000 1000
00100	0000 0000 0001 0000
00101	0000 0000 0010 0000
00110	0000 0000 0100 0000
00111	0000 0000 1000 0000
01000	0000 0001 0000 0000
01001	0000 0010 0000 0000
01010	0000 0100 0000 0000
01011	0000 1000 0000 0000
01100	0001 0000 0000 0000
01101	0010 0000 0000 0000
01110	0100 0000 0000 0000
01111	1000 0000 0000 0000
1xxxx	0000 0000 0000 0000

Type 1 configuration registers transactions that target a downstream bus other then the secondary bus are output on the PCI bus as type 1 PCI configuration transactions. Figure 3-6 shows the address phase of a type 1 configuration transaction on the PCI bus as defined by the PCI specification.

31 24	**23 16**	**15 11**	**10 8**	**7 2**	**1**	**0**
Reserved	**Bus Number**	**Device Number**	**Function Number**	**Register Number**	**0**	**1**

Figure 3-6. Type 1 Configuration Transaction Address Phase Encoding

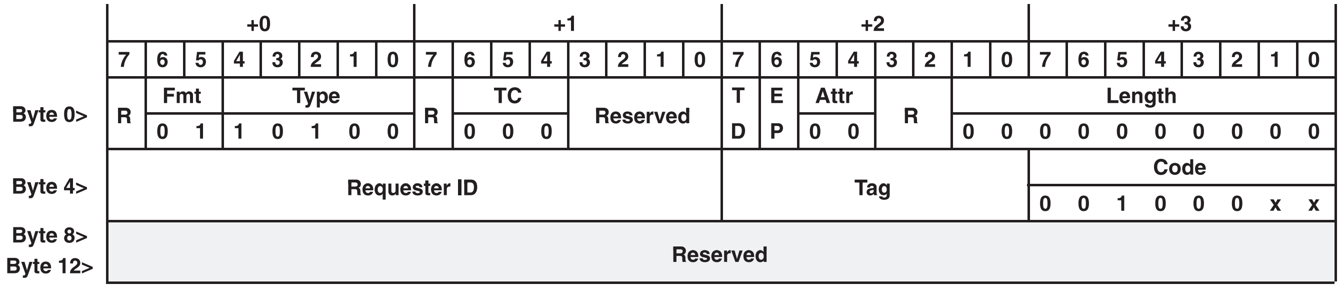
3.7 PCI Interrupt Conversion to PCI Express Messages

The bridge converts interrupts from the PCI bus sideband interrupt signals to PCI Express interrupt messages.

Table 3-7, Figure 3-7, and Figure 3-8 illustrate the format for both the assert and deassert INTx messages.

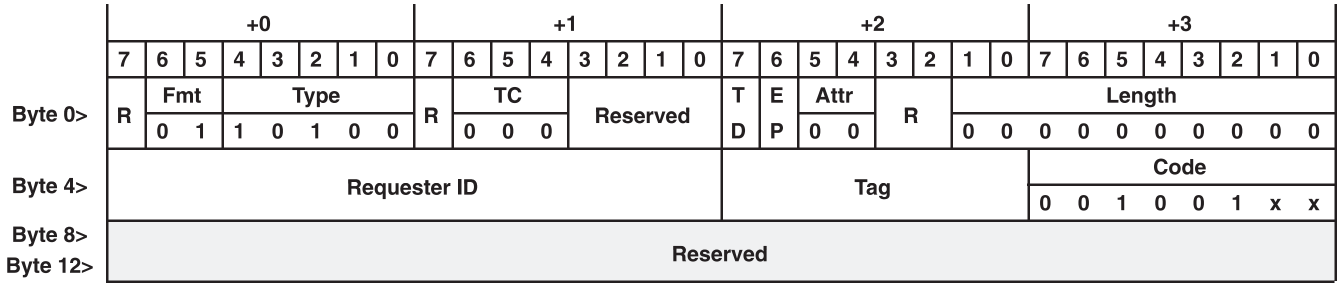
Table 3-7. Interrupt Mapping In The Code Field

INTERRUPT	CODE FIELD
$\overline{\text{INTA}}$	00
$\overline{\text{INTB}}$	01
$\overline{\text{INTC}}$	10
$\overline{\text{INTD}}$	11



	+0 (bits 7–0)	+1 (bits 7–0)	+2 (bits 7–0)	+3 (bits 7–0)
Byte 0>	R; Fmt 0 1; Type 1 0 1 0 0	R; TC 0 0 0; Reserved	TD; EP; Attr 0 0; R	Length 0 0 0 0 0 0 0 0 0 0
Byte 4>	Requester ID		Tag	Code 0 0 1 0 0 0 x x
Byte 8> Byte 12>	Reserved			

Figure 3-7. PCI Express ASSERT_INTX Message



	+0 (bits 7–0)	+1 (bits 7–0)	+2 (bits 7–0)	+3 (bits 7–0)
Byte 0>	R; Fmt 0 1; Type 1 0 1 0 0	R; TC 0 0 0; Reserved	TD; EP; Attr 0 0; R	Length 0 0 0 0 0 0 0 0 0 0
Byte 4>	Requester ID		Tag	Code 0 0 1 0 0 1 x x
Byte 8> Byte 12>	Reserved			

Figure 3-8. PCI Express DEASSERT_INTX Message

3.8 $\overline{\text{PME}}$ Conversion to PCI Express Messages

When the PCI bus $\overline{\text{PME}}$ input transitions low, the bridge generates and sends a PCI Express PME message upstream. The requester ID portion of the PME message uses the stored value in the secondary bus number register as the bus number, 0 as the device number, and 0 as the function number. The Tag field for each PME message is 00h. A $\overline{\text{PME}}$ message is sent periodically until the $\overline{\text{PME}}$ signal transitions high.

Figure 3-9 illustrates the format for a PCI Express PME message.

<table>
<tr><th></th><th colspan="8">+0</th><th colspan="8">+1</th><th colspan="8">+2</th><th colspan="8">+3</th></tr>
<tr><td></td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td rowspan="2">Byte 0></td><td rowspan="2">R</td><td colspan="2">Fmt</td><td colspan="5">Type</td><td rowspan="2">R</td><td colspan="3">TC</td><td colspan="4" rowspan="2">Reserved</td><td>T</td><td>E</td><td colspan="2">Attr</td><td colspan="2" rowspan="2">R</td><td colspan="10">Length</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D</td><td>P</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="2">Byte 4></td><td colspan="16" rowspan="2">Requester ID</td><td colspan="8" rowspan="2">Tag</td><td colspan="8">Code</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Byte 8>
Byte 12></td><td colspan="32">Reserved</td></tr>
</table>

Figure 3-9. PCI Express PME Message

3.9 PCI Express to PCI Bus Lock Conversion

The bus-locking protocol defined in the *PCI Express Base Specification* and *PCI Local Bus Specification* is provided on the bridge as an additional compatibility feature. The PCI bus LOCK signal is a dedicated output that is enabled by setting bit 12 in the general control register at offset D4h. See Section 4.65, *General Control Register*, for details.

NOTE

The use of LOCK is only supported by PCI-Express to PCI Bridges in the downstream direction (away from the root complex).

PCI Express locked-memory read request transactions are treated the same as PCI Express memory read transactions except that the bridge returns a completion for a locked-memory read. Also, the bridge uses the PCI LOCK protocol when initiating the memory read transaction on the PCI bus.

When a PCI Express locked-memory read request transaction is received and the bridge is not already locked, the bridge arbitrates for use of the LOCK terminal by asserting REQ. If the bridge receives GNT and the LOCK terminal is high, then the bridge drives the LOCK terminal low after the address phase of the first locked-memory read transaction to take ownership of LOCK. The bridge continues to assert LOCK except during the address phase of locked transactions. If the bridge receives GNT and the LOCK terminal is low, then the bridge deasserts its REQ and waits until LOCK is high and the bus is idle before re-arbitrating for the use of LOCK.

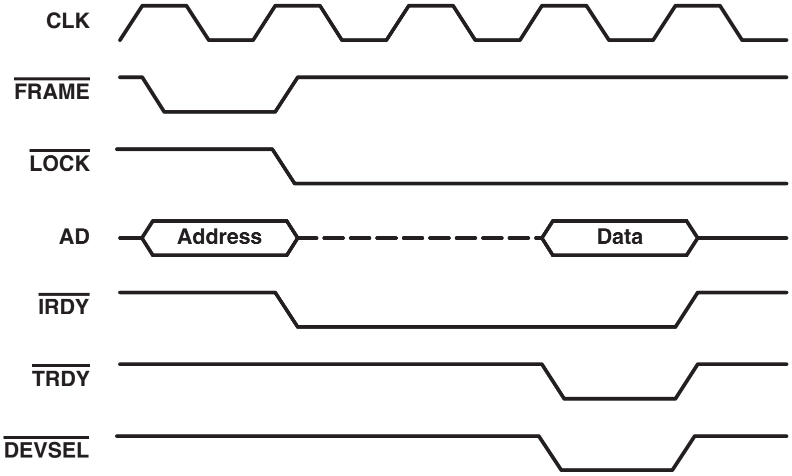


Figure 3-10. Starting a Locked Sequence

Once the bridge has ownership of LOCK, the bridge initiates the lock read as a memory read transaction on the PCI bus. When the target of the locked-memory read returns data, the bridge is considered locked and all transactions not associated with the locked sequence are blocked by the bridge.

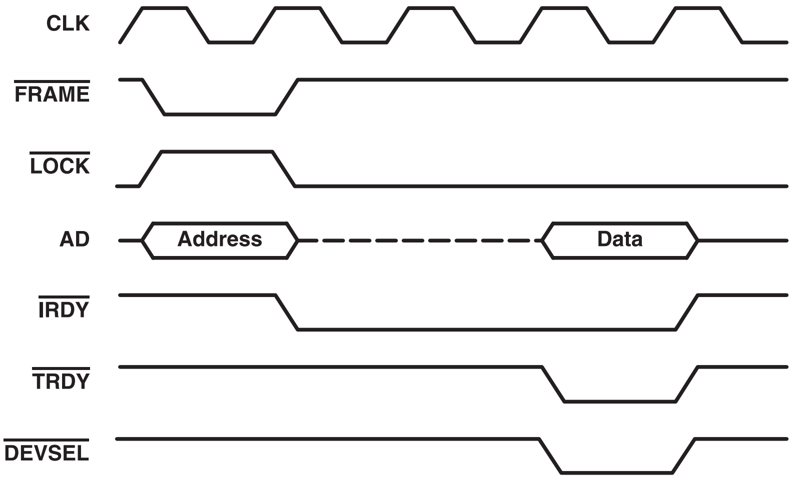


Figure 3-11. Continuing a Locked Sequence

Because PCI Express does not have a unique locked-memory write request packet, all PCI Express memory write requests that are received while the bridge is locked are considered part of the locked sequence and are transmitted to PCI as locked-memory write transactions.

The bridge terminates the locked sequence when an unlock message is received from PCI Express and all previous locked transactions have been completed.

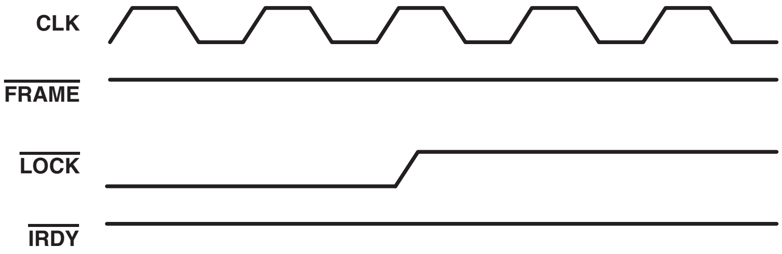


Figure 3-12. Terminating a Locked Sequence

In the erroneous case that a normal downstream memory read request is received during a locked sequence, the bridge responds with an unsupported request completion status. Note that this condition must never occur, because the *PCI Express Specification* requires the root complex to block normal memory read requests at the source. All locked sequences that end successfully or with an error condition must be immediately followed by an unlock message. This unlock message is required to return the bridge to a known unlocked state.

3.10 Two-Wire Serial-Bus Interface

The bridge provides a two-wire serial-bus interface to load subsystem identification information and specific register defaults from an external EEPROM. The serial-bus interface signals (SDA and SCL) are shared with two of the GPIO terminals (3 and 4). If the serial bus interface is enabled, then the GPIO3 and GPIO4 terminals are disabled. If the serial bus interface is disabled, then the GPIO terminals operate as described in Section 3.13.

3.10.1 Serial-Bus Interface Implementation

To enable the serial-bus interface, a pullup resistor must be implemented on the SCL signal. At the rising edge of $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$, whichever occurs later in time, the SCL terminal is checked for a pullup resistor. If one is detected, then bit 3 (SBDETECT) in the serial-bus control and status register (see Section 4.58) is set. Software may disable the serial-bus interface at any time by writing a 0b to the SBDETECT bit. If no external EEPROM is required, then the serial-bus interface is permanently disabled by attaching a pulldown resistor to the SCL signal.

The bridge implements a two-terminal serial interface with one clock signal (SCL) and one data signal (SDA). The SCL signal is a unidirectional output from the bridge and the SDA signal is bidirectional. Both are open-drain signals and require pullup resistors. The bridge is a bus master device and drives SCL at approximately 60 kHz during data transfers and places SCL in a high-impedance state (0 frequency) during bus idle states. The serial EEPROM is a bus slave device and must acknowledge a slave address equal to A0h. Figure 3-13 illustrates an example application implementing the two-wire serial bus.

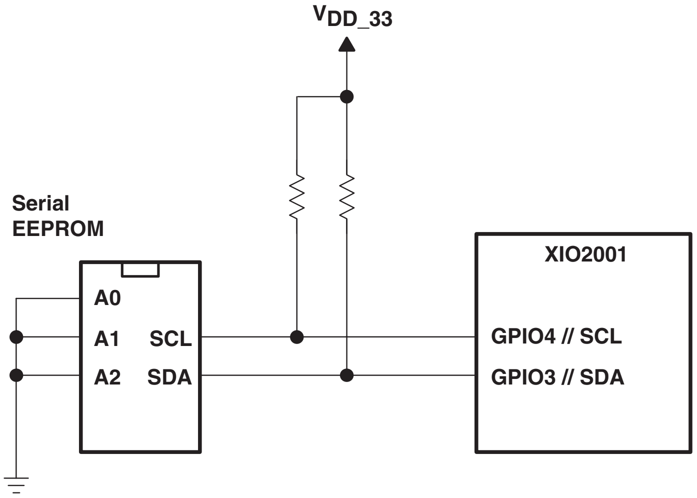


Figure 3-13. Serial EEPROM Application

3.10.2 Serial-Bus Interface Protocol

All data transfers are initiated by the serial-bus master. The beginning of a data transfer is indicated by a start condition, which is signaled when the SDA line transitions to the low state while SCL is in the high state, as illustrated in Figure 3-14. The end of a requested data transfer is indicated by a stop condition, which is signaled by a low-to-high transition of SDA while SCL is in the high state, as shown in Figure 3-14. Data on SDA must remain stable during the high state of the SCL signal, as changes on the SDA signal during the high state of SCL are interpreted as control signals, that is, a start or stop condition.

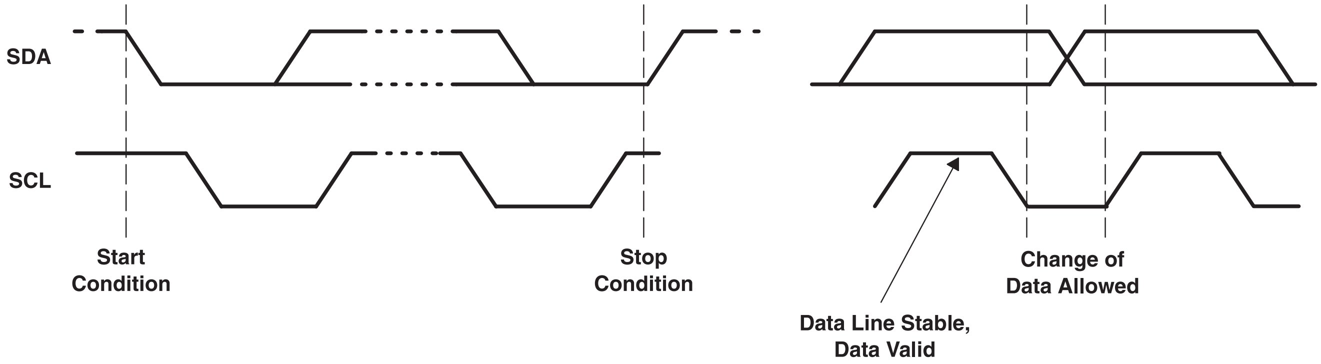


Figure 3-14. Serial-Bus Start/Stop Conditions and Bit Transfers

Data is transferred serially in 8-bit bytes. During a data transfer operation, the exact number of bytes that are transmitted is unlimited. However, each byte must be followed by an acknowledge bit to continue the data transfer operation. An acknowledge (ACK) is indicated by the data byte receiver pulling the SDA signal low, so that it remains low during the high state of the SCL signal. Figure 3-15 illustrates the acknowledge protocol.

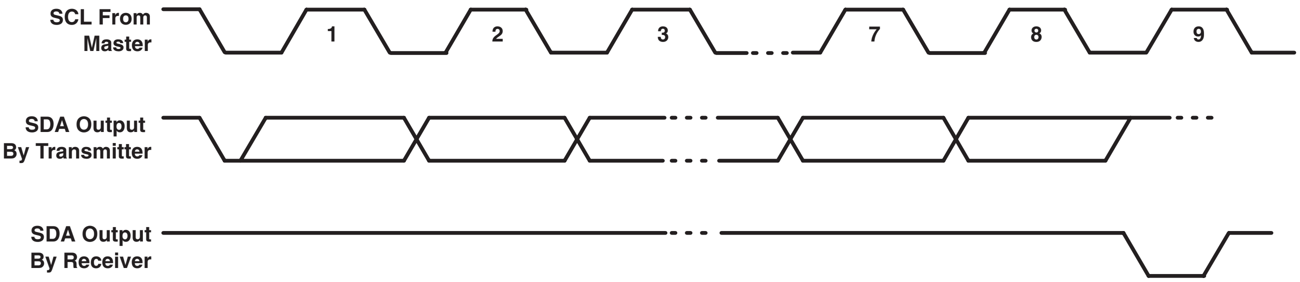
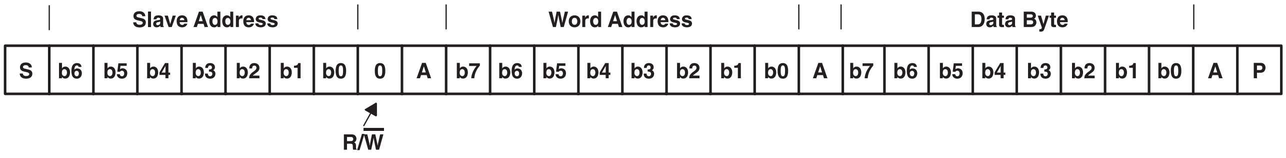


Figure 3-15. Serial-Bus Protocol Acknowledge

The bridge performs three basic serial-bus operations: single byte reads, single byte writes, and multibyte reads. The single byte operations occur under software control. The multibyte read operations are performed by the serial EEPROM initialization circuitry immediately after a PCI Express reset. See Section 3.10.3, *Serial-Bus EEPROM Application*, for details on how the bridge automatically loads the subsystem identification and other register defaults from the serial-bus EEPROM.

Figure 3-16 illustrates a single byte write. The bridge issues a start condition and sends the 7-bit slave device address and the R/W command bit is equal to 0b. A 0b in the R/W command bit indicates that the data transfer is a write. The slave device acknowledges if it recognizes the slave address. If no acknowledgment is received by the bridge, then bit 1 (SB_ERR) is set in the serial-bus control and status register (PCI offset B3h, see Section 4.58). Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then the bridge delivers the data byte MSB first and expects a final acknowledgment before issuing the stop condition.



	Slave Address									Word Address									Data Byte								
S	b6	b5	b4	b3	b2	b1	b0	0	A	b7	b6	b5	b4	b3	b2	b1	b0	A	b7	b6	b5	b4	b3	b2	b1	b0	A	P

R/$\overline{W}$

A = Slave Acknowledgement S/P = Start/Stop Condition

Figure 3-16. Serial-Bus Protocol – Byte Write

Figure 3-17 illustrates a single byte read. The bridge issues a start condition and sends the 7-bit slave device address and the R/$\overline{W}$ command bit is equal to 0b (write). The slave device acknowledges if it recognizes the slave address. Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then, the bridge issues a restart condition followed by the 7-bit slave address and the R/$\overline{W}$ command bit is equal to 1b (read). Once again, the slave device responds with an acknowledge. Next, the slave device sends the 8-bit data byte, MSB first. Since this is a 1-byte read, the bridge responds with no acknowledge (logic high) indicating the last data byte. Finally, the bridge issues a stop condition.

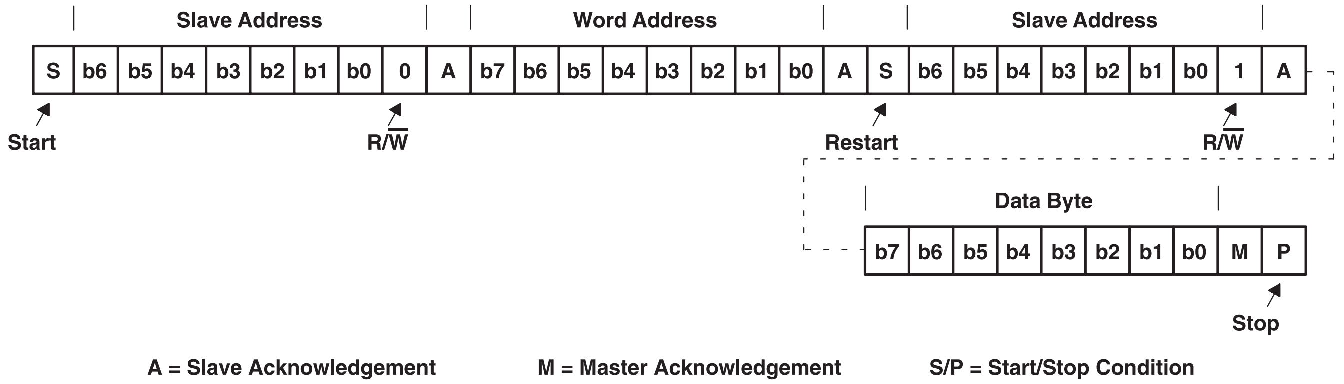


Figure 3-17. Serial-Bus Protocol – Byte Read

Figure 3-18 illustrates the serial interface protocol during a multi-byte serial EEPROM download. The serial-bus protocol starts exactly the same as a 1-byte read. The only difference is that multiple data bytes are transferred. The number of transferred data bytes is controlled by the bridge master. After each data byte, the bridge master issues acknowledge (logic low) if more data bytes are requested. The transfer ends after a bridge master no acknowledge (logic high) followed by a stop condition.

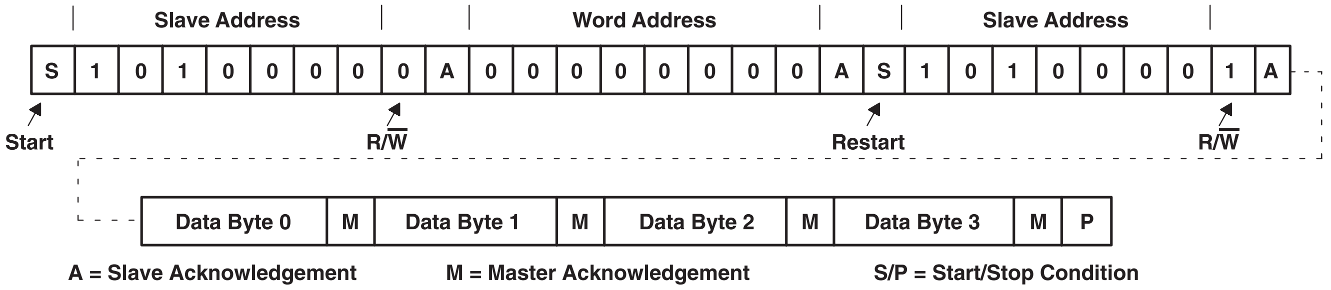


Figure 3-18. Serial-Bus Protocol – Multibyte Read

Bit 7 (PROT_SEL) in the serial-bus control and status register changes the serial-bus protocol. Each of the three previous serial-bus protocol figures illustrates the PROT_SEL bit default (logic low). When this control bit is asserted, the word address and corresponding acknowledge are removed from the serial-bus protocol. This feature allows the system designer a second serial-bus protocol option when selecting external EEPROM devices.

3.10.3 Serial-Bus EEPROM Application

The registers and corresponding bits that are loaded through the EEPROM are provided in Table 3-8.

Table 3-8. EEPROM Register Loading Map

SERIAL EEPROM WORD ADDRESS	BYTE DESCRIPTION
00h	PCI-Express to PCI bridge function indicator (00h)
01h	Number of bytes to download (25h)
02h	PCI 44h, subsystem vendor ID, byte 0
03h	PCI 45h, subsystem vendor ID, byte 1
04h	PCI 46h, subsystem ID, byte 0s
05h	PCI 47h, subsystem ID, byte 1s
06h	PCI D4h, general control, byte 0

Table 3-8. EEPROM Register Loading Map (continued)

SERIAL EEPROM WORD ADDRESS	BYTE DESCRIPTION
07h	PCI D5h, general control, byte 1
08h	PCI D6h, general control, byte 2
09h	PCI D7h, general control, byte 3
0Ah	PCI D8h, clock control
0Bh	PCI D9h, clock mask
0Ch	Reserved—no bits loaded
0Dh	PCI DCh, arbiter control
0Eh	PCI DDh, arbiter request mask
0Fh	PCI C0h, control and diagnostic register, byte 0
10h	PCI C1h, control and diagnostic register, byte 1
11h	PCI C2h, control and diagnostic register, byte 2
12h	PCI C3h, control and diagnostic register, byte 3
13h	PCI C4h, control and diagnostic register, byte 0
14h	PCI C5h, control and diagnostic register, byte 1
15h	PCI C6h, control and diagnostic register, byte 2
15h	PCI C6h, control and diagnostic register, byte 2
16h	PCI C7h, control and diagnostic register, byte 3
17h	PCI C8h, control and diagnostic register, byte 0
18h	PCI C9h, control and diagnostic register, byte 1
19h	PCI CAh, control and diagnostic register, byte 2
1Ah	PCI CBh, control and diagnostic register, byte 3
1Bh	Reserved—no bits loaded
1Ch	Reserved—no bits loaded
1Dh	PCI E0h, serial IRQ mode control
1Eh	PCI E2h, serial IRQ edge control, byte 0
1Fh	PCI E3h, serial IRQ edge control, byte 1
20h	PCI E8h, PFA_REQ_LENGTH_LIMIT
21h	PCI E9h, PFA_REQ_CNT_LIMIT
22h	PCI EAh, CACHE_TMR_XFR_LIMIT
23h	PCI ECh, CACHE_TIMER_LOWER_LIMIT, Byte 0
24h	PCI EDh, CACHE_TIMER_LOWER_LIMIT, Byte 1
25h	PCI EEh, CACHE_TIMER_UPPER_LIMIT, Byte 0
26h	PCI EFh, CACHE_TIMER_UPPER_LIMIT, Byte 1
27h	End-of-list indicator (80h)

This format must be explicitly followed for the bridge to correctly load initialization values from a serial EEPROM. All byte locations must be considered when programming the EEPROM.

The serial EEPROM is addressed by the bridge at slave address 1010 000b. This slave address is internally hardwired and cannot be changed by the system designer. Therefore, all three hardware address bits for the EEPROM are tied to V_{SS} to achieve this address. The serial EEPROM in the sample application circuit (Figure 3-13) assumes the 1010b high-address nibble. The lower three address bits are terminal inputs to the chip, and the sample application shows these terminal inputs tied to V_{SS}.

During an EEPROM download operation, bit 4 (ROMBUSY) in the serial-bus control and status register is asserted. After the download is finished, bit 0 (ROM_ERR) in the serial-bus control and status register may be monitored to verify a successful download.

3.10.4 Accessing Serial-Bus Devices Through Software

The bridge provides a programming mechanism to control serial-bus devices through system software. The programming is accomplished through a doubleword of PCI configuration space at offset B0h. Table 3-9 lists the registers that program a serial-bus device through software.

Table 3-9. Registers Used To Program Serial-Bus Devices

PCI OFFSET	REGISTER NAME	DESCRIPTION
B0h	Serial-bus data (see Section 4.55)	Contains the data byte to send on write commands or the received data byte on read commands.
B1h	Serial-bus word address (see Section 4.56)	The content of this register is sent as the word address on byte writes or reads. This register is not used in the quick command protocol. Bit 7 (PROT_SEL) in the serial-bus control and status register (offset B3h, see Section 4.58) is set to 1b to enable the slave address to be sent.
B2h	Serial-bus slave address (see Section 4.57)	Write transactions to this register initiate a serial-bus transaction. The slave device address and the R/$\overline{W}$ command selector are programmed through this register.
B3h	Serial-bus control and status (see Section 4.58)	Serial interface enable, busy, and error status are communicated through this register. In addition, the protocol-select bit (PROT_SEL) and serial-bus test bit (SBTEST) are programmed through this register.

To access the serial EEPROM through the software interface, the following steps are performed:

1. The control and status byte is read to verify the EEPROM interface is enabled (SBDETECT asserted) and not busy (REQBUSY and ROMBUSY deasserted).
2. The serial-bus word address is loaded. If the access is a write, then the data byte is also loaded.
3. The serial-bus slave address and R/W command selector byte is written.
4. REQBUSY is monitored until this bit is deasserted.
5. SB_ERR is checked to verify that the serial-bus operation completed without error. If the operation is a read, then the serial-bus data byte is now valid.

3.11 Advanced Error Reporting Registers

In the extended PCI Express configuration space, the bridge supports the advanced error reporting capabilities structure. For the PCI Express interface, both correctable and uncorrectable error statuses are provided. For the PCI bus interface, secondary uncorrectable error status is provided. All uncorrectable status bits have corresponding mask and severity control bits. For correctable status bits, only mask bits are provided.

Both the primary and secondary interfaces include first error pointer and header log registers. When the first error is detected, the corresponding bit position within the uncorrectable status register is loaded into the first error pointer register. Likewise, the header information associated with the first failing transaction is loaded into the header log. To reset this first error control logic, the corresponding status bit in the uncorrectable status register is cleared by a writeback of 1b.

For systems that require high data reliability, ECRC is fully supported on the PCI Express interface. The primary side advanced error capabilities and control register has both ECRC generation and checking enable control bits. When the checking bit is asserted, all received TLPs are checked for a valid ECRC field. If the generation bit is asserted, then all transmitted TLPs contain a valid ECRC field.

3.12 Data Error Forwarding Capability

The bridge supports the transfer of data errors in both directions.

If a downstream PCI Express transaction with a data payload is received that targets the internal PCI bus and the EP bit is set indicating poisoned data, then the bridge must ensure that this information is transferred to the PCI bus. To do this, the bridge forces a parity error on each PCI bus data phase by inverting the parity bit calculated for each double-word of data.

If the bridge is the target of a PCI transaction that is forwarded to the PCI Express interface and a data parity error is detected, then this information is passed to the PCI Express interface. To do this, the bridge sets the EP bit in the upstream PCI Express header.

3.13 General-Purpose I/O Interface

Up to five general-purpose input/output (GPIO) terminals are provided for system customization. These GPIO terminals are 3.3-V tolerant.

The exact number of GPIO terminals varies based on implementing the clock run, power override, and serial EEPROM interface features. These features share four of the five GPIO terminals. When any of the three shared functions are enabled, the associated GPIO terminal is disabled.

All five GPIO terminals are individually configurable as either inputs or outputs by writing the corresponding bit in the GPIO control register at offset B4h (See Section 4.59). A GPIO data register at offset B6h exists to either read the logic state of each GPIO input or to set the logic state of each GPIO output. The power-up default state for the GPIO control register is input mode.

3.14 Set Slot Power Limit Functionality

The *PCI Express Specification* provides a method for devices to limit internal functionality and save power based on the value programmed into the captured slot power limit scale (CSPLS) and capture slot power limit value (CSPLV) fields of the PCI Express device capabilities register at offset 74h. See Section 4.49, *Device Capabilities Register*, for details. The bridge writes these fields when a set slot power limit message is received on the PCI Express interface.

After the deassertion of $\overline{\text{PERST}}$, the XIO2001 compares the information within the CSPLS and CSPLV fields of the device capabilities register to the minimum power scale (MIN_POWER_SCALE) and minimum power value (MIN_POWER_VALUE) fields in the general control register at offset D4h. See Section 4.65, *General Control Register*, for details. If the CSPLS and CSPLV fields are less than the MIN_POWER_SCALE and MIN_POWER_VALUE fields, respectively, then the bridge takes the appropriate action that is defined below.

The power usage action is programmable within the bridge. The general control register includes a 3-bit POWER_OVRD field. This field is programmable to the following options:

1. Ignore slot power limit fields.
2. Assert the PWR_OVRD terminal.
3. Disable secondary clocks as specified by the clock mask register at offset D9h (see Section 4.67).
4. Disable secondary clocks as specified by the clock mask register and assert the PWR_OVRD terminal.
5. Respond with unsupported request to all transactions except type 0/1 configuration transactions and set slot power limit messages

3.15 PCI Express and PCI Bus Power Management

The bridge supports both software-directed power management and active state power management through standard PCI configuration space. Software-directed registers are located in the power management capabilities structure located at offset 48h (see Section 4.31). Active state power management control registers are located in the PCI Express capabilities structure located at offset 70h (see Section 4.41).

During software-directed power management state changes, the bridge initiates link state transitions to L1 or L2/L3 after a configuration write transaction places the device in a low power state. The power management state machine is also responsible for gating internal clocks based on the power state. Table 3-10 identifies the relationship between the D-states and bridge clock operation.

Table 3-10. Clocking In Low Power States

CLOCK SOURCE	D0/L0	D1/L1	D2/L1	D3/L2/L3
PCI express reference clock input (REFCLK)	On	On	On	On/Off
Internal PCI bus clock to bridge function	On	Off	Off	Off

The link power management (LPM) state machine manages active state power by monitoring the PCI Express transaction activity. If no transactions are pending and the transmitter has been idle for at least the minimum time required by the *PCI Express Specification*, then the LPM state machine transitions the link to either the L0s or L1 state. By reading the bridge’s L0s and L1 exit latency in the link capabilities register, the system software may make an informed decision relating to system performance versus power savings. The ASLPMC field in the link control register provides an L0s only option, L1 only option, or both L0s and L1 option.

3.16 Auto Pre-Fetch Agent

The auto pre-fetch agent is an internal logic module that will generate speculative read requests on behalf of a PCI master to improve upstream memory read performance.

The auto pre-fetch agent will generate a read thread on the PCI-express bus when it receives an upstream prefetchable memory read request on the PCI bus. A read thread is a sequence of one or more read requests with contiguous read addresses. The first read of thread will be started by a master on the PCI bus requesting a read that is forwarded to the root complex by the bridge. Each subsequent read in the thread will be initiated by the auto pre-fetch agent. Each subsequent read will use the address that immediately follows the last address of data in the previous read of the thread. Each read request in the thread will be assigned to an upstream request processor. The pre-fetch agent can issue reads for two threads at one time, alternating between the threads.

4 Classic PCI Configuration Space

The programming model of the XIO2001 PCI-Express to PCI bridge is compliant to the classic PCI-to-PCI bridge programming model. The PCI configuration map uses the type 1 PCI bridge header.

All bits marked with a are sticky bits and are reset by a global reset ($\overline{\text{GRST}}$) or the internally-generated power-on reset. All bits marked with a ┤ are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-1. Classic PCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		000h
Status		Command		004h
Class code			Revision ID	008h
BIST	Header type	Latency timer	Cache line size	00Ch
Device control base address				010h
Reserved				014h
Secondary latency timer	Subordinate bus number	Secondary bus number	Primary bus number	018h
Secondary status		I/O limit	I/O base	01Ch
Memory limit		Memory base		020h
Prefetchable memory limit		Prefetchable memory base		024h
Prefetchable base upper 32 bits				028h
Prefetchable limit upper 32 bits				02Ch
I/O limit upper 16 bits		I/O base upper 16 bits		030h
Reserved			Capabilities pointer	034h
Expansion ROM base address				038h
Bridge control		Interrupt pin	Interrupt line	03Ch
Reserved		Next item pointer	SSID/SSVID CAP ID	040h
Subsystem ID (1)		Subsystem vendor ID (1)		044h
Power management capabilities		Next item pointer	PM CAP ID	048h
PM Data	PMCSR_BSE	Power management CSR		04Ch
MSI message control		Next item pointer	MSI CAP ID	050h
MSI message address				054h
MSI upper message address				058h
Reserved		MSI message data		05Ch
MSI Mask Bits Register				060h
MSI Pending Bits Register				064h
Reserved				068h–06Ch
PCI Express capabilities register		Next item pointer	PCI Express capability ID	070h
Device Capabilities				074h
Device status		Device control		078h
Link Capabilities				07Ch
Link status		Link control		080h
Slot Capabilities				084h
Slot Status		Slot Control		088h
Root Capabilities		Root Control		08Ch
Root Status				090h
Device Capabilities 2				094h

(1) One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.
Registers highlighted in gray are reserved or not implemented.

Table 4-1. Classic PCI Configuration Register Map (continued)

<table>
<tr><th colspan="4">REGISTER NAME</th><th>OFFSET</th></tr>
<tr><td colspan="2">Device Status 2</td><td colspan="2">Device Control 2</td><td>098h</td></tr>
<tr><td colspan="4">Link Capabilities 2</td><td>09Ch</td></tr>
<tr><td colspan="2">Link Status 2</td><td colspan="2">Link Control 2</td><td>0A0h</td></tr>
<tr><td colspan="4">Slot Capabilities 2</td><td>0A4h</td></tr>
<tr><td colspan="2">Slot Status 2</td><td colspan="2">Slot Control 2</td><td>0A8h</td></tr>
<tr><td colspan="4">Reserved</td><td>0ACh</td></tr>
<tr><td>Serial-bus control and status (1)</td><td>Serial-bus slave address (1)</td><td>Serial-bus word address (1)</td><td>Serial-bus data (1)</td><td>0B0h</td></tr>
<tr><td colspan="2">GPIO data (1)</td><td colspan="2">GPIO control (1)</td><td>0B4h</td></tr>
<tr><td colspan="4">Reserved</td><td>0B8h–0BCh</td></tr>
<tr><td colspan="4">TL Control and diagnostic register 0 (1)</td><td>0C0h</td></tr>
<tr><td colspan="4">DLL Control and diagnostic register 1 (1)</td><td>0C4h</td></tr>
<tr><td colspan="4">PHY Control and diagnostic register 2 (1)</td><td>0C8h</td></tr>
<tr><td colspan="4">Reserved</td><td>0CCh</td></tr>
<tr><td colspan="4">Subsystem access (1)</td><td>0D0h</td></tr>
<tr><td colspan="4">General control (1)</td><td>0D4h</td></tr>
<tr><td>Reserved</td><td>Clock run status (1)</td><td>Clock mask</td><td>Clock control</td><td>0D8h</td></tr>
<tr><td>Reserved</td><td>Arbiter time-out status</td><td>Arbiter request mask (1)</td><td>Arbiter control (1)</td><td>0DCh</td></tr>
<tr><td colspan="2">Serial IRQ edge control (1)</td><td>Reserved</td><td>Serial IRQ mode control (1)</td><td>0E0h</td></tr>
<tr><td colspan="2">Reserved</td><td colspan="2">Serial IRQ status</td><td>0E4h</td></tr>
<tr><td colspan="2">Cache Timer Transfer Limit</td><td colspan="2">PFA Request Limit</td><td>0E8h</td></tr>
<tr><td colspan="2">Cache Timer Upper Limit</td><td colspan="2">Cache Timer Lower Limit</td><td>0ECh</td></tr>
<tr><td colspan="4">Reserved</td><td>0F0h–0FCh</td></tr>
</table>

4.1 Vendor ID Register

This 16-bit read-only register contains the value 104Ch, which is the vendor ID assigned to Texas Instruments.

PCI register offset:	00h
Register type:	Read-only
Default value:	104Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

4.2 Device ID Register

This 16-bit read-only register contains the value 8231h, which is the device ID assigned by TI for the bridge.

PCI register offset:	02h
Register type:	Read-only
Default value:	8240h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0

4.3 Command Register

The command register controls how the bridge behaves on the PCI Express interface. See Table 4-2 for a complete description of the register contents.

PCI register offset:	04h
Register type:	Read-only, Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-2. Command Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	RSVD	R	Reserved. Returns 00000b when read.
10	INT_DISABLE	R	INTx disable. This bit enables device specific interrupts. Since the bridge does not generate any internal interrupts, this bit is read-only 0b.
9	FBB_ENB	R	Fast back-to-back enable. The bridge does not generate fast back-to-back transactions; therefore, this bit returns 0b when read.
8	SERR_ENB	RW	SERR enable bit. When this bit is set, the bridge can signal fatal and nonfatal errors on the PCI Express interface on behalf of SERR assertions detected on the PCI bus. 0 = Disable the reporting of nonfatal errors and fatal errors (default) 1 = Enable the reporting of nonfatal errors and fatal errors
7	STEP_ENB	R	Address/data stepping control. The bridge does not support address/data stepping, and this bit is hardwired to 0b.
6	PERR_ENB	RW	Controls the setting of bit 8 (DATAPAR) in the status register (offset 06h, see Section 4.4) in response to a received poisoned TLP from PCI Express. A received poisoned TLP is forwarded with bad parity to conventional PCI regardless of the setting of this bit. 0 = Disables the setting of the master data parity error bit (default) 1 = Enables the setting of the master data parity error bit
5	VGA_ENB	R	VGA palette snoop enable. The bridge does not support VGA palette snooping; therefore, this bit returns 0b when read.
4	MWI_ENB	RW	Memory write and invalidate enable. When this bit is set, the bridge translates PCI Express memory write requests into memory write and invalidate transactions on the PCI interface. 0 = Disable the promotion to memory write and invalidate (default) 1 = Enable the promotion to memory write and invalidate
3	SPECIAL	R	Special cycle enable. The bridge does not respond to special cycle transactions; therefore, this bit returns 0b when read.
2	MASTER_ENB	RW	Bus master enable. When this bit is set, the bridge is enabled to initiate transactions on the PCI Express interface. 0 = PCI Express interface cannot initiate transactions. The bridge must disable the response to memory and I/O transactions on the PCI interface (default). 1 = PCI Express interface can initiate transactions. The bridge can forward memory and I/O transactions from PCI secondary interface to the PCI Express interface.
1	MEMORY_ENB	RW	Memory space enable. Setting this bit enables the bridge to respond to memory transactions on the PCI Express interface. 0 = PCI Express receiver cannot process downstream memory transactions and must respond with an unsupported request (default) 1 = PCI Express receiver can process downstream memory transactions. The bridge can forward memory transactions to the PCI interface.
0	IO_ENB	RW	I/O space enable. Setting this bit enables the bridge to respond to I/O transactions on the PCI Express interface. 0 = PCI Express receiver cannot process downstream I/O transactions and must respond with an unsupported request (default) 1 = PCI Express receiver can process downstream I/O transactions. The bridge can forward I/O transactions to the PCI interface.

4.4 Status Register

The status register provides information about the PCI Express interface to the system. See Table 4-3 for a complete description of the register contents.

PCI register offset:	06h
Register type:	Read-only, Read/Clear
Default value:	0010h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 4-3. Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit is set when the PCI Express interface receives a poisoned TLP. This bit is set regardless of the state of bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.3). 0 = No parity error detected 1 = Parity error detected
14	SYS_ERR	RCU	Signaled system error. This bit is set when the bridge sends an ERR_FATAL or ERR_NONFATAL message and bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.3) is set. 0 = No error signaled 1 = ERR_FATAL or ERR_NONFATAL signaled
13	MABORT	RCU	Received master abort. This bit is set when the PCI Express interface of the bridge receives a completion-with-unsupported-request status. 0 = Unsupported request not received on the PCI Express interface 1 = Unsupported request received on the PCI Express interface
12	TABORT_REC	RCUT	Received target abort. This bit is set when the PCI Express interface of the bridge receives a completion-with-completer-abort status. 0 = Completer abort not received on the PCI Express interface 1 = Completer abort received on the PCI Express interface
11	TABORT_SIG	RCUT	Signaled target abort. This bit is set when the PCI Express interface completes a request with completer abort status. 0 = Completer abort not signaled on the PCI Express interface 1 = Completer abort signaled on the PCI Express interface
10:9	PCI_SPEED	R	DEVSEL timing. These bits are read-only 00b, because they do not apply to PCI Express.
8	DATAPAR	RCU	Master data parity error. This bit is set if bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.3) is set and the bridge receives a completion with data marked as poisoned on the PCI Express interface or poisons a write request received on the PCI Express interface. 0 = No uncorrectable data error detected on the primary interface 1 = Uncorrectable data error detected on the primary interface
7	FBB_CAP	R	Fast back-to-back capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b.
6	RSVD	R	Reserved. Returns 0b when read.
5	66MHZ	R	66-MHz capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b.
4	CAPLIST	R	Capabilities list. This bit returns 1b when read, indicating that the bridge supports additional PCI capabilities.
3	INT_STATUS	R	Interrupt status. This bit reflects the interrupt status of the function. This bit is read-only 0b since the bridge does not generate any interrupts internally.
2:0	RSVD	R	Reserved. Returns 000b when read.

4.5 Class Code and Revision ID Register

This read-only register categorizes the base class, subclass, and programming interface of the bridge. The base class is 06h, identifying the device as a bridge. The subclass is 04h, identifying the function as a PCI-to-PCI bridge, and the programming interface is 00h. Furthermore, the TI device revision is indicated in the lower byte (03h). See Table 4-4 for a complete description of the register contents.

PCI register offset:	08h
Register type:	Read-only
Default value:	0604 0000

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-4. Class Code and Revision ID Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	BASECLASS	R	Base class. This field returns 06h when read, which classifies the function as a bridge device.
23:16	SUBCLASS	R	Subclass. This field returns 04h when read, which classifies the function as a PCI-to-PCI bridge.
15:8	PGMIF	R	Programming interface. This field returns 00h when read.
7:0	CHIPREV	R	Silicon revision. This field returns the silicon revision of the function.

4.6 Cache Line Size Register

This register is used to determine when a downstream write is memory write (MW) or memory write invalidate (MWI).

A posted write TLP will normally be sent as a MW on the PCI bus. It will be sent as a MWI when the following conditions are met:

- Cacheline size register has a value that is a power of two (1, 2, 4, 8, 16, 32, 64, or 128)
- The write starts on a cacheline boundary
- The write is one or more cachelines in length
- First and last bytes have all lanes enabled
- Memory write invalidates are enabled

PCI register offset:	0Ch
Register type:	Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.7 Primary Latency Timer Register

This read-only register has no meaningful context for a PCI Express device and returns 00h when read.

PCI register offset: 0Dh
Register type: Read only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.8 Header Type Register

This read-only register indicates that this function has a type one PCI header. Bit 7 of this register is 0b indicating that the bridge is a single-function device.

PCI register offset: 0Eh
Register type: Read only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.9 BIST Register

Since the bridge does not support a built-in self test (BIST), this read-only register returns the value of 00h when read.

PCI register offset: 0Fh
Register type: Read only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.10 Device Control Base Address Register

This register programs the memory base address that accesses the device control registers. By default, this register is read only. If bit 5 of the Control and Diagnostic Register 2 (see Section 4.63) is set, then the bits 31:12 of this register become read/write. See Table 4-5 for a complete description of the register contents.

PCI register offset: 10h
Register type: Read-only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-5. Device Control Base Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:12	ADDRESS	R or RW	Memory Address. The memory address field for XIO2001 uses 20 read/write bits indicating that 4096 bytes of memory space are required. While less than this is actually used, typical systems will allocate this space on a 4K boundary. If the BAR0_EN bit (bit 5 at C8h) is ‘0’, then these bits are read-only and return zeros when read. If the BAR0_EN bit is ‘1’, then these bits are read/write.
11:4	RSVD	R	Reserved. These bits are read-only and return 00h when read.
3	PRE_FETCH	R	Prefetchable. This bit is read-only 0b indicating that this memory window is not prefetchable.
2:1	MEM_TYPE	R	Memory type. This field is read-only 00b indicating that this window can be located anywhere in the 32-bit address space.
0	MEM_IND	R	Memory space indicator. This field returns 0b indicating that memory space is used.

4.11 Primary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI Express interface is connected to.

PCI register offset:	18h
Register type:	Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.12 Secondary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI interface is connected to. The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset:	19h
Register type:	Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.13 Subordinate Bus Number Register

This read/write register specifies the bus number of the highest number PCI bus segment that is downstream of the bridge. The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset:	1Ah
Register type:	Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.14 Secondary Latency Timer Register

This read/write register specifies the secondary bus latency timer for the bridge, in units of PCI clock cycles.

PCI register offset:	1Bh
Register type:	Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.15 I/O Base Register

This read/write register specifies the lower limit of the I/O addresses that the bridge forwards downstream. See Table 4-6 for a complete description of the register contents.

PCI register offset:	1Ch
Register type:	Read-only, Read/Write
Default value:	01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4-6. I/O Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOBASE	RW	I/O base. Defines the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be 000h. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O base upper 16 bits register (offset 30h, see Section 4.24).
3:0	IOTYPE	R	I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing.

4.16 I/O Limit Register

This read/write register specifies the upper limit of the I/O addresses that the bridge forwards downstream. See Table 4-7 for a complete description of the register contents.

PCI register offset:	1Dh
Register type:	Read-only, Read/Write
Default value:	01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4-7. I/O Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOLIMIT	RW	I/O limit. Defines the top address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O limit upper 16 bits register (offset 32h, see Section 4.25).
3:0	IOTYPE	R	I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing.

4.17 Secondary Status Register

The secondary status register provides information about the PCI bus interface. See Table 4-8 for a complete description of the register contents.

PCI register offset:	1Eh
Register type:	Read-only, Read/Clear
Default value:	02X0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0

Table 4-8. Secondary Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit reports the detection of an uncorrectable address, attribute, or data error by the bridge on its internal PCI bus secondary interface. This bit must be set when any of the following three conditions are true: • The bridge detects an uncorrectable address or attribute error as a potential target. • The bridge detects an uncorrectable data error when it is the target of a write transaction. • The bridge detects an uncorrectable data error when it is the master of a read transaction (immediate read data). The bit is set irrespective of the state of bit 0 (PERR_EN) in the bridge control register at offset 3Eh (see Section 4.29). 0 = Uncorrectable address, attribute, or data error not detected on secondary interface 1 = Uncorrectable address, attribute, or data error detected on secondary interface
14	SYS_ERR	RCU	Received system error. This bit is set when the bridge detects an $\overline{\text{SERR}}$ assertion. 0 = No error asserted on the PCI interface 1 = $\overline{\text{SERR}}$ asserted on the PCI interface
13	MABORT	RCU	Received master abort. This bit is set when the PCI interface of the bridge reports the detection of a master abort termination by the bridge when it is the master of a transaction on its secondary interface. 0 = Master abort not received on the PCI interface 1 = Master abort received on the PCI interface
12	TABORT_REC	RCU	Received target abort. This bit is set when the PCI interface of the bridge receives a target abort. 0 = Target abort not received on the PCI interface 1 = Target abort received on the PCI interface
11	TABORT_SIG	RCU	Signaled target abort. This bit reports the signaling of a target abort termination by the bridge when it responds as the target of a transaction on its secondary interface. 0 = Target abort not signaled on the PCI interface 1 = Target abort signaled on the PCI interface
10:9	PCI_SPEED	R	DEVSEL timing. These bits are 01b indicating that this is a medium speed decoding device.
8	DATAPAR	RCU	Master data parity error. This bit is set if the bridge is the bus master of the transaction on the PCI bus, bit 0 (PERR_EN) in the bridge control register (offset 3Eh see Section 4.29) is set, and the bridge either asserts $\overline{\text{PERR}}$ on a read transaction or detects $\overline{\text{PERR}}$ asserted on a write transaction. 0 = No data parity error detected on the PCI interface 1 = Data parity error detected on the PCI Interface
7	FBB_CAP	R	Fast back-to-back capable. This bit returns a 1b when read indicating that the secondary PCI interface of bridge supports fast back-to-back transactions.
6	RSVD	R	Reserved. Returns 0b when read.
5	66MHZ	R	66-MHz capable. The bridge operates at a PCI bus CLK frequency of 66 MHz; therefore, this bit always returns a 1b.
4:0	RSVD	R	Reserved. Returns 00000b when read.

4.18 Memory Base Register

This read/write register specifies the lower limit of the memory addresses that the bridge forwards downstream. See Table 4-9 for a complete description of the register contents.

PCI register offset:	20h
Register type:	Read-only, Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-9. Memory Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMBASE	RW	Memory base. Defines the lowest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h.
3:0	RSVD	R	Reserved. Returns 0h when read.

4.19 Memory Limit Register

This read/write register specifies the upper limit of the memory addresses that the bridge forwards downstream. See Table 4-10 for a complete description of the register contents.

PCI register offset:	22h
Register type:	Read-only, Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-10. Memory Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMLIMIT	RW	Memory limit. Defines the highest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh.
3:0	RSVD	R	Reserved. Returns 0h when read.

4.20 Prefetchable Memory Base Register

This read/write register specifies the lower limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 4-11 for a complete description of the register contents.

PCI register offset:	24h
Register type:	Read-only, Read/Write
Default value:	0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-11. Prefetchable Memory Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PREBASE	RW	Prefetchable memory base. Defines the lowest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. The prefetchable base upper 32 bits register (offset 28h, see Section 4.22) specifies the bit [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	R	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.21 Prefetchable Memory Limit Register

This read/write register specifies the upper limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 4-12 for a complete description of the register contents.

PCI register offset:	26h
Register type:	Read-only, Read/Write
Default value:	0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-12. Prefetchable Memory Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PRELIMIT	RW	Prefetchable memory limit. Defines the highest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The prefetchable limit upper 32 bits register (offset 2Ch, see Section 4.23) specifies the bit [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	R	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.22 Prefetchable Base Upper 32-Bit Register

This read/write register specifies the upper 32 bits of the prefetchable memory base register. See Table 4-13 for a complete description of the register contents.

PCI register offset:	28h
Register type:	Read/Write
Default value:	0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-13. Prefetchable Base Upper 32-Bit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PREBASE	RW	Prefetchable memory base upper 32 bits. Defines the upper 32 bits of the lowest address of the prefetchable memory address range that determines when to forward memory transactions downstream.

4.23 Prefetchable Limit Upper 32-Bit Register

This read/write register specifies the upper 32 bits of the prefetchable memory limit register. See Table 4-14 for a complete description of the register contents.

PCI register offset:	2Ch
Register type:	Read/Write
Default value:	0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-14. Prefetchable Limit Upper 32-Bit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PRELIMIT	RW	Prefetchable memory limit upper 32 bits. Defines the upper 32 bits of the highest address of the prefetchable memory address range that determines when to forward memory transactions downstream.

4.24 I/O Base Upper 16-Bit Register

This read/write register specifies the upper 16 bits of the I/O base register. See Table 4-15 for a complete description of the register contents.

PCI register offset:	30h
Register type:	Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-15. I/O Base Upper 16-Bit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOBASE	RW	I/O base upper 16 bits. Defines the upper 16 bits of the lowest address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be 00000h.

4.25 I/O Limit Upper 16-Bit Register

This read/write register specifies the upper 16 bits of the I/O limit register. See Table 4-16 for a complete description of the register contents.

PCI register offset:	32h
Register type:	Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-16. I/O Limit Upper 16-Bit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOLIMIT	RW	I/O limit upper 16 bits. Defines the upper 16 bits of the top address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be FFFFFh.

4.26 Capabilities Pointer Register

This read-only register provides a pointer into the PCI configuration header where the PCI power management block resides. Since the PCI power management registers begin at 40h, this register is hardwired to 40h.

PCI register offset:	34h
Register type:	Read-only
Default value:	40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

4.27 Interrupt Line Register

This read/write register is programmed by the system and indicates to the software which interrupt line the bridge has assigned to it. The default value of this register is FFh, indicating that an interrupt line has not yet been assigned to the function. Since the bridge does not generate interrupts internally, this register is a scratch pad register.

PCI register offset:	3Ch
Register type:	Read/Write
Default value:	FFh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1

4.28 Interrupt Pin Register

The interrupt pin register is read-only 00h indicating that the bridge does not generate internal interrupts. While the bridge does not generate internal interrupts, it does forward interrupts from the secondary interface to the primary interface.

PCI register offset:	3Dh
Register type:	Read-only
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.29 Bridge Control Register

The bridge control register provides extensions to the command register that are specific to a bridge. See Table 4-17 for a complete description of the register contents.

PCI register offset:	3Eh
Register type:	Read-only, Read/Write, Read/Clear
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-17. Bridge Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11	DTSERR	RW	Discard timer $\overline{\text{SERR}}$ enable. Applies only in conventional PCI mode. This bit enables the bridge to generate either an ERR_NONFATAL (by default) or ERR_FATAL transaction on the primary interface when the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridge. The severity is selectable only if advanced error reporting is supported. 0 = Do not generate ERR_NONFATAL or ERR_FATAL on the primary interface as a result of the expiration of the secondary discard timer. Note that an error message can still be sent if advanced error reporting is supported and bit 10 (DISCARD_TIMER_MASK) in the secondary uncorrectable error mask register (offset 130h, see Section 5.11) is clear (default). 1 = Generate ERR_NONFATAL or ERR_FATAL on the primary interface if the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridges.
10	DTSTATUS	RCU	Discard timer status. This bit indicates if a discard timer expires and a delayed transaction is discarded. 0 = No discard timer error 1 = Discard timer error
9	SEC_DT	RW	Selects the number of PCI clocks that the bridge waits for a master on the secondary interface to repeat a delayed transaction request. The counter starts once the delayed completion (the completion of the delayed transaction on the primary interface) has reached the head of the downstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the delayed transaction with the initiating master on the secondary bus). If the master does not repeat the transaction before the counter expires, then the bridge deletes the delayed transaction from its queue and sets the discard timer status bit. 0 = The secondary discard timer counts 2^{15} PCI clock cycles (default) 1 = The secondary discard timer counts 2^{10} PCI clock cycles
8	PRI_DEC	R	Primary discard timer. This bit has no meaning in PCI Express and is hardwired to 0b.
7	FBB_EN	RW	Fast back-to-back enable. This bit allows software to enable fast back-to-back transactions on the secondary PCI interface. 0 = Fast back-to-back transactions are disabled (default) 1 = Secondary interface fast back-to-back transactions are enabled
6	SRST	RW	Secondary bus reset. This bit is set when software wishes to reset all devices downstream of the bridge. Setting this bit causes the $\overline{\text{PRST}}$ signal on the secondary interface to be asserted. 0 = Secondary interface is not in reset state (default) 1 = Secondary interface is in the reset state

Table 4-17. Bridge Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
5	MAM	RW	Master abort mode. This bit controls the behavior of the bridge when it receives a master abort or an unsupported request. 0 = Do not report master aborts. Returns FFFF FFFFh on reads and discard data on writes (default) 1 = Respond with an unsupported request on PCI Express when a master abort is received on PCI. Respond with target abort on PCI when an unsupported request completion on PCI Express is received. This bit also enables error signaling on master abort conditions on posted writes.
4	VGA16	RW	VGA 16-bit decode. This bit enables the bridge to provide full 16-bit decoding for VGA I/O addresses. This bit only has meaning if the VGA enable bit is set. 0 = Ignore address bits [15:10] when decoding VGA I/O addresses (default) 1 = Decode address bits [15:10] when decoding VGA I/O addresses
3	VGA	RW	VGA enable. This bit modifies the response by the bridge to VGA compatible addresses. If this bit is set, then the bridge decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A 0000h to 000B FFFFh • I/O addresses in the first 64 KB of the I/O address space (address bits [31:16] are 0000h) and where address bits [9:0] are in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – address bits [15:10] may possess any value and are not used in the decoding) If this bit is set, then forwarding of VGA addresses is independent of the value of bit 2 (ISA), the I/O address and memory address ranges defined by the I/O base and limit registers, the memory base and limit registers, and the prefetchable memory base and limit registers of the bridge. The forwarding of VGA addresses is qualified by bits 0 (IO_ENB) and 1 (MEMORY_ENB) in the command register (offset 04h, see Section 4.3). 0 = Do not forward VGA compatible memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges (default). 1 = Forward VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the I/O enable and memory enable bits are set) independent of the I/O and memory address ranges and independent of the ISA enable bit.
2	ISA	RW	ISA enable. This bit modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O base and I/O limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, then the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1K block. 0 = Forward downstream all I/O addresses in the address range defined by the I/O base and I/O limit registers (default) 1 = Forward upstream ISA I/O addresses in the address range defined by the I/O base and I/O limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1-KB block)
1	SERR_EN	RW	$\overline{\text{SERR}}$ enable. This bit controls forwarding of system error events from the secondary interface to the primary interface. The bridge forwards system error events when: • This bit is set • Bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.3) is set • $\overline{\text{SERR}}$ is asserted on the secondary interface 0 = Disable the forwarding of system error events (default) 1 = Enable the forwarding of system error events

Table 4-17. Bridge Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
0	PERR_EN	RW	Parity error response enable. Controls the bridge's response to data, uncorrectable address, and attribute errors on the secondary interface. Also, the bridge always forwards data with poisoning, from conventional PCI to PCI Express on an uncorrectable conventional PCI data error, regardless of the setting of this bit. 0 = Ignore uncorrectable address, attribute, and data errors on the secondary interface (default) 1 = Enable uncorrectable address, attribute, and data error detection and reporting on the secondary interface

4.30 Capability ID Register

This read-only register identifies the linked list item as the register for Subsystem ID and Subsystem Vendor ID capabilities. The register returns 0Dh when read.

PCI register offset:	40h
Register type:	Read-only
Default value:	0Dh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	1	1	0	1

4.31 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 48h pointing to the PCI Power Management Capabilities registers.

PCI register offset:	41h
Register type:	Read-only
Default value:	48h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	1	0	0	0

4.32 Subsystem Vendor ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset:	44h
Register type:	Read-only
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.33 Subsystem ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset:	46h
Register type:	Read-only
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.34 Capability ID Register

This read-only register identifies the linked list item as the register for PCI Power Management ID Capabilities. The register returns 01h when read.

PCI register offset:	48h
Register type:	Read-only
Default value:	01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.35 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 50h pointing to the MSI Capabilities registers.

PCI register offset:	49h
Register type:	Read-only
Default value:	50h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	1	0	0	0	0

4.36 Power Management Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI power management. See Table 4-18 for a complete description of the register contents.

PCI register offset:	4Ah
Register type:	Read-only
Default value:	0603h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1

Table 4-18. Power Management Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	PME_SUPPORT	R	$\overline{\text{PME}}$ support. This 5-bit field indicates the power states from which the bridge may assert PME. Because the bridge never generates a $\overline{\text{PME}}$ except on a behalf of a secondary device, this field is read-only and returns 00000b.
10	D2_SUPPORT	R	This bit returns a 1b when read, indicating that the function supports the D2 device power state.
9	D1_SUPPORT	R	This bit returns a 1b when read, indicating that the function supports the D1 device power state.
8:6	AUX_CURRENT	R	3.3 V_{AUX} auxiliary current requirements. This field returns 000b since the bridge does not generate $\overline{\text{PME}}$ from $D3_{cold}$.
5	DSI	R	Device specific initialization. This bit returns 0b when read, indicating that the bridge does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. Returns 0b when read.
3	PME_CLK	R	$\overline{\text{PME}}$ clock. This bit returns 0b indicating that the PCI clock is not needed to generate $\overline{\text{PME}}$.
2:0	PM_VERSION	R	Power management version. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see Section 4.65) is 0b, then this field returns 010b indicating revision 1.1 compatibility. If PCI_PM_VERSION_CTRL is 1b, then this field returns 011b indicating revision 1.2 compatibility.

4.37 Power Management Control/Status Register

This register determines and changes the current power state of the bridge. No internal reset is generated when transitioning from the $D3_{hot}$ state to the D0 state. See Table 4-19 for a complete description of the register contents.

PCI register offset:	4Ch
Register type:	Read-only, Read/Write
Default value:	0008h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 4-19. Power Management Control/Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PME_STAT	R	$\overline{\text{PME}}$ status. This bit is read-only and returns 0b when read.
14:13	DATA_SCALE	R	Data scale. This 2-bit field returns 00b when read since the bridge does not use the data register.
12:9	DATA_SEL	R	Data select. This 4-bit field returns 0h when read since the bridge does not use the data register.
8	PME_EN	RW	$\overline{\text{PME}}$ enable. This bit has no function and acts as scratchpad space. The default value for this bit is 0b.
7:4	RSVD	R	Reserved. Returns 0h when read.
3	NO_SOFT_RESET	R	No soft reset. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see Section 4.65) is 0b, then this bit returns 0b for compatibility with version 1.1 of the *PCI Power Management Specification*. If PCI_PM_VERSION_CTRL is 1b, then this bit returns 1b indicating that no internal reset is generated and the device retains its configuration context when transitioning from the $D3_{hot}$ state to the D0 state.
2	RSVD	R	Reserved. Returns 0b when read.
1:0	PWR_STATE	RW	Power state. This 2-bit field determines the current power state of the function and sets the function into a new power state. This field is encoded as follows: 00 = D0 (default) 01 = D1 10 = D2 11 = $D3_{hot}$

4.38 Power Management Bridge Support Extension Register

This read-only register indicates to host software what the state of the secondary bus will be when the bridge is placed in D3. See Table 4-20 for a complete description of the register contents.

PCI register offset:	4Eh
Register type:	Read-only
Default value:	40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

Table 4-20. PM Bridge Support Extension Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	BPCC	R	Bus power/clock control enable. This bit indicates to the host software if the bus secondary clocks are stopped when the bridge is placed in D3. The state of the BPCC bit is controlled by bit 11 (BPCC_E) in the general control register (offset D4h, see Section 4.65). 0 = The secondary bus clocks are not stopped in D3 1 = The secondary bus clocks are stopped in D3
6	BSTATE	R	B2/B3 support. This bit is read-only 1b indicating that the bus state in D3 is B2.
5:0	RSVD	R	Reserved. Returns 00 0000b when read.

4.39 Power Management Data Register

The read-only register is not applicable to the bridge and returns 00h when read.

PCI register offset:	4Fh
Register type:	Read-only
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.40 MSI Capability ID Register

This read-only register identifies the linked list item as the register for message signaled interrupts capabilities. The register returns 05h when read.

PCI register offset:	50h
Register type:	Read-only
Default value:	05h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	1

4.41 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 70h pointing to the subsystem ID capabilities registers.

PCI register offset:	51h
Register type:	Read-only
Default value:	70h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	1	1	0	0	0	0

4.42 MSI Message Control Register

This register controls the sending of MSI messages. See Table 4-21 for a complete description of the register contents.

PCI register offset:	52h
Register type:	Read-only, Read/Write
Default value:	0088h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0

Table 4-21. MSI Message Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7	64CAP	R	64-bit message capability. This bit is read-only 1b indicating that the bridge supports 64-bit MSI message addressing.
6:4	MM_EN	RW	Multiple message enable. This bit indicates the number of distinct messages that the bridge is allowed to generate. 000 = 1 message (default) 001 = 2 messages 010 = 4 messages 011 = 8 messages 100 = 16 messages 101 = Reserved 110 = Reserved 111 = Reserved
3:1	MM_CAP	R	Multiple message capabilities. This field indicates the number of distinct messages that bridge is capable of generating. This field is read-only 100b indicating that the bridge can signal 1 interrupt for each IRQ supported on the serial IRQ stream up to a maximum of 16 unique interrupts.
0	MSI_EN	RW	MSI enable. This bit enables MSI interrupt signaling. MSI signaling must be enabled by software for the bridge to signal that a serial IRQ has been detected. 0 = MSI signaling is prohibited (default) 1 = MSI signaling is enabled

4.43 MSI Message Lower Address Register

This register contains the lower 32 bits of the address that a MSI message writes to when a serial IRQ is detected. See Table 4-22 for a complete description of the register contents.

PCI register offset:	54h
Register type:	Read-only, Read/Write
Default value:	0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-22. MSI Message Lower Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:2	ADDRESS	RW	System specified message address
1:0	RSVD	R	Reserved. Returns 00b when read.

4.44 MSI Message Upper Address Register

This register contains the upper 32 bits of the address that a MSI message writes to when a serial IRQ is detected. If this register contains 0000 0000h, then 32-bit addressing is used; otherwise, 64-bit addressing is used.

PCI register offset:	58h
Register type:	Read/Write
Default value:	0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.45 MSI Message Data Register

This register contains the data that software programmed the bridge to send when it send a MSI message. See Table 4-23 for a complete description of the register contents.

PCI register offset:	5Ch
Register type:	Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-23. MSI Message Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MSG	RW	System specific message. This field contains the portion of the message that the bridge forwards unmodified.
3:0	MSG_NUM	RW	Message number. This portion of the message field may be modified to contain the message number is multiple messages are enable. The number of bits that are modifiable depends on the number of messages enabled in the message control register. 1 message = No message data bits can be modified (default) 2 messages = Bit 0 can be modified 4 messages = Bits 1:0 can be modified 8 messages = Bits 2:0 can be modified 16 messages = Bits 3:0 can be modified

4.46 PCI Express Capability ID Register

This read-only register identifies the linked list item as the register for subsystem ID and subsystem vendor ID capabilities. The register returns 10h when read.

PCI register offset:	70h
Register type:	Read-only
Default value:	10h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0

4.47 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 00h, indicating no additional capabilities are supported.

PCI register offset:	71h
Register type:	Read-only
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.48 PCI Express Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI Express. See Table 4-24 for a complete description of the register contents.

PCI register offset:	72h
Register type:	Read-only
Default value:	0072h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1

Table 4-24. PCI Express Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:14	RSVD	R	Reserved. Returns 00b when read.
13:9	INT_NUM	R	Interrupt message number. This field is used for MSI support and is implemented as read-only 00000b in the bridge.
8	SLOT	R	Slot implemented. This bit is not valid for the bridge and is read-only 0b.
7:4	DEV_TYPE	R	Device/port type. This read-only field returns 0111b indicating that the device is a PCI Express-to-PCI bridge.
3:0	VERSION	R	Capability version. This field returns 2h indicating revision 2 of the PCI Express capability.

4.49 Device Capabilities Register

The device capabilities register indicates the device specific capabilities of the bridge. See Table 4-25 for a complete description of the register contents.

PCI register offset:	74h
Register type:	Read-only
Default value:	0000 8D82

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	1	1	0	1	1	0	0	0	0	0	1	0

Table 4-25. Device Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:28	RSVD	R	Reserved. Returns 0h when read.
27:26	CSPLS	RU	Captured slot power limit scale. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 9:8 are written to this field. The value in this field specifies the scale used for the slot power limit. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x
25:18	CSPLV	RU	Captured slot power limit value. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 7:0 are written to this field. The value in this field in combination with the slot power limit scale value (bits 27:26) specifies the upper limit of power supplied to the slot. The power limit is calculated by multiplying the value in this field by the value in the slot power limit scale field.
17:16	RSVD	R	Reserved. Return 00b when read.
15	RBER	R	Role based error reporting. This bit is hardwired to 1 indicating that this bridge supports Role Based Error Reporting.
14	PIP	R	Power indicator present. This bit is hardwired to 0b indicating that a power indicator is not implemented.
13	AIP	R	Attention indicator present. This bit is hardwired to 0b indicating that an attention indicator is not implemented.
12	ABP	R	Attention button present. This bit is hardwired to 0b indicating that an attention button is not implemented.
11:9	EP_L1_LAT	RU	Endpoint L1 acceptable latency. This field indicates the maximum acceptable latency for a transition from L1 to L0 state. This field can be programmed by writing to the L1_LATENCY field (bits 15:13) in the general control register (offset D4h, see Section 4.65). The default value for this field is 110b which indicates a range from 32μs to 64μs. This field cannot be programmed to be less than the latency for the PHY to exit the L1 state.
8:6	EP_L0S_LAT	RU	Endpoint L0s acceptable latency. This field indicates the maximum acceptable latency for a transition from L0s to L0 state. This field can be programmed by writing to the L0s_LATENCY field (bits 18:16) in the general control register (offset D4h, see Section 4.65). The default value for this field is 110b which indicates a range from 2μs to 4μs. This field cannot be programmed to be less than the latency for the PHY to exit the L0s state.
5	ETFS	R	Extended tag field supported. This field indicates the size of the tag field not supported.
4:3	PFS	R	Phantom functions supported. This field is read-only 00b indicating that function numbers are not used for phantom functions.
2:0	MPSS	R	Maximum payload size supported. This field indicates the maximum payload size that the device can support for TLPs. This field is encoded as 010b indicating the maximum payload size for a TLP is 512 bytes.

4.50 Device Control Register

The device control register controls PCI Express device specific parameters. See Table 4-26 for a complete description of the register contents.

PCI register offset:	78h
Register type:	Read-only, Read/Write
Default value:	2000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-26. Device Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	CFG_RTRY_ENB	RW	Configuration retry status enable. When this read/write bit is set to 1b, the bridge returns a completion with completion retry status on PCI Express if a configuration transaction forwarded to the secondary interface did not complete within the implementation specific time-out period. When this bit is set to 0b, the bridge does not generate completions with completion retry status on behalf of configuration transactions. The default value of this bit is 0b.
14:12	MRRS	RW	Maximum read request size. This field is programmed by host software to set the maximum size of a read request that the bridge can generate. The bridge uses this field to determine how much data to fetch on a read request. This field is encoded as: 000 = 128B 001 = 256B 010 = 512B (default) 011 = 1024B 100 = 2048B 101 = 4096B 110 = Reserved 111 = Reserved
11	ENS	R	Enable no snoop. This bit is hardwired to 0 since this device never sets the No Snoop attribute in transactions that it initiates.
10	APPE	RW	Auxiliary power PM enable. This bit has no effect in the bridge. 0 = AUX power is disabled (default) 1 = AUX power is enabled
9	PFE	R	Phantom function enable. Since the bridge does not support phantom functions, this bit is read-only 0b.
8	ETFE	R	Extended tag field enable. Since the bridge does not support extended tags, this bit is read-only 0b.
7:5	MPS	RW	Maximum payload size. This field is programmed by host software to set the maximum size of posted writes or read completions that the bridge can initiate. This field is encoded as: 000 = 128B (default) 001 = 256B 010 = 512B 011 = 1024B 100 = 2048B 101 = 4096B 110 = Reserved 111 = Reserved
4	ERO	R	Enable relaxed ordering. Since the bridge does not support relaxed ordering, this bit is read-only 0b.
3	URRE	RW	Unsupported request reporting enable. If this bit is set, then the bridge sends an ERR_NONFATAL message to the root complex when an unsupported request is received. 0 = Do not report unsupported requests to the root complex (default) 1 = Report unsupported requests to the root complex
2	FERE	RW	Fatal error reporting enable. If this bit is set, then the bridge is enabled to send ERR_FATAL messages to the root complex when a system error event occurs. 0 = Do not report fatal errors to the root complex (default) 1 = Report fatal errors to the root complex

Table 4-26. Device Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
1	NFERE	RW	Nonfatal error reporting enable. If this bit is set, then the bridge is enabled to send ERR_NONFATAL messages to the root complex when a system error event occurs. 0 = Do not report nonfatal errors to the root complex (default) 1 = Report nonfatal errors to the root complex
0	CERE	RW	Correctable error reporting enable. If this bit is set, then the bridge is enabled to send ERR_COR messages to the root complex when a system error event occurs. 0 = Do not report correctable errors to the root complex (default) 1 = Report correctable errors to the root complex

4.51 Device Status Register

The device status register provides PCI Express device specific information to the system. See Table 4-27 for a complete description of the register contents.

PCI register offset: 7Ah
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-27. Device Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:6	RSVD	R	Reserved. Returns 00 0000 0000b when read.
5	PEND	RU	Transaction pending. This bit is set when the bridge has issued a non-posted transaction that has not been completed.
4	APD	RU	AUX power detected. This bit indicates that AUX power is present. 0 = No AUX power detected 1 = AUX power detected
3	URD	RCU	Unsupported request detected. This bit is set by the bridge when an unsupported request is received.
2	FED	RCU	Fatal error detected. This bit is set by the bridge when a fatal error is detected.
1	NFED	RCU	Nonfatal error detected. This bit is set by the bridge when a nonfatal error is detected.
0	CED	RCU	Correctable error detected. This bit is set by the bridge when a correctable error is detected.

4.52 Link Capabilities Register

The link capabilities register indicates the link specific capabilities of the bridge. See Table 4-28 for a complete description of the register contents.

PCI register offset: 7Ch
Register type: Read-only
Default value: 000Y XC11h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	y	y

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	y	x	x	x	1	1	0	0	0	0	0	1	0	0	0	1

Table 4-28. Link Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_NUM	R	Port number. This field indicates port number for the PCI Express link. This field is read-only 00h indicating that the link is associated with port 0.
23:22	RSVD	R	Reserved. Return 00b when read.
21	LBN_CAP	R	Link bandwidth notification. This bit is hardwired to 0b since this field is not applicable to a bridge.
20	DLLLAR_CAP	R	DLL link active reporting capable. This bit is hardwired to 0b since the bridge does not support this capability.
19	SDER_CAP	R	Surprise down error reporting capable. This bit is hardwired to 0b since the bridge does not support this capability.
18	CLK_PM	R	Clock Power Management. This bit is hardwired to 1 to indicate that XIO2001 supports Clock Power Management through CLKREQ protocol.
17:15	L1_LATENCY	R	L1 exit latency. This field indicates the time that it takes to transition from the L1 state to the L0 state. Bit 6 (CCC) in the link control register (offset 80h, see Section 4.53) equals 1b for a common clock and equals 0b for an asynchronous clock. For a common reference clock, the value of this field is determined by bits 20:18 (L1_EXIT_LAT_ASYNC) of the control and diagnostic register 1 (offset C4h, see Section 4.62). For an asynchronous reference clock, the value of this field is determined by bits 17:15 (L1_EXIT_LAT_COMMON) of the control and diagnostic register 1 (offset C4h, see Section 4.62).
14:12	L0S_LATENCY	R	L0s exit latency. This field indicates the time that it takes to transition from the L0s state to the L0 state. Bit 6 (CCC) in the link control register (offset 80h, see Section 4.53) equals 1b for a common clock and equals 0b for an asynchronous clock. For a common reference clock, the value of 011b indicates that the L1 exit latency falls between 256 ns to less than 512 ns. For an asynchronous reference clock, the value of 100b indicates that the L1 exit latency falls between 512 ns to less than 1 µs.
11:10	ASLPMS	R	Active state link PM support. This field indicates the level of active state power management that the bridge supports. The value 11b indicates support for both L0s and L1 through active state power management.
9:4	MLW	R	Maximum link width. This field is encoded 00 0001b to indicate that the bridge only supports a x1 PCI Express link.
3:0	MLS	R	Maximum link speed. This field is encoded 1h to indicate that the bridge supports a maximum link speed of 2.5 Gb/s.

4.53 Link Control Register

The link control register controls link specific behavior. See Table 4-29 for a complete description of the register contents.

PCI register offset: 80h
Register type: Read-only, Read/Write
Default value: 0Y0Xh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	y	0	0	0	0	0	0	x	x

Table 4-29. Link Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11	LABW_IEN	R	Link autonomous bandwidth interrupt enable. This bit is hardwired to 0b since this field is not applicable to a bridge.
10	LBWN_IEN	R	Link bandwidth management interrupt enable. This bit is hardwired to 0b since this field is not applicable to a bridge.

Table 4-29. Link Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
9	HWAW_DIS	R	Hardware autonomous width disable. This bit is hardwired to 0b since this field is not supported by this bridge.
8	CPM_EN	RW	Clock Power Management Enable. This bit is used to enable the bridge to use $\overline{\text{CLKREQ}}$ for clock power management 0 = Clock Power Management is disabled. $\overline{\text{CLKREQ}}$ is held low. 1 = Clock Power Management is enabled and the bridge is permitted to use the $\overline{\text{CLKREQ}}$ signal to allow the REFCLK input to be stopped The default value for this is bit is determined by bit 23 (CPM_EN_DEF_OVRD) in the general control register (offset D4h, see Section 4.65).
7	ES	RW	Extended synch. This bit forces the bridge to extend the transmission of FTS ordered sets and an extra TS2 when exiting from L1 prior to entering to L0. 0 = Normal synch (default) 1 = Extended synch
6	CCC	RW	Common clock configuration. When this bit is set, it indicates that the bridge and the device at the opposite end of the link are operating with a common clock source. A value of 0b indicates that the bridge and the device at the opposite end of the link are operating with separate reference clock sources. The bridge uses this common clock configuration information to report the L0s and L1 exit latencies. 0 = Reference clock is asynchronous (default) 1 = Reference clock is common
5	RL	R	Retrain link. This bit has no function and is read-only 0b.
4	LD	R	Link disable. This bit has no function and is read-only 0b.
3	RCB	RW	Read completion boundary. This bit is an indication of the RCB of the root complex. The state of this bit has no affect on the bridge, since the RCB of the bridge is fixed at 128 bytes. 0 = 64 bytes (default) 1 = 128 bytes
2	RSVD	R	Reserved. Returns 0b when read.
1:0	ASLPMC	RW	Active state link PM control. This field enables and disables the active state PM. The default value for this is bit is determined by bits 29:28 (ASPM_CTRL_DEF_OVRD) in the general control register (offset D4h, see Section 4.65). 00 = Active state PM disabled (default) 01 = L0s entry enabled 10 = L1 entry enabled 11 = L0s and L1 entry enabled

4.54 Link Status Register

The link status register indicates the current state of the PCI Express link. See Table 4-30 for a complete description of the register contents.

PCI register offset:	82h
Register type:	Read-only
Default value:	X011h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	x	0	0	0	0	0	0	0	1	0	0	0	1

Table 4-30. Link Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	LABW	R	Link autonomous bandwidth status. This bit has no function and is read-only 0b.
14	LBWM	R	Link bandwidth management status. This bit has no function and is read-only 0b.
13	DLLLA	R	Data link layer link active. This bit has no function and is read-only 0b.

Table 4-30. Link Status Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
12	SCC	R	Slot clock configuration. This bit indicates that the bridge uses the same physical reference clock that the platform provides on the connector. If the bridge uses an independent clock irrespective of the presence of a reference on the connector, then this bit must be cleared. 0 = Independent 125-MHz reference clock is used 1 = Common 100-MHz reference clock is used
11	LT	R	Link training. This bit has no function and is read-only 0b.
10	TE	R	Retrain link. This bit has no function and is read-only 0b.
9:4	NLW	R	Negotiated link width. This field is read-only 00 0001b indicating the lane width is x1.
3:0	LS	R	Link speed. This field is read-only 1h indicating the link speed is 2.5 Gb/s.

4.55 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see Section 4.57) that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) of the serial-bus control and status register (offset B3h, see Section 4.58) is cleared. This register is reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset.

PCI register offset:	B0h
Register type:	Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.56 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to the serial-bus device. The word address is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see Section 4.57) that initiates the bus cycle. This register is reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset.

PCI register offset:	B1h
Register type:	Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.57 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the slave address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle is a read or a write cycle. Writing to this register initiates the cycle on the serial interface. See Table 4-31 for a complete description of the register contents.

PCI register offset:	B2h
Register type:	Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-31. Serial-Bus Slave Address Register Descriptions

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1 (1)	SLAVE_ADDR	RW	Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b.
0 (1)	RW_CMD	RW	Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle.
			0 = A single byte write is requested (default). 1 = A single byte read is requested.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.58 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial bus. See Table 4-32 for a complete description of the register contents.

PCI register offset:	B3h
Register type:	Read-only, Read/Write, Read/Clear
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-32. Serial-Bus Control and Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7 (1)	PROT_SEL	RW	Protocol select. This bit selects the serial-bus address mode used. 0 = Slave address and word address are sent on the serial-bus (default) 1 = Only the slave address is sent on the serial-bus
6	RSVD	R	Reserved. Returns 0b when read.
5 (1)	REQBUSY	RU	Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress. 0 = No serial-bus cycle 1 = Serial-bus cycle in progress
4 (1)	ROMBUSY	RU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM.
			0 = No EEPROM activity 1 = EEPROM download in progress
3 (1)	SBDETECT	RWU	Serial Bus Detect. This bit is set when an EEPROM is detected at $\overline{\text{PERST}}$.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-32. Serial-Bus Control and Status Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2 (1)	SBTEST	RW	Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 = Serial-bus clock at normal operating frequency ~ 60 kHz (default) 1 = Serial-bus clock frequency increased for test purposes ~ 4 MHz
1 (1)	SB_ERR	RCU	Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle. 0 = No error 1 = Serial-bus error
0 (1)	ROM_ERR	RCU	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from serial EEPROM. 0 = No error 1 = EEPROM load error

4.59 GPIO Control Register

This register controls the direction of the five GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO0 ($\overline{\text{CLKRUN}}$), GPIO1 (PWR_OVRD), GPIO3 (SDA), and GPIO4 (SCL). See Table 4-33 for a complete description of the register contents.

PCI register offset:	B4h
Register type:	Read-only, Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-33. GPIO Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:5	RSVD	R	Reserved. Return 000h when read.
4 (1)	GPIO4_DIR	RW	GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode. 0 = Input (default) 1 = Output
3 (1)	GPIO3_DIR	RW	GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode. 0 = Input (default) 1 = Output
2 (1)	GPIO2_DIR	RW	GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode. 0 = Input (default) 1 = Output
(1)	GPIO1_DIR	RW	GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode. 0 = Input (default) 1 = Output
0 (1)	GPIO0_DIR	RW	GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode. 0 = Input (default) 1 = Output

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.60 GPIO Data Register

This register reads the state of the input mode GPIO terminals and changes the state of the output mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO3 (SDA), and GPIO4 (SCL). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. See Table 4-34 for a complete description of the register contents.

PCI register offset:	B6h
Register type:	Read-only, Read/Write
Default value:	00XXh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x

Table 4-34. GPIO Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:5	RSVD	R	Reserved. Returns 000h when read.
4 (1)	GPIO4_DATA	RW	GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode.
3 (1)	GPIO3_DATA	RW	GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode.
2 (1)	GPIO2_DATA	RW	GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode.
1 (1)	GPIO1_DATA	RW	GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode.
0 (1)	GPIO0_DATA	RW	GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.61 TL Control and Diagnostic Register 0

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4-35 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset:	C0h
Register type:	Read/Write
Default value:	0000 0001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4-35. Control and Diagnostic Register 0 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24 (1)	PRI_BUS_NUM	R	This field contains the captured primary bus number.
23:19 (1)	PRI_DEVICE_ NUM	R	This field contains the captured primary device number.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-35. Control and Diagnostic Register 0 Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
18	ALT_ERROR_REP	RW	Alternate Error Reporting. This bit controls the method that the XIO2001 uses for error reporting. 0 = Advisory Non-Fatal Error reporting supported (default) 1 = Advisory Non-Fatal Error reporting not supported
17:16	RSVD	R	Reserved. Returns 00b when read.
15:14 (1)	RSVD	RW	Reserved. Bits 15:14 default to 00b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 00b.
13:12	RSVD	R	Reserved. Returns 00b when read.
11:7 (1)	RSVD	RW	Reserved. Bits 11:7 default to 00000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 00000b.
6:3	RSVD	R	Reserved. Returns 0h when read.
2 (1)	CFG_ACCESS_MEM_REG	RW	Configuration access to memory-mapped registers. When this bit is set, the bridge allows configuration access to memory-mapped configuration registers.
1 (1)	RSVD	RW	Reserved. Bit 1 defaults to 0b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0b.
0 (1)	FORCE_CLKREQ	RW	Force $\overline{\text{CLKREQ}}$. When this bit is set, the bridge will force the $\overline{\text{CLKREQ}}$ output to always be asserted. The default setting for this bit is 1b.

4.62 Control and Diagnostic Register 1

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4-36 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset:	C4h
Register type:	Read/Write
Default value:	0012 0108h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0

Table 4-36. Control and Diagnostic Register 1 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
32:21	RSVD	R	Reserved. Returns 000h when read.
20:18 (1)	L1_EXIT_LAT_ASYNC	RW	L1 exit latency for asynchronous clock. When bit 6 (CCC) of the link control register (offset 80h, see Section 4.53) is set, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 7Ch, see Section 4.52). This field defaults to 100b.
17:15 (1)	L1_EXIT_LAT_COMMON	RW	L1 exit latency for common clock. When bit 6 (CCC) of the link control register (offset 80h, see Section 4.53) is clear, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 7Ch, see Section 4.52). This field defaults to 100b.
14:11 (1)	RSVD	RW	Reserved. Bits 14:11 default to 0000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0000b.
10 (1)	SBUS_RESET_MASK	RW	Secondary bus reset bit mask. When this bit is set, the bridge masks the reset caused by bit 6 (SRST) of the bridge control register (offset 3Eh, see Section 4.29). This bit defaults to 0b.
9:6 (1)	L1ASPM_TIMER	RW	L1ASPM entry timer. This field specifies the value (in 512-ns ticks) of the L1ASPM entry timer. This field defaults to 0100b.

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(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-36. Control and Diagnostic Register 1 Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
5:2(1)	L0s_TIMER	RW	L0s entry timer. This field specifies the value (in 62.5-MHz clock ticks) of the L0s entry timer. This field defaults to 0010b.
1:0(1)	RSVD	RW	Reserved. Bits 1:0 default to 00b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 00b.

4.63 Control and Diagnostic Register 2

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4-37 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset:	C8h
Register type:	Read/Write
Default value:	3214 2000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-37. Control and Diagnostic Register 2 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24(1)	N_FTS_ ASYNC_CLK	RW	N_FTS for asynchronous clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is clear, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field shall default to 32h.
23:16(1)	N_FTS_ COMMON_ CLK	RW	N_FTS for common clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is set, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field defaults to 14h.
15:13	PHY_REV	R	PHY revision number
12:8 (1)	LINK_NUM	RW	Link number
7(1)	EN_L2_PWR_ SAVE	RW	Enable L2 Power Savings 0= Power savings not enabled when in L2 1= Power savings enabled when in L2.
6	RSVD	R	Reserved. Returns 0b when read.
5(1)	BAR0_EN	RW	BAR 0 Enable. 0 = BAR at offset 10h is disabled (default) 1 = BAR at offset 10h is enabled
4:0(1)	RSVD	RW	Reserved. Bits 4:0 default to 00000b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 00000b.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.64 Subsystem Access Register

The contents of this read/write register are aliased to the subsystem vendor ID and subsystem ID registers at PCI offsets 84h and 86h. See Table 4-38 for a complete description of the register contents.

PCI register offset:	D0h
Register type:	Read/Write
Default value:	0000 0000h

BIT NUMBER	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-38. Subsystem Access Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:16 (1)	SubsystemID	RW	Subsystem ID. The value written to this field is aliased to the subsystem ID register at PCI offset 46h (see Section 4.33).
15:0 (1)	SubsystemVendorID	RW	Subsystem vendor ID. The value written to this field is aliased to the subsystem vendor ID register at PCI offset 44h (see Section 4.32).

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.65 General Control Register

This read/write register controls various functions of the bridge. See Table 4-39 for a complete description of the register contents.

PCI register offset:	D4h
Register type:	Read-only, Read/Write
Default value:	8600 025Fh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1

Table 4-39. General Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:30(1)	CFG_RETRY_CNTR	RW	Configuration retry counter. Configures the amount of time that a configuration request must be retried on the secondary PCI bus before it may be completed with configuration retry status on the PCI Express side. 00 = 25 µs 01 = 1 ms 10 = 25 ms (default) 11 = 50 ms
29:28(1)	ASPM_CTRL_DEF_OVRD	RW	Active State Power Management Control Default Override. These bits are used to determine the power up default for bits 1:0 of the Link Control Register in the PCI Express Capability Structure. 00 = Power on default indicates that the active state power management is disable (00b) (default) 01 = Power on default indicates that the active state power management is enabled for L0s (01b) 10 = Power on default indicates that the active state power management is enabled for L1s (10b) 11 = Power on default indicates that the active state power management is enabled for L0s and L1s (11b)
27 (1)	LOW_POWER_EN	RW	Low-power enable. When this bit is set, the half-amplitude, no pre-emphasis mode for the PCI Express TX drivers is enabled. The default for this bit is 0b.
26 (1)	PCI_PM_VERSION_CTRL	RW	PCI power management version control. This bit controls the value reported in bits 2:0 (PM_VERSION) in the power management capabilities register (offset 4Ah, see Section 4.36). It also controls the value of bit 3 (NO_SOFT_RESET) in the power management control/status register (offset 4Ch, see Section 4.37). 0 = Version fields reports 010b and NO_SOFT_RESET reports 0b for Power Management 1.1 compliance 1 = Version fields reports 011b and NO_SOFT_RESET reports 1b for Power Management 1.2 compliance (default)
25 (1)	RSVD	RW	Reserved. Bit 25 defaults to 0b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 0b.
24	RSVD	R	Reserved. Returns 0b when read.
23 (1)	CPM_EN_DEF_OVRD	RW	Clock power management enable default override. This bit determines the power-up default for bits 1:0 (CPM_EN) of the link control register (offset 80h, see Section 4.53) in the PCI Express Capability structure. 0 = Power-on default indicates that clock power management is disabled (00b) (default) 1 = Power-on default indicates that clock power management is enabled for L0s and L1 (11b)

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-39. General Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
22:20 (1)	POWER_OVRD	RW	Power override. This bit field determines how the bridge responds when the slot power limit is less than the amount of power required by the bridge and the devices behind the bridge. 000 = Ignore slot power limit (default). 001 = Assert the PWR_OVRD terminal. 010 = Disable secondary clocks selected by the clock mask register. 011 = Disable secondary clocks selected by the clock mask register and assert the PWR_OVRD terminal. 100 = Respond with unsupported request to all transactions except for configuration transactions (type 0 or type 1) and set slot power limit messages. 101,110, 111 = Reserved
19 (1)	READ_PREFETCH_DIS	RW	Read Prefetch Disable. This bit is used to control the pre-fetch functionality on PCI memory read transactions. 0 = Memory read, memory read line, and memory read multiple will be treated as prefetchable reads (default) 1 = Memory read line, and memory read multiple will be treated as pre-fetchable reads. Memory read will not be prefetchable. No auto-prefetch reads will be made for these requests.
18:16 (1)	L0s_LATENCY	RW	L0s maximum exit latency. This field programs the maximum acceptable latency when exiting the L0s state. This sets bits 8:6 (EP_L0S_LAT) in the device capabilities register (offset 74h, see Section 4.49). 000 = Less than 64 ns (default) 001 = 64 ns up to less than 128 ns 010 = 128 ns up to less than 256 ns 011 = 256 ns up to less than 512 ns 100 = 512 ns up to less than 1 µs 101 = 1 µs up to less than 2 µs 110 = 2 µs to 4 µs 111 = More than 4 µs
15:13 (1)	L1_LATENCY	RW	L1 maximum exit latency. This field programs the maximum acceptable latency when exiting the L1 state. This sets bits 11:9 (EP_L1_LAT) in the device capabilities register (offset 74h, see Section 4.49). 000 = Less than 1 µs (default) 001 = 1 µs up to less than 2 µs 010 = 2 µs up to less than 4 µs 011 = 4 µs up to less than 8 µs 100 = 8 µs up to less than 16 µs 101 = 6 µs up to less than 32 µs 110 = 32 µs to 64 µs 111 = More than 64 µs
12 (1)	VC_CAP_EN	R	VC Capability Structure Enable. This bit is hardwired to 0b indicating that the VC Capability structure is permanently disabled.
11 (2)	BPCC_E	RW	Bus power clock control enable. This bit controls whether the secondary bus PCI clocks are stopped when the XIO2001 is placed in the D3 state. It is assumed that if the secondary bus clocks are required to be active, that a reference clock continues to be provided on the PCI Express interface. 0 = Secondary bus clocks are not stopped in D3 (default) 1 = Secondary bus clocks are stopped on D3
10 (2)	BEACON_ENABLE	RW	Beacon enable. This bit controls the mechanism for waking up the physical PCI Express link when in L2. 0 = $\overline{\text{WAKE}}$ mechanism is used exclusively. Beacon is not used (default) 1 = Beacon and $\overline{\text{WAKE}}$ mechanisms are used

(2) These bits are sticky and must retain their value when the bridge is powered by V_{AUX}.

Table 4-39. General Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
9:8[1]	MIN_POWER_SCALE	RW	Minimum power scale. This value is programmed to indicate the scale of bits 7:0 (MIN_POWER_VALUE). 00 = 1.0x 01 = 0.1x 10 = 0.01x (default) 11 = 0.001x
7:0[1]	MIN_POWER_VALUE	RW	Minimum power value. This value is programmed to indicate the minimum power requirements. This value is multiplied by the minimum power scale field (bits 9:8) to determine the minimum power requirements for the bridge. The default is 5Fh, indicating that the bridge requires 0.95 W of power. This field can be reprogrammed through an EEPROM or the system BIOS.

4.66 Clock Control Register

This register enables and disables the PCI clock outputs (CLKOUT). See Table 4-40 for a complete description of the register contents.

PCI register offset: D8h

Register type: Read-only, Read/Write

Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-40. Clock Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7[1]	RSVD	R	Reserved. Returns 0b when read.
6[1]	CLOCK6_DISABLE	RW	Clock output 6 disable. This bit disables secondary CLKOUT6. 0 = Clock enabled (default) 1 = Clock disabled
5[1]	CLOCK5_DISABLE	RW	Clock output 5 disable. This bit disables secondary CLKOUT5. 0 = Clock enabled (default) 1 = Clock disabled
4[1]	CLOCK4_DISABLE	RW	Clock output 4 disable. This bit disables secondary CLKOUT4. 0 = Clock enabled (default) 1 = Clock disabled
3[1]	CLOCK3_DISABLE	RW	Clock output 3 disable. This bit disables secondary CLKOUT3. 0 = Clock enabled (default) 1 = Clock disabled
2[1]	CLOCK2_DISABLE	RW	Clock output 2 disable. This bit disables secondary CLKOUT2. 0 = Clock enabled (default) 1 = Clock disabled
1[1]	CLOCK1_DISABLE	RW	Clock output 1 disable. This bit disables secondary CLKOUT1. 0 = Clock enabled (default) 1 = Clock disabled
0[1]	CLOCK0_DISABLE	RW	Clock output 0 disable. This bit disables secondary CLKOUT0. 0 = Clock enabled (default) 1 = Clock disabled

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.67 Clock Mask Register

This register selects which PCI bus clocks are disabled when bits 22:20 (POWER_OVRD) in the general control register (offset D4h, see Section 4.65) are set to 010h or 011h. This register has no effect on the clock outputs if the POWER_OVRD bits are not set to 010h or 011h or if the slot power limit is greater than the power required. See Table 4-41 for a complete description of the register contents.

PCI register offset:	D9h
Register type:	Read-only, Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-41. Clock Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	RSVD	R	Reserved. Returns 0b when read.
6 (1)	CLOCK6_MASK	RW	Clock output 6 mask. This bit disables CLKOUT6 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
5 (1)	CLOCK5_MASK	RW	Clock output 5 mask. This bit disables CLKOUT5 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
4 (1)	CLOCK4_MASK	RW	Clock output 4 mask. This bit disables CLKOUT4 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
3 (1)	CLOCK3_MASK	RW	Clock output 3 mask. This bit disables CLKOUT3 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
2 (1)	CLOCK2_MASK	RW	Clock output 2 mask. This bit disables CLKOUT2 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
1 (1)	CLOCK1_MASK	RW	Clock output 1 mask. This bit disables CLKOUT1 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled
0 (1)	CLOCK0_MASK	RW	Clock output 0 mask. This bit disables CLKOUT0 when the POWER_OVRD bits are set to 010b or 011b and the slot power limit is exceeded. 0 = Clock enabled (default) 1 = Clock disabled

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.68 Clock Run Status Register

The clock run status register indicates the state of the PCI clock-run features in the bridge. See Table 4-42 for a complete description of the register contents.

PCI register offset:	DAh
Register type:	Read-only
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-42. Clock Run Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1	RSVD	R	Reserved. Returns 000 0000b when read.
0 (1)	SEC_CLK_STATUS	RU	Secondary clock status. This bit indicates the status of the PCI bus secondary clock outputs. 0 = Secondary clock running 1 = Secondary clock stopped

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.69 Arbiter Control Register

The arbiter control register controls the bridge internal arbiter. The arbitration scheme used is a two-tier rotational arbitration. The bridge is the only secondary bus master that defaults to the higher priority arbitration tier. See Table 4-43 for a complete description of the register contents.

PCI register offset:	DCh
Register type:	Read/Write
Default value:	40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

Table 4-43. Clock Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7(1)	PARK	RW	Bus parking mode. This bit determines where the internal arbiter parks the secondary bus. When this bit is set, the arbiter parks the secondary bus on the bridge. When this bit is cleared, the arbiter parks the bus on the last device mastering the secondary bus. 0 = Park the secondary bus on the last secondary bus master (default) 1 = Park the secondary bus on the bridge
6 (1)	BRIDGE_TIER_SEL	RW	Bridge tier select. This bit determines in which tier the bridge is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)
5(1)	TIER_SEL5	RW	$\overline{\text{GNT5}}$ tier select. This bit determines in which tier $\overline{\text{GNT5}}$ is placed in the arbitration scheme. 0 = Lowest priority tier (default) 1 = Highest priority tier
4(1)	TIER_SEL4	RW	$\overline{\text{GNT4}}$ tier select. This bit determines in which tier $\overline{\text{GNT4}}$ is placed in the arbitration scheme. 0 = Lowest priority tier (default) 1 = Highest priority tier
3(1)	TIER_SEL3	RW	$\overline{\text{GNT3}}$ tier select. This bit determines in which tier $\overline{\text{GNT3}}$ is placed in the arbitration scheme. 0 = Lowest priority tier (default) 1 = Highest priority tier
2(1)	TIER_SEL2	RW	$\overline{\text{GNT2}}$ tier select. This bit determines in which tier $\overline{\text{GNT2}}$ is placed in the arbitration scheme. 0 = Lowest priority tier (default) 1 = Highest priority tier
1(1)	TIER_SEL1	RW	$\overline{\text{GNT1}}$ tier select. This bit determines in which tier $\overline{\text{GNT1}}$ is placed in the arbitration scheme. 0 = Lowest priority tier (default) 1 = Highest priority tier

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(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-43. Clock Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
0 (1)	TIER_SEL0	RW	$\overline{\text{GNT0}}$ tier select. This bit determines in which tier $\overline{\text{GNT0}}$ is placed in the arbitration scheme. 0 = Lowest priority tier (default) 1 = Highest priority tier

4.70 Arbiter Request Mask Register

The arbiter request mask register enables and disables support for requests from specific masters on the secondary bus. The arbiter request mask register also controls if a request input is automatically masked on an arbiter time-out. See Table 4-44 for a complete description of the register contents.

PCI register offset:	DDh
Register type:	Read/Write
Default value:	00h

BIT NUMBER	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0

Table 4-44. Arbiter Request Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7 (1)	ARB_TIMEOUT	RW	Arbiter time-out. This bit enables the arbiter time-out feature. The arbiter time-out is defined as the number of PCI clocks after the PCI bus has gone idle for a device to assert $\overline{\text{FRAME}}$ before the arbiter assumes the device will not respond. 0 = Arbiter time disabled (default) 1 = Arbiter time-out set to 16 PCI clocks
6 (1)	AUTO_MASK	RW	Automatic request mask. This bit enables automatic request masking when an arbiter time-out occurs. 0 = Automatic request masking disabled (default) 1 = Automatic request masking enabled
5 (1)	REQ5_MASK	RW	Request 5 ($\overline{\text{REQ5}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0. 0 = Use request 5 (default) 1 = Ignore request 5
4 (1)	REQ4_MASK	RW	Request 4 ($\overline{\text{REQ4}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0. 0 = Use request 4 (default) 1 = Ignore request 4
3 (1)	REQ3_MASK	RW	Request 3 ($\overline{\text{REQ3}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0. 0 = Use request 3 (default) 1 = Ignore request 3
2 (1)	REQ2_MASK	RW	Request 2 ($\overline{\text{REQ2}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0. 0 = Use request 2 (default) 1 = Ignore request 2
1 (1)	REQ1_MASK	RW	Request 1 ($\overline{\text{REQ1}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0. 0 = Use request 2 (default) 1 = Ignore request 2
0 (1)	REQ0_MASK	RW	Request 0 ($\overline{\text{REQ0}}$) Mask. Setting this bit forces the internal arbiter to ignore requests signal on request input 0. 0 = Use request 0 (default) 1 = Ignore request 0

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.71 Arbiter Time-Out Status Register

The arbiter time-out status register contains the status of each request (request 5–0) time-out. The time-out status bit for the respective request is set if the device did not assert $\overline{\text{FRAME}}$ after the arbiter time-out value. See Table 4-45 for a complete description of the register contents.

PCI register offset:	DEh
Register type:	Read/Clear
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-45. Arbiter Time-Out Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:6	RSVD	R	Reserved. Returns 00b when read.
5	REQ5_TO	RCU	Request 5 Time Out Status 0 = No time-out 1 = Time-out has occurred
4	REQ4_TO	RCU	Request 4 Time Out Status 0 = No time-out 1 = Time-out has occurred
3	REQ3_TO	RCU	Request 3 Time Out Status 0 = No time-out 1 = Time-out has occurred
2	REQ2_TO	RCU	Request 2 Time Out Status 0 = No time-out 1 = Time-out has occurred
1	REQ1_TO	RCU	Request 1Time Out Status 0 = No time-out 1 = Time-out has occurred
0	REQ0_TO	RCU	Request 0 Time Out Status 0 = No time-out 1 = Time-out has occurred

4.72 Serial IRQ Mode Control Register

This register controls the behavior of the serial IRQ controller. See Table 4-46 for a complete description of the register contents.

PCI register offset:	E0h
Register type:	Read-only, Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4-46. Serial IRQ Mode Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	R	Reserved. Returns 0h when read.
3:2 (1)	START_WIDTH	RW	Start frame pulse width. Sets the width of the start frame for a SERIRQ stream. 00 = 4 clocks (default) 01 = 6 clocks 10 = 8 clocks 11 = Reserved
1 (1)	POLLMODE	RW	Poll mode. This bit selects between continuous and quiet mode. 0 = Continuous mode (default) 1 = Quiet mode
0 (1)	DRIVEMODE	RW	RW Drive mode. This bit selects the behavior of the serial IRQ controller during the recovery cycle. 0 = Drive high (default) 1 = 3-state

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.73 Serial IRQ Edge Control Register

This register controls the edge mode or level mode for each IRQ in the serial IRQ stream. See Table 4-47 for a complete description of the register contents.

PCI register offset:	E2h
Register type:	Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-47. Serial IRQ Edge Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15 (1)	IRQ15_MODE	RW	IRQ 15 edge mode 0 = Edge mode (default) 1 = Level mode
14 (1)	IRQ14_MODE	RW	IRQ 14 edge mode 0 = Edge mode (default) 1 = Level mode
13 (1)	IRQ13_MODE	RW	IRQ 13 edge mode 0 = Edge mode (default) 1 = Level mode
12 (1)	IRQ12_MODE	RW	IRQ 12 edge mode 0 = Edge mode (default) 1 = Level mode

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-47. Serial IRQ Edge Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
11[1]	IRQ11_MODE	RW	IRQ 11 edge mode 0 = Edge mode (default) 1 = Level mode
10[1]	IRQ10_MODE	RW	IRQ 10 edge mode 0 = Edge mode (default) 1 = Level mode
9[1]	IRQ9_MODE	RW	IRQ 9 edge mode 0 = Edge mode (default) 1 = Level mode
8[1]	IRQ8_MODE	RW	IRQ 8 edge mode 0 = Edge mode (default) 1 = Level mode
7[1]	IRQ7_MODE	RW	IRQ 7 edge mode 0 = Edge mode (default) 1 = Level mode
6[1]	IRQ6_MODE	RW	IRQ 6 edge mode 0 = Edge mode (default) 1 = Level mode
5[1]	IRQ5_MODE	RW	IRQ 5 edge mode 0 = Edge mode (default) 1 = Level mode
4[1]	IRQ4_MODE	RW	IRQ 4 edge mode 0 = Edge mode (default) 1 = Level mode
3[1]	IRQ3_MODE	RW	IRQ 3 edge mode 0 = Edge mode (default) 1 = Level mode
2[1]	IRQ2_MODE	RW	IRQ 2 edge mode 0 = Edge mode (default) 1 = Level mode
1[1]	IRQ1_MODE	RW	IRQ 1 edge mode 0 = Edge mode (default) 1 = Level mode
0[1]	IRQ0_MODE	RW	IRQ 0 edge mode 0 = Edge mode (default) 1 = Level mode

4.74 Serial IRQ Status Register

This register indicates when a level mode IRQ is signaled on the serial IRQ stream. After a level mode IRQ is signaled, a write-back of 1b to the asserted IRQ status bit re-arms the interrupt. IRQ interrupts that are defined as edge mode in the serial IRQ edge control register are not reported in this status register. See Table 4-48 for a complete description of the register contents.

PCI register offset: E4h
Register type: Read/Clear
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4-48. Serial IRQ Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15[1]	IRQ15	RCU	IRQ 15 asserted. This bit indicates that the IRQ15 has been asserted. 0 = Deasserted 1 = Asserted
14[1]	IRQ14	RCU	IRQ 14 asserted. This bit indicates that the IRQ14 has been asserted. 0 = Deasserted 1 = Asserted
13[1]	IRQ13	RCU	IRQ 13 asserted. This bit indicates that the IRQ13 has been asserted. 0 = Deasserted 1 = Asserted
12[1]	IRQ12	RCU	IRQ 12 asserted. This bit indicates that the IRQ12 has been asserted. 0 = Deasserted 1 = Asserted
11[1]	IRQ11	RCU	IRQ 11 asserted. This bit indicates that the IRQ11 has been asserted. 0 = Deasserted 1 = Asserted
10[1]	IRQ10	RCU	IRQ 10 asserted. This bit indicates that the IRQ10 has been asserted. 0 = Deasserted 1 = Asserted
9[1]	IRQ9	RCU	IRQ 9 asserted. This bit indicates that the IRQ9 has been asserted. 0 = Deasserted 1 = Asserted
8[1]	IRQ8	RCU	IRQ 8 asserted. This bit indicates that the IRQ8 has been asserted. 0 = Deasserted 1 = Asserted
7[1]	IRQ7	RCU	IRQ 7 asserted. This bit indicates that the IRQ7 has been asserted. 0 = Deasserted 1 = Asserted

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 4-48. Serial IRQ Status Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
6[1]	IRQ6	RCU	IRQ 6 asserted. This bit indicates that the IRQ6 has been asserted. 0 = Deasserted 1 = Asserted
5[1]	IRQ5	RCU	IRQ 5 asserted. This bit indicates that the IRQ5 has been asserted. 0 = Deasserted 1 = Asserted
4[1]	IRQ4	RCU	IRQ 4 asserted. This bit indicates that the IRQ4 has been asserted. 0 = Deasserted 1 = Asserted
3[1]	IRQ3	RCU	IRQ 3 asserted. This bit indicates that the IRQ3 has been asserted. 0 = Deasserted 1 = Asserted
2[1]	IRQ2	RCU	IRQ 2 asserted. This bit indicates that the IRQ2 has been asserted. 0 = Deasserted 1 = Asserted
1[1]	IRQ1	RCU	IRQ 1 asserted. This bit indicates that the IRQ1 has been asserted. 0 = Deasserted 1 = Asserted
0[1]	IRQ0	RCU	IRQ 0 asserted. This bit indicates that the IRQ0 has been asserted. 0 = Deasserted 1 = Asserted

4.75 Pre-Fetch Agent Request Limits Register

This register is used to set the Pre-Fetch Agent's limits on retrieving data using upstream reads. See Table 4-49 for a complete description of the register contents.

PCI register offset:	E8h
Register type:	Read/Clear
Default value:	0443h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	1

Table 4-49. Pre-Fetch Agent Request Limits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11:8 (1)	PFA_REQ_CNT_LIMIT	RW	Request count limit. Determines the number of Pre-Fetch reads that takes place in each burst. 4'h0 = Auto-prefetch agent is disabled. 4'h1 = Thread is limited to one buffer. No auto-prefetch reads will be generated. 4'h2:F = Thread will be limited to initial read and (PFA_REQ_CNT_LIMIT – 1)
7:6	PFA_CPL_CACHE_MODE	RW	Completion cache mode. Determines the rules for completing the caching process. 00 = No caching. • Pre-fetching is disabled. • All remaining read completion data will be discarded after any of the data has been returned to the PCI master. 01 = Light caching. • Pre-fetching is enabled. • All remaining read completion data will be discarded after data has been returned to the PCI master and the PCI master terminated the transfer. • All remaining read completion data will be cached after data has been returned to the PCI master and the bridge has terminated the transfer with RETRY. 10 = Full caching. • Pre-fetching is enabled. • All remaining read completion data will be cached after data has been returned to the PCI master and the PCI master terminated the transfer. • All remaining read completion data will be cached after data has been returned to the PCI master and the bridge has terminated the transfer with RETRY. 11 = Reserved.
5:4	RSVD	R	Reserved. Returns 00b when read.
3:0	PFA_REQ_LENGTH_LIMIT	RW	Request Length Limit. Determines the number of bytes in the thread that the pre-fetch agent will read for that thread. 0000 = 64 bytes 0001 = 128 bytes 0010 = 256 bytes 0011 = 512 bytes 0100 = 1 Kbytes 0101 = 2 Kbytes 0110 = 4 Kbytes 0111 = 8 Kbytes 1000:1111 = Reserved

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.76 Cache Timer Transfer Limit Register

This register is used to set the number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded. See Table 4-50 for a complete description of the register contents.

PCI register offset:	EAh
Register type:	Read/Clear
Default value:	0008h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 4-50. Cache Timer Transfer Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7:0[1]	CACHE_TMR_XFR _LIMIT	RW	Number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.77 Cache Timer Lower Limit Register

Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the "cache miss limit" check can be triggered. See Table 4-51 for a complete description of the register contents.

PCI register offset: ECh
Register type: Read/Clear
Default value: 007Fh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Table 4-51. Cache Timer Lower Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11:0[1]	CACHE_TIMER _LOWER_LIMIT	RW	Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the "cache miss limit" check can be triggered.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.78 Cache Timer Upper Limit Register

Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer. See Table 4-52 for a complete description of the register contents.

PCI register offset: EEh
Register type: Read/Clear
Default value: 01C0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0

Table 4-52. Cache Timer Upper Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11:0[1]	CACHE_TIMER _UPPER_LIMIT	RW	Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5 PCI Express Extended Configuration Space

The programming model of the PCI Express extended configuration space is compliant to the *PCI Express Base Specification* and the *PCI Express to PCI/PCI-X Bridge Specification* programming models. The PCI Express extended configuration map uses the PCI Express advanced error reporting capability.

All bits marked with a ┫ are sticky bits and are reset by a global reset (GRST) or the internally-generated power-on reset. All bits marked with a ┫ are reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, PERST, GRST, or the internally-generated power-on reset.

Table 5-1. PCI Express Extended Configuration Register Map

REGISTER NAME		OFFSET
Next capability offset / capability version	PCI Express advanced error reporting capabilities ID	100h
Uncorrectable error status register(1)		104h
Uncorrectable error mask register(1)		108h
Uncorrectable error severity register(1)		10Ch
Correctable error status register(1)		110h
Correctable error mask(1)		114h
Advanced error capabilities and control(1)		118h
Header log register(1)		11Ch
Header log register(1)		120h
Header log register(1)		124h
Header log register(1)		128h
Secondary uncorrectable error status(1)		12Ch
Secondary uncorrectable error mask(1)		130h
Secondary uncorrectable error severity register(1)		134h
Secondary error capabilities and control register(1)		138h
Secondary header log register(1)		13Ch
Secondary header log register(1)		140h
Secondary header log register(1)		144h
Secondary header log register(1)		148h
Reserved		14Ch–FFCh

(1) These bits are reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset.

5.1 Advanced Error Reporting Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express advanced error reporting capabilities. The register returns 0001h when read.

PCI Express extended register offset:	100h
Register type:	Read-only
Default value:	0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

5.2 Next Capability Offset/Capability Version Register

This read-only register identifies the next location in the PCI Express extended capabilities link list. The upper 12 bits in this register shall be 000h, indicating that the Advanced Error Reporting Capability is the last capability in the linked list. The least significant four bits identify the revision of the current capability block as 1h.

PCI Express extended register offset:	102h
Register type:	Read-only
Default value:	0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

5.3 Uncorrectable Error Status Register

The uncorrectable error status register reports the status of individual errors as they occur on the primary PCI Express interface. Software may only clear these bits by writing a 1b to the desired location. See Table 5-2 for a complete description of the register contents.

PCI Express extended register offset:	104h
Register type:	Read-only, Read/Clear
Default value:	0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-2. Uncorrectable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:22	RSVD	R	Reserved. Returns 000 0000 0000b when read.
21	ACS_VIOLATION	R	ACS Violation. Not supported, ths bit returns 0b when read.
20(1)	UR_ERROR	RCU	Unsupported request error. This bit is asserted when an unsupported request is received.
19(1)	ECRC_ERROR	RCU	Extended CRC error. This bit is asserted when an extended CRC error is detected.
18(1)	MAL_TLP	RCU	Malformed TLP. This bit is asserted when a malformed TLP is detected.
17(1)	RX_OVERFLOW	RCU	Receiver overflow. This bit is asserted when the flow control logic detects that the transmitting device has illegally exceeded the number of credits that were issued.
16(1)	UNXP_CPL	RCU	Unexpected completion. This bit is asserted when a completion packet is received that does not correspond to an issued request.
15(1)	CPL_ABORT	RCU	Completer abort. This bit is asserted when the bridge signals a completer abort.
14(1)	CPL_TIMEOUT	RCU	Completion time-out. This bit is asserted when no completion has been received for an issued request before the time-out period.
13(1)	FC_ERROR	RCU	Flow control error. This bit is asserted when a flow control protocol error is detected either during initialization or during normal operation.
12(1)	PSN_TLP	RCU	Poisoned TLP. This bit is asserted when a poisoned TLP is received.
11:6	RSVD	R	Reserved. Returns 00 0000b when read.
5	SD_ERROR	R	Surprise down error. Not supported, this bit returns 0b when read.
4 (1)	DLL_ERROR	RCU	Data link protocol error. This bit is asserted if a data link layer protocol error is detected.
3:0	RSVD	R	Reserved. Returns 0h when read.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.4 Uncorrectable Error Mask Register

The uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5-3 for a complete description of the register contents.

PCI Express extended register offset:	108h
Register type:	Read-only, Read/Write
Default value:	0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-3. Uncorrectable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:22	RSVD	R	Reserved. Returns 000 0000 0000b when read.
21	ACS_VIOLATION_MASK	RW	ACS Violation mask. Not supported, this bit returns 0b when read.
20 (1)	UR_ERROR_MASK	RW	Unsupported request error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
19 (1)	ECRC_ERROR_MASK	RW	Extended CRC error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
18 (1)	MAL_TLP_MASK	RW	Malformed TLP mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
17 (1)	RX_OVERFLOW_MASK	RW	Receiver overflow mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
16 (1)	UNXP_CPL_MASK	RW	Unexpected completion mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
15 (1)	CPL_ABORT_MASK	RW	Completer abort mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
14 (1)	CPL_TIMEOUT_MASK	RW	Completion time-out mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
13 (1)	FC_ERROR_MASK	RW	Flow control error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
12 (1)	PSN_TLP_MASK	RW	Poisoned TLP mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
11:6	RSVD	R	Reserved. Returns 000 0000b when read.
5	SD_ERROR_MASK	R	SD error mask. Not supported, returns 0b when read.
4 (1)	DLL_ERROR_MASK	RW	Data link protocol error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 5-3. Uncorrectable Error Mask Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
3:0	RSVD	R	Reserved. Returns 0h when read.

5.5 Uncorrectable Error Severity Register

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 5-4 for a complete description of the register contents.

PCI Express extended register offset:	10Ch
Register type:	Read-only, Read/Write
Default value:	0006 2031h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	1

Table 5-4. Uncorrectable Error Severity Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:22	RSVD	R	Reserved. Returns 000 0000 0000b when read.
21	ACS_VIOLATION_SEVR	R	ACS violation severity. Not supported, returns 0b when read.
20(1)	UR_ERROR_SEVRO	RW	Unsupported request error severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
19(1)	ECRC_ERROR_SEVRR	RW	Extended CRC error severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
18(1)	MAL_TLP_SEVR	RW	Malformed TLP severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
17(1)	RX_OVERFLOW_SEVR	RW	Receiver overflow severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
16(1)	UNXP_CPL_SEVRP	RW	Unexpected completion severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
15(1)	CPL_ABORT_SEVR	RW	Completer abort severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
14(1)	CPL_TIMEOUT_SEVR	RW	Completion time-out severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
13(1)	FC_ERROR_SEVR	RW	Flow control error severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL

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(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 5-4. Uncorrectable Error Severity Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
12 (1)	PSN_TLP_SEVR	RW	Poisoned TLP severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
11:6	RSVD	R	Reserved. Returns 000 000b when read.
5	SD_ERROR_SEVR	R	SD error severity. Not supported, returns 1b when read.
4 (1)	DLL_ERROR_SEVR	RW	Data link protocol error severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL
3:1	RSVD	R	Reserved. Retirms 000b wjem read/
0	RSVD	R	Reserved. Returns 1h when read.

5.6 Correctable Error Status Register

The correctable error status register reports the status of individual errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 5-5 for a complete description of the register contents.

PCI Express extended register offset:	110h
Register type:	Read-only, Read/Clear
Default value:	0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-5. Correctable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
13 (1)	ANFES	RCU	Advisory Non-Fatal Error Status. This bit is asserted when an Advisor Non-Fatal Error has been reported.
12 (1)	REPLAY_TMOUT	RCU	Replay timer time-out. This bit is asserted when the replay timer expires for a pending request or completion that has not been acknowledged.
11:9	RSVD	R	Reserved. Returns 000b when read.
8 (1)	REPLAY_ROLL	RCU	REPLAY_NUM rollover. This bit is asserted when the replay counter rolls over after a pending request or completion has not been acknowledged.
7 (1)	BAD_DLLP	RCU	Bad DLLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a DLLP.
6 (1)	BAD_TLP	RCU	Bad TLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a TLP.
5:1	RSVD	R	Reserved. Returns 00000b when read.
0 (1)	RX_ERROR	RCU	Receiver error. This bit is asserted when an 8b/10b error is detected by the PHY at any time.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.7 Correctable Error Mask Register

The correctable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5-6 for a complete description of the register contents.

PCI Express extended register offset:	114h
Register type:	Read-only, Read/Write
Default value:	0000 2000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-6. Correctable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
13 (1)	ANFEM	RW	Advisory Non-Fatal Error Mask. 0 = Error condition is unmasked 1 = Error condition is masked (default)
12 (1)	REPLAY_TMOUT_MASK	RW	Replay timer time-out mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
11:9	RSVD	R	Reserved. Returns 000b when read.
8 (1)	REPLAY_ROLL_MASK	RW	REPLAY_NUM rollover mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
7 (1)	BAD_DLLP_MASK	RW	Bad DLLP error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
6 (1)	BAD_TLP_MASK	RW	Bad TLP error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
5:1	RSVD	R	Reserved. Returns 00000b when read.
0 (1)	RX_ERROR_MASK	RW	Receiver error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.8 Advanced Error Capabilities and Control Register

The advanced error capabilities and control register allows the system to monitor and control the advanced error reporting capabilities. See Table 5-7 for a complete description of the register contents.

PCI Express extended register offset:	118h
Register type:	Read-only, Read/Write
Default value:	0000 00A0h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 5-7. Advanced Error Capabilities and Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:9	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000 0000b when read.
8 (1)	ECRC_CHK_EN	RW	Extended CRC check enable 0 = Extended CRC checking is disabled 1 = Extended CRC checking is enabled
7	ECRC_CHK_CAPABLE	R	Extended CRC check capable. This read-only bit returns a value of 1b indicating that the bridge is capable of checking extended CRC information.
6 (1)	ECRC_GEN_EN	RW	Extended CRC generation enable 0 = Extended CRC generation is disabled 1 = Extended CRC generation is enabled
5	ECRC_GEN_CAPABLE	R	Extended CRC generation capable. This read-only bit returns a value of 1b indicating that the bridge is capable of generating extended CRC information.
4:0 (1)	FIRST_ERR	RU	First error pointer. This 5-bit value reflects the bit position within the uncorrectable error status register (offset 104h, see Section 5.3) corresponding to the class of the first error condition that was detected.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.9 Header Log Register

The header log register stores the TLP header for the packet that lead to the most recently detected error condition. Offset 11Ch contains the first DWORD. Offset 128h contains the last DWORD (in the case of a 4DW TLP header). Each DWORD is stored with the least significant byte representing the earliest transmitted. This register shall only be reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI Express extended register offset:	11Ch, 120h, 124h, and 128h
Register type:	Read-only
Default value:	0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.10 Secondary Uncorrectable Error Status Register

The secondary uncorrectable error status register reports the status of individual PCI bus errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 5-8 for a complete description of the register contents.

PCI Express extended register offset:	12Ch
Register type:	Read-only, Read/Clear
Default value:	0000 0000h

BIT NUMBER	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-8. Secondary Uncorrectable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
13	INTERNAL_ERROR	R	Internal bridge error. This error bit is associated with a PCI-X error and returns 0b when read.
12 (1)	SERR_DETECT	RCU	$\overline{\text{SERR}}$ assertion detected. This bit is asserted when the bridge detects the assertion of SERR on the secondary bus.
11 (1)	PERR_DETECT	RCU	PERR assertion detected. This bit is asserted when the bridge detects the assertion of PERR on the secondary bus.
10 (1)	DISCARD_TIMER	RCU	Delayed transaction discard timer expired. This bit is asserted when the discard timer expires for a pending delayed transaction that was initiated on the secondary bus.
9 (1)	UNCOR_ADDR	RCU	Uncorrectable address error. This bit is asserted when the bridge detects a parity error during the address phase of an upstream transaction.
8	UNCOR_ATTRIB	R	Uncorrectable attribute error. This error bit is associated with a PCI-X error and returns 0b when read.
7 (1)	UNCOR_DATA	RCU	Uncorrectable data error. This bit is asserted when the bridge detects a parity error during a data phase of an upstream write transaction, or when the bridge detects the assertion of PERR when forwarding read completion data to a PCI device.
6	UNCOR_SPLTMSG	R	Uncorrectable split completion message data error. This error bit is associated with a PCI-X error and returns 0b when read.
5	UNXPC_SPLTCMP	R	Unexpected split completion error. This error bit is associated with a PCI-X error and returns 0b when read.
4	RSVD	R	Reserved. Returns 0b when read.
3 (1)	MASTER_ABORT	RCU	Received master abort. This bit is asserted when the bridge receives a master abort on the PCI interface.
2 (1)	TARGET_ABORT	RCU	Received target abort. This bit is asserted when the bridge receives a target abort on the PCI interface.
1	MABRT_SPLIT	R	Master abort on split completion. This error bit is associated with a PCI-X error and returns 0b when read.
0	TABRT_SPLIT	R	Target abort on split completion status. This error bit is associated with a PCI-X error and returns 0b when read.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.11 Secondary Uncorrectable Error Mask Register

The secondary uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5-9 for a complete description of the register contents.

PCI Express extended register offset:	130h
Register type:	Read-only, Read/Write
Default value:	0000 17A8h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	1	1	1	1	0	1	0	1	0	0	0

Table 5-9. Secondary Uncorrectable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13 (1)	INTERNAL_ERROR_MASK	RW	Internal bridge error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
12 (1)	SERR_DETECT_MASK	RW	$\overline{\text{SERR}}$ assertion detected 0 = Error condition is unmasked 1 = Error condition is masked (default)
11 (1)	PERR_DETECT_MASK	RW	$\overline{\text{PERR}}$ assertion detectedi 0 = Error condition is unmasked 1 = Error condition is masked (default)
10 (1)	DISCARD_TIMER_MASK	RW	Delayed transaction discard timer expired 0 = Error condition is unmasked 1 = Error condition is masked (default)
9 (1)	UNCOR_ADDR_MASK	RW	Uncorrectable address error 0 = Error condition is unmasked 1 = Error condition is masked (default)
8 (1)	UNCOR_ATTRIB_MASK	RW	Uncorrectable attribute error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
7 (1)	UNCOR_DATA_MASK	RW	Uncorrectable data error 0 = Error condition is unmasked 1 = Error condition is masked (default)
6 (1)	UNCOR_SPLTMSG_MASK	RW	Uncorrectable split completion message data error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
5 (1)	SC_ERROR_MASK	RW	Unexpected split completion error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
4	RSVD	R	Reserved. Returns 0b when read.
3 (1)	MASTER_ABORT_MASK	RW	Received master abort 0 = Error condition is unmasked 1 = Error condition is masked (default)
2 (1)	TARGET_ABORT_MASK	RW	Received target abort 0 = Error condition is unmasked 1 = Error condition is masked (default)
1 (1)	MABRT_SPLIT_MASK	RW	Master abort on split completion. This mask bit is associated with a PCI-X error and has no effect on the bridge.
0	TABRT_SPLIT_MASK	R	Target abort on split completion. This mask bit is associated with a PCI-X error and has no effect on the bridge.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.12 Secondary Uncorrectable Error Severity

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 5-10 for a complete description of the register contents.

PCI Express extended register offset:	134h
Register type:	Read-only, Read/Write
Default value:	0000 1340h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0

Table 5-10. Secondary Uncorrectable Error Severity Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13(1)	INTERNAL_ERROR_SEVR	RW	Internal bridge error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
12 (1)	SERR_DETECT_SEVR	RW	$\overline{\text{SERR}}$ assertion detected 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
11 (1)	PERR_DETECT_SEVR	RW	$\overline{\text{PERR}}$ assertion detected 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
10 (1)	DISCARD_TIMER_SEVR	RW	Delayed transaction discard timer expired 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
9 (1)	UNCOR_ADDR_SEVR	RW	Uncorrectable address error 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
8 (1)	UNCOR_ATTRIB_SEVR	RW	Uncorrectable attribute error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
7 (1)	UNCOR_DATA_SEVR	RW	Uncorrectable data error 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
6 (1)	UNCOR_SPLTMSG_SEVR	RW	Uncorrectable split completion message data error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
5 (1)	UNCOR_SPLTCMP_SEVR	RW	Unexpected split completion error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
4	RSVD	R	Reserved. Returns 0b when read.
3 (1)	MASTER_ABORT_SEVR	RW	Received master abort 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
2 (1)	TARGET_ABORT_SEVR	RW	Received target aborta 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
1 (1)	MABRT_SPLIT_SEVR	RW	Master abort on split completion. This severity bit is associated with a PCI-X error and has no effect on the bridge.
0	TABRT_SPLIT_SEVR	R	Target abort on split completion. This severity bit is associated with a PCI-X error and has no effect on the bridge.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.13 Secondary Error Capabilities and Control Register

The secondary error capabilities and control register allows the system to monitor and control the secondary advanced error reporting capabilities. See Table 5-11 for a complete description of the register contents.

PCI Express extended register offset:	138h
Register type:	Read-only
Default value:	0000 0000h

BIT NUMBER	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-11. Secondary Error Capabilities and Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:5	RSVD	R	Reserved. Return 000 0000 0000 0000 0000 0000 0000b when read.
4:0 (1)	SEC_FIRST_ERR	RU	First error pointer. This 5-bit value reflects the bit position within the secondary uncorrectable error status register (offset 12Ch, see Section 5.10) corresponding to the class of the first error condition that was detected.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.14 Secondary Header Log Register

The secondary header log register stores the transaction address and command for the PCI bus cycle that led to the most recently detected error condition. Offset 13Ch accesses register bits 31:0. Offset 140h accesses register bits 63:32. Offset 144h accesses register bits 95:64. Offset 148h accesses register bits 127:96. See Table 5-12 for a complete description of the register contents.

PCI Express extended register offset:	13Ch, 140h, 144h, and 148h
Register type:	Read-only
Default value:	0000 0000h

BIT NUMBER	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5-12. Secondary Header Log Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
127:64 (1)	ADDRESS	RU	Transaction address. The 64-bit value transferred on AD[31:0] during the first and second address phases. The first address phase is logged to 95:64 and the second address phase is logged to 127:96. In the case of a 32-bit address, bits 127:96 are set to 0.
63:44	RSVD	R	Reserved. Returns 0 0000h when read.
43:40 (1)	UPPER_CMD	RU	Transaction command upper. Contains the status of the $\overline{\text{C/BE}}$ terminals during the second address phase of the PCI transaction that generated the error if using a dual-address cycle.
39:36 (1)	LOWER_CMD	RU	Transaction command lower. Contains the status of the $\overline{\text{C/BE}}$ terminals during the first address phase of the PCI transaction that generated the error.
35:0	TRANS_ATTRIBUTE	R	Transaction attribute. Because the bridge does not support the PCI-X attribute transaction phase, these bits have no function, and return 0 0000 0000h when read.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6 Memory-Mapped TI Proprietary Register Space

The programming model of the memory-mapped TI proprietary register space is unique to this device.

All bits marked with a ┤ are sticky bits and are reset by a global reset ($\overline{\text{GRST}}$) or the internally-generated power-on reset. All bits marked with a (2) are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$ or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 6-1. Device Control Memory Window Register Map

REGISTER NAME				**OFFSET**
Reserved		Revision ID	Device control map ID	000h
Reserved				004h–03Ch
GPIO data (1)		GPIO control (1)		040h
Serial-bus control and status (1)	Serial-bus slave address (1)	Serial-bus word address (1)	Serial-bus data (1)	044h
Serial IRQ edge control (1)		Reserved	Serial IRQ mode control (1)	048h
Reserved		Serial IRQ status (1)		04Ch
Cache Timer Transfer Limit (1)		PFA Request Limit (1)		050h
Cache Timer Upper Limit (1)		Cache Timer Lower Limit (1)		054h
Reserved				058h–FFFh

(2) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.
(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.1 Device Control Map ID Register

The device control map ID register identifies the TI proprietary layout for this device control map. The value 04h identifies this as a PCI Express-to-PCI bridge.

Device control memory window register offset:	00h
Register type:	Read-only
Default value:	04h

BIT NUMBER	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	1	0	0

6.2 Revision ID Register

The revision ID register identifies the revision of the TI proprietary layout for this device control map. The value 00h identifies the revision as the initial layout.

Device control memory window register offset:	01h
Register type:	Read-only
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

6.3 GPIO Control Register

This register controls the direction of the five GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO3 (SDA), and GPIO4 (SCL). This register is an alias of the GPIO control register in the classic PCI configuration space(offset B4h, see Section 4.59). See Table 6-2 for a complete description of the register contents.

Device control memory window register offset:	40h
Register type:	Read-only, Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-2. GPIO Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:5	RSVD	R	Reserved. Returns 0000 0000 000b when read.
4 (1)	GPIO4_DIR	RW	GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode. 0 = Input (default) 1 = Output
3 (1)	GPIO3_DIR	RW	GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode. 0 = Input (default) 1 = Output
2 (1)	GPIO2_DIR	RW	GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode. 0 = Input (default) 1 = Output
1 (1)	GPIO1_DIR	RW	GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode. 0 = Input (default) 1 = Output
0 (1)	GPIO0_DIR	RW	GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode. 0 = Input (default) 1 = Output

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.4 GPIO Data Register

This register reads the state of the input mode GPIO terminals and changes the state of the output mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO0 (CLKRUN), GPIO1 (PWR_OVRD), GPIO3 (SDA), and GPIO4 (SCL). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. This register is an alias of the GPIO data register in the classic PCI configuration space (offset B6h, see Section 4.60). See Table 6-3 for a complete description of the register contents.

Device control memory window register offset:	42h
Register type:	Read-only, Read/Write
Default value:	00XXh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x

Table 6-3. GPIO Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:5	RSVD	R	Reserved. Returns 000 0000 0000b when read.
4 (1)	GPIO4_Data	RW	GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode.
3 (1)	GPIO3_Data	RW	GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode.
2 (1)	GPIO2_Data	RW	GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode.
1 (1)	GPIO1_Data	RW	GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode.
0 (1)	GPIO0_Data	RW	GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.5 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) in the serial-bus control and status register (offset 47h, see Section 6.8) is cleared. This register is an alias for the serial-bus data register in the PCI header (offset B0h, see Section 4.55). This register is reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset.

Device control memory window register offset:	44h
Register type:	Read/Write
Default value:	00h

BIT NUMBER	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	1

6.6 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to on the serial-bus interface. The word address is loaded into this register prior to writing the serial-bus slave address register that initiates the bus cycle. This register is an alias for the serial-bus word address register in the PCI header (offset B1h, see Section 4.56). This register is reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset.

Device control memory window register offset:	45h
Register type:	Read/Write
Default value:	00h

BIT NUMBER	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0

6.7 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle will be a read or a write cycle. Writing to this register initiates the cycle on the serial interface. This register is an alias for the serial-bus slave address register in the PCI header (offset B2h, see Section 4.57). See Table 6-4 for a complete description of the register contents.

Device control memory window register offset:	46h
Register type:	Read/Write
Default value:	00h

BIT NUMBER	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0

Table 6-4. Serial-Bus Slave Address Register Descriptions

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1 (1)	SLAVE_ADDR	RW	Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b.
0 (1)	RW_CMD	RW	Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle.
			0 = A single byte write is requested (default) 1 = A single byte read is requested

(1) These bits are reset by a PCI Express reset (PERST), a GRST, or the internally-generated power-on reset.

6.8 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial-bus. This register is an alias for the serial-bus control and status register in the PCI header (offset B3h, see Section 4.58). See Table 6-5 for a complete description of the register contents.

Device control memory window register offset:	47h
Register type:	Read-only, Read/Write, Read/Clear
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6-5. Serial-Bus Control and Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7(1)	PROT_SEL	RW	Protocol select. This bit selects the serial-bus address mode used. 0 = Slave address and word address are sent on the serial-bus (default) 1 = Only the slave address is sent on the serial-bus
6	RSVD	R	Reserved. Returns 0b when read.
5 (1)	REQBUSY	RU	Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress. 0 = No serial-bus cycle 1 = Serial-bus cycle in progresss
4 (1)	ROMBUSY	RU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM. 0 = No EEPROM activity 1 = EEPROM download in progress
3 (1)	SBDETECT	RWU	Serial EEPROM detected. This bit enables the serial-bus interface. The value of this bit controls whether the GPIO3//SDA and GPIO4//SCL terminals are configured as GPIO signals or as serial-bus signals. This bit is automatically set to 1b when a serial EEPROM is detected. **Note:** A serial EEPROM is only detected once following $\overline{\text{PERST}}$. 0 = No EEPROM present, EEPROM load process does not happen. GPIO3//SDA and GPIO4//SCL terminals are configured as GPIO signals. 1 = EEPROM present, EEPROM load process takes place. GPIO3//SDA and GPIO4//SCL terminals are configured as serial-bus signals.
2 (1)	SBTEST	RW	Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 = Serial-bus clock at normal operating frequency ~ 60 kHz (default) 1 = Serial-bus clock frequency increased for test purposes ~ 4 MHz
1 (1)	SB_ERR	RCU	Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle. 0 = No error 1 = Serial-bus error
0 (1)	ROM_ERR	RCU	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from a serial EEPROM. 0 = No error 1 = EEPROM load error

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.9 Serial IRQ Mode Control Register

This register controls the behavior of the serial IRQ controller. This register is an alias for the serial IRQ mode control register in the classic PCI configuration space (offset E0h, see Section 4.72). See Table 4-46 for a complete description of the register contents.

Device control memory window register offset:	48h
Register type:	Read-only, Read/Write
Default value:	00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6-6. Serial IRQ Mode Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	RSVD	R	Reserved. Returns 0h when read.
3:2 (1)	START_WIDTH	RW	Start frame pulse width. Sets the width of the start frame for a SERIRQ stream. 00 = 4 clocks (default) 01 = 6 clocks 10 = 8 clocks 11 = Reserved
1 (1)	POLLMODE	RW	Poll mode. This bit selects between continuous and quiet mode. 0 = Continuous mode (default) 1 = Quiet mode
0 (1)	DRIVEMODE	RW	RW Drive mode. This bit selects the behavior of the serial IRQ controller during the recovery cycle. 0 = Drive high (default) 1 = 3-state

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.10 Serial IRQ Edge Control Register

This register controls the edge mode or level mode for each IRQ in the serial IRQ stream. This register is an alias for the serial IRQ edge control register in the classic PCI configuration space (offset E2h, see Section 4.73). See Table 6-7 for a complete description of the register contents.

Device control memory window register offset:	4Ah
Register type:	Read/Write
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-7. Serial IRQ Edge Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15[1]	IRQ15_MODE	RW	IRQ 15 edge mode 0 = Edge mode (default) 1 = Level mode
14[1]	IRQ14_MODE	RW	IRQ 14 edge mode 0 = Edge mode (default) 1 = Level mode
13[1]	IRQ13_MODE	RW	IRQ 13 edge mode 0 = Edge mode (default) 1 = Level mode
12[1]	IRQ12_MODE	RW	IRQ 12 edge mode 0 = Edge mode (default) 1 = Level mode
11[1]	IRQ11_MODE	RW	IRQ 11 edge mode 0 = Edge mode (default) 1 = Level mode
10[1]	IRQ10_MODE	RW	IRQ 10 edge mode 0 = Edge mode (default) 1 = Level mode
9[1]	IRQ9_MODE	RW	IRQ 9 edge mode 0 = Edge mode (default) 1 = Level mode
8[1]	IRQ8_MODE	RW	IRQ 8 edge mode 0 = Edge mode (default) 1 = Level mode
7[1]	IRQ7_MODE	RW	IRQ 7 edge mode 0 = Edge mode (default) 1 = Level mode
6[1]	IRQ6_MODE	RW	IRQ 6 edge mode 0 = Edge mode (default) 1 = Level mode
5[1]	IRQ5_MODE	RW	IRQ 5 edge mode 0 = Edge mode (default) 1 = Level mode
4[1]	IRQ4_MODE	RW	IRQ 4 edge mode 0 = Edge mode (default) 1 = Level mode

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(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 6-7. Serial IRQ Edge Control Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
3[1]	IRQ3_MODE	RW	IRQ 3 edge mode 0 = Edge mode (default) 1 = Level mode
2[1]	IRQ2_MODE	RW	IRQ 2 edge mode 0 = Edge mode (default) 1 = Level mode
1[1]	IRQ1_MODE	RW	IRQ 1 edge mode 0 = Edge mode (default) 1 = Level mode
0[1]	IRQ0_MODE	RW	IRQ 0 edge mode 0 = Edge mode (default) 1 = Level mode

6.11 Serial IRQ Status Register

This register indicates when a level mode IRQ is signaled on the serial IRQ stream. After a level mode IRQ is signaled, a write-back of 1b to the asserted IRQ status bit re-arms the interrupt. IRQ interrupts that are defined as edge mode in the serial IRQ edge control register are not reported in this status register. This register is an alias for the serial IRQ status register in the classic PCI configuration space (offset E4h, see Section 4.74). See Table 4-48 for a complete description of the register contents.

Device control memory window register offset:	4Ch
Register type:	Read/Clear
Default value:	0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6-8. Serial IRQ Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15[1]	IRQ15	RCU	IRQ 15 asserted. This bit indicates that the IRQ15 has been asserted. 0 = Deasserted 1 = Asserted
14[1]	IRQ14	RCU	IRQ 14 asserted. This bit indicates that the IRQ14 has been asserted. 0 = Deasserted 1 = Asserted
13[1]	IRQ13	RCU	IRQ 13 asserted. This bit indicates that the IRQ13 has been asserted. 0 = Deasserted 1 = Asserted

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(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 6-8. Serial IRQ Status Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
12(1)	IRQ12	RCU	IRQ 12 asserted. This bit indicates that the IRQ12 has been asserted. 0 = Deasserted 1 = Asserted
11(1)	IRQ11	RCU	IRQ 11 asserted. This bit indicates that the IRQ11 has been asserted. 0 = Deasserted 1 = Asserted
10(1)	IRQ10	RCU	IRQ 10 asserted. This bit indicates that the IRQ10 has been asserted. 0 = Deasserted 1 = Asserted
9(1)	IRQ9	RCU	IRQ 9 asserted. This bit indicates that the IRQ9 has been asserted. 0 = Deasserted 1 = Asserted
8(1)	IRQ8	RCU	IRQ 8 asserted. This bit indicates that the IRQ8 has been asserted. 0 = Deasserted 1 = Asserted
7(1)	IRQ7	RCU	IRQ 7 asserted. This bit indicates that the IRQ7 has been asserted. 0 = Deasserted 1 = Asserted
6(1)	IRQ6	RCU	IRQ 6 asserted. This bit indicates that the IRQ6 has been asserted. 0 = Deasserted 1 = Asserted
5(1)	IRQ5	RCU	IRQ 5 asserted. This bit indicates that the IRQ5 has been asserted. 0 = Deasserted 1 = Asserted
4(1)	IRQ4	RCU	IRQ 4 asserted. This bit indicates that the IRQ4 has been asserted. 0 = Deasserted 1 = Asserted
3(1)	IRQ3	RCU	IRQ 3 asserted. This bit indicates that the IRQ3 has been asserted. 0 = Deasserted 1 = Asserted
2(1)	IRQ2	RCU	IRQ 2 asserted. This bit indicates that the IRQ2 has been asserted. 0 = Deasserted 1 = Asserted
1(1)	IRQ1	RCU	IRQ 1 asserted. This bit indicates that the IRQ1 has been asserted. 0 = Deasserted 1 = Asserted

Table 6-8. Serial IRQ Status Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
0[1]	IRQ0	RCU	IRQ 0 asserted. This bit indicates that the IRQ0 has been asserted. 0 = Deasserted 1 = Asserted

6.12 Pre-Fetch Agent Request Limits Register

This register is used to set the Pre-Fetch Agent's limits on retrieving data using upstream reads. This register is an alias for the pre-fetch agent request limits register in the classic PCI configuration space (offset E8h, see Section 4.75). See Table 6-9 for a complete description of the register contents.

Device control memory window register offset:	50h
Register type:	Read/Clear
Default value:	0443h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	1

Table 6-9. Pre-Fetch Agent Request Limits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11:8[1]	PFA_REQ_ CNT_LIMIT	RW	Request count limit. Determines the number of Pre-Fetch reads that takes place in each burst. 4'h0 = Auto-prefetch agent is disabled. 4'h1 = Thread is limited to one buffer. No auto-prefetch reads will be generated. 4'h2:F = Thread will be limited to initial read and (PFA_REQ_CNT_LIMIT – 1)
7:6	PFA_CPL_CACHE_ MODE	RW	Completion cache mode. Determines the rules for completing the caching process. 00 = No caching. • Pre-fetching is disabled. • All remaining read completion data will be discarded after any of the data has been returned to the PCI master. 01 = Light caching. • Pre-fetching is enabled. • All remaining read completion data will be discarded after data has been returned to the PCI master and the PCI master terminated the transfer. • All remaining read completion data will be cached after data has been returned to the PCI master and the bridge has terminated the transfer with RETRY. 10 = Full caching. • Pre-fetching is enabled. • All remaining read completion data will be cached after data has been returned to the PCI master and the PCI master terminated the transfer. • All remaining read completion data will be cached after data has been returned to the PCI master and the bridge has terminated the transfer with RETRY. 11 = Reserved.
5:4	RSVD	R	Reserved. Returns 00b when read.

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(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 6-9. Pre-Fetch Agent Request Limits Register Description (continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
3:0	PFA_REQ_LENGTH_LIMIT	RW	Request Length Limit. Determines the number of bytes in the thread that the pre-fetch agent will read for that thread. 0000 = 64 bytes 0001 = 128 bytes 0010 = 256 bytes 0011 = 512 bytes 0100 = 1 Kbytes 0101 = 2 Kbytes 0110 = 4 Kbytes 0111 = 8 Kbytes 1000:1111 = Reserved

6.13 Cache Timer Transfer Limit Register

This register is used to set the number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded. This register is an alias for the pre-fetch agent request limits register in the classic PCI configuration space (offset EAh, see Section 4.76). See Table 6-10 for a complete description of the register contents.

Device control memory window register offset:	52h
Register type:	Read/Clear
Default value:	0008h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0

Table 6-10. Cache Timer Transfer Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7:0(1)	CACHE_TMR_XFR_LIMIT	RW	Number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.14 Cache Timer Lower Limit Register

Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the "cache miss limit" check can be triggered. See Table 6-11 for a complete description of the register contents.

Device control memory window register offset:	54h
Register type:	Read/Clear
Default value:	007Fh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

Table 6-11. Cache Timer Lower Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11:0[1]	CACHE_TIMER_LOWER_LIMIT	RW	Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the "cache miss limit" check can be triggered.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.15 Cache Timer Upper Limit Register

Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer. See Table 6-12 for a complete description of the register contents.

Device control memory window register offset:	56h
Register type:	Read/Clear
Default value:	01C0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0

Table 6-12. Cache Timer Upper Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11:0[1]	CACHE_TIMER_UPPER_LIMIT	RW	Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer.

(1) These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) [1]

			VALUE	UNIT
V_{DD_33}	Supply voltage range		–0.5 to 3.6	V
V_{DD_15}			–0.5 to 1.65	V
V_I	Input voltage range	PCI	–0.5 to PCIR + 0.5	V
		PCI Express (RX)	–0.6 to 0.6	V
		PCI Express REFCLK (single-ended)	–0.5 to V_{DD_33} + 0.5	V
		PCI Express REFCLK (differential)	–0.3 to 1.15	V
		Miscellaneous 3.3-V IO	–0.5 to V_{DD_33} + 0.5	V
V_O	Output voltage range	PCI	–0.5 to V_{DD_33} + 0.5	V
		PCI Express (TX)	–0.5 to V_{DD_15} + 0.5	V
		Miscellaneous 3.3-V IO	–0.5 to V_{DD_33} + 0.5	V
$V_{ESD-HBM}$	Human-Body Model ESD rating	R = 1.5 K, C = 100 pF	2	kV
$V_{ESD-CDM}$	Charged-Device Model ESD rating	200 pF	500	V
	Input clamp current, (V_I < 0 or V_I > VDD) [2]		±20	mA
	Output clamp current, (V_O < 0 or V_O > VDD) [3]		±20	mA
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Applies for external input and bidirectional buffers. V_I < 0 or V_I > V_{DD} or V_I > PCIR.
(3) Applies for external input and bidirectional buffers. V_O < 0 or V_O > V_{DD} or V_O > PCIR.

7.2 Recommended Operating Conditions

		OPERATION	MIN	NOM	MAX	UNIT
V_{DD_15} V_{DDA_15}	Supply voltage	1.5 V	1.35	1.5	1.65	V
V_{DD_33} V_{DDA_33} $V_{DDA\_33\_AUX}$	Supply voltage	3.3 V	3	3.3	3.6	V
PCIR	PCI bus clamping rail voltage (with 1 kΩ resistor)	3.3 V	3	3.3	3.6	V
		5 V	4.75	5	5.25	

7.3 Nominal Power Consumption

DEVICES	POWER STATE (1)	VOLTS	AMPERES	WATTS
No downstream PCI devices	D0 idle	1.5	0.147	0.221
		3.3	0.062	0.205
		Totals:	0.209	0.426
One downstream PCI device	D0 idle	1.5	0.148	0.222
		3.3	0.077	0.254
		Totals:	0.225	0.476
One downstream PCI device	D0 active	1.5	0.157	0.236
		3.3	0.165	0.545
		Totals:	0.322	0.780
One downstream (max voltage)	D0 active	1.65	0.168	0.277
		3.6	0.188	0.677
		Totals:	0.356	0.954

(1) D0 idle power state: Downstream PCI device is in PCI state D0. Downstream device driver is loaded. Downstream device is not actively transferring data.
D0 active power state: Downstream PCI device is in PCI state D0. Downstream device driver is loaded. Downstream device is acitvely transferring data (worst case scenario).

7.4 PCI Express Differential Transmitter Output Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
UI (1) Unit interval	TXP, TXN	399.88	400	400.12	ps	Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.
$V_{TX-DIFF-PP}$ Differential peak-to-peak output voltage	TXP, TXN	0.8		1.2	V	$V_{TX-DIFF-PP} = 2*\|V_{TXP} - V_{TXN}\|$
$V_{TX-DIFF-PP-LOW}$ Low-power differential peak-to-peak TX voltage swing	TXP, TXN	0.4		1.2	V	$V_{TX-DIFF-PP} = 2*\|V_{TXP} - V_{TXN}\|$
$V_{TX-DE-RATIO-3.5dB}$ TX de-emphasis level ratio	TXP, TXN	3		4	dB	This is the ratio of the $V_{TX-DIFF-PP}$ of the second and following bits after a transition divided by the $V_{TX-DIFF-PP}$ of the first bit after a transition.
T_{TX-EYE} (2) (3) (4) Minimum TX eye width	TXP, TXN	0.75			UI	Does not include SSC or Ref_{CLK} jitter. Includes R_j at 10^{-12}.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ (2) Maximum time between the jitter median and maximum deviation from the median	TXP, TXN			0.125	UI	Measured differentially at zero crossing points after applying the 2.5 GT/s clock recovery function.
$T_{TX-RISE-FALL}$ (2) TX output rise/fall time	TXP, TXN	0.125			UI	Measured differentially from 20% to 80% of swing.
BW_{TX-PLL} (5) Maximum TX PLL bandwidth	TXP, TXN			22	MHz	Second order PLL jitter transfer bounding function.
$BW_{TX-PLL-LO-3DB}$ (5) (6) Minimum TX PLL bandwidth	TXP, TXN	1.5			MHz	Second order PLL jitter transfer bounding function.
$RL_{TX-DIFF}$ Tx package plus Si differential return loss	TXP, TXN	10			dB	
RL_{TX-CM} Tx package plus Si common mode return loss	TXP, TXN	6			dB	Measured over 0.05–1.25 GHz range

(1) SCC permits a 0, –5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.
(2) Measurements at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although deconvolution is recommended.
(3) Transmitter jitter is measured by driving the transmitter under test with a low jitter "ideal" clock and connecting the DUT to a reference board.
(4) Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.
(5) The Tx PLL Bandwidth must lie between the min and max ranges given in the above table. PLL peaking must lie below the value listed above. Note: the PLL B/W extends from zero up to the value(s) specified in the above table.
(6) A single combination of PLL BW and peaking is specified for 2.5 GT/s implemenations.

PCI Express Differential Transmitter Output Ranges *(continued)*

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
$Z_{\text{TX-DIFF\_DC}}$ DC differential TX impedance	TXP, TXN	80		120	Ω	Low impedance defined during signaling.
$V_{\text{TX-CM-AC-P}}$ (7) T_X AC common mode voltage	TXP, TXN			20	mV	
$I_{\text{TX-SHORT}}$ Transmitter short-circuit current limit	TXP, TXN			90	mA	The total current transmitter can supply when shorted to ground.
$V_{\text{TX-DC-CM}}$ Transmitter DC common-mode voltage	TXP, TXN	0		3.6	V	The allowed DC common-mode voltage at the transmitter pins under any conditions.
$V_{\text{TX-CM-DC-ACTIVE-IDLE-DELTA}}$ Absolute delta of DC common mode voltage during L0 and electrical idle	TXP, TXN	0		100	mV	|VTX-CM-DC – VTX-CM-Idle-DC| ≤ 100 mV $V_{\text{TX-CM-DC}} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ [during L0] $V_{\text{TX-CM-Idle-DC}} = DC_{(avg)}$ of $\|V_{TXP} + V_{TXN}\|/2$ [during electrical idle]
$V_{\text{TX-CM-DC-LINE-DELTA}}$ Absolute delta of DC common mode voltage between P and N	TXP, TXN	0		25	mV	$\|V_{\text{TXP-CM-DC}} – V_{\text{TXN-CM-DC}}\| \le 25$ mV when $V_{\text{TXP-CM-DC}} = DC_{(avg)}$ of $\|V_{TXP}\|$ [during L0] $V_{\text{TXN-CM-DC}} = DC_{(avg)}$ of $\|V_{TXN}\|$ [during L0]
$V_{\text{TX-IDLE-DIFF-AC-p}}$ Electrical idle differential peak output voltage	TXP, TXN	0		20	mV	$V_{\text{TX-IDLE-DIFFp}} = \|V_{\text{TXP-Idle}} – V_{\text{TXN-Idle}}\| \le 20$ mV
$V_{\text{TX-RCV-DETECT}}$ The amount of voltage change allowed during receiver detection	TXP, TXN			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.
$T_{\text{TX-IDLE-MIN}}$ Minimum time spent in electrical idle	TXP, TXN	20			ns	Minimum time a transmitter must be in electrical idle.
$T_{\text{TX-IDLE-SET-TO-IDLE}}$ Maximum time to transition to a valid electrical idle after sending an EIOS	TXP, TXN			8	ns	After sending the required number of EIOSs, the transmitter must meet all electrical idle specifications within this time. This is measured from the end of the last EIOS to the transmitter in electrical idle.
$T_{\text{TX-IDLE-TO-DIFF-DATA}}$ Maximum time to transition to a valid diff signaling after leaving electrical idle	TXP, TXN			8	ns	Maximum time to transistion to valid diff signaling after leaving electrical idle. This is considered a debounce time to the Tx.
C_{TX} AC coupling capacitor	TXP, TXN	75		200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

(7) Measurement is made over at least 10 UI.

7.5 PCI Express Differential Receiver Input Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
UI (1) Unit interval	RXP, RXN	399.88		400.12	ps	Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations.
$V_{\text{RX-DIFF-PP-CC}}$ (2) Differential input peak-to-peak voltage	RXP, RXN	0.175		1.200	V	$V_{\text{RX-DIFFp-p}} = 2*\|V_{RXP} – V_{RXN}\|$
$T_{\text{RX-EYE}}$ (2) (3) Minimum receiver eye width	RXP, RXN	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver is derived as $T_{\text{RX-MAX-JITTER}} = 1 – T_{\text{RX-EYE}} = 0.6$ UI
$T_{\text{RX-EYE-MEDIAN-to-MAX-JITTER}}$ (2) (3) Maximum time between the jitter median and maximum deviation from the median	RXP, RXN			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{\text{RX-DIFFp-p}} = 0$ V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the TX UI.

(1) No test load is necessarily associated with this value.

(2) Specified at the measurement point and measured over any 250 consecutive UIs. A test load must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UIs is used as a reference for the eye diagram.

(3) A TRX-EYE = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UIs must be used as the reference for the eye diagram.

PCI Express Differential Receiver Input Ranges *(continued)*

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
$BW_{RX\text{-}PLL\text{-}HI}$ (4) Maximum Rx PLL bandwidth	RXP, RXN			22	MHz	Second order PLL jitter transfer bounding function.
$BW_{RX\text{-}PLL\text{-}LO\text{-}3DB}$ (4) Minimum Rx PLL for 3 dB peaking	RXP, RXN	1.5			MHz	Second order PLL jitter transfer bounding function.
$V_{RX\text{-}CM\text{-}AC\text{-}P}$ (2) AC peak common mode input voltage	RXP, RXN			150	mV	$V_{RX\text{-}CM\text{-}AC\text{-}P} = RMS(\|V_{RXP} + V_{RXN}\|/2 – V_{RX\text{-}CM\text{-}DC})$ $V_{RX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\|V_{RXP} + V_{RXN}\|/2$.
$RL_{RX\text{-}DIFF}$ (5) Differential return loss	RXP, RXN	10			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and –300 mV, respectively.
$RL_{RX\text{-}CM}$ (5) Common mode return loss	RXP, RXN	6			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and –300 mV, respectively.
$Z_{RX\text{-}DIFF\text{-}DC}$ (6) DC differential input impedance	RXP, RXN	80		120	Ω	RX dc differential mode impedance
$Z_{RX\text{-}DC}$ (5) (6) DC input impedance	RXP, RXN	40		60	Ω	Required RXP as well as RXN dc impedance (50 Ω ±20% tolerance).
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ (7) DC input CM input impedance for V > 0 during reset or powerdown	RXP, RXN	50			kΩ	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 to 200 mV with respect to ground.
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}NEG}$ (7) DC input CM input impedance for V > 0 during reset or powerdown	RXP, RXN	1			kΩ	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 to 200 mV with respect to ground.
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$ Electrical idle detect threshold	RXP, RXN	65		175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2^*\|V_{RXP} – V_{RXN}\|$ measured at the receiver package terminals
$T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTER\text{-}TIME}$ Unexpected electrical idle enter detect threshold integration time	RXP, RXN			10	ms	An unexpected electrical idle ($V_{RX\text{-}DIFFp\text{-}p} < V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$) must be recognized no longer than $T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTER\text{-}TIME}$ to signal an unexpected idle condition.

(4) A single PLL bandwidth and peaking value of 1.5 to 22 MHz and 3 dB are defined.

(5) The receiver input impedance results in a differential return loss greater than or equal to 15 dB with the P line biased to 300 mV and the N line biased to .300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 . to ground for both the P and N line (i.e., as measured by a Vector Network Analyzer with 50-. probes). The series capacitors CTX is optional for the return loss measurement.

(6) Impedance during all link training status state machine (LTSSM) states. When transitioning from a PCI Express reset to the detect state (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on the unconfigured lane of a port.

(7) $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}NEG}$ and $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ are defined respectively for negative and postive voltages at the input of the receiver.

7.6 PCI Express Differential Reference Clock Input Ranges(1)

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
$f_{IN\text{-}DIFF}$ Differential input frequency	REFCLK+ REFCLK–		100		MHz	The input frequency is 100 MHz + 300 ppm and –2800 ppm including SSC-dictated variations.
$f_{IN\text{-}SE}$ Single-ended input frequency	REFCLK+		125		MHz	The input frequency is 125 MHz + 300 ppm and –300 ppm.
$V_{RX\text{-}DIFFp\text{-}p}$ Differential input peak-to-peak voltage	REFCLK+ REFCLK–	-0.30		1.150	V	$V_{RX\text{-}DIFFp\text{-}p} = 2^*\|V_{REFCLK+} – V_{REFCLK-}\|$
$V_{IH\text{-}SE}$	REFCLK+	0.7 V_{DDA_33}		V_{DDA_33}	V	Single-ended, reference clock mode high-level input voltage
$V_{IL\text{-}SE}$	REFCLK+	0		0.3 V_{DDA_33}	V	Single-ended, reference clock mode low-level input voltage
$V_{RX\text{-}CM\text{-}ACp}$ AC peak common mode input voltage	REFCLK+ REFCLK–			140	mV	$V_{RX\text{-}CM\text{-}ACp} = RMS(\|V_{REFCLK+} + V_{REFCLK-}\|/2\ V_{RX\text{-}CM\text{-}DC})$ $V_{RX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\|V_{REFCLK+} + V_{REFCLK-}\|/2$
Duty cycle	REFCLK+ REFCLK–	40%		60%		Differential and single-ended waveform input duty cycle
$Z_{C\text{-}DC}$ Clock source DC impedance	REFCLK+ REFCLK–	40		60	Ω	REFCLK± dc differential mode impedance

(1) The XIO2001 is compliant with the defined system jitter models for a PCI-Express reference clock and associated TX/RX link. Any usage of the XIO2001 in a system configuration that does not conform to the defined system jitter models requires the system designer to validate the system jitter budgets.

PCI Express Differential Reference Clock Input Ranges (1) *(continued)*

PARAMETER	TERMINALS	MIN	NOM	MAX	UNIT	COMMENTS
Z_{RX-DC} DC input impedance	REFCLK+ REFCLK–		20		kΩ	REFCLK+ dc single-ended mode impedance

7.7 PCI Bus Electrical Characteristics (1)

over recommended operating conditions

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage (2)	PCIR = 3.3 V		0.5 × V_{DD_33}	PCIR + 0.5	V
		PCIR = 5 V		2.0	PCIR + 0.5	
V_{IL}	Low-level input voltage (2)	PCIR = 3.3 V		–0.5	0.3 × V_{DD_33}	V
		PCIR = 5 V		–0.5	0.8	
V_I	Input voltage			0	PCIR	V
V_O	Output voltage (3)			0	V_{DD_33}	V
t_t	Input transition time (t_{rise} and t_{fall})			1	4	ns
V_{OH}	High-level output voltage	PCIR = 3.3 V	I_{OH} = –500 µA	0.9 × V_{DD_33}		V
		PCIR = 5 V	I_{OH} = –2 mA	2.4		
V_{OL}	Low-level output voltage	PCIR = 3.3 V	I_{OH} = 1500 µA		0.1 × V_{DD_33}	V
		PCIR = 5 V	I_{OH} = 6 mA		0.55	
I_{OZ}	High-impedance, output current (3)	PCIR = 3.3 V			±10	µA
		PCIR = 5 V			±70	
I_I	Input current	PCIR = 3.3 V			±10	µA
		PCIR = 5 V			±70	

(1) This table applies to CLK, CLKOUT6:0, AD31:0, C/BE[3:0], DEVSEL, FRAME, GNT5:0, INTD:A, IRDY, PAR, PERR, REQ5:0, PRST, SERR, STOP, TRDY, SERIRQ, M66EN, and LOCK terminals.
(2) Applies to external inputs and bidirectional buffers.
(3) Applies to external outputs and bidirectional buffers.

7.8 3.3-V I/O Electrical Characteristics (1)

over recommended operating conditions

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage (2)	V_{DD_33}		0.7 V_{DD_33}	V_{DD_33}	V
V_{IL}	VIL Low-level input voltage (2)	V_{DD_33}		0	0.3 V_{DD_33}	V
V_I	Input voltage			0	V_{DD_33}	V
V_O	Output voltage (3)			0	V_{DD_33}	V
t_t	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis (4)				0.13 V_{DD_33}	V
V_{OH}	High-level output voltage	V_{DD_33}	I_{OH} = –4 mA	0.8 V_{DD_33}		V
V_{OL}	Low-level output voltage	V_{DD_33}	I_{OL} = 4 mA		0.22 V_{DD_33}	V
I_{OZ}	High-impedance, output current (3)	V_{DD_33}	V_I = 0 to V_{DD_33}		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor (1)	V_{DD_33}	V_I = 0 to V_{DD_33}		±100	µA
I_I	Input current (5)	V_{DD_33}	V_I = 0 to V_{DD_33}		±1	µA

(1) Applies to GRST (pullup), EXT_ARB_EN (pulldown), CLKRUN_EN (pulldown), and most GPIO (pullup).
(2) Applies to external inputs and bidirectional buffers.
(3) Applies to external outputs and bidirectional buffers.
(4) Applies to PERST, GRST, and PME.
(5) Applies to external input buffers.

7.9 PCI Bus Timing Requirements[1]

over recommended operating conditions

PARAMETER		TEST CONDITION	33 MHz		66 MHz		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	CLK to shared signal valid propagation delay time	C_L = 50 pF		11			ns
		C_L = 30 pF				6	
	CLK to shared signal invalid propagation delay time	C_L = 50 pF	2				
		C_L = 30 pF			1		
t_{ON}	tEnable time, high-impedance-to-active delay time from CLK	C_L = 50 pF	2				ns
		C_L = 30 pF			1		
t_{OFF}	Disable time, active-to-high-impedance delay time from CLK	C_L = 50 pF		28			ns
		C_L = 30 pF				14	
t_{su}	Setup time on shared signals before CLK valid (rising edge)		7		3		ns
t_h	Hold time on shared signals after CLK valid (rising edge)		0		0		ns

(1) The PCI shared signals are AD31:0, $\overline{\text{C/BE[3:0]}}$, $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, $\overline{\text{STOP}}$, IDSEL, $\overline{\text{DEVSEL}}$, $\overline{\text{LOCK}}$, SERIRQ, PAR, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, and $\overline{\text{CLKRUN}}$.

7.10 PNP Thermal Characteristics[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-free-air thermal resistance	Low-K JEDEC test board, 1s (single signal layer), no air flow		50.8		°C/W
		High-K JEDEC test board, 2s2p (double signal layer, double buried power plane), no air flow		24.9		
θ_{JC}	Junction-to-case thermal resistance	Cu cold plate measurement process		18.9		°C/W
θ_{JB}	Junction-to-board thermal resistance	EIA/JESD 51-8		14.6		°C/W
ψ_{JT}	Junction-to-top of package	EIA/JESD 51-2		0.26		°C/W
ψ_{JB}	Junction-to-board	EIA/JESD 51-6		7.93		°C/W
T_A	Operating ambient temperature range	XIO2001PNP	0		70	°C
		XIO2001IPNP	–40		85	
T_J	Virtual junction temperature	XIO2001PNP	0		105	°C
		XIO2001IPNP	–40		105	

(1) For more details, refer to TI application note *IC Package Thermal Metrics* (SPRA953).

7.11 ZAJ Thermal Characteristics[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-free-air thermal resistance	Low-K JEDEC test board, 1s (single signal layer), no air flow		82		°C/W
		High-K JEDEC test board, 2s2p (double signal layer, double buried power plane), no air flow		58.8		
θ_{JC}	Junction-to-case thermal resistance	Cu cold plate measurement process		19		°C/W
θ_{JB}	Junction-to-board thermal resistance	EIA/JESD 51-8		32		°C/W
ψ_{JT}	Junction-to-top of package	EIA/JESD 51-2		0.5		°C/W
ψ_{JB}	Junction-to-board	EIA/JESD 51-6		30		°C/W
T_A	Operating ambient temperature range	XIO2001ZGU	0		70	°C
		XIO2001IZGU	–40		85	

(1) For more details, refer to TI application note *IC Package Thermal Metrics* (SPRA953).

ZAJ Thermal Characteristics [1] *(continued)*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_J	Virtual junction temperature	XIO2001ZGU	0		105	°C
		XIO2001IZGU	–40		105	

7.12 ZGU Thermal Characteristics [1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-free-air thermal resistance	Low-K JEDEC test board, 1s (single signal layer), no air flow		85		°C/W
		High-K JEDEC test board, 2s2p (double signal layer, double buried power plane), no air flow		48.3		
θ_{JC}	Junction-to-case thermal resistance	Cu cold plate measurement process		8.5		°C/W
θ_{JB}	Junction-to-board thermal resistance	EIA/JESD 51-8		25.4		°C/W
ψ_{JT}	Junction-to-top of package	EIA/JESD 51-2		0.5		°C/W
ψ_{JB}	Junction-to-board	EIA/JESD 51-6		24		°C/W
T_A	Operating ambient temperature range	XIO2001ZGU	0		70	°C
		XIO2001IZGU	–40		85	
T_J	Virtual junction temperature	XIO2001ZGU	0		105	°C
		XIO2001IZGU	–40		105	

(1) For more details, refer to TI application note *IC Package Thermal Metrics* (SPRA953).

7.13 Parameter Measurement Information

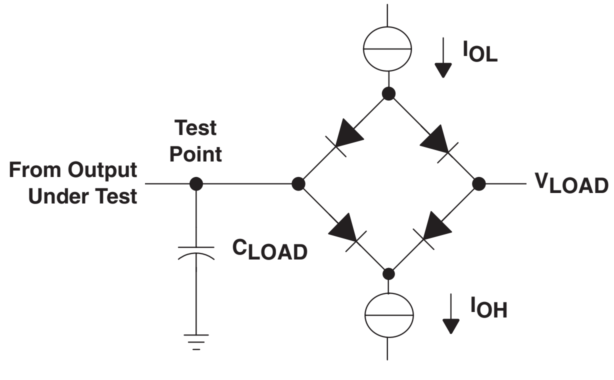
PCI Bus

LOAD CIRCUIT PARAMETERS

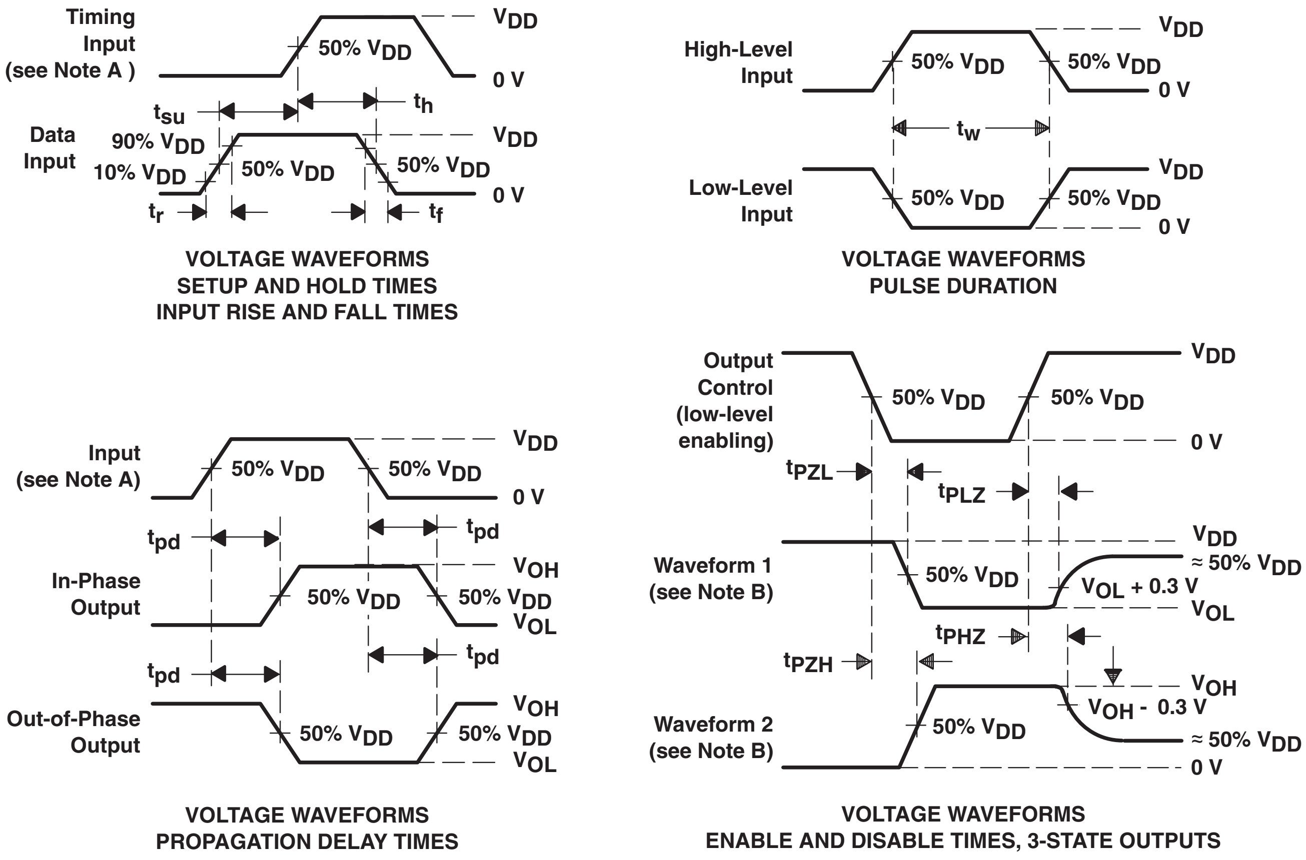
TIMING PARAMETER		C_{LOAD}† (pF)	I_{OL} (mA)	I_{OH} (mA)	V_{LOAD} (V)
t_{en}	t_{PZH}	30/50	12	- 12	0
	t_{PZL}				3
t_{dis}	t_{PHZ}	30/50	12	- 12	1.5
	t_{PLZ}				
t_{pd}		30/50	12	- 12	‡

† C_{LOAD} includes the typical load-circuit distributed capacitance.

‡ $\frac{V_{LOAD} - V_{OL}}{I_{OL}} = 50\ \Omega$, where $V_{OL} = 0.6$ V, $I_{OL} = 12$ mA



LOAD CIRCUIT



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES INPUT RISE AND FALL TIMES

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

For tPLZ and tPHZ, VOL and VOH are measured values.

Figure 7-1. Load Circuit And Voltage Waveforms

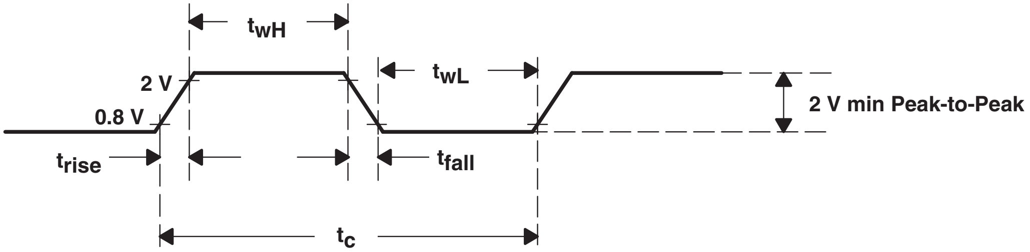


Figure 7-2. CLK Timing Waveform

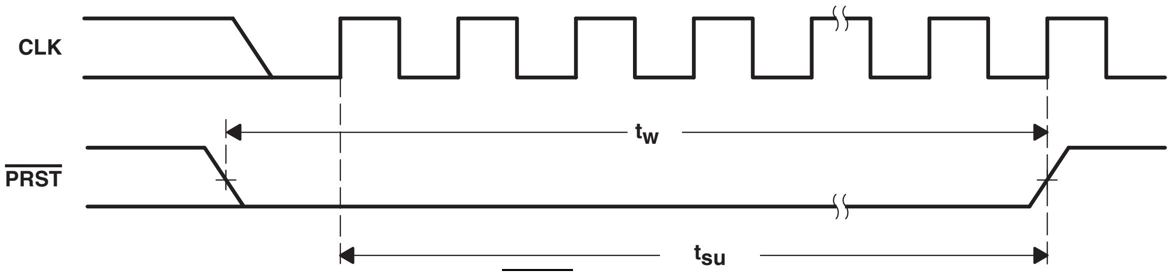


Figure 7-3. $\overline{\text{PRST}}$ Timing Waveforms

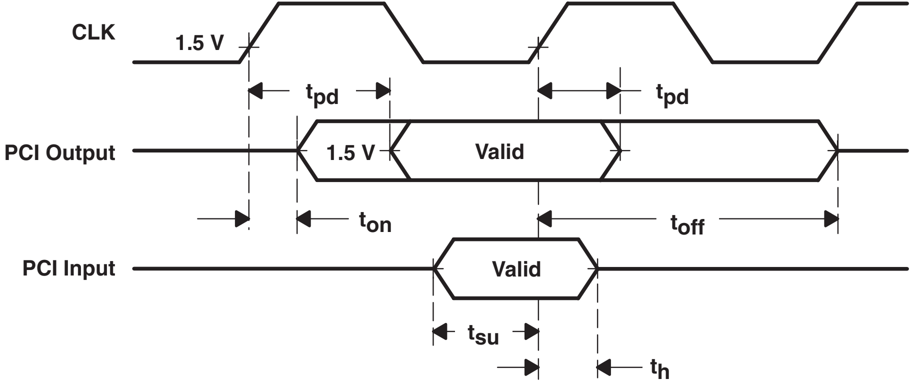


Figure 7-4. Shared Signals Timing Waveforms

8 Glossary

ACRONYM	DEFINTION
BIST	Built-in self test
ECRC	End-to-end cyclic redundancy code
EEPROM	Electrically erasable programmable read-only memory
GP	General purpose
GPIO	General-purpose input output
ID	Identification
IF	Interface
IO	Input output
I^{2}C	Intelligent Interface Controller
LPM	Link power management
LSB	Least significant bit
MSB	Most significant bit
MSI	Message signaled interrupts
PCI	Peripheral component interface
PME	PCI power management event
RX	Receive
SCL	Serial-bus clock
SDA	Serial-bus data
TC	Traffic class
TLP	Transaction layer packet or protocol
TX	Transmit

VC	Virtual channel

PACKAGE OPTION ADDENDUM

5-Jul-2010

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
XIO2001IPNP	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
XIO2001IZAJ	ACTIVE	BGA	ZAJ	144	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	Request Free Samples
XIO2001IZGU	ACTIVE	BGA MICROSTAR	ZGU	169	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	Request Free Samples
XIO2001PNP	ACTIVE	HTQFP	PNP	128	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
XIO2001ZAJ	ACTIVE	BGA	ZAJ	144	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	Request Free Samples
XIO2001ZGU	ACTIVE	BGA MICROSTAR	ZGU	169	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	Request Free Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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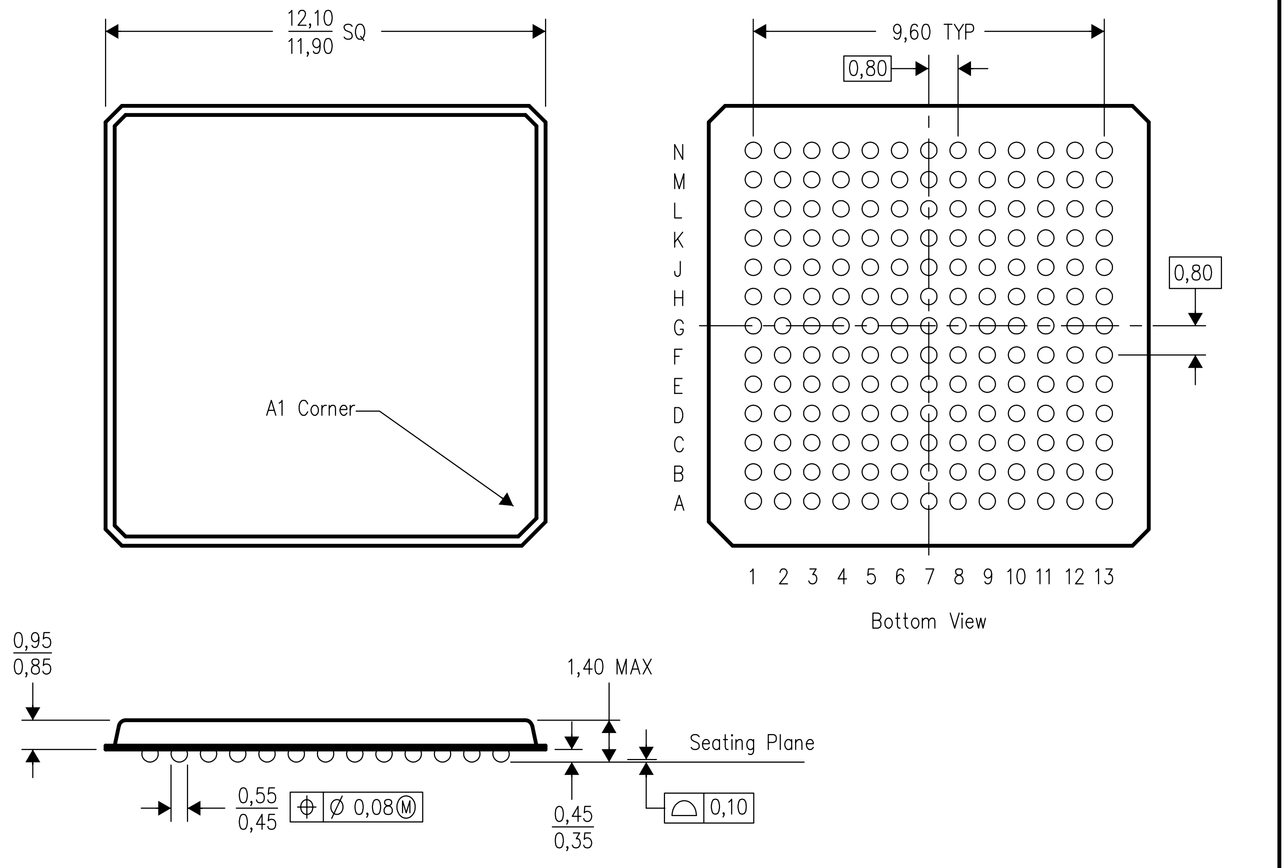
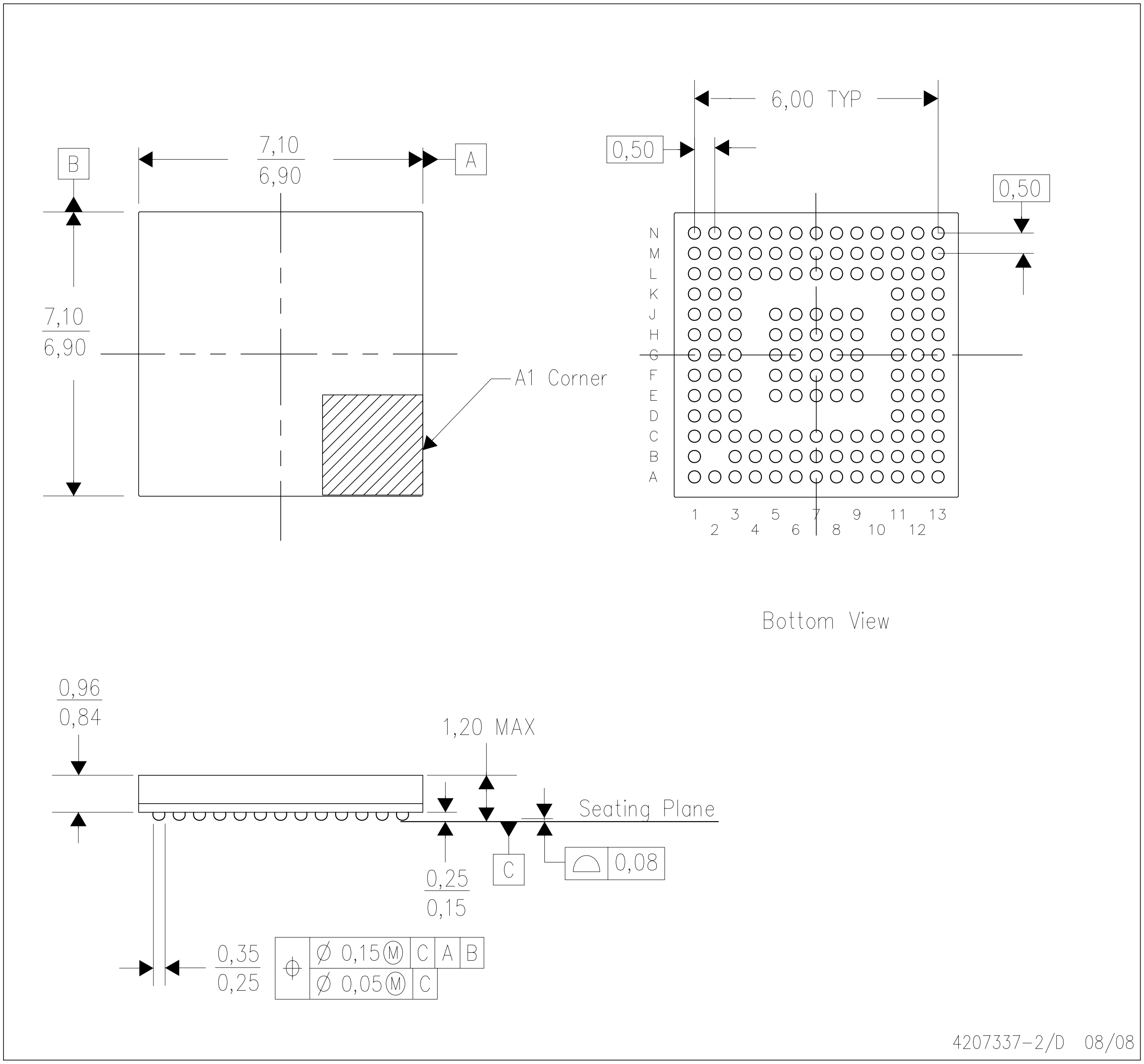
ZGU (S–PBGA–N169) PLASTIC BALL GRID ARRAY



4204394–3/B 07/05

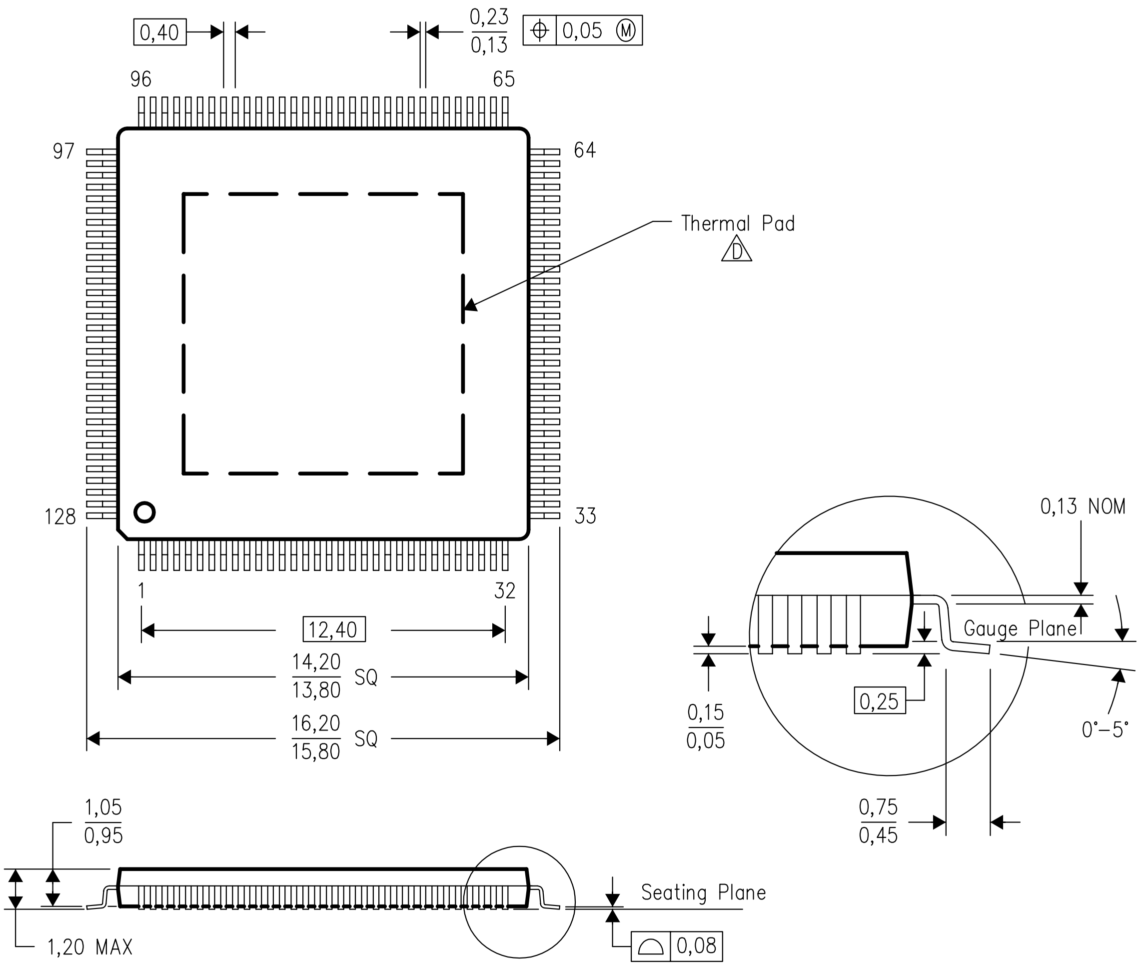
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Micro Star BGA configuration
- D. This is a lead–free solder ball design.

ZAJ (S–PBGA–N144) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. This is a Pb–free solder ball design.

PNP (S-PQFP-G128) PowerPAD™ PLASTIC QUAD FLATPACK



4146962/E 09/04

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

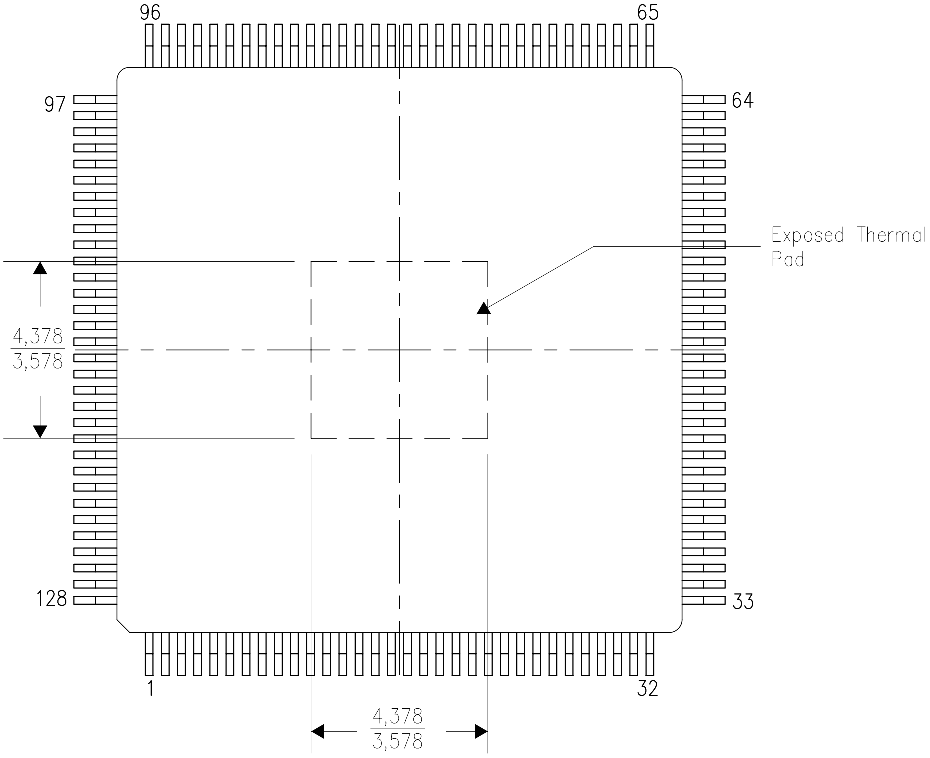
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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