To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

μPA1730TP

SWITCHING
P-CHANNEL POWER MOS FET

DESCRIPTION

The μPA1730TP which has a heat spreader is a P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

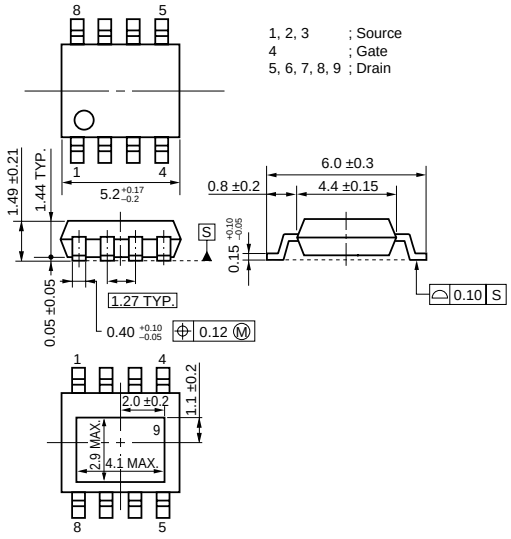
FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 9.5 mΩ MAX. (V_{GS} = –10 V, I_D = –6.5 A)
  $R_{DS(on)2}$ = 13.5 mΩ MAX. (V_{GS} = –4.5 V, I_D = –6.5 A)
  $R_{DS(on)3}$ = 15.0 mΩ MAX. (V_{GS} = –4.0 V, I_D = –6.5 A)
- Low C_{iss}: C_{iss} = 3800 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power HSOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1730TP	Power HSOP8

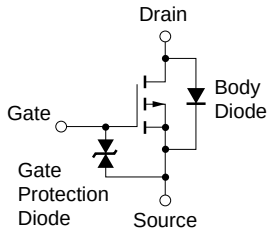
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Unless otherwise noted, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)1}$	∓28	A
Drain Current (DC) Note1	$I_{D(DC)2}$	∓15	A
Drain Current (pulse) Note2	$I_{D(pulse)}$	∓100	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	40	W
Total Power Dissipation (T_A = 25°C) Note1	P_{T2}	3	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note3	I_{AS}	–15	A
Single Avalanche Energy Note3	E_{AS}	22.5	mJ

EQUIVALENT CIRCUIT



Notes 1. Mounted on a glass epoxy board (1 inch x 1 inch x 0.8 mm), PW = 10 sec.
2. PW ≤ 10 μs, Duty Cycle ≤ 1%
3. Starting T_{ch} = 25°C, V_{DD} = –15 V, R_G = 25 Ω, V_{GS} = –20 → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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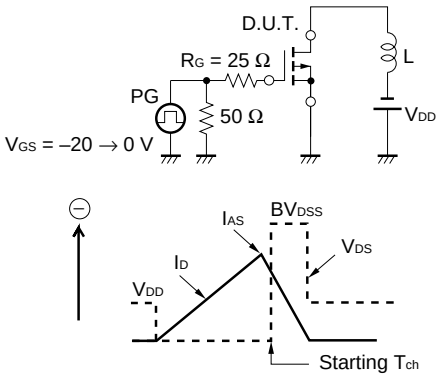
Date Published March 2002 NS CP(K)
Printed in Japan

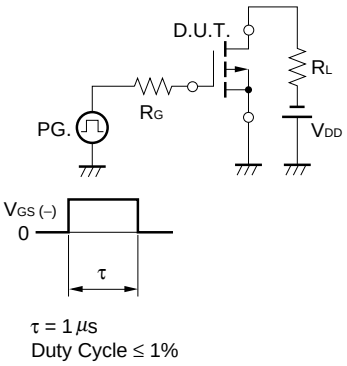
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, Unless otherwise noted, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–1.6	–2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –6.5 A	11.0	23.0		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –6.5 A		7.6	9.5	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –6.5 A		10.3	13.5	mΩ
	$R_{DS(on)3}$	V_{GS} = –4.0 V, I_D = –6.5 A		11.3	15.0	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		3800		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		1200		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		500		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –6.5 A		15		ns
Rise Time	t_r	V_{GS} = –10 V		20		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		130		ns
Fall Time	t_f			50		ns
Total Gate Charge	Q_G	V_{DD} = –24 V		70		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		9		nC
Gate to Drain Charge	Q_{GD}	I_D = –13.0 A		17		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 13 A, V_{GS} = 0 V		0.80		V
Reverse Recovery Time	t_{rr}	I_F = 13 A, V_{GS} = 0 V		53		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/ μs		57		nC

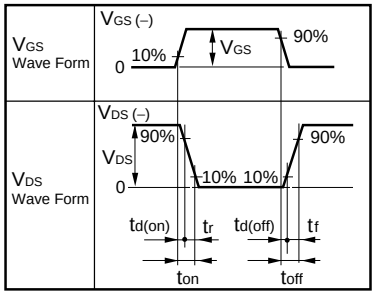
TEST CIRCUIT 1 AVALANCHE CAPABILITY



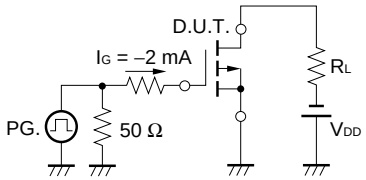
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

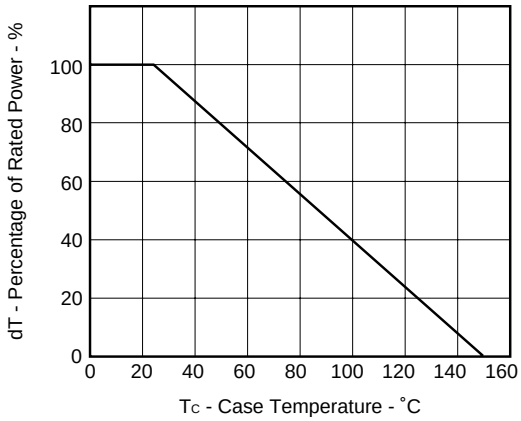


TEST CIRCUIT 3 GATE CHARGE

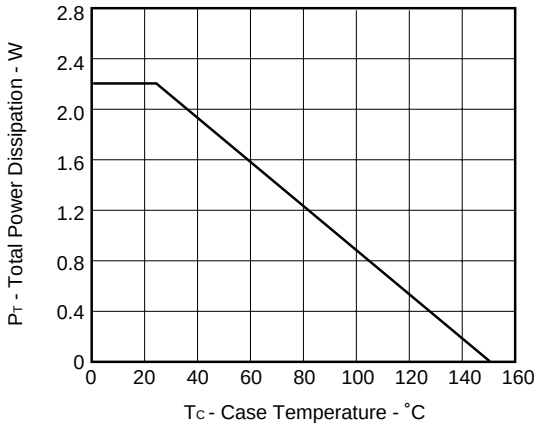


TYPICAL CHARACTERISTICS (T_A = 25°C)

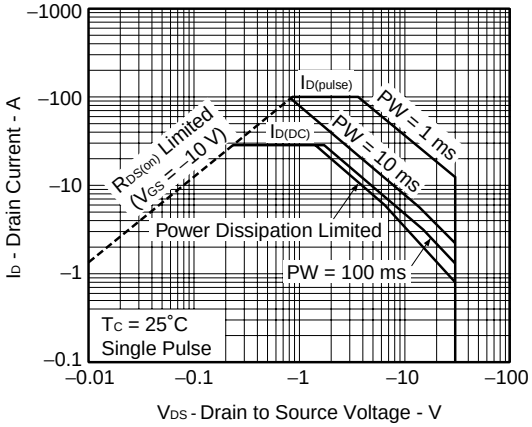
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



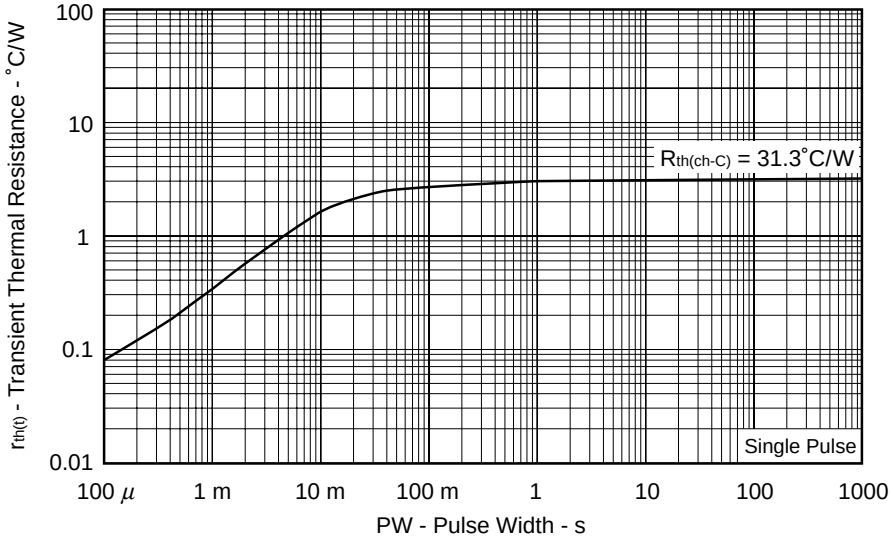
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



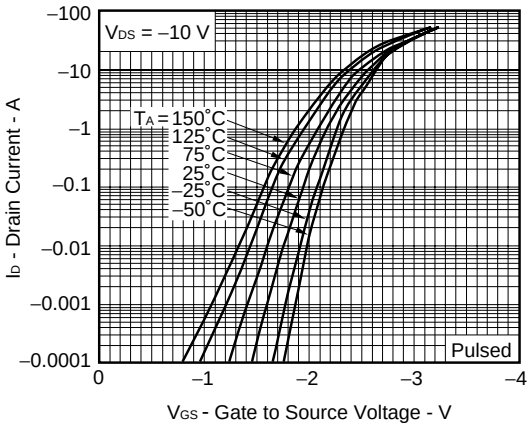
FORWARD BIAS SAFE OPERATING AREA



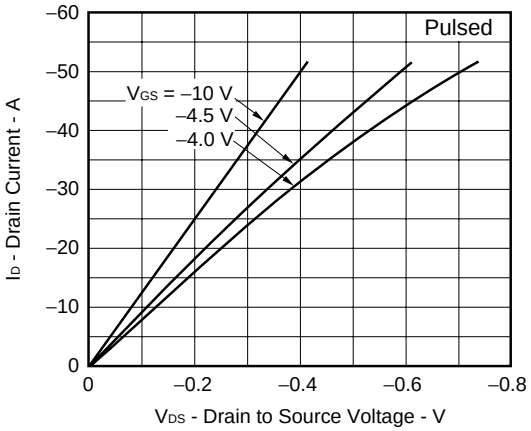
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



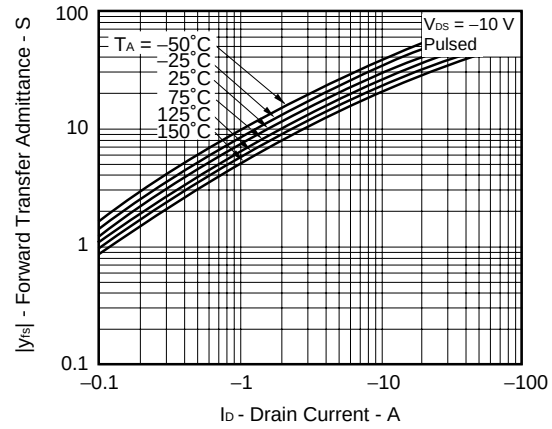
FORWARD TRANSFER CHARACTERISTICS



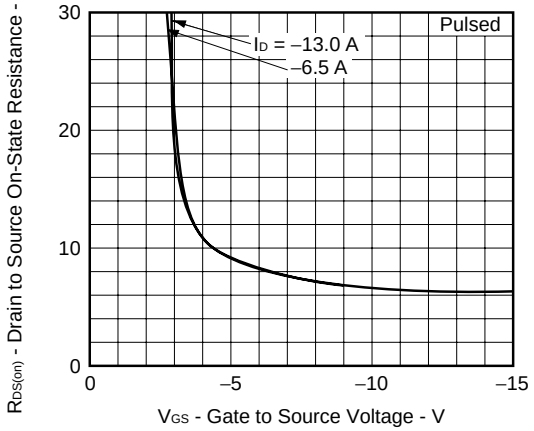
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



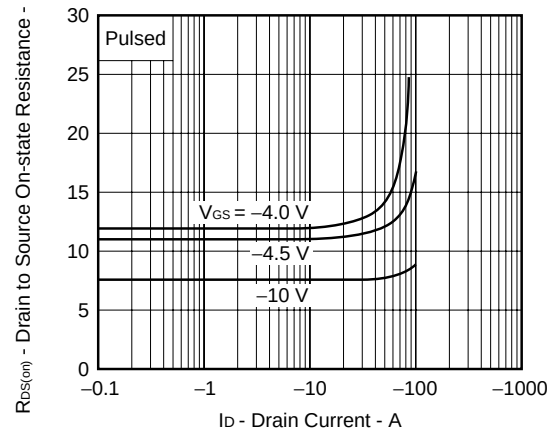
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



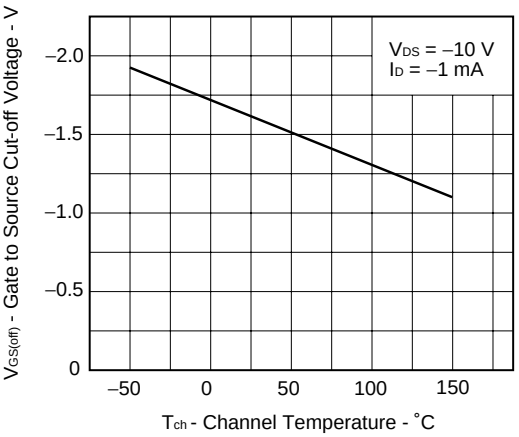
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



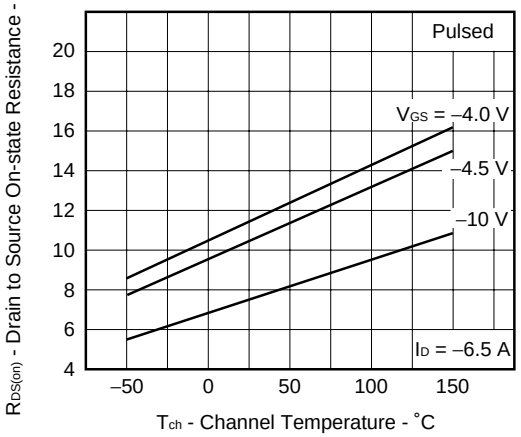
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



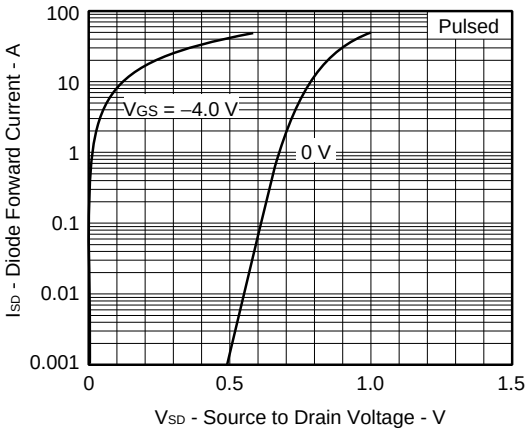
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



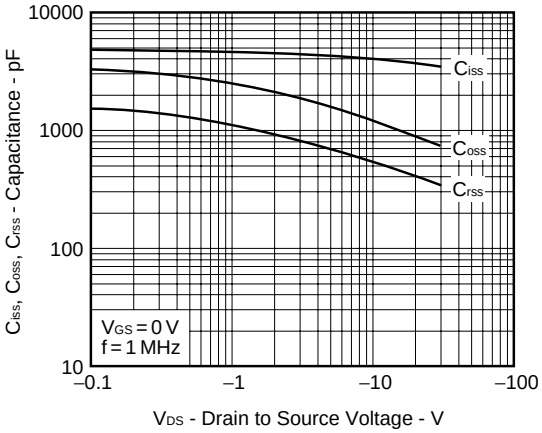
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



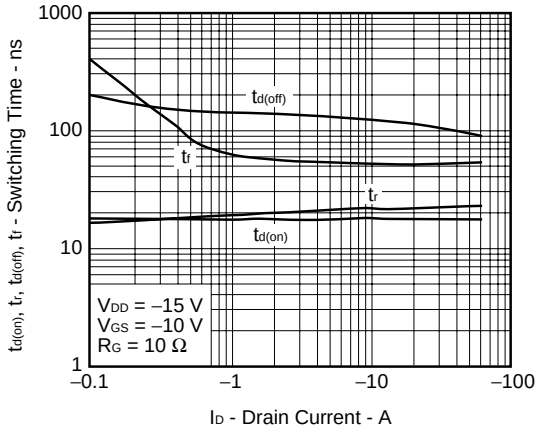
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



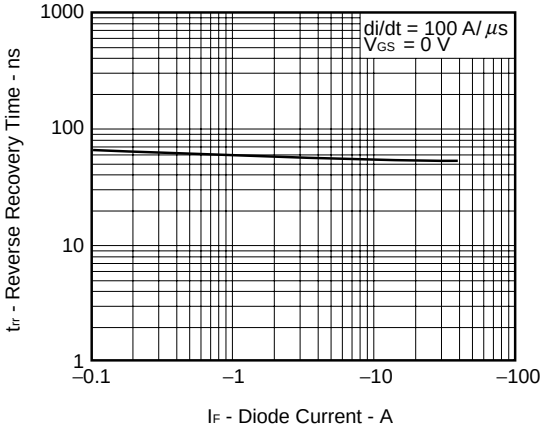
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



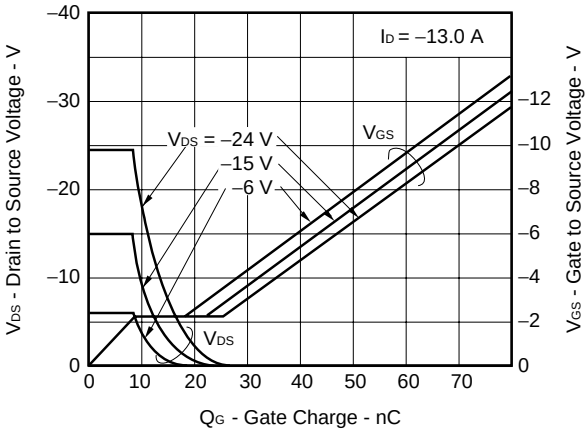
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



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