

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

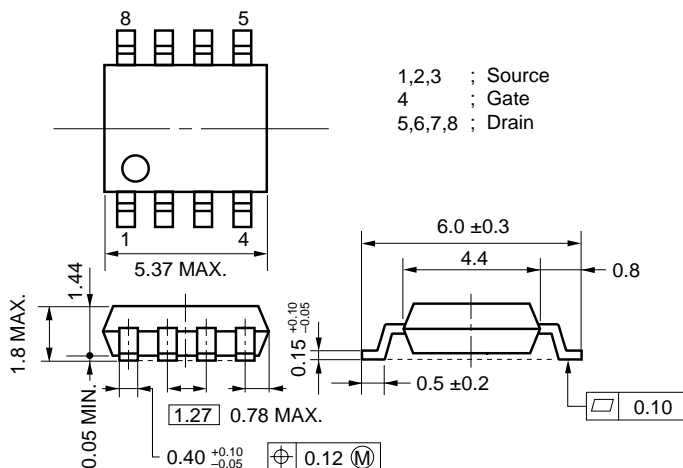
DESCRIPTION

The μ PA1722 is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

FEATURES

- Low on-resistance
 $R_{DS(on)1} = 21.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.5 \text{ A)}$
 $R_{DS(on)2} = 29.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4.5 \text{ A)}$
 $R_{DS(on)3} = 32.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 4.5 \text{ A)}$
- Low C_{iss} : $C_{iss} = 980 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



ORDERING INFORMATION

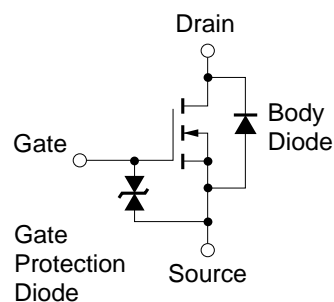
PART NUMBER	PACKAGE
μ PA1722G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	± 20	V
Drain Current (DC)	I _{D(DC)}	± 9	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	± 36	A
Total Power Dissipation (T _A = 25°C) ^{Note2}	P _T	2.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

- Notes** 1. $PW \leq 10 \mu s$, Duty Cycle $\leq 1 \%$
 2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm

EQUIVALENT CIRCUIT



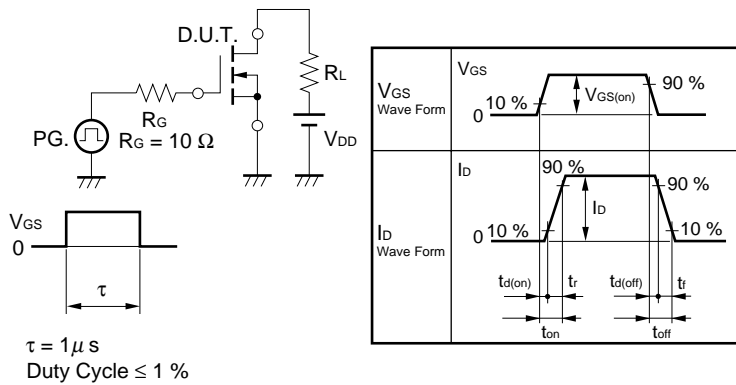
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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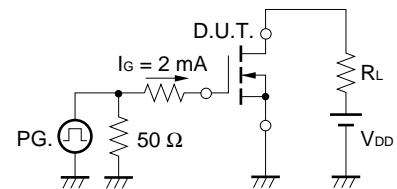
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.5 A		14.0	21.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.5 A		19.0	29.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 4.5 A		22.0	32.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.5 A	5.0	9.2		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = 10 V		980		pF
Output Capacitance	C _{oSS}	V _{GS} = 0 V		320		pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		125		pF
Turn-on Delay Time	t _{d(on)}	I _D = 4.5 A		20		ns
Rise Time	t _r	V _{GS(on)} = 10 V		80		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 15 V		60		ns
Fall Time	t _f	R _G = 10 Ω		30		ns
Total Gate Charge	Q _G	I _D = 9 A		20		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V		2.3		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		6.0		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 9 A, V _{GS} = 0 V		0.84		V
Reverse Recovery Time	t _{rr}	I _F = 9 A, V _{GS} = 0 V		35		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		45		nC

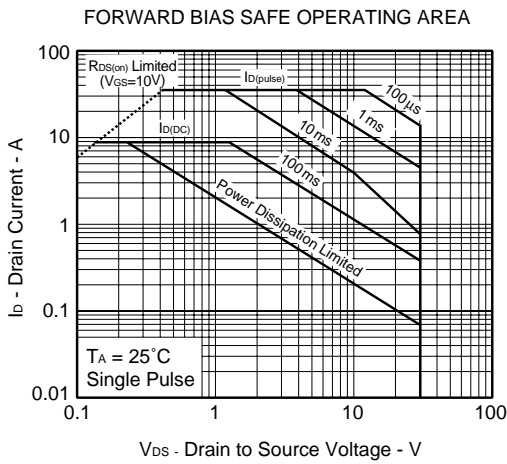
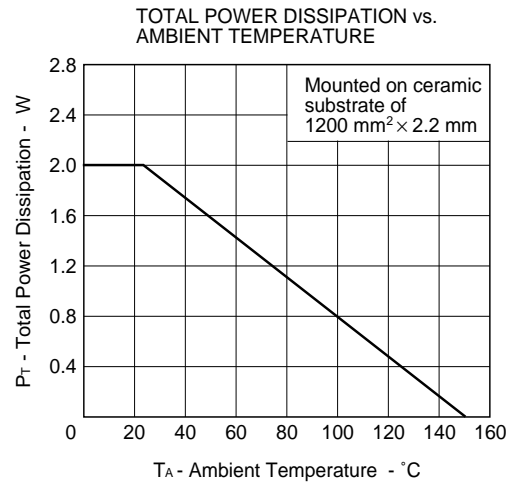
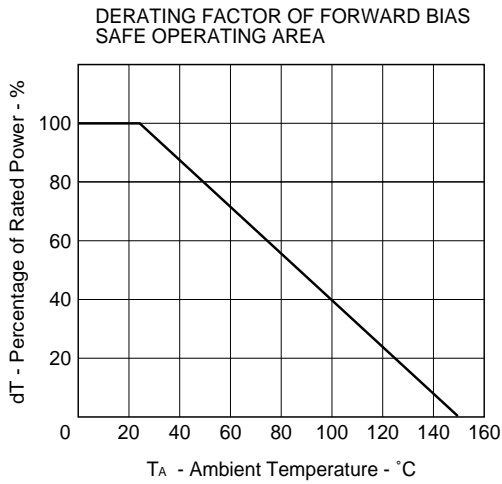
TEST CIRCUIT 1 SWITCHING TIME



TEST CIRCUIT 2 GATE CHARGE

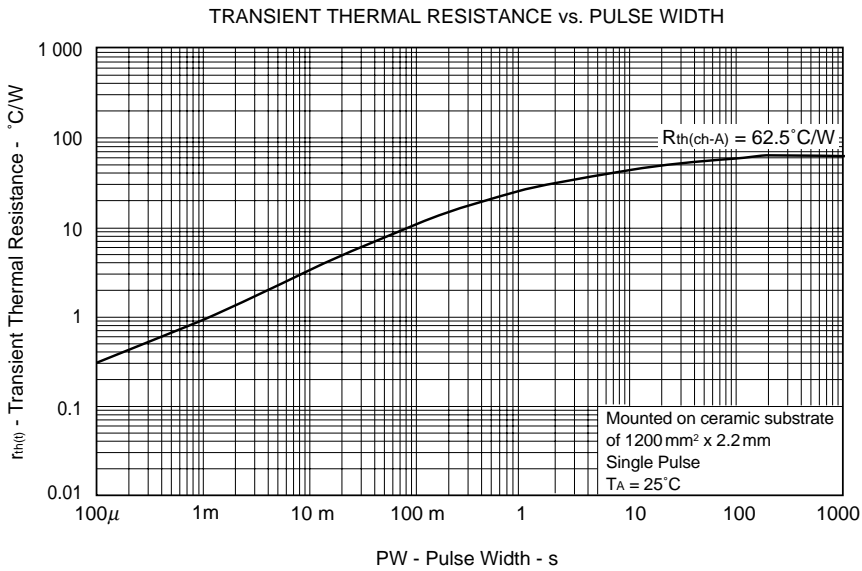


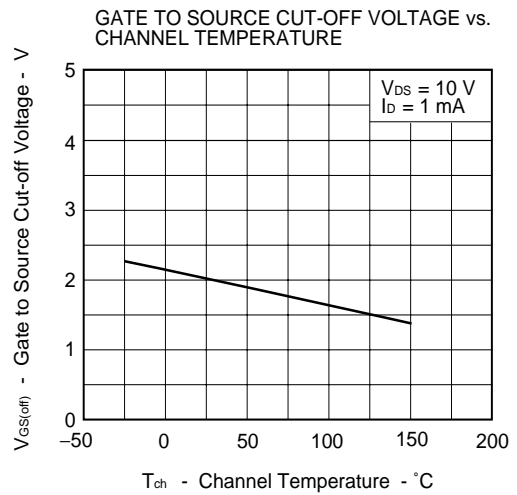
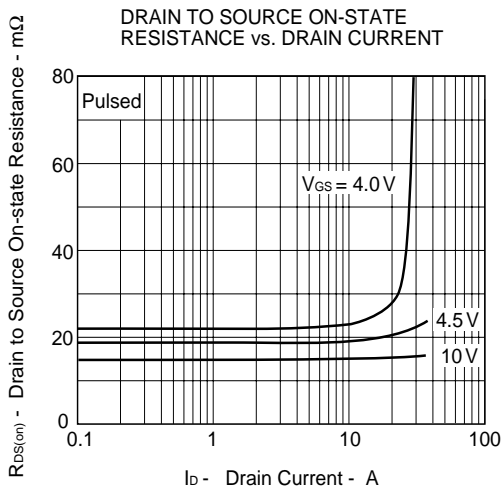
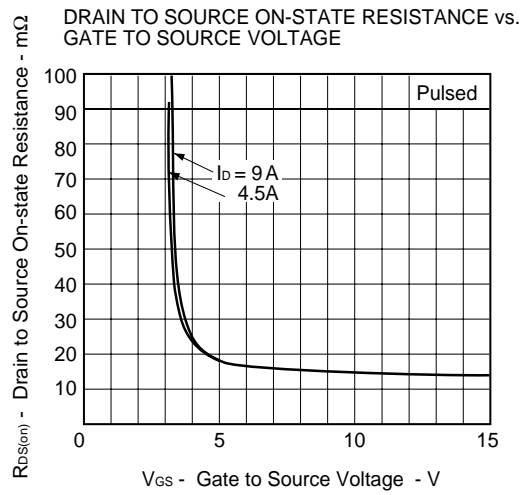
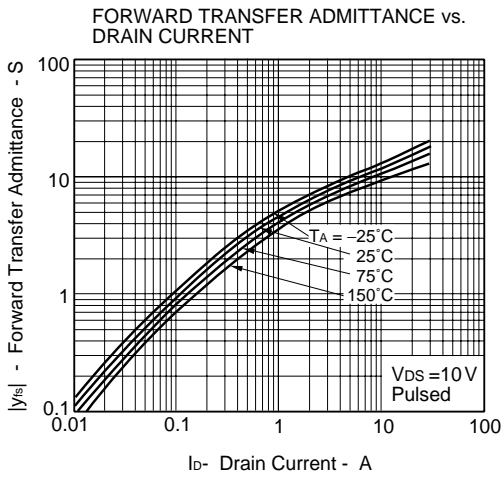
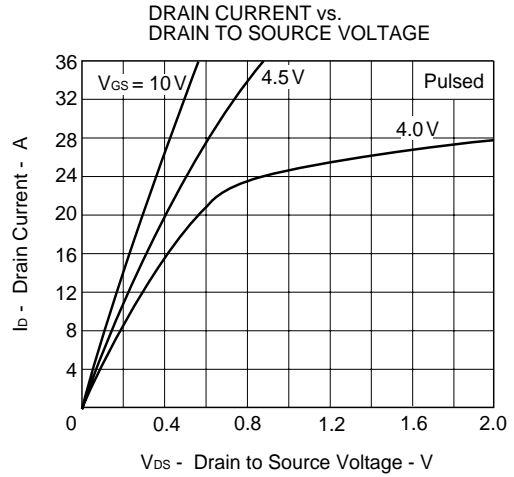
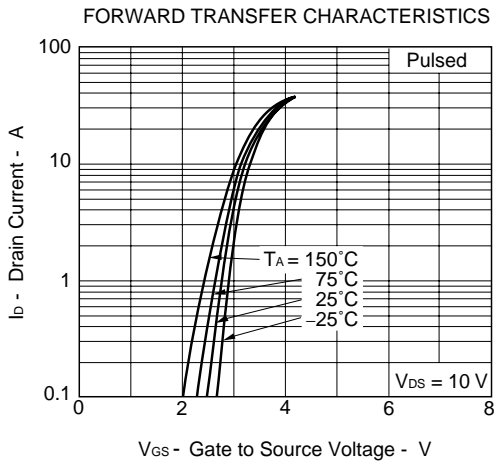
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



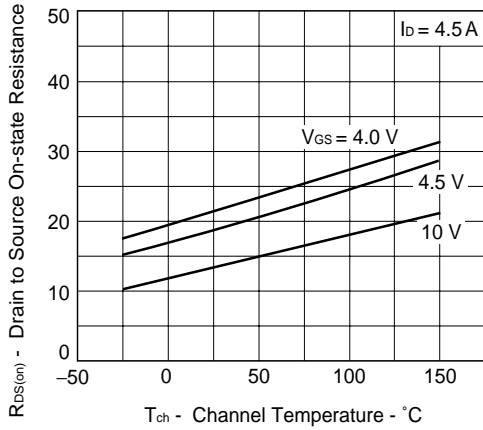
Remark

Mounted on ceramic substrate of $1200\text{ mm}^2 \times 2.2\text{ mm}$

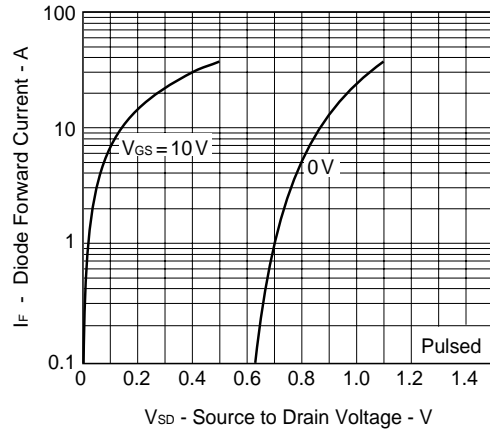




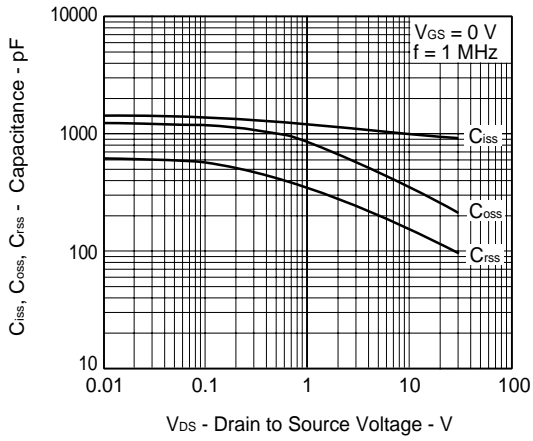
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



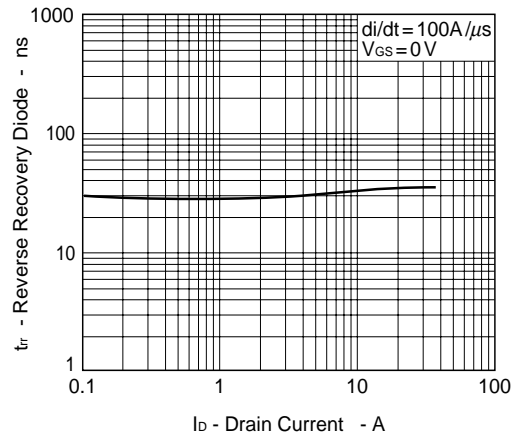
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



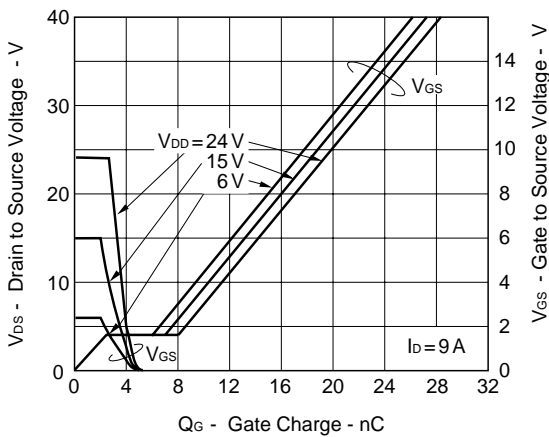
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



[MEMO]

[MEMO]

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