Product Brief
October 2001

TDCS6440G SONET/SDH 40 Gbits/s Cross Connect

Features

- Versatile IC which supports an aggregate bandwidth of 40 Gbits/s.
- Supports flexible 64-port STS-12 data links.
- Supports full nonblocking fabric with switching granularity of STS-1/STM-1.
- Support for line/path switching.
- Supports any valid mix of STS-1 and concatenated payloads from STS-3c to STS-192c.
- Provides a standard 5-pin P1149.1 JTAG port with memory BIST scan, and boundary scan.
- Low-power 1.5 V operation with 3.3 V inputs and outputs.
- Configurable on-chip TSI block for switching of STS-1s.
- On-chip connection memory for flexible configuration of working connections and protect connections for each STS-1.
- 792-pin LBGA package.
- –40 °C to +85 °C industrial temperature range.

Interface

- Provides 64 STS-12 interfaces which can be used as 16 STS-48 interfaces or as 4 STS-192 interfaces.
- Robust receiver interface capable of handling STS-12 streams having combined static- and dynamic-frame offsets of up to 24 bytes without creating traffic disruption.
- Frames to and performs integrity check on each STS-12 interface.
- Each STS-12 input interface consists of an LVDS data input with integral clock and data recovery (CDR).
- Each STS-12 output interface consists of an LVDS output.
- Ability to insert on an AIS-L or pass-through when an LOF condition occurs.
- Interfaces have A1/A2 framing, link trace, parity, and a communications link.

Cross Connect

- Supports up to 768 STS-1 time slots.
- 64 input channels and 64 output channels.
- Each input time slot can be connected to any/all output time slots.
- Each output time slot can be connected to any input time slot or be assigned AIS-P or UNEQ-P.
- Fully programmable and nonblocking cross connect.
- Supports drop-and-continue and full broadcast capabilities.
- Ability to insert path AIS and UNEQ indications on any STS-1 under software control.

Protection Switching

- Supports 1 + 1, 1:1, 1:N, UPSR, and BLSR protection mechanisms with four-connection memory.
- Separate line and path protection mechanisms.
- Supports equipment protection switching.
- On-chip working/protected memory paths for easy switch configurations.

Microprocessor Interface

- Microprocessor interface supports both synchronous and asynchronous operations.
- 16-bit wide data bus interface and 13-bit wide address bus.

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Applications

- SONET/SDH digital cross connect equipment.
- SONET/SDH add-drop multiplex equipment.
- High-speed core switches.
- SONET/SDH test equipment.
- TDCS6440G will interface seamlessly to a number of Agere Systems Inc.'s existing/next-generation high-speed framers.

Description

The TDCS6440G has four sections: receive interface channels, a cross connect fabric core, transmit channels, and a microprocessor interface. The block diagram of the TDCS6440G is shown in Figure 1.

All data stream channels must be synchronous in frequency, but can be asynchronous in phase.

The TDCS6440G does not perform pointer processing functions. These are performed by the line and tributary cards, which align the payload at known positions relative to a common frame signal.

The TDCS6440G performs SONET and SDH cross connect functions.

The A1, A2, B1, H1, H2, H3, K1, and K2 bytes are used for their original SONET/SDH purposes.

Note: Throughout this document, the term channel always refers to an STS-12 data stream that is carried on a single LVDS link.

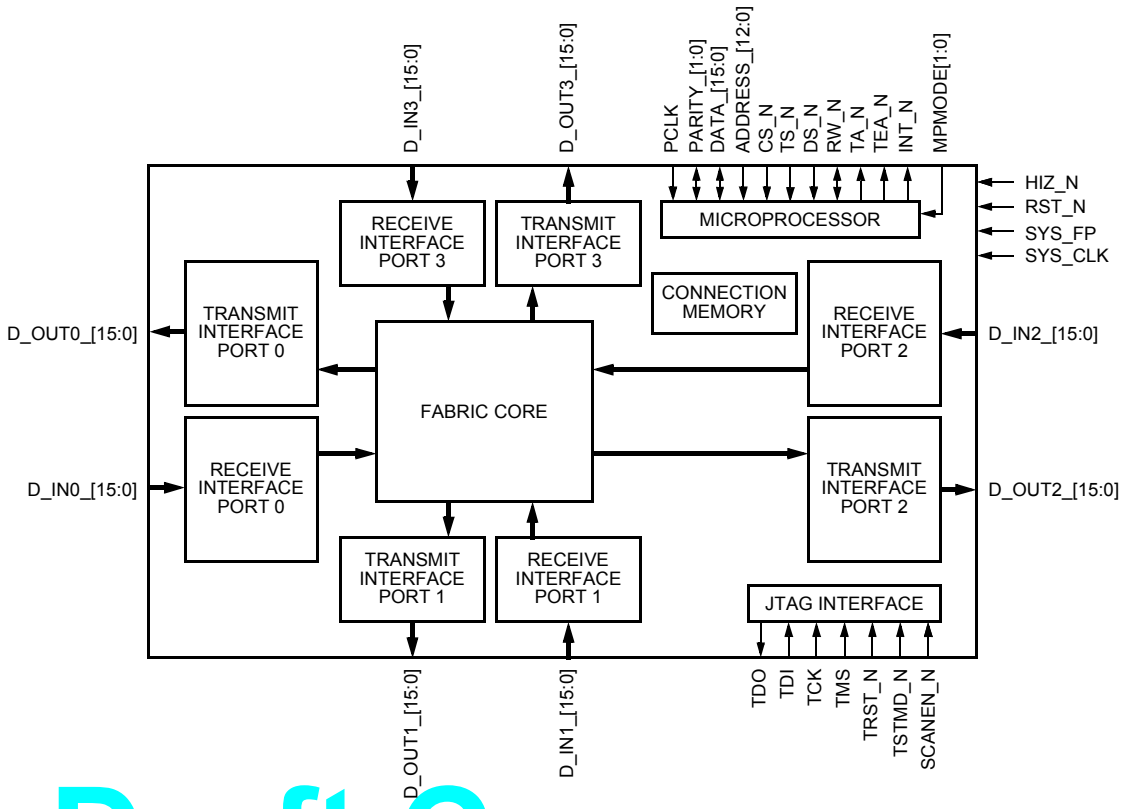

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Figure 1. TDCS6440G Block Diagram

Description (continued)

Supervisory Features

Supervisory features built into the TDCS6440G provide diagnostic capabilities and fault coverage.

- TOH serial port integrity
- Frame pulse integrity
- LVDS link integrity
- Framer monitoring
- FIFO aligner monitoring
- Frame offset monitoring
- Microprocessor interface monitoring

Test Features

Test features built into the LVDS transceivers are a key element in providing testing and debugging capabilities for the many aspects of chip level, board level, and system level functionality.

- A1/A2 error insert
- B1 error insert
- Scrambler/descrambler disable
- TOH serial output port parity error insert

Software Reset

An asynchronous software reset is provided. The software reset is self-clearing, and resets the whole device.

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