TOSHIBA BI-DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM8GZ47, SM8JZ47, SM8GZ47A, SM8JZ47A

AC POWER CONTROL APPLICATIONS

- Repetitive Peak Off-State Voltage: VDRM = 400V, 600V
- R.M.S On-State Current: IT (RMS) = 8A
- High Commutating (dv / dt)
- Isolation Voltage: VISOL = 1500V AC

ABSOLUTE MAXIMUM RATINGS

CHARACTERIS	SYMBOL	RATING	THAU	
Repetitive Peak	SM8GZ47 SM8GZ47A	. V _{DRM}	400	
Off-State Voltage	SM8JZ47 SM8JZ47A	V DRM	600	
R.M.S On-State Current (Full Sine Waveform To	-	I _{T (RMS)}	8	> A
Peak One Cycle Surge Current (Non-Repetitive		I _{TSM}	80 (50Hz) 88 (60Hz)	A
I ² t Limit Value		I ² t	32	$\left\langle A^{2}s\right\rangle$
Critical Rate of Rise of C Current	n-State (Note 1)	di / dt	50	A / µs
Peak Gate Power Dissip	ation	PGM	5 <	\ W
Average Gate Power Dis	ssipation	PG (AV)	0.5	¥
Peak Gate Voltage		VGM	10	>
Peak Gate Current		◯ l _{GM}	2	A
Junction Temperature /) 	-40~125	°C
Storage Temperature Ra	T _{stg}	-40~125	°C	
Isolation Voltage (AC, t =	= 1min.)	VISOL	1500	٧

Weight: 1.7 g (typ.)

Note 1: di / dt Test Condition V_{DRM} = 0.5×Rated

> I_{TM} ≤ 12A t_{gw} ≥ 10μs

t_{gr} ≤ 250ns

 $iGP = IGT \times 2.0$

Note 2. Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHAF	RACTERIST	IC	SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Repetitive Peak (Current	Off-State		I _{DRM}	V _{DRM} = Rated		_	_	20	μΑ
		I	V _{GT} V _D =	V _D = 12V	T2 (+), Gate (+)	1	_	1.5	- V
		II			T2 (+), Gate (-)	À	_	1.5	
		III		$R_L = 20\Omega$	T2 (-), Gate (-)	(7	1.5	
		IV			T2 (-), Gate (+)		Ú –		
		I			T2 (+), Gate (+)	<u> </u>	_	30	- mA
Gate Trigger Current	SM8GZ4			V _D = 12V R _L = 20Ω	T2 (+), Gate (-)		_	30	
	SM8JZ47	, III			T2 (-), Gate (-)		_	30	
		IV	- I _{GT}		T2 (-), Gate (+)	1		-	
		I			T2(+), Gate (+)	_	4	20	
	SM8GZ4				T2 (+), Gate (-)	- [> -	20	
	SM8JZ47A	'A III			√√√2 (¬), Gate (−)	+(20	
		IV			T2 (-), Gate (+)	()	4	/ _	-
Peak On-State Voltage		V _{TM}	I _{TM} = 12A			\supset	1.5	V	
Gate Non-Trigge	er Voltage		V_{GD}	V _D = Rated, Tc = 125°C		0.2	_	_	V
Holding Current			I _H	$V_D = 12V$, $I_{TM} = 1A$			_	50	mA
Thermal Resistar	nce		R _{th (j-c)}	Junction to Case, AC) –	_	3.6	°C/W
Critical Rate of Rise of Off-State Voltage SM8GZ47 SM8JZ47 SM8JZ47A		dv / dt		P _{DRM} = Rated, T _J = 125°C		300	-	V / μs	
				Exponential Rise		-	200	_	ν / μ3
Critical Rate of SM8GZ47 SM8JZ47			(dv / dt) c	V _{DRM} = 400V, T = 125°C (di /dt) c = -4.5AV ms		10	_		- V / μs
Voltage at Commutation		SM8GZ47A SM8JZ47A				4	_	_	

MARKING

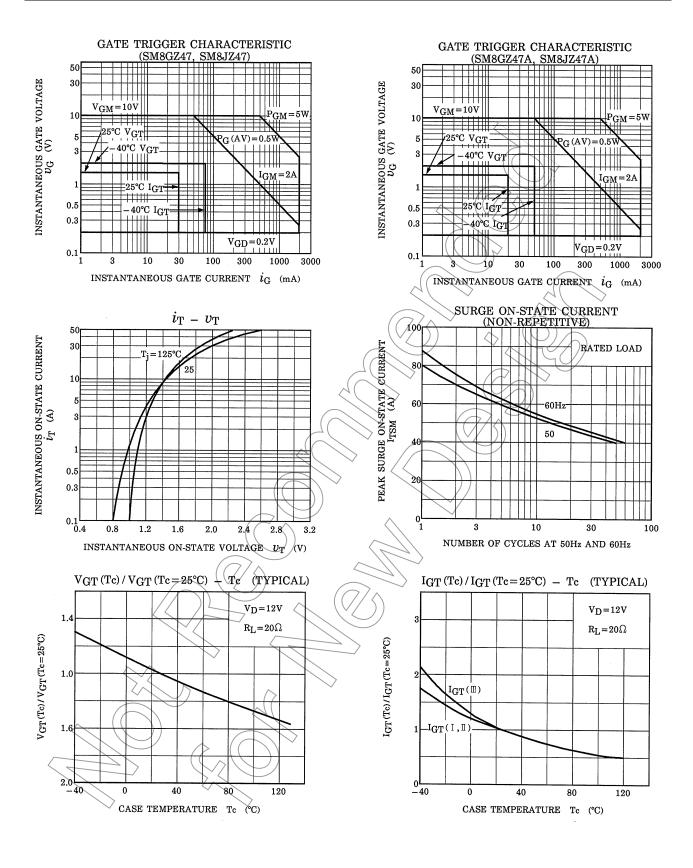


indicator*2

Part No. (or abbreviation code) *1 Lot No.

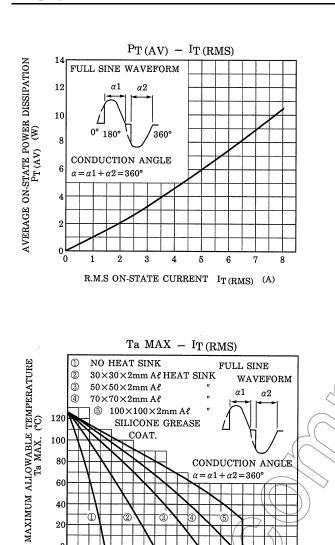
	Part No. (or abbreviation code)	Part No.
*1	M8GZ47	SM8GZ47, SM8GZ47A
•	'	SM8JZ47, SM8JZ47A
*2	Nothing	SM8GZ47, SM8JZ47
• 2	A	SM8GZ47A, SM8JZ47A

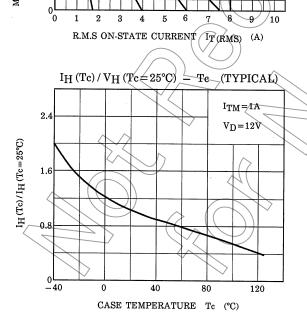
A line indicates
lead (Pb)-free package o
lead (Pb)-free finish.

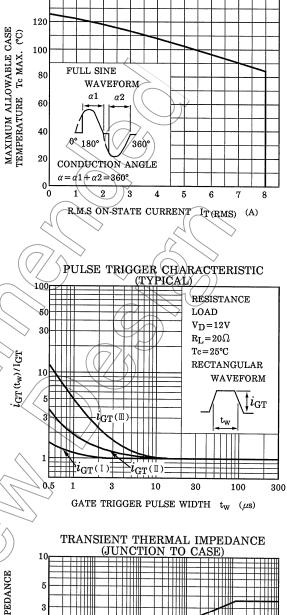


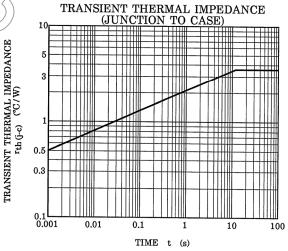
140

Tc MAX - IT (RMS)









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