General Description

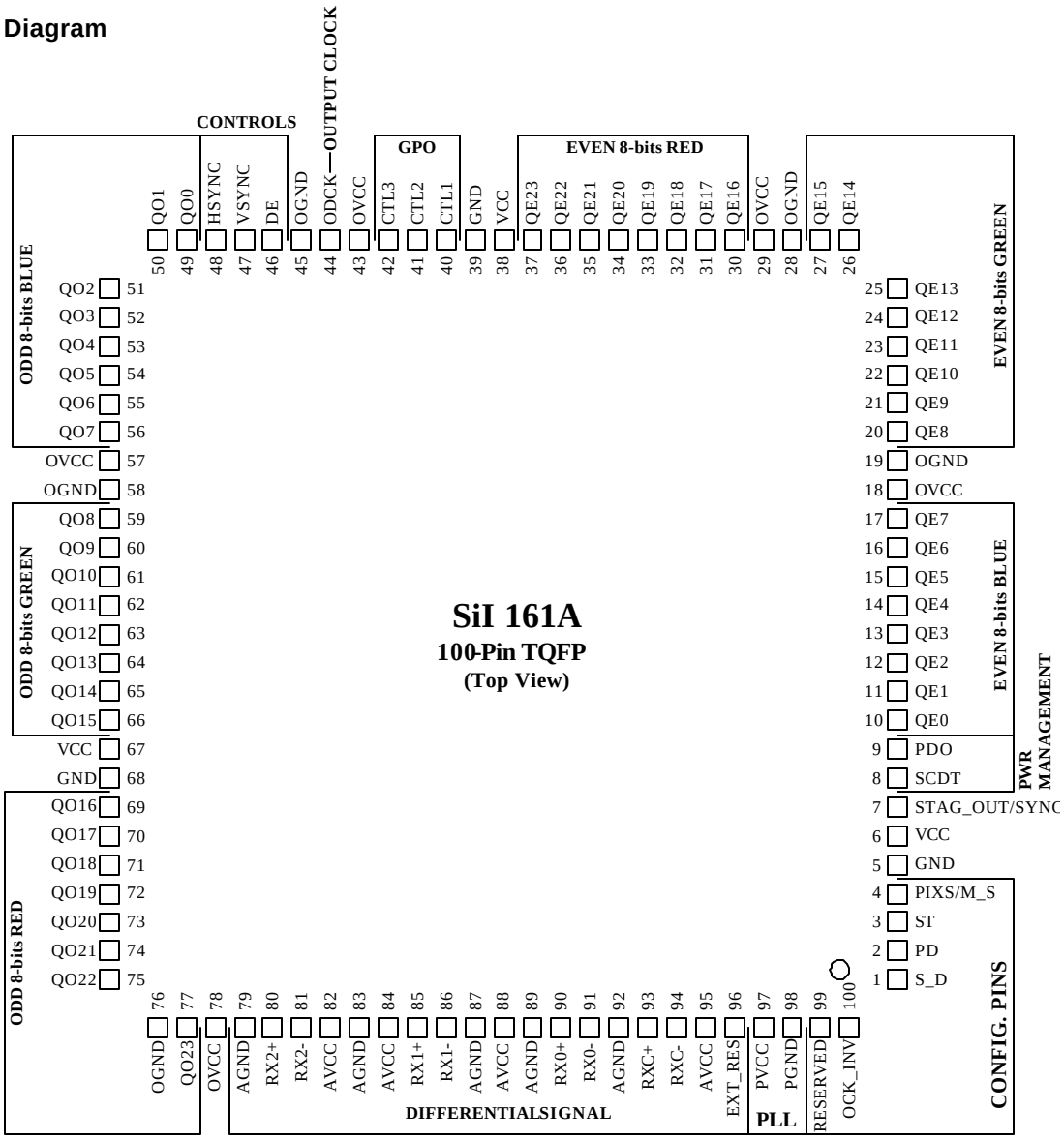
The SiI 161A receiver uses PanelLink Digital technology to support high resolution displays up to UXGA. The SiI 161A receiver supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode. In addition, the receiver data output is time staggered to reduce ground bounce that affects EMI. Since all PanelLink products are designed on scaleable CMOS architecture to support future performance requirements while maintaining the same logical interface, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

PanelLink Digital technology simplifies PC and display interface design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

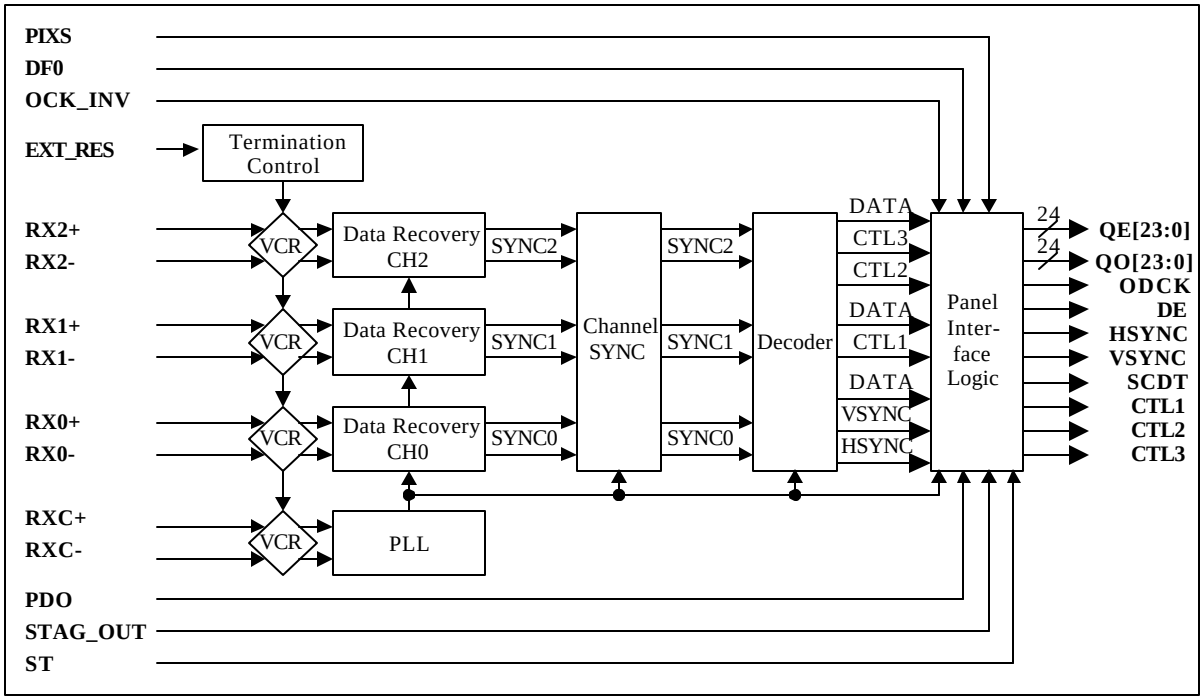
Features

- Low Power: 3.3V core operation
- Time staggered data output for reduced ground bounce
- Sync Detect: for Plug & Display "Hot Plugging"
- Cable Distance Support: over 5m with twisted-pair, fiber-optics ready
- Compliant with DVI 1.0 (DVI is backwards compatible with VESA® P&D™ and DFP)
- Supports Dual-Link operation up to 330 Mega-pixels/second

SiI 161A Pin Diagram



Functional Block Diagram



Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage 3.3V	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{CC}+ 0.3	V
V_O	Output Voltage	-0.3		V_{CC}+ 0.3	V
T_A	Ambient Temperature (with power applied)	-25		105	°C
T_{STG}	Storage Temperature	-65		150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		21		°C/W

Notes: [1] Permanent device damage may occur if absolute maximum conditions are exceeded.
[2] Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND -0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	µA

Note: [1] Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3 ns or one third of the clock cycle.

DC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OHD}	Output High Drive Data and Controls	V_{OUT} = 2.4 V; ST = 1 ST = 0	4.2 2.1	8 4	18 9	mA
I_{OLD}	Output Low Drive Data and Controls	V_{OUT} = 0.8 V; ST = 1	-7	-11	-15	mA
		V_{OUT} = 0.4 V; ST = 1 ST = 0	-5.2 -2.6	-5.5 -2.8	-11 -5.5	mA
I_{OHC}	ODCK, DE High Drive	V_{OUT} = 2.4 V; ST = 1 ST = 0	8.5 4.2	17 9	37 18	mA
I_{OLC}	ODCK, DE Low Drive	V_{OUT} = 0.8V; ST = 1	-15	-20	-25	mA
		V_{OUT} = 0.4 V; ST = 1 ST = 0	-10.4 -5.2	-16 -8	-23 -11	mA
V_{ID}	Differential Input Voltage Single Ended Amplitude		75		1000	mV
I_{PD}	Power-down Current[2]				1	mA
I_{CCR}	Receiver Supply Current	ODCK=82.5MHz, 2-pixel/clock mode C_{LOAD}= 10pF R_{EXT_SWING} = 510Ω Typical Pattern[3]		240	270	mA
		ODCK=82.5MHz, 2-pixel/clock mode C_{LOAD} = 10pF R_{EXT_SWING} = 510Ω Worst Case Pattern[4]		270	330	mA
I_{PDO}	Receiver Supply Current with Ouputs Powered Down	ODCK=82.5MHz, 2-pixel/clock mode C_{LOAD} = 10pF R_{EXT_SWING} = 510Ω Worst Case Pattern[4]		240		mA

Notes: [1] Guaranteed by design.

[2] The transmitter must be in power-down mode, powered off, or disconnected for the current to be under this maximum.

[3] The Typical Pattern contains a gray scale area, checkerboard area, and text.

[4] Black and white checkerboard pattern, each checker is two pixel wide.

AC Specifications

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]	165MHz			245	ps
T_{CCS}	Channel to Channel Differential Input Skew[1]	165MHz			4	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter tolerance[2,3]	65 MHz			465	ps
		112 MHz			270	ps
		165 MHz			182	ps
D_{LHT}	Low-to-High Transition Time: Data and Controls (70 C, 82.5 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			2.6	ns
		C_L = 5pF; ST = 0			2.7	ns
	Low-to-High Transition Time: Data and Controls (70 C, 165 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			2.4	ns
		C_L = 5pF; ST = 0			3.0	ns
	Low-to-High Transition Time: ODCK (70 C, 82.5 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			1.3	ns
		C_L = 5pF; ST = 0			1.7	ns
	Low-to-High Transition Time: ODCK (70 C, 165 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			1.4	ns
		C_L = 5pF; ST = 0			1.7	ns
D_{HLT}	High-to-Low Transition Time: Data and Controls (70 C, 82.5 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			2.8	ns
		C_L = 5pF; ST = 0			3.4	ns
	High-to-Low Transition Time: Data and Controls (70 C, 165 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			2.3	ns
		C_L = 5pF; ST = 0			3.3	ns
	High-to-Low Transition Time: ODCK (70 C, 82.5 MHz, 2-pixel/clock, PIXS=1)	C_L = 10pF; ST = 1			1.1	ns
		C_L = 5pF; ST = 0			1.5	ns
	High-to-Low Transition Time: ODCK (70 C, 165 MHz, 1-pixel/clock, PIXS=0)	C_L = 10pF; ST = 1			1.2	ns
		C_L = 5pF; ST = 0			1.5	ns
T_{SETUP}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Setup Time to ODCK falling edge (OCK_INV = 0) or to ODCK rising edge (OCK_INV = 1) at 165 MHz *OCK_INV = 1	C_L = 10pF; ST = 1	0.7 *0.7			ns
		C_L = 5pF; ST = 0	0.7 *0.4			ns
T_{HOLD}	Data, DE, VSYNC, HSYNC, and CTL[3:1] Hold Time from ODCK falling edge, (OCK_INV = 0) or from ODCK rising edge (OCK_INV = 1) at 165 MHz, *OCK_INV = 0	C_L = 10pF; ST = 1	3.8 *3.8			ns
		C_L = 5pF; ST = 0	4.2 *3.8			ns

Notes:
1. Guaranteed by design.
2. Jitter defined as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures*.
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured when transmitter was powered down (see SiI /AN-0005 “PanelLink Basic Design/Application Guide,” Section 2.4).

AC Specifications *(continued)*

Under normal operating conditions unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{CIP}	ODCK Cycle Time[1] (1-pixel/clock)		6.06		40	ns
F_{CIP}	ODCK Frequency[1] (1-pixel/clock)		25		165	MHz
R_{CIP}	ODCK Cycle Time[1] (2-pixels/clock)		12.1		80	ns
F_{CIP}	ODCK Frequency[1] (2-pixels/clock)		12.5		82.5	MHz
R_{CIH}	ODCK High Time[4] (165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF; ST = 1	1.7			ns
		C_L = 5pF; ST = 0	1.3			ns
R_{CIL}	ODCK Low Time[4] (165MHz, 1-pixel/clock, PIXS = 0)	C_L = 10pF; ST = 1	2.0			ns
		C_L = 5pF; ST = 0	1.4			ns
T_{PDL}	Delay from PD Low to high impedance outputs[1]				10	ns
T_{HSC}	Link disabled (DE inactive) to SCDT low[1]			100		ms
	Link disabled (Tx power down) to SCDT low[5]				250	ms
T_{FSC}	Link enabled (DE active) to SCDT high[1]			25	40	DE edges
T_{ST}	ODCK high to even data output[1]			0.25		R_{CIP}

Notes:
1. Guaranteed by design.
2. Jitter defined as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electrical Measurement Procedures*.
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured when transmitter was powered down (see SiI/AN-0005 "*PanelLink Basic Design/Application Guide*," Section 2.4).

Setup and Hold Timings for data rates other than 165 MHz:

The measurements shown above are minimum setup and hold timings based on the maximum data rate of 165 MHz. To estimate the setup and hold times for slower data rates (for either different resolutions or 2 pixel per clock mode), the following formula can be used:

Time (at new frequency) = Time (165 MHz) + (Clock Period at new frequency – Clock Period at 165 MHz)/2

For the case of high strength output (ST=1) with a 10 pf load, and using the standard ODCK (ODCK_INV = 0), the table below shows the minimum set up and hold times for other speeds as follows:

Data Rate (MHz)	Clock (ns)	Setup (ns)	Hold (ns)	
165	6.06	0.70	3.80	UXGA 1 pixel/clock
112	8.93	2.13	5.23	SXGA 1 pixel/clock
82.5	12.12	3.73	6.83	UXGA 2 pixels/clock
56	17.86	6.60	9.70	SXGA 2 pixels/clock

Timing Diagrams

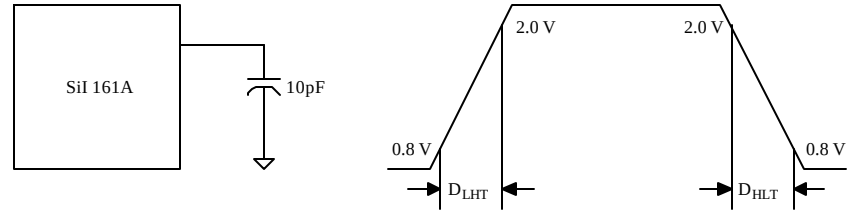


Figure 1. Digital Output Transition Times

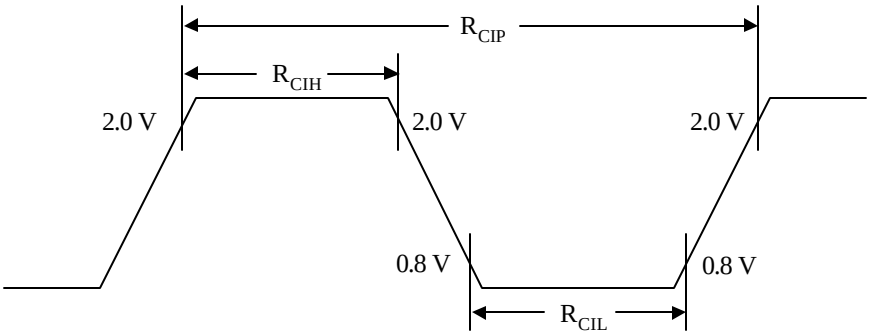


Figure 2. Receiver Clock Cycle/High/Low Times

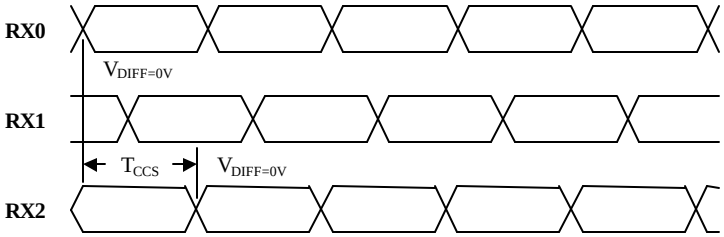


Figure 3. Channel-to-Channel Skew Timing

Output Timing

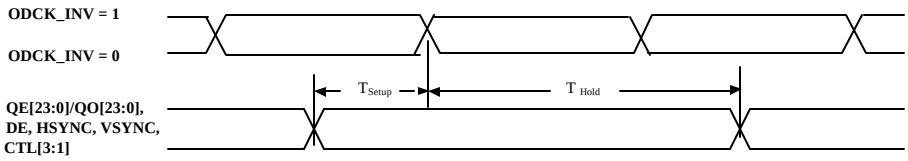


Figure 4. Output Data, DE, and Control Signals Setup/Hold Times to ODCK Falling Edge when ODCK_INV=0, or ODCK Rising Edge when ODCK_INV = 1.

Output Timing *(continued)*

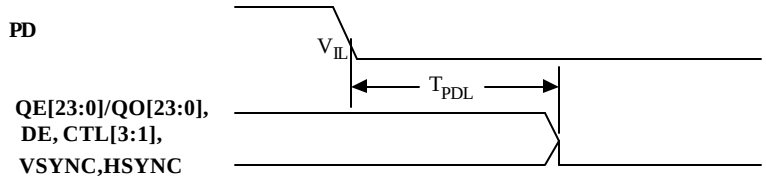


Figure 5. Output Signals Disabled Timing from PD Active

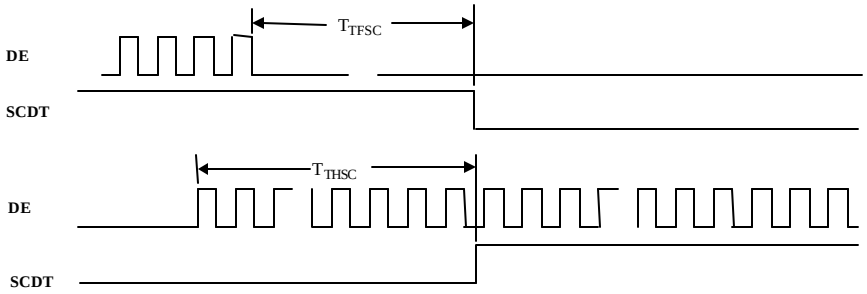


Figure 6. SCDT Timing from DE Inactive/Active

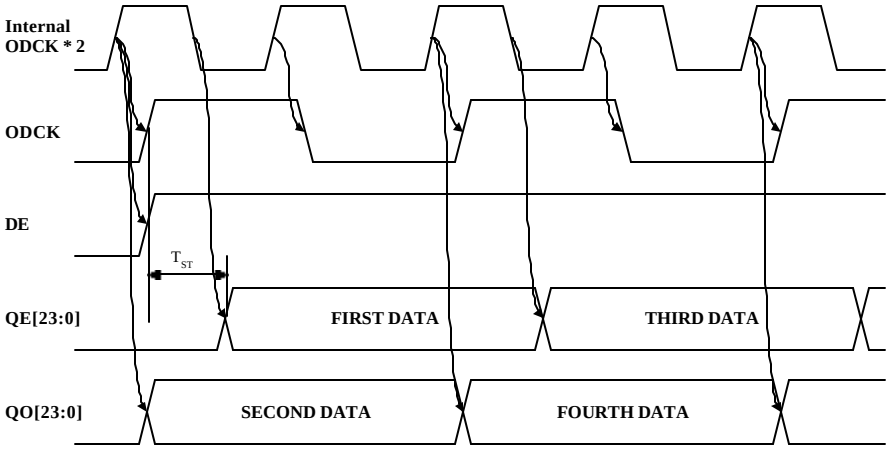


Figure 7. TFT 2-Pixels/Clock Staggered Output Timing Diagram

Output Pins Description

Pin Name	Pin #	Type	Description
QE23-QE0	See SiI 161A Pin Diagram	Out	Output Even Data[23:0] corresponds to 24-bit pixel data for 1-pixel/clock input mode and to the first 24-bit pixel data for 2-pixels/clock mode. Output data is synchronized with output data clock (ODCK). Refer to the TFT Signal Mapping application note (SiI/AN-0007) which tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
QO23-QO0	See SiI 161A Pin Diagram	Out	Output Odd Data[23:0] corresponds to the second 24-bit pixel data for 2-pixels/clock mode. During 1-pixel/clock mode, these outputs are driven low. Output data is synchronized with output data clock (ODCK). Refer to the TFT Signal Mapping application note (SiI/AN-0007) which tabulates the relationship between the input data to the transmitter and output data from the receiver. A low level on PD or PDO will put the output drivers into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.
ODCK	44	Out	Output Data Clock. This output can be inverted using the OCK_INV pin. A low level on PD or PDO will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground.
DE	46	Out	Output Data Enable. This signal qualifies the active data area. A HIGH level signifies active display time and a LOW level signifies blanking time. This output signal is synchronized with the output data. A low level on PD or PDO will put the output driver into a high impedance (tri-state) mode. A weak internal pull-down device brings the output to ground. In Dual Link Applications, the DE output pin of the Master is connected to the SYNC input pin of the Slave.
HSYNC VSYNC CTL1 CTL2 CTL3	48 47 40 41 42	Out Out Out Out Out	Horizontal Sync input control signal. Vertical Sync input control signal. General output control signal 1. This output is **not** powered down by PDO. General output control signal 2. General output control signal 3. A low level on PD or PDO will put the output drivers (except CTL1 by PDO) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground.

Configuration Pins Description

Pin Name	Pin #	Type	Description
OCK_INV	100	In	ODCK Polarity. A LOW level selects normal ODCK output. A HIGH level selects inverted ODCK output. All other output signals are not affected by this pin. They will maintain the same timing no matter the setting of OCK_INV pin (See Fig. 8 on p.10). NOTE OCK_INV cannot be set HIGH (inverted) when operating in Dual Link Mode
PIXS/M_S	4	In	Pixel Select. A LOW level indicates one pixel (up to 24-bits) per clock mode using QE[23:0]. A HIGH level indicates two pixels (up to 48-bits) per clock mode using QE[23:0] for first pixel and QO[23:0] for second pixel. Master/Slave. When S_D pin is HIGH (Dual Link), this pin becomes M_S. When HIGH, it is in Master mode. When LOW, it is in Slave mode. The Master receiver is in one/two-pixels per clock mode depending upon Dual/Single (S_D) Link operation. The Slave receiver is always in one-pixel per clock mode.
STAG_OUT/ SYNC	7	In	Staggered Output. A HIGH level selects normal simultaneous outputs on all odd and even data lines. A LOW level selects staggered output drive. This function is only available in 2-pixels per clock mode. Synchronization. When S_D pin is HIGH (Dual Link), this pin is used to synchronize the Slave receiver to the Master receiver. The SYNC input pin of the Slave receiver is connected to the DE output pin of the Master receiver.
ST	3	In	Output Drive. A HIGH level selects HIGH output drive strength. A LOW level selects LOW output drive strength.
S_D	1	In	Single/Dual Link Mode. When HIGH, it is in Dual Link Mode. When LOW it is in Single Link Mode. The Slave receiver is always in Dual Link mode. The Master receiver switches between Single and Dual Link mode depending upon the SCDT output of the Slave receiver that is connected to the S_D input of the Master receiver.

Power Management Pins Description

Pin Name	Pin #	Type	Description
SCDT	8	Out	Sync Detect. A HIGH level is outputted when DE is actively toggling indicating that the link is alive. A LOW level is outputted when DE is inactive, indicating the link is down. Can be connected to PDO to power down the outputs when DE is not detected. The SCDT output itself, however, remains in the active mode at all times. In Dual Link applications the SCDT pin of the Slave receiver is connected to the S_D pin of the Master receiver.
PDO	9	In	Output Driver Power Down (active LOW). A HIGH level indicates normal operation. A LOW level puts all the output drivers only (except SCDT and CTL1) into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. PDO is a sub-set of the PD description. The chip is not in power-down mode with this pin. SCDT and CTL1 are not tri-stated by this pin.
PD	2	In	Power Down (active LOW). A HIGH level indicates normal operation. A LOW level indicates power down mode. During power down mode, all the output drivers are put into a high impedance (tri-state) mode. A weak internal pull-down device brings each output to ground. Additionally, all analog logic is powered down, and all inputs are disabled.

Differential Signal Data Pins Description

Pin Name	Pin #	Type	Description
RX0+	90	Analog	TMDS Low Voltage Differential Signal input data pairs.
RX0-	91	Analog	
RX1+	85	Analog	
RX1-	86	Analog	
RX2+	80	Analog	
RX2-	81	Analog	
RXC+	93	Analog	TMDS Low Voltage Differential Signal input data pairs.
RXC-	94	Analog	
EXT_RES	96	Analog	Impedance Matching Control. Resistor value should be approximately ten times the characteristic impedance of the cable. In the common case of 50Ω transmission line, an external 560Ω resistor must be connected between AVCC and this pin.

Reserved Pin Description

Pin Name	Pin #	Type	Description
RESERVED	99	In	Must be tied HIGH for normal operation.

Power and Ground Pins Description

Pin Name	Pin #	Type	Description
VCC	6,38,67	Power	Digital Core VCC, must be set to 3.3V.
GND	5,39,68	Ground	Digital Core GND.
OVCC	18,29,43,57,78	Power	Output VCC, must be set to 3.3V.
OGND	19,28,45,58,76	Ground	Output GND.
AVCC	82,84,88,95	Power	Analog VCC must be set to 3.3V.
AGND	79,83,87,89,92	Ground	Analog GND.
PVCC	97	Power	PLL Analog VCC must be set to 3.3V.
PGND	98	Ground	PLL Analog GND.

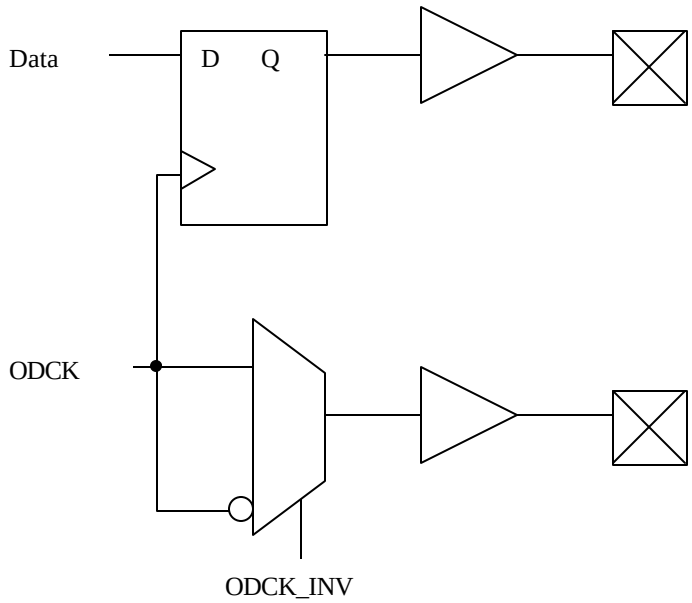


Figure 8: Block Diagram for ODCK_INV: note that ODCK_INV affects only the phase of the clock output, but does not change timing for data latching.

TFT Panel Data Mapping

The following table shows the output data mapping in one pixel per clock mode for the SiI 161A. This output data mapping is dependent upon the SiI PanelLink transmitters having the exact same type of input data mappings. Please refer to the SiI PanelLink transmitter for the specific input data mappings and to the TFT Signal Mapping application note (SiI AN-0007).

	SiI 161A	
	1-Pixel/Clock Output	
	18bpp	**24bpp**
BLUE[7:0]	QE[7:2]	QE[7:0]
GREEN[7:0]	QE[15:10]	QE[15:8]
RED[7:0]	QE[23:18]	QE[23:16]

Table 1. One Pixel/Clock Mode Data Mapping

	SiI 161A	
	2-Pixel/Clock Output	
	18bpp	**24bpp**
BLUE[7:0] - 0	QE[7:2]	QE[7:0]
GREEN[7:0] – 0	QE[15:10]	QE[15:8]
RED[7:0] – 0	QE[23:18]	QE[23:16]
BLUE[7:0] – 1	QO[7:2]	QO[7:0]
GREEN[7:0] – 1	QO[15:10]	QO[15:8]
RED[7:0] – 1	QO[23:18]	QO[23:16]

Table 2. Two Pixel/Clock Mode Data Mapping

Note: For 18-bit mode, the Flat Panel Timing Controller interfaces to the SiI 161A exactly the same as in the 24-bit mode; however, only 6-bits per channel (color) are interfaced instead of the full 8. As can be seen from the above table, the data mapping for less than 24-bit per pixel interfaces are MSB justified.

Dual Link Mode Operation

SiI161A operates up to the full DVI Single Link bandwidth of 165MHz. In Dual Link applications, two SiI161A chips can be used to support pixel clock speeds up to 330MHz. These applications will only support panels with 48-bit, 2-pixel per clock interfaces. See Figure 9 for connection details.

In Single Link mode, the transmitter system does not send any Data over the second link connected to the Slave receiver. Therefore, the Slave receiver is not active and its outputs are tri-stated. All the Data, both EVEN and ODD pixels, are sent over the link connected to the Master receiver. Therefore all the Data, both EVEN and ODD pixels, for the panel is output by the Master receiver, which operates in 48-bit, 2-pixels per clock interface mode.

In Dual Link mode, the transmitter system sends EVEN Data over the link connected to the Master receiver and the ODD Data over the link connected to the Slave receiver. Therefore, the EVEN Data for the panel is output by the Master receiver and the ODD Data is output by the Slave receiver. The Master receiver's ODD Data bus is tri-stated to allow the Slave receiver's EVEN Data bus to output the ODD Data for the panel.

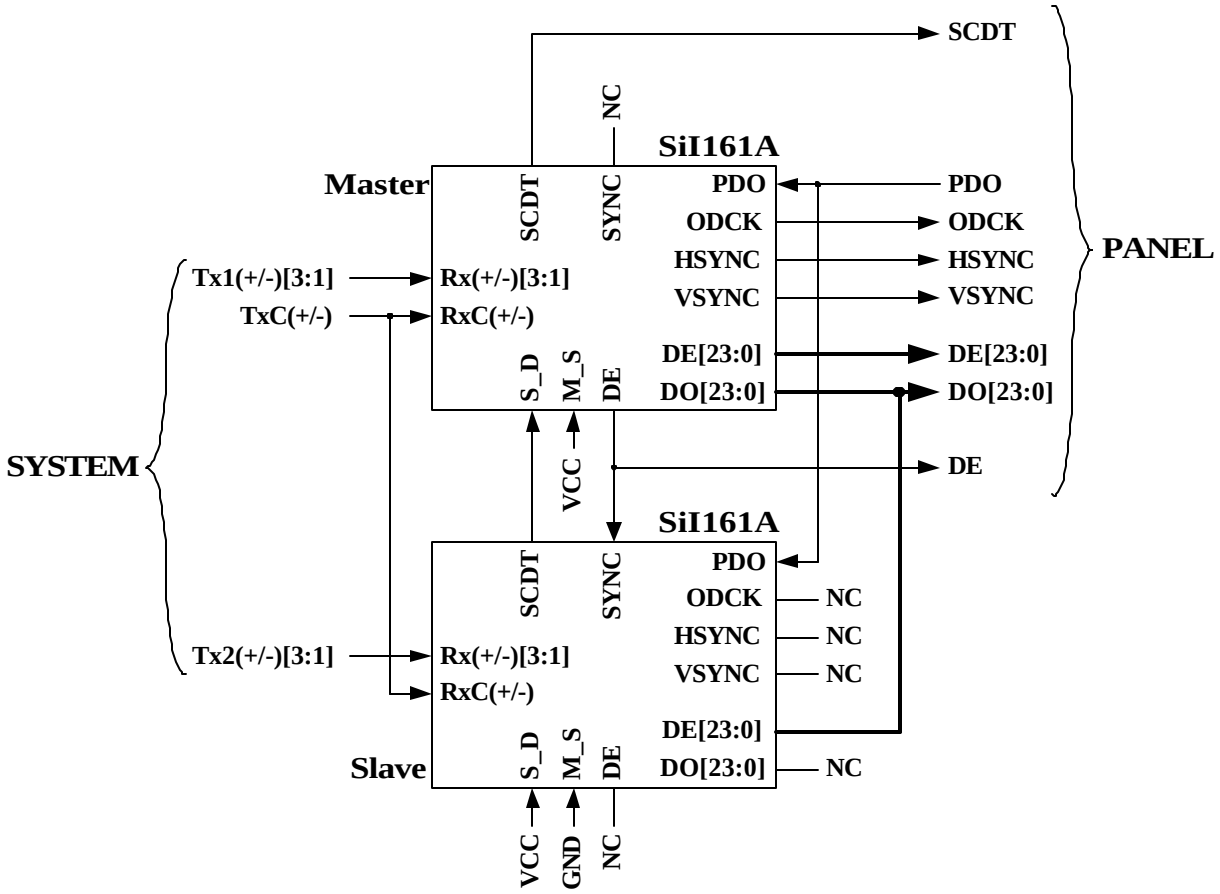


Figure 9: SiI161A Dual Link Block Diagram

Configuration:

Master –

The Master receiver will automatically configure to either Single or Dual Link operation (two or one pixel per clock mode, respectively) depending on the transmitter system output. This is accomplished by connecting the SCDT output pin of the Slave to the S_D pin on the Master. When the transmitter sends data on the second link, the SCDT output of the slave (and the S_D pin on the Master) becomes high, setting to Dual Link (one-pixel per clock) mode. If there is no data on the second link, the SCDT output of the Slave (and the S_D pin on the Master) becomes LOW, and the Master receiver is in Single Link (two-pixels per clock) mode.

The Master receiver is configured by tieing the M_S pin to HIGH. When it is in Dual Link mode, the Master receiver is in one-pixel per clock mode outputting the EVEN data for the panel. The Master receiver's ODD data bus is tri-stated to allow the Slave receiver's EVEN data bus to be used as the ODD data bus for the panel. When it is in Single Link mode, the Master receiver is in two-pixels per clock mode outputting both the EVEN and ODD data for the panel. The Slave receiver's EVEN data bus is tri-stated to allow the Master receiver's ODD data bus to be used as the ODD data for the panel.

The DE output pin of the Master receiver is connected to the SYNC input pin of the Slave receiver. This is used for output synchronization between the Master receiver and Slave receiver. DE, HSYNC, VSYNC, and ODCK for the panel are all taken from the Master receiver.

Slave –

The Slave receiver is always configured for Dual Link (one pixel/clock) operation. This is accomplished by tieing the S_D pin to HIGH. The Slave receiver is never used in Single Link mode since the Master receiver is the primary receiver for Single Link Operation.

The Slave receiver is configured by tieing the M_S pin to LOW. The Slave receiver will always contain the ODD data bus for the panel in Dual Link operation. Therefore, it will never be in two-pixels per clock mode.

The SCDT output pin of the Slave receiver is connected to the S_D input pin of the Master receiver to automatically configure the Master for either Single or Dual Link mode depending upon whether the Slave receiver is active or not.

The SYNC input pin of the Slave receiver is connected to the DE output pin of the Master receiver for synchronization.

Since DE, HSYNC, VSYNC, and ODCK for the panel are all taken from the Master receiver, these pins are not connected from the Slave receiver.

Power Down Outputs –

The Slave receiver's outputs are automatically tri-stated in Single Link mode, since it is not active. The Master receiver's outputs are automatically tri-stated in Single or Dual Link mode when there are no sync signals coming from the transmitter. Both the Master and Slave receiver's outputs can also be tri-stated by driving the PDO pins to LOW manually.

For additional information about dual link operation, please see Application Notes SiI-AN-0030, (SiI161A Dual Link Receiver Implementation) and SiI-AN-0037 (SiI168 Transmitter Dual Link Applications).

Package Dimensions

PanelLink®

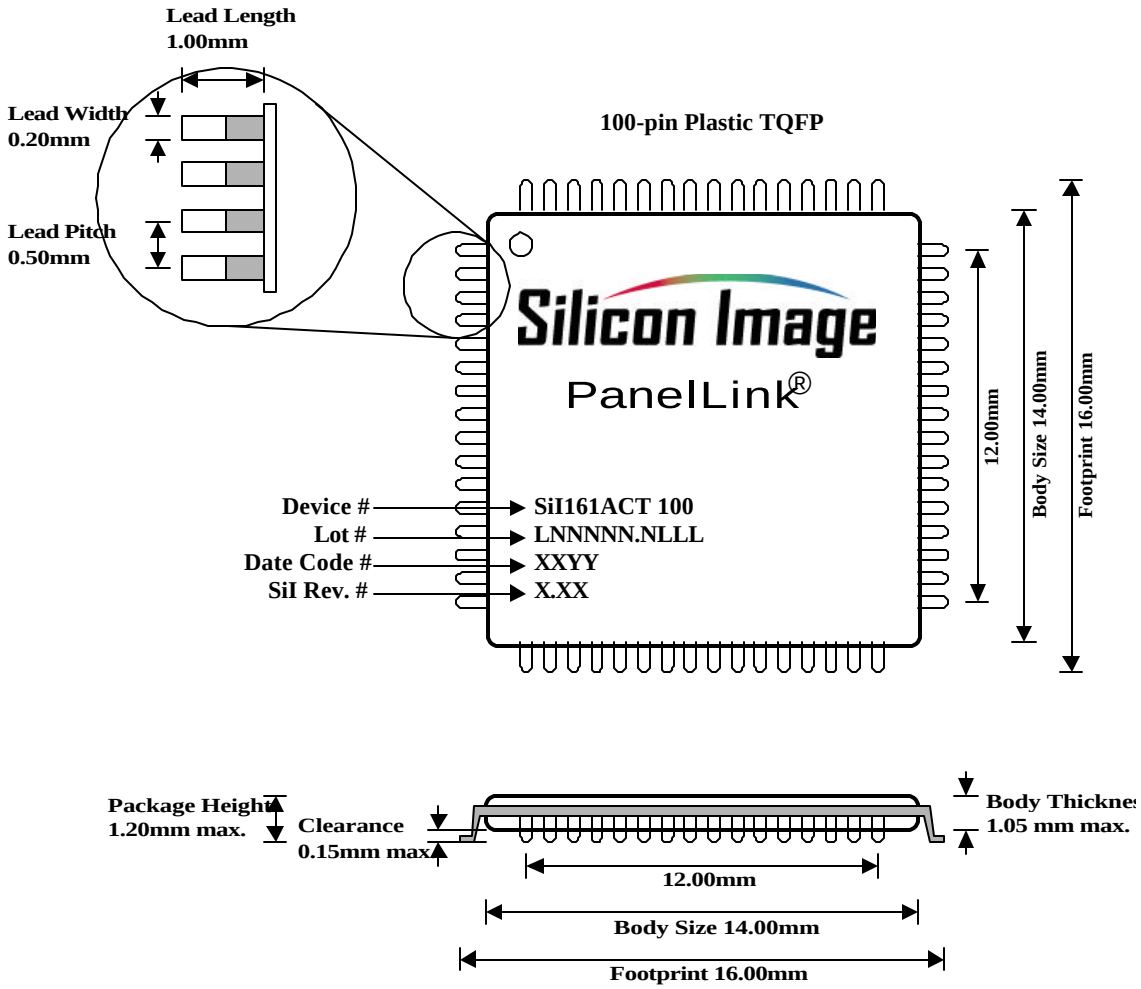


Figure 10:100-pin TQFP Package Dimensions
JEDEC code MS-026AED

PCB Thermal Design Options:

The SiI161A is packaged in a thermally enhanced 100 pin TQFP with an exposed metal pad (7.5mm x 7.5 mm) on the package designed for improved thermal dissipation. To improve the heat removal from the package, the exposed thermal pad may be soldered to a thermal landing area on the PCB, as described in the following section, entitled "Implementation Guidelines for Thermal Land Design".

Implementation of the thermal landing area on the PCB can, in some cases, make trace routing and board design complicated. In some applications, it may be desirable to eliminate the thermal landing area on the PCB.

Generally the thermal performance of a package can be represented by the following parameter (JEDEC standard JESD 51-2, 51-6):

θ_{JA} , Thermal resistance from junction to ambient

$$\theta_{JA} = (T_J - T_A) / P_H$$

Where T_J is the junction temperature
T_A is the ambient temperature
P_H is the power dissipation

θ_{JA} represents the resistance to the heat flows from the chip to ambient air. It is an index of heat dissipation capability. Lower θ_{JA} means better thermal performance.

Implementation of the thermal landing area, combined with complete soldering of the package to the landing area results in a θ_{JA} of 21°C/W. If the SiI161A package is assembled to a standard PCB, without the thermal landing area, the θ_{JA} increases to 29°C/W. For comparison, the non-thermally enhanced 100 pin TQFP package has a θ_{JA} of 53°C/W, so the advantage of the exposed metal pad in the thermally enhanced SiI161A package is significant, even without a landing area on the PCB.

In order to determine the requirements for soldering the SiI161A to the PCB, the following analysis is insightful. Assuming a worst case scenario, with operation at the maximum ambient temperature of 70°C, at maximum voltage (3.6V) and worst case pattern (330 mA) – the junction temperature would be 35°C above ambient, or 105°C. This is still well below the maximum junction temperature of 125°C, providing suitable margin even without requiring the use of solder and a specific landing area on the PCB. For comparison, with the improved thermal dissipation that results from complete soldering of the thermal pad on the chip to a thermal landing area on the PCB, the package temperature would be 23°C above ambient – or roughly 12°C cooler than a chip with no solder.

Based on this analysis, the need for designing a thermal landing area on a PCB for use with the SiI161A receiver should be considered an optional design choice by the customer, and is not an absolute requirement.

For more information regarding Thermal Design Options, please see Application Note SiI-AN-0045, Enhanced Thermal Packaging Options for SiI-161A.

Implementation Guidelines for Thermal Land Design:

As described above, a thermal land on the PCB may be incorporated on the PCB to improve the heat removal from the package. An example of this is shown in Figure 11, which depicts the exposed heat pad and Figure 12, which shows a TQFP Thermal Land Design on a PCB. The size of this thermal land can be smaller or larger than the exposed pad on the package. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the thermal land and the inner edges of pad pattern for the leads to avoid any shorts.

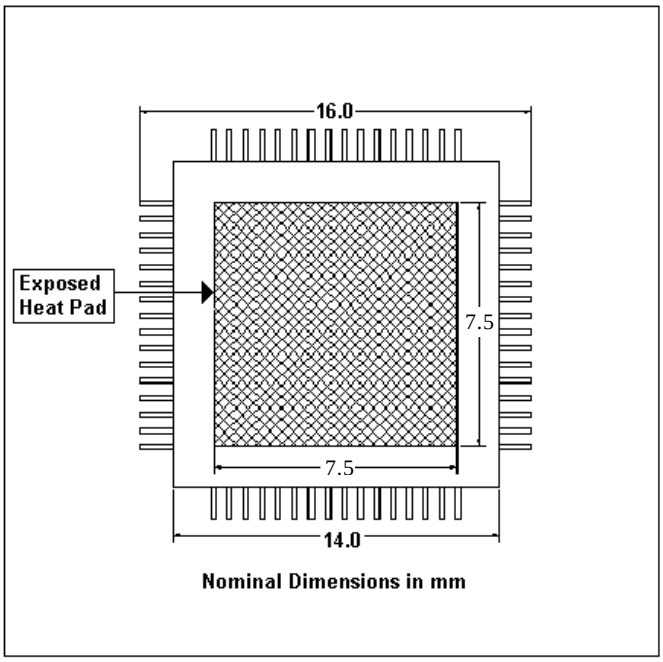


Figure 11. Bottom View of Thermally Enhanced 100-pin TQFP Package

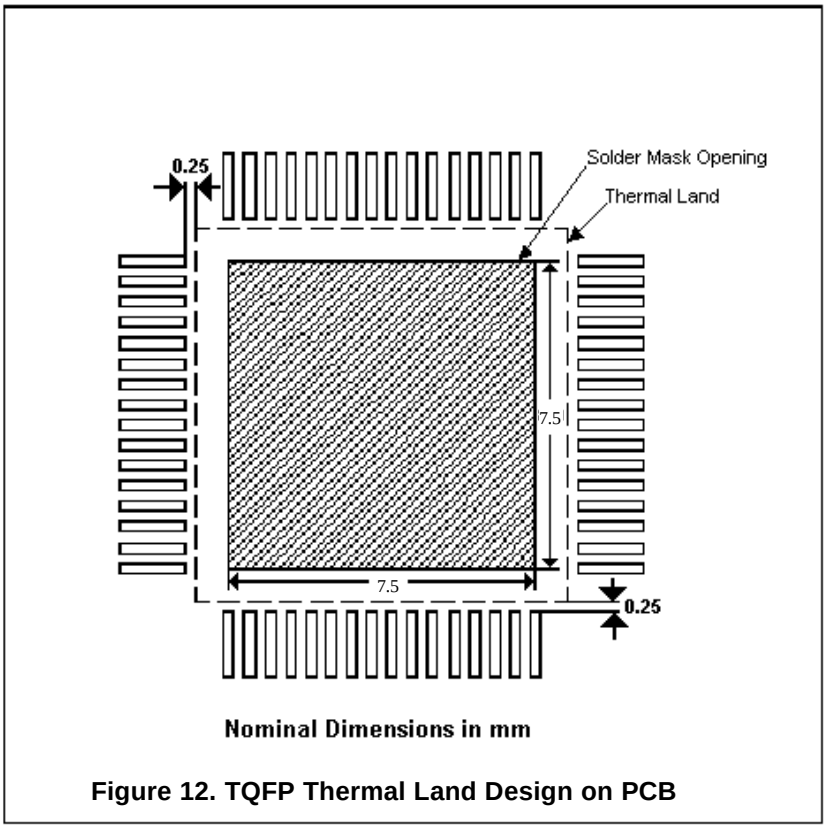


Figure 12. TQFP Thermal Land Design on PCB

When a thermal land on the PCB is used to provide a means of improved heat transfer from the package to the board through a solder joint, thermal vias are required to remove the heat from the PCB. It is recommended that these vias connect to the ground plane of the PCB. These vias provide a heat transfer path from the top surface of the PCB to the inner layers and the bottom surface of the package. An array of vias should be incorporated in the thermal pad at 1.2 mm pitch grid, as shown in Figure 13. Thermal Pad Via Grid. It is also recommended that the via diameter should be around 12 to 13 mils (0.30 to 0.33 mm) and the via barrel should be plated with 1 oz copper to plug the via. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be "tented" with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 4 mils (0.1 mm) larger than the via diameter.

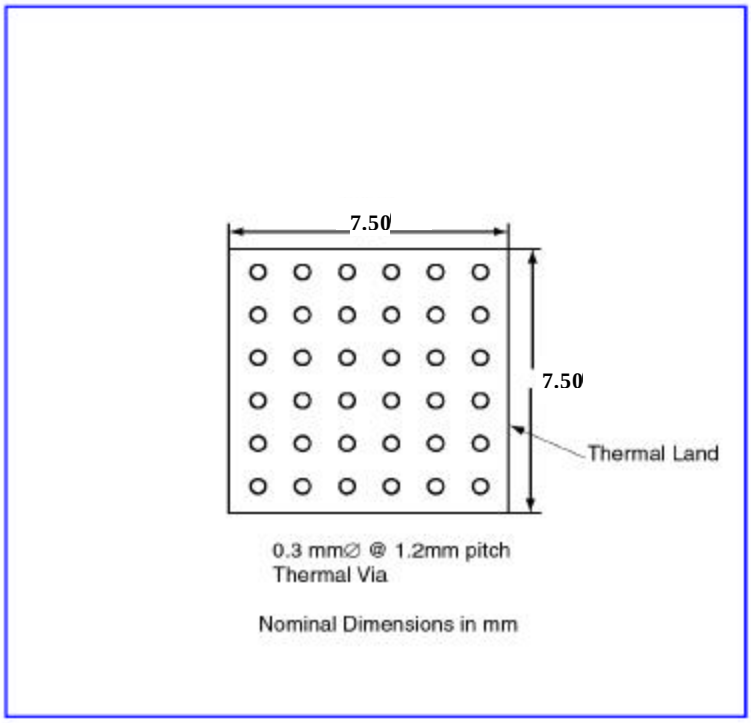


Figure 13. Thermal Pad Via Grid

Board Mounting Guidelines

The following are general recommendations for mounting exposed pad leadframe devices on the motherboard. This should serve as the starting point in assembly process development and it is recommended that the process should be developed based on past experience in mounting standard, non-thermally enhanced packages.

Stencil Design:

For improved heat transfer, the exposed pad on the package may be soldered to a thermal land on the PCB. This requires solder paste application not only on the pad pattern for lead attachment but also on the thermal land using the stencil. While for standard (non-thermally enhanced) leadframe based packages the stencil thickness depends on the lead pitch and package coplanarity only, the package standoff also needs to be considered for the thermally enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 5 to 8 mils (depending upon the pitch) should still provide good solder joint between the exposed pad and the thermal land. The aperture openings should be the same as the solder mask opening on the thermal land. Since a large stencil opening may result in poor release, the aperture opening can be subdivided into an array of smaller openings, similar to the thermal land pattern shown in Figure 14. Recommended Stencil Design. The above guidelines will result in the solder joint area to be about 80 to 90% of the exposed pad area.

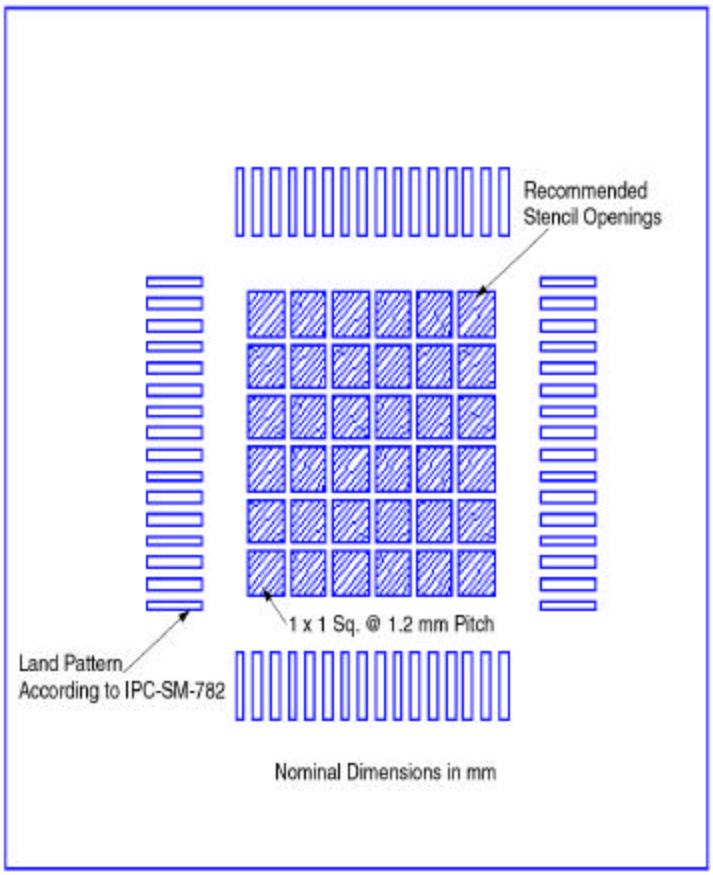


Figure 14. Recommended Stencil Design

Application Information

To obtain the most updated Application Notes and other useful information for your design application, please visit the Silicon Image web site at ***www.Siimage.com***, or contact your local Silicon Image sales office.

Ordering Information

Part Number: SiI161ACT100

Revision History

Revision	Date	Comment
A	3/00	Full release
B	7/00	Corrections to AC timing figures and values
C	11/00	Addition of information for Dual Link Implementation and Thermal Design
D	3/01	Corrected Functional Block Diagram

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