OVERVIEW

The SM5006 series are crystal oscillator module ICs, that incorporate high-frequency, low current consumption oscillator and output buffer circuits. Highly accurate thin-film feedback resistors and high-frequency capacitors are built-in, eliminating the need for external components to make a stable 3rd overtone oscillator.

FEATURES

- Up to 107MHz operation
- Capacitors C_G, C_D built-in
- Inverter amplifier feedback resistor built-in
- TTL input level
- 16mA (V_{DD} = 4.5V) drive capability
- 4mA (V_{DD} = 4.5V) drive capability (5006AH×)
- Output three-state function
- 2.7 to 5.5V supply voltage
- Oscillator frequency output
- 8-pin SOP (SM5006×××S)
- Chip form (CF5006×××)

SERIES CONFIGURATION

Version*1	gm ratio	3V operating		5V operating			Built-in capacitance		R_f [kΩ]	Input level	Output duty level
		Output load (max) [pF]	Recommended operating frequency range*2 [MHz]	Output load (max) [pF]	Recommended operating frequency range*2 [MHz]	Output waveform*3 t_r /t_f [ns]	C_G [pF]	C_D [pF]			
SM5006ANAS	0.5	–	–	50	22 to 30	8/8	8	16	8.2	TTL	CMOS
SM5006ANBS	1	–	–	50	30 to 40	8/8	8	16	5.6	TTL	CMOS
SM5006ANCS	2	15	22 to 30	50	40 to 60	7/7	8	16	4.9	TTL	CMOS
SM5006ANDS	2	15	30 to 50	50	50 to 70	7/7	8	16	2.6	TTL	CMOS
SM5006ANES	3	15	50 to 70	30 (15)*4	70 to 100	6/6	8	16	2.6	TTL	CMOS
SM5006ANFS	4	–	–	30 (15)*4	80 to 107	6/6	8	16	2.6	TTL	CMOS
SM5006CNCS	2	15	22 to 30	15 50	40 to 60 40 to 50	8/8	8	16	4.9	TTL	CMOS
SM5006CNDS	2	15	30 to 40	15	50 to 70	8/8	8	16	2.6	TTL	CMOS
SM5006CNES	3	15	50 to 70	15	70 to 100	7/7	8	16	2.6	TTL	CMOS
SM5006BNCS	2	15	22 to 70	15 50	22 to 100 22 to 70	7/7	8	16	No	TTL	CMOS
SM5006BNES	3	15	22 to 70	30 (15)*4	70 to 107	6/6	8	16	No	TTL	CMOS
SM5006DNCS	2	15	22 to 40	15 50	22 to 70 22 to 50	8/8	8	16	No	TTL	CMOS
SM5006DNES	3	15	22 to 70	15 50	22 to 100 22 to 70	7/7	8	16	No	TTL	CMOS
SM5006AKAS	0.5	–	–	15	22 to 30	4/4	8	16	8.2	TTL	TTL
SM5006AKBS	1	–	–	15	30 to 40	4/4	8	16	5.6	TTL	TTL
SM5006AKCS	2	–	–	15	40 to 60	4/4	8	16	4.9	TTL	TTL
SM5006AKDS	2	–	–	15	50 to 70	4/4	8	16	2.6	TTL	TTL
SM5006CKDS	2	–	–	15	50 to 70	4/4	8	16	2.6	TTL	TTL
SM5006BKCS	2	–	–	15	22 to 70	4/4	8	16	No	TTL	TTL
SM5006DKCS	2	–	–	15	22 to 70	4/4	8	16	No	TTL	TTL
SM5006AHAS	0.5	–	–	15	22 to 30	7/7	8	16	8.2	TTL	CMOS
SM5006AHBS	1	–	–	15	30 to 40	7/7	8	16	5.6	TTL	CMOS
SM5006AHCS	2	–	–	15	40 to 60	7/7	8	16	4.9	TTL	CMOS
SM5006AHDS	2	–	–	15	50 to 70	7/7	8	16	2.6	TTL	CMOS

*1. Chip form devices have designation CF5006×××.

*2. The recommended operating frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillator frequency band is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

*3. 5006×N×: C_L = 50pF, CMOS load, 5006×K×: C_L = 15pF, 10TTL load, 5006AH×: C_L = 15pF, CMOS load

*4. SOP package only

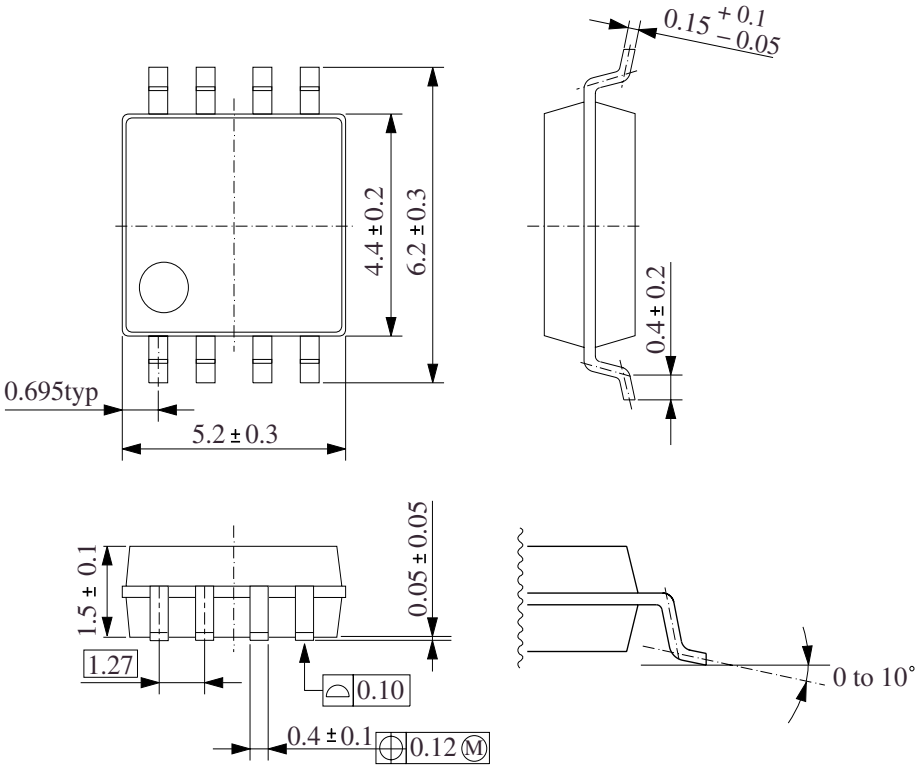
ORDERING INFORMATION

Device	Package
SM5006×××S	8-pin SOP
CF5006×××–1	Chip form

PACKAGE DIMENSIONS

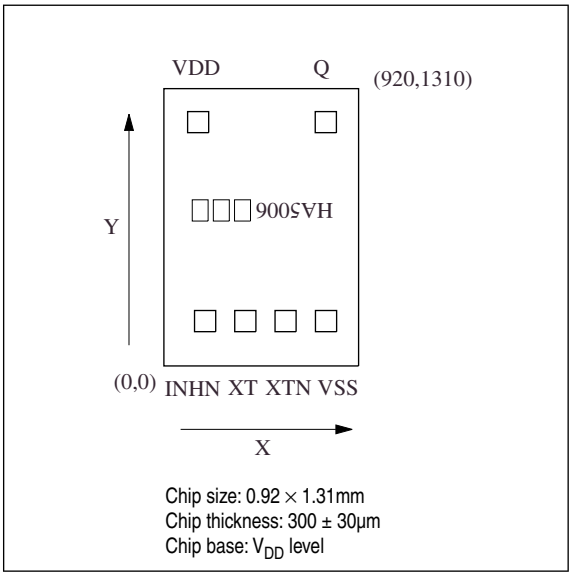
(Unit: mm)

• 8-pin SOP



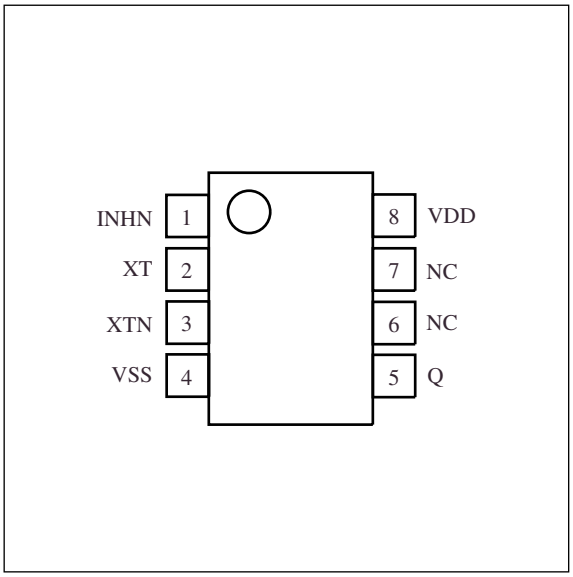
PAD LAYOUT

(Unit: µm)



PINOUT

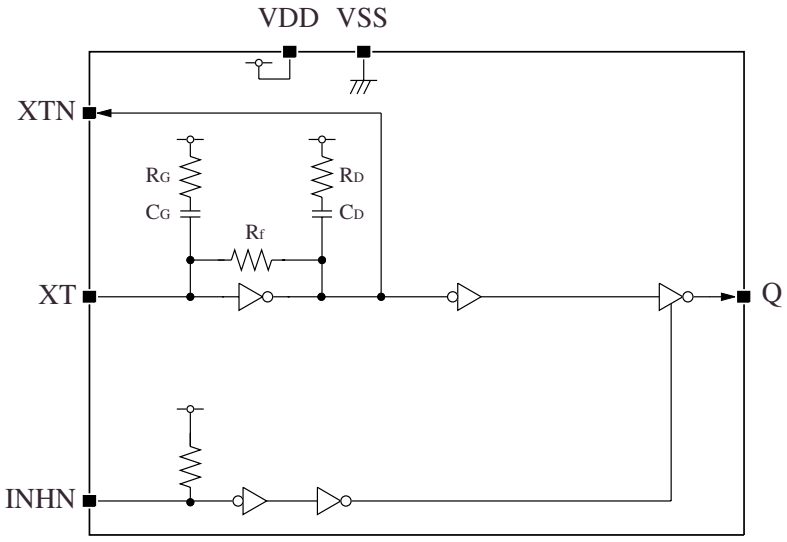
(Top view)



PIN DESCRIPTION and PAD DIMENSIONS

Number	Name	I/O	Description		Pad dimensions [µm]	
					X	Y
1	INHN	I	Output state control input. High impedance when LOW. Pull-up resistor built in		195	212
2	XT	I	Amplifier input.	Crystal oscillator connection pins. Crystal oscillator connected between XT and XTN	385	212
3	XTN	O	Amplifier output.		575	212
4	VSS	–	Ground		766	212
5	Q	O	Output. Output frequency (f_O)		765	1152
6	NC	–	No connection		–	–
7	NC	–	No connection		–	–
8	VDD	–	Supply voltage		162	1152

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.5 to 7.0	V
Input voltage range	V_{IN}		–0.5 to V_{DD} + 0.5	V
Output voltage range	V_{OUT}		–0.5 to V_{DD} + 0.5	V
Operating temperature range	T_{opr}		–40 to 85	°C
Storage temperature range	T_{stg}	Chip form	–65 to 150	°C
		8-pin SOP	–55 to 125	
Output current	I_{OUT}	5006×N×, ×K×	25	mA
		5006AH×	10	
Power dissipation	P_D	8-pin SOP	500	mW

Recommended Operating Conditions

SM5006 series (package form)

V_{SS} = 0V

Parameter	Symbol	Series	Condition	Rating			Unit
				min	typ	max	
Supply voltage	V_{DD}	ANA, ANB, CNC, CND, DNC	f ≤ 50MHz, C_L = 50pF	4.5	–	5.5	V
			f ≤ 70MHz, C_L = 15pF	4.5	–	5.5	
			f ≤ 40MHz, C_L = 15pF	2.7	–	3.6	
		ANC, AND, BNC, CNE, DNE	f ≤ 70MHz, C_L = 50pF	4.5	–	5.5	V
			f ≤ 100MHz, C_L = 15pF	4.5	–	5.5	
			f ≤ 50MHz, C_L = 15pF	2.7	–	3.6	
			f ≤ 70MHz, C_L = 15pF	3.0	–	3.6	
		ANE, ANF, BNE	f ≤ 100MHz, C_L = 15pF	4.5	–	5.5	V
			f ≤ 107MHz, C_L = 15pF	4.5	–	5.5	
			f ≤ 50MHz, C_L = 15pF	2.7	–	3.6	
			f ≤ 70MHz, C_L = 15pF	3.0	–	3.6	
		AKA, AKB, AKC, CKD, DKC	f ≤ 70MHz, C_L = 15pF	4.5	–	5.5	V
		AKD, BKC	f ≤ 70MHz, C_L = 15pF	4.5	–	5.5	V
		AHA, AHB, AHC, AHD	f ≤ 70MHz, C_L = 15pF	4.5	–	5.5	V
Input voltage	V_{IN}	All series		V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}	ANA, ANB, CNC, CND, DNC	f ≤ 50MHz, C_L = 50pF, 4.5 ≤ V_{DD} ≤ 5.5	– 40	–	+ 85	°C
			f ≤ 70MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	0	–	+ 70	
			f ≤ 40MHz, C_L = 15pF, 2.7 ≤ V_{DD} ≤ 3.6	– 10	–	+ 70	
		ANC, AND, BNC, CNE, DNE	f ≤ 50MHz, C_L = 50pF, 4.5 ≤ V_{DD} ≤ 5.5	– 40	–	+ 80	°C
			f ≤ 70MHz, C_L = 50pF, 4.5 ≤ V_{DD} ≤ 5.5	– 20	–	+ 80	
			f ≤ 70MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	– 40	–	+ 85	
			f ≤ 100MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	0	–	+ 70	
			f ≤ 50MHz, C_L = 15pF, 2.7 ≤ V_{DD} ≤ 3.6	– 20	–	+ 80	
			f ≤ 70MHz, C_L = 15pF, 3.0 ≤ V_{DD} ≤ 3.6	– 20	–	+ 80	
		ANE, ANF, BNE	f ≤ 70MHz, C_L = 50pF, 4.5 ≤ V_{DD} ≤ 5.5	– 20	–	+ 80	°C
			f ≤ 100MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	– 40	–	+ 85	
			f ≤ 107MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	– 20	–	+ 80	
			f ≤ 50MHz, C_L = 15pF, 2.7 ≤ V_{DD} ≤ 3.6	– 20	–	+ 80	
			f ≤ 70MHz, C_L = 15pF, 3.0 ≤ V_{DD} ≤ 3.6	– 20	–	+ 80	
		AKA, AKB, AKC, CKD, DKC	f ≤ 50MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	– 40	–	+ 85	°C
			f ≤ 70MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	0	–	+ 70	
		AKD, BKC	f ≤ 50MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	– 40	–	+ 85	°C
			f ≤ 70MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	– 20	–	+ 80	
		AHA, AHB, AHC, AHD	f ≤ 50MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	– 40	–	+ 85	°C
			f ≤ 70MHz, C_L = 15pF, 4.5 ≤ V_{DD} ≤ 5.5	– 15	–	+ 75	

CF5006 series (chip form)

$V_{SS} = 0V$

Parameter	Symbol	Series	Condition	Rating			Unit
				min	typ	max	
Supply voltage	V_{DD}	ANA, ANB, CNC, CND, DNC	$f \leq 50MHz$, $C_L = 50pF$	4.5	–	5.5	V
			$f \leq 70MHz$, $C_L = 15pF$	4.5	–	5.5	
			$f \leq 40MHz$, $C_L = 15pF$	2.7	–	3.6	
		ANC, AND, BNC, CNE, DNE	$f \leq 70MHz$, $C_L = 50pF$	4.5	–	5.5	V
			$f \leq 100MHz$, $C_L = 15pF$	4.5	–	5.5	
			$f \leq 50MHz$, $C_L = 15pF$	2.7	–	3.6	
			$f \leq 70MHz$, $C_L = 15pF$	3.0	–	3.6	
		ANE, ANF, BNE	$f \leq 70MHz$, $C_L = 50pF$	4.5	–	5.5	V
			$f \leq 107MHz$, $C_L = 30pF$	4.5	–	5.5	
			$f \leq 50MHz$, $C_L = 15pF$	2.7	–	3.6	
			$f \leq 70MHz$, $C_L = 15pF$	3.0	–	3.6	
		AKA, AKB, AKC, CKD, DKC	$f \leq 70MHz$, $C_L = 15pF$	4.5	–	5.5	V
		AKD, BKC	$f \leq 70MHz$, $C_L = 15pF$	4.5	–	5.5	V
		AHA, AHB, AHC, AHD	$f \leq 70MHz$, $C_L = 15pF$	4.5	–	5.5	V
Input voltage	V_{IN}	All series		V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}	ANA, ANB, CNC, CND, DNC	$f \leq 50MHz$, $C_L = 50pF$, $4.5 \leq V_{DD} \leq 5.5$	– 40	–	+ 85	°C
			$f \leq 70MHz$, $C_L = 15pF$, $4.5 \leq V_{DD} \leq 5.5$	– 15	–	+ 75	
			$f \leq 40MHz$, $C_L = 15pF$, $2.7 \leq V_{DD} \leq 3.6$	– 10	–	+ 70	
		ANC, AND, BNC, CNE, DNE	$f \leq 70MHz$, $C_L = 50pF$, $4.5 \leq V_{DD} \leq 5.5$	– 40	–	+ 85	°C
			$f \leq 100MHz$, $C_L = 15pF$, $4.5 \leq V_{DD} \leq 5.5$	– 20	–	+ 80	
			$f \leq 50MHz$, $C_L = 15pF$, $2.7 \leq V_{DD} \leq 3.6$	– 20	–	+ 80	
			$f \leq 70MHz$, $C_L = 15pF$, $3.0 \leq V_{DD} \leq 3.6$	– 20	–	+ 80	
		ANE, ANF, BNE	$f \leq 70MHz$, $C_L = 50pF$, $4.5 \leq V_{DD} \leq 5.5$	– 40	–	+ 85	°C
			$f \leq 100MHz$, $C_L = 30pF$, $4.5 \leq V_{DD} \leq 5.5$	– 40	–	+ 85	
			$f \leq 107MHz$, $C_L = 30pF$, $4.5 \leq V_{DD} \leq 5.5$	– 20	–	+ 80	
			$f \leq 50MHz$, $C_L = 15pF$, $2.7 \leq V_{DD} \leq 3.6$	– 20	–	+ 80	
			$f \leq 70MHz$, $C_L = 15pF$, $3.0 \leq V_{DD} \leq 3.6$	– 20	–	+ 80	
		AKA, AKB, AKC, CKD, DKC	$f \leq 50MHz$, $C_L = 15pF$, $4.5 \leq V_{DD} \leq 5.5$	– 40	–	+ 85	°C
			$f \leq 70MHz$, $C_L = 15pF$, $4.5 \leq V_{DD} \leq 5.5$	– 15	–	+ 75	
		AKD, BKC	$f \leq 50MHz$, $C_L = 15pF$, $4.5 \leq V_{DD} \leq 5.5$	– 40	–	+ 85	°C
			$f \leq 70MHz$, $C_L = 15pF$, $4.5 \leq V_{DD} \leq 5.5$	– 20	–	+ 80	
		AHA, AHB, AHC, AHD	$f \leq 50MHz$, $C_L = 15pF$, $4.5 \leq V_{DD} \leq 5.5$	– 40	–	+ 85	°C
			$f \leq 70MHz$, $C_L = 15pF$, $4.5 \leq V_{DD} \leq 5.5$	– 20	–	+ 80	

Electrical Characteristics

5006×N series

3V operation: V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, Ta = −20 to 80 °C unless otherwise noted.

Parameter	Symbol	Condition			Rating			Unit
					min	typ	max	
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, V_{DD} = 2.7V, I_{OH} = 8mA			2.2	2.4	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, V_{DD} = 2.7V, I_{OL} = 8mA			–	0.3	0.4	V
Output leakage current	I_Z	Q: Measurement cct 2, INHN = LOW, V_{DD} = 5.5V		V_{OH} = V_{DD}	–	–	10	µA
				V_{OL} = V_{SS}	–	–	10	
HIGH-level input voltage	V_{IH}	INHN			2.0	–	–	V
LOW-level input voltage	V_{IL}	INHN			–	–	0.5	V
Current consumption	I_{DD}	INHN = open, Measurement cct 3, load cct 1, V_{DD} = 3.0 to 3.6V, C_L = 15pF	f = 30MHz	SM5006ANCS CF5006ANC SM5006BNCS CF5006BNC	–	8	16	mA
			f = 30MHz, Ta = −10 to 70°C	SM5006CNCS CF5006CNC	–	8	16	
			f = 50MHz	SM5006ANDS CF5006AND	–	13	26	
			f = 70MHz	SM5006BNES CF5006BNE SM5006CNES CF5006CNE SM5006DNES CF5006DNE	–	15	30	
			f = 40MHz, Ta = −10 to 70°C	SM5006CNDS CF5006CND SM5006DNCS CF5006DNC	–	11	22	
			f = 70MHz	SM5006ANES CF5006ANE SM5006ANFS CF5006ANF	–	20	40	
INHN pull-up resistance	R_{UP}	Measurement cct 4			50	–	150	kΩ
Feedback resistance	R_f	Measurement cct 5	SM5006ANAS, CF5006ANA		6.97	8.2	9.43	kΩ
			SM5006ANBS, CF5006ANB		4.76	5.6	6.44	
			SM5006ANCS, CF5006ANC SM5006CNCS, CF5006CNC		4.16	4.9	5.64	
			SM5006ANDS, CF5006AND SM5006ANES, CF5006ANE SM5006ANFS, CF5006ANF SM5006CNDS, CF5006CND SM5006CNES, CF5006CNE		2.21	2.6	2.99	
Built-in resistance	R_G	Design value, determined by the R_f value			17	20	23	Ω
	R_D	Design value, determined by the R_f value			17	20	23	
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.			7.44	8	8.56	pF
	C_D	Design value. A monitor pattern on a wafer is tested.			14.88	16	17.12	

5V operation: V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition			Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, V_{DD} = 4.5V, I_{OH} = 16mA			4.0	4.2	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, V_{DD} = 4.5V, I_{OL} = 16mA			–	0.3	0.4	V
Output leakage current	I_Z	Q: Measurement cct 2, INHN = LOW, V_{DD} = 5.5V		$V_{OH} = V_{DD}$	–	–	10	µA
				$V_{OL} = V_{SS}$	–	–	10	
HIGH-level input voltage	V_{IH}	INHN			2.0	–	–	V
LOW-level input voltage	V_{IL}	INHN			–	–	0.8	V
Current consumption	I_{DD}	INHN = open, Measurement cct 3, load cct 1, V_{DD} = 4.5 to 5.5V, C_L = 50pF	f = 30MHz	SM5006ANAS CF5006ANA	–	18	35	mA
			f = 40MHz	SM5006ANBS CF5006ANB	–	20	40	
			f = 60MHz	CF5006ANC	–	30	60	
			f = 60MHz, Ta = –20 to 80°C	SM5006ANCS	–	30	50	
			f = 70MHz	CF5006AND CF5006BNC	–	40	80	
			f = 70MHz, Ta = –20 to 80°C	SM5006ANDS SM5006BNCS	–	40	70	
		INHN = open, Measurement cct 3, load cct 1, V_{DD} = 4.5 to 5.5V	f = 60MHz, C_L = 15pF, Ta = –15 to 75°C	CF5006CNC	–	28	50	
			f = 60MHz, C_L = 15pF, Ta = 0 to 70°C	SM5006CNCS	–	28	50	
			f = 70MHz, C_L = 15pF, Ta = –15 to 75°C	CF5006CND CF5006DNC	–	35	65	
			f = 70MHz, C_L = 15pF, Ta = 0 to 70°C	SM5006CNDS SM5006DNCS	–	35	65	
			f = 100MHz, C_L = 15pF, Ta = –20 to 80°C	CF5006CNE CF5006DNE	–	45	80	
			f = 100MHz, C_L = 15pF, Ta = 0 to 70°C	SM5006CNES SM5006DNES	–	45	80	
			f = 100MHz, C_L = 30pF	CF5006ANE	–	50	100	
			f = 100MHz, C_L = 15pF	SM5006ANES	–	45	90	
			f = 107MHz, C_L = 30pF, Ta = –20 to 80°C	CF5006ANF CF5006BNE	–	60	100	
			f = 107MHz, C_L = 15pF, Ta = –20 to 80°C	SM5006ANFS SM5006BNES	–	50	90	
INHN pull-up resistance	R_{UP}	Measurement cct 4			50	–	150	kΩ
Feedback resistance	R_f	Measurement cct 5	SM5006ANAS, CF5006ANA		6.97	8.2	9.43	kΩ
			SM5006ANBS, CF5006ANB		4.76	5.6	6.44	
			SM5006ANCS, CF5006ANC SM5006CNCS, CF5006CNC		4.16	4.9	5.64	
			SM5006ANDS, CF5006AND SM5006ANES, CF5006ANE SM5006ANFS, CF5006ANF SM5006CNDS, CF5006CND SM5006CNES, CF5006CNE		2.21	2.6	2.99	
Built-in resistance	R_G	Design value, determined by the R_f value			17	20	23	Ω
	R_D	Design value, determined by the R_f value			17	20	23	
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.			7.44	8	8.56	pF
	C_D	Design value. A monitor pattern on a wafer is tested.			14.88	16	17.12	

5006×K series

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition			Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, V_{DD} = 4.5V, I_{OH} = 16mA	SM5006AKAS, CF5006AKA SM5006AKBS, CF5006AKB SM5006AKCS, CF5006AKC SM5006CKDS, CF5006CKD SM5006DKCS, CF5006DKC		3.9	4.2	–	V
			SM5006AKDS, CF5006AKD SM5006BKCS, CF5006BKC		4.0	4.2	–	
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, V_{DD} = 4.5V, I_{OL} = 16mA			–	0.3	0.4	V
Output leakage current	I_Z	Q: Measurement cct 2, INHN = LOW, V_{DD} = 5.5V		$V_{OH} = V_{DD}$	–	–	10	µA
				$V_{OL} = V_{SS}$	–	–	10	
HIGH-level input voltage	V_{IH}	INHN			2.0	–	–	V
LOW-level input voltage	V_{IL}	INHN			–	–	0.8	V
Current consumption	I_{DD}	INHN = open, Measurement cct 3, load cct 1, V_{DD} = 4.5 to 5.5V, C_L = 15pF	f = 30MHz	SM5006AKAS CF5006AKA	–	16	32	mA
			f = 40MHz	SM5006AKBS CF5006AKB	–	18	36	
			f = 60MHz, Ta = –15 to 75°C	CF5006AKC CF5006DKC	–	25	50	
			f = 60MHz, Ta = 0 to 70°C	SM5006AKCS SM5006DKCS	–	25	50	
			f = 70MHz, Ta = –20 to 80°C	CF5006AKD CF5006BKC	–	35	70	
			f = 70MHz, Ta = –15 to 75°C	CF5006CKD	–	35	70	
			f = 70MHz, Ta = 0 to 70°C	SM5006AKDS SM5006BKCS SM5006CKDS	–	35	70	
INHN pull-up resistance	R_{UP}	Measurement cct 4			50	–	150	kΩ
Feedback resistance	R_f	Measurement cct 5	SM5006AKAS, CF5006AKA		6.97	8.2	9.43	kΩ
			SM5006AKBS, CF5006AKB		4.76	5.6	6.44	
			SM5006AKCS, CF5006AKC		4.16	4.9	5.64	
			SM5006AKDS, CF5006AKD SM5006CKDS, CF5006CKD		2.21	2.6	2.99	
Built-in resistance	R_G	Design value, determined by the R_f value			17	20	23	Ω
	R_D	Design value, determined by the R_f value			17	20	23	
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.			7.44	8	8.56	pF
	C_D	Design value. A monitor pattern on a wafer is tested.			14.88	16	17.12	

5006AH series

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition			Rating min	Rating typ	Rating max	Unit
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, V_{DD} = 4.5V, I_{OH} = 4mA			3.9	4.2	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, V_{DD} = 4.5V, I_{OL} = 4mA			–	0.3	0.5	V
Output leakage current	I_Z	Q: Measurement cct 2, INHN = LOW, V_{DD} = 5.5V		$V_{OH} = V_{DD}$	–	–	10	µA
				$V_{OL} = V_{SS}$	–	–	10	
HIGH-level input voltage	V_{IH}	INHN			2.0	–	–	V
LOW-level input voltage	V_{IL}	INHN			–	–	0.8	V
Current consumption	I_{DD}	INHN = open, Measurement cct 3, load cct 1, V_{DD} = 4.5 to 5.5V, C_L = 15pF	f = 30MHz	SM5006AHAS CF5006AHA	–	15	30	mA
			f = 40MHz	SM5006AHBS CF5006AHB	–	18	36	
			f = 60MHz, Ta = –20 to 80°C	CF5006AHC	–	25	50	
			f = 60MHz, Ta = –15 to 75°C	SM5006AHCS	–	25	50	
			f = 70MHz, Ta = –20 to 80°C	CF5006AHD	–	32	65	
			f = 70MHz, Ta = –15 to 75°C	SM5006AHDS	–	32	65	
INHN pull-up resistance	R_{UP}	Measurement cct 4			50	–	150	kΩ
Feedback resistance	R_f	Measurement cct 5	SM5006AHAS, CF5006AHA		6.97	8.2	9.43	kΩ
			SM5006AHBS, CF5006AHB		4.76	5.6	6.44	
			SM5006AHCS, CF5006AHC		4.16	4.9	5.64	
			SM5006AHDS, CF5006AHD		2.21	2.6	2.99	
Built-in resistance	R_G	Design value, determined by the R_f value			17	20	23	Ω
	R_D	Design value, determined by the R_f value			17	20	23	
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.			7.44	8	8.56	pF
	C_D	Design value. A monitor pattern on a wafer is tested.			14.88	16	17.12	

Switching Characteristics

5006×N series

3V operation: V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = −20 to 80°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Output rise time	t_{r1}	Measurement cct 3, load cct 1, 0.1V_{DD} to 0.9V_{DD}, C_L = 15pF, Ta = −10 to 70°C	SM5006ANAS, CF5006ANA SM5006ANBS, CF5006ANB SM5006CNCS, CF5006CNC SM5006CNDS, CF5006CND SM5006DNCS, CF5006DNC	–	3.5	7.0	ns
	t_{r2}	Measurement cct 3, load cct 1, 0.1V_{DD} to 0.9V_{DD}, C_L = 15pF	SM5006ANCS, CF5006ANC SM5006ANDS, CF5006AND SM5006ANES, CF5006ANE SM5006ANFS, CF5006ANF SM5006BNCS, CF5006BNC SM5006BNES, CF5006BNE SM5006CNES, CF5006CNE SM5006DNES, CF5006DNE	–	3.5	7.0	
Output fall time	t_{f1}	Measurement cct 3, load cct 1, 0.9V_{DD} to 0.1V_{DD}, C_L = 15pF, Ta = −10 to 70°C	SM5006ANAS, CF5006ANA SM5006ANBS, CF5006ANB SM5006CNCS, CF5006CNC SM5006CNDS, CF5006CND SM5006DNCS, CF5006DNC	–	3.5	7.0	ns
	t_{f2}	Measurement cct 3, load cct 1, 0.9V_{DD} to 0.1V_{DD}, C_L = 15pF	SM5006ANCS, CF5006ANC SM5006ANDS, CF5006AND SM5006ANES, CF5006ANE SM5006ANFS, CF5006ANF SM5006BNCS, CF5006BNC SM5006BNES, CF5006BNE SM5006CNES, CF5006CNE SM5006DNES, CF5006DNE	–	3.5	7.0	
Output duty cycle*1	Duty	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 3.3V, C_L = 15pF, f = 30MHz	SM5006ANAS, CF5006ANA SM5006ANBS, CF5006ANB SM5006ANCS, CF5006ANC SM5006CNCS, CF5006CNC	40	–	60	%
		Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 3.3V, C_L = 15pF, f = 40MHz	SM5006CNDS, CF5006CND SM5006DNCS, CF5006DNC	40	–	60	
		Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 3.3V, C_L = 15pF, f = 50MHz	SM5006ANDS, CF5006AND SM5006BNCS, CF5006BNC	40	–	60	
		Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 3.3V, C_L = 15pF, f = 70MHz	SM5006ANES, CF5006ANE SM5006ANFS, CF5006ANF SM5006BNES, CF5006BNE SM5006CNES, CF5006CNE SM5006DNES, CF5006DNE	40	–	60	
Output disable delay time	t_{PLZ}	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 5V, $C_L \leq$ 15pF		–	–	100	ns
Output enable delay time	t_{PZL}			–	–	100	ns

*1. The duty cycle characteristic is checked the sample chips of each production lot.

5V operation: V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
Output rise time	t_{r1}	Measurement cct 3, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$, C_L = 15pF	SM5006ANAS, CF5006ANA SM5006ANBS, CF5006ANB SM5006CNCS, CF5006CNC SM5006CNDS, CF5006CND SM5006DNCS, CF5006DNC	–	2.0	4.0	ns
			SM5006ANCS, CF5006ANC SM5006ANDS, CF5006AND SM5006BNCS, CF5006BNC SM5006CNES, CF5006CNE SM5006DNES, CF5006DNE	–	1.5	3.0	
	t_{r2}	Measurement cct 3, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$, C_L = 30pF	CF5006ANE CF5006ANF CF5006BNE	–	2.0	4.0	
	t_{r3}	Measurement cct 3, load cct 1, $0.1V_{DD}$ to $0.9V_{DD}$, C_L = 50pF	SM5006ANAS, CF5006ANA SM5006ANBS, CF5006ANB SM5006CNCS, CF5006CNC SM5006CNDS, CF5006CND SM5006DNCS, CF5006DNC	–	4.0	8.0	
			SM5006ANCS, CF5006ANC SM5006ANDS, CF5006AND SM5006BNCS, CF5006BNC SM5006CNES, CF5006CNE SM5006DNES, CF5006DNE	–	3.5	7.0	
			SM5006ANES, CF5006ANE SM5006ANFS, CF5006ANF SM5006BNES, CF5006BNE	–	3.0	6.0	
Output fall time	t_{f1}	Measurement cct 3, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$, C_L = 15pF	SM5006ANAS, CF5006ANA SM5006ANBS, CF5006ANB SM5006CNCS, CF5006CNC SM5006CNDS, CF5006CND SM5006DNCS, CF5006DNC	–	2.0	4.0	ns
			SM5006ANCS, CF5006ANC SM5006ANDS, CF5006AND SM5006BNCS, CF5006BNC SM5006CNES, CF5006CNE SM5006DNES, CF5006DNE	–	1.5	3.0	
	t_{f2}	Measurement cct 3, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$, C_L = 30pF	CF5006ANE CF5006ANF CF5006BNE	–	2.0	4.0	
	t_{f3}	Measurement cct 3, load cct 1, $0.9V_{DD}$ to $0.1V_{DD}$, C_L = 50pF	SM5006ANAS, CF5006ANA SM5006ANBS, CF5006ANB SM5006CNCS, CF5006CNC SM5006CNDS, CF5006CND SM5006DNCS, CF5006DNC	–	4.0	8.0	
			SM5006ANCS, CF5006ANC SM5006ANDS, CF5006AND SM5006BNCS, CF5006BNC SM5006CNES, CF5006CNE SM5006DNES, CF5006DNE	–	3.5	7.0	
			SM5006ANES, CF5006ANE SM5006ANFS, CF5006ANF SM5006BNES, CF5006BNE	–	3.0	6.0	

Parameter	Symbol	Condition			Rating			Unit
					min	typ	max	
Output duty cycle*1	Duty	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 5.0V	f = 30MHz, C_L = 50pF	SM5006ANAS CF5006ANA	45	–	55	%
			f = 40MHz, C_L = 50pF	SM5006ANBS CF5006ANB	45	–	55	
			f = 60MHz, C_L = 50pF	SM5006ANCS CF5006ANC	45	–	55	
			f = 70MHz, C_L = 50pF	SM5006ANDS CF5006AND SM5006BNCS CF5006BNC	45	–	55	
			f = 100MHz, C_L = 30pF	CF5006ANE	45	–	55	
			f = 100MHz, C_L = 15pF	SM5006ANES	45	–	55	
			f = 107MHz, C_L = 30pF	CF5006ANF CF5006BNE	45	–	55	
			f = 107MHz, C_L = 15pF	SM5006ANFS SM5006BNES	45	–	55	
			f = 50MHz, C_L = 50pF	SM5006CNCS CF5006CNC SM5006DNCS CF5006DNC	45	–	55	
			f = 100MHz, C_L = 15pF	SM5006CNES CF5006CNE SM5006DNES CF5006DNE	45	–	55	
			f = 60MHz, C_L = 15pF	SM5006CNCS CF5006CNC	40	–	60	
			f = 70MHz, C_L = 15pF	SM5006CNDS CF5006CND SM5006DNCS CF5006DNC	40	–	60	
Output disable delay time	t_{PLZ}	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 5V, $C_L \leq$ 15pF			–	–	100	ns
Output enable delay time	t_{PZL}				–	–	100	ns

*1. The duty cycle characteristic is checked the sample chips of each production lot.

5006×K series

V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition			Rating min	Rating typ	Rating max	Unit
Output rise time	t_r	Measurement cct 3, load cct 1, 0.4V to 2.4V, V_{DD} = 4.5 to 5.5V		C_L = 15pF	–	2	4	ns
				C_L = 50pF	–	–	7	
Output fall time	t_f	Measurement cct 3, load cct 1, 2.4V to 0.4V, V_{DD} = 4.5 to 5.5V		C_L = 15pF	–	2	4	ns
				C_L = 50pF	–	–	7	
Output duty cycle*1	Duty	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 5.0V, C_L = 15pF	f = 30MHz	SM5006AKAS CF5006AKA	45	–	55	%
			f = 40MHz	SM5006AKBS CF5006AKB	45	–	55	
			f = 60MHz	SM5006AKCS CF5006AKC	40	–	60	
			f = 70MHz	SM5006AKDS CF5006AKD SM5006BKCS CF5006BKC	45	–	55	
			f = 50MHz	SM5006DKCS CF5006DKC	45	–	55	
			f = 70MHz	SM5006CKDS CF5006CKD SM5006DKCS CF5006DKC	40	–	60	
Output disable delay time	t_{PLZ}	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 5V, $C_L \leq$ 15pF			–	–	100	ns
Output enable delay time	t_{PZL}				–	–	100	ns

*1. The duty cycle characteristic is checked the sample chips of each production lot.

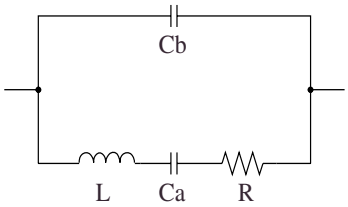
5006AH series

V_{DD} = 4.5 to 5.5V, V_{SS} = 0V, Ta = –40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition			Rating min	Rating typ	Rating max	Unit
Output rise time	t_{r1}	Measurement cct 3, load cct 1, 0.1V_{DD} to 0.9V_{DD}		C_L = 15pF	–	5.0	7.0	ns
	t_{r2}			C_L = 50pF	–	13	21	
Output fall time	t_{f1}	Measurement cct 3, load cct 1, 0.9V_{DD} to 0.1V_{DD}		C_L = 15pF	–	5.0	7.0	ns
	t_{f2}			C_L = 50pF	–	13	21	
Output duty cycle*1	Duty	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 5.0V, C_L = 15pF	f = 30MHz	SM5006AHAS CF5006AHA	45	–	55	%
			f = 40MHz	SM5006AHBS CF5006AHB	45	–	55	
			f = 50MHz	SM5006AHCS CF5006AHC	45	–	55	
			f = 60MHz, Ta = –20 to 80°C	CF5006AHC	40	–	60	
			f = 60MHz, Ta = –15 to 75°C	SM5006AHCS	40	–	60	
			f = 70MHz, Ta = –20 to 80°C	CF5006AHD	40	–	60	
			f = 70MHz, Ta = –15 to 75°C	SM5006AHDS	40	–	60	
Output disable delay time	t_{PLZ}	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 5V, $C_L \leq$ 15pF			–	–	100	ns
Output enable delay time	t_{PZL}				–	–	100	ns

*1. The duty cycle characteristic is checked the sample chips of each production lot.

Current consumption and Output waveform with NPC's standard crystal



f [MHz]	R [Ω]	L [mH]	Ca [fF]	Cb [pF]
30	18.62	16.24	1.733	5.337
40	20.53	11.34	1.396	3.989
50	22.17	7.40	1.370	4.105
70	25.42	4.18	1.254	5.170
100	16.60	3.56	0.726	5.394
107	35.83	2.98	0.732	2.265

FUNCTIONAL DESCRIPTION

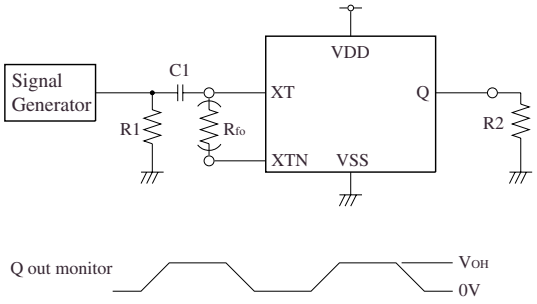
Standby Function

When INHN goes LOW, the oscillator output on Q goes high impedance.

INHN	Q	Oscillator
HIGH (or open)	f_O output frequency	Normal operation
LOW	High impedance	Normal operation

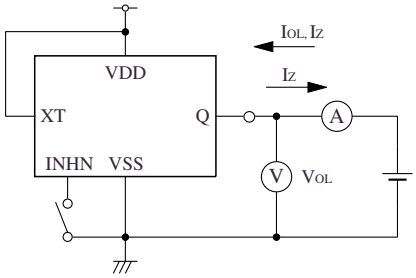
MEASUREMENT CIRCUITS

Measurement cct 1

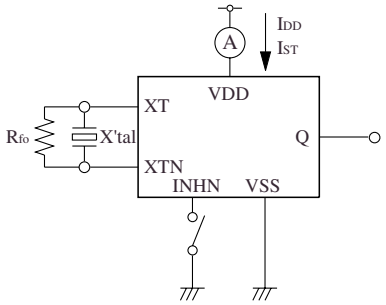


$3.5V_{P-P}$, 10MHz sine wave input signal (5V operation)
$2.0V_{P-P}$, 10MHz sine wave input signal (3V operation)
C1 : 0.001µF
R1 : 50Ω
R2 : 250Ω (5006×N×/5V operation)
275Ω (5006×N×/3V operation)
245Ω (5006AKA, AKB, AKC, CKD, DKC)
250Ω (5006AKD, BKC)
975Ω (5006AH×)
R_{f0} : 2.7kΩ (5006B××, D××)

Measurement cct 2

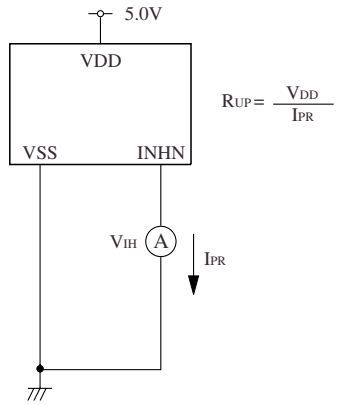


Measurement cct 3

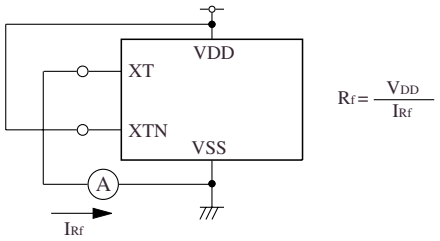


R_{f0} : 2.7kΩ (5006B××, D××)

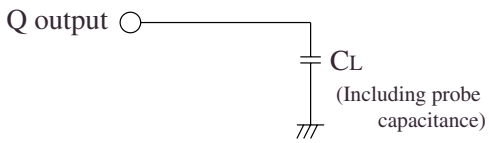
Measurement cct 4



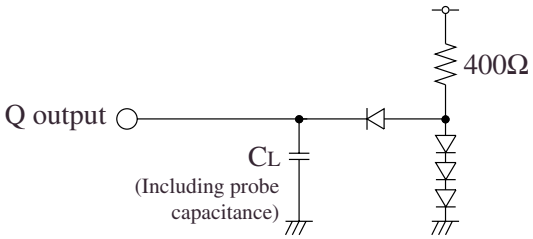
Measurement cct 5



Load cct 1

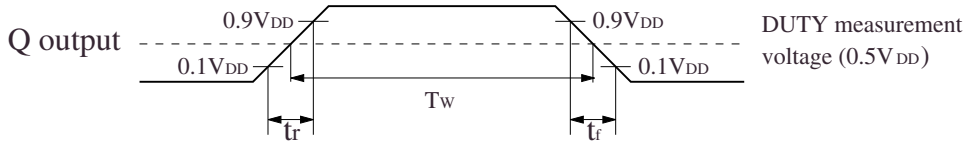


Load cct 2

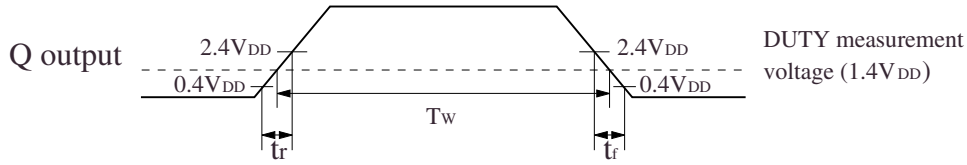


Switching Time Measurement Waveform

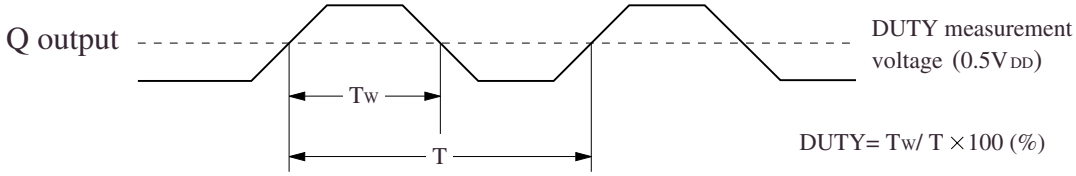
Output duty level (CMOS)



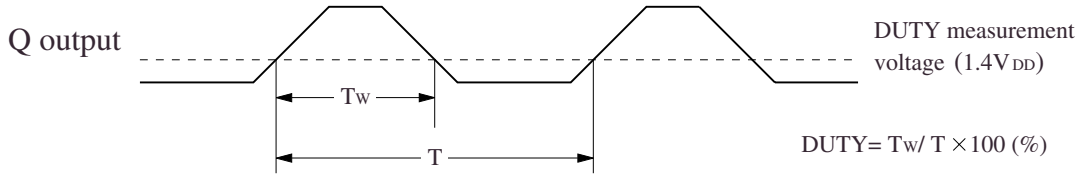
Output duty level (TTL)



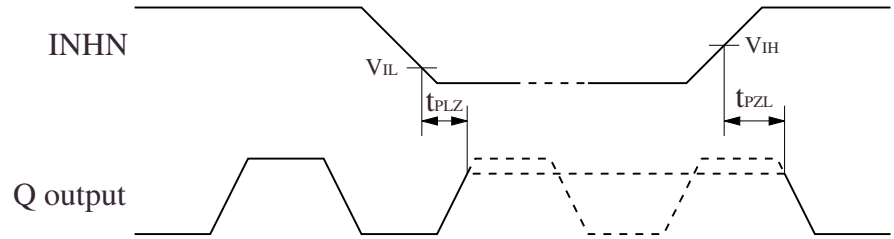
Output duty cycle (CMOS)



Output duty cycle (TTL)



Output Enable/Disable Delay



INHN input waveform $t_r = t_f \leq 10ns$

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