TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

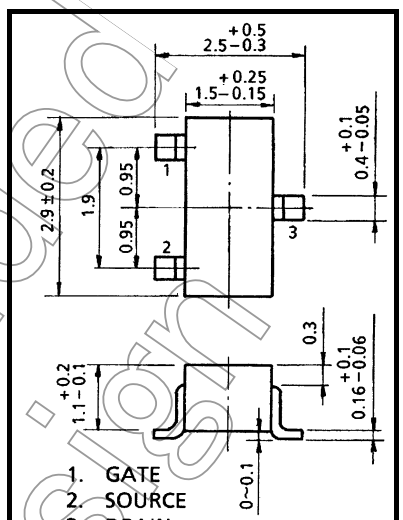
SSM3J02F

Power Management Switch

High Speed Switching Applications

- Small package
- Low on resistance : R_{on} = 0.5 Ω (max) (@V_{GS} = −4 V)
  : R_{on} = 0.7 Ω (max) (@V_{GS} = −2.5 V)
- Low gate threshold voltage

Unit: mm



JEDEC	TO-236MOD
JEITA	SC-59
TOSHIBA	2-3F1F

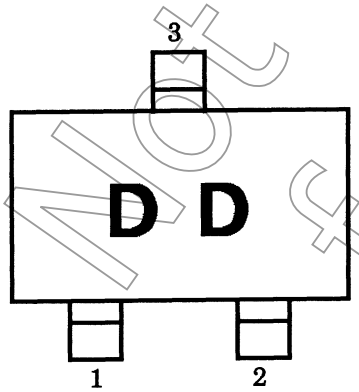
Weight: 0.012 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

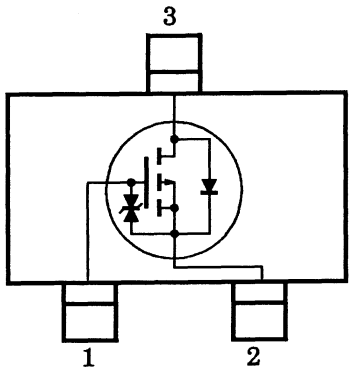
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	−30	V
Gate-source voltage		V_{GSS}	±10	V
Drain current	DC	I_D	−600	mA
	Pulse	I_{DP}	−1200	
Drain power dissipation (Ta = 25°C)		P_D	200	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Marking



Equivalent Circuit



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

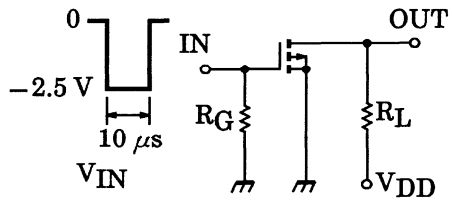
Not Recommended for New Design

Electrical Characteristics (Ta = 25°C)

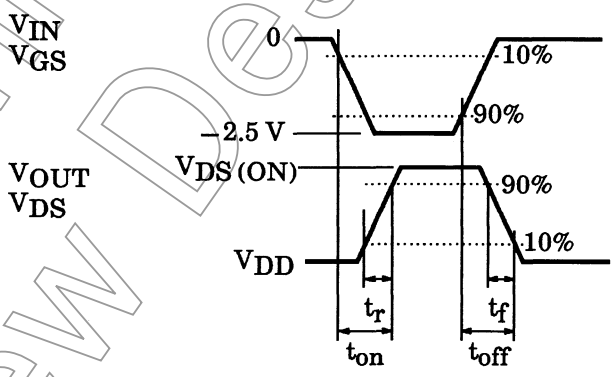
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±1	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = −30 V, V_{GS} = 0	—	—	−1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −0.1 mA	−0.6	—	−1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = −0.3 A (Note)	0.6	—	—	S
Drain-source ON resistance		$R_{DS\ (ON)}$	I_D = −0.3 A, V_{GS} = −4 V (Note)	—	0.4	0.5	Ω
			I_D = −0.3 A, V_{GS} = −2.5 V (Note)	—	0.55	0.7	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	150	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	21	—	pF
Output capacitance		C_{oss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	61	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = −15 V, I_D = −0.3 A, V_{GS} = 0~−2.5 V, R_G = 4.7 Ω	—	55	—	ns
	Turn-off time	t_{off}		—	52	—	

Note: Pulse test

Switching Time Test Circuit



V_{DD} = −15 V
R_G = 4.7 Ω
D.U. ≦ 1%
V_{IN} : t_r, t_f < 5 ns
COMMON SOURCE
Ta = 25°C



Precaution

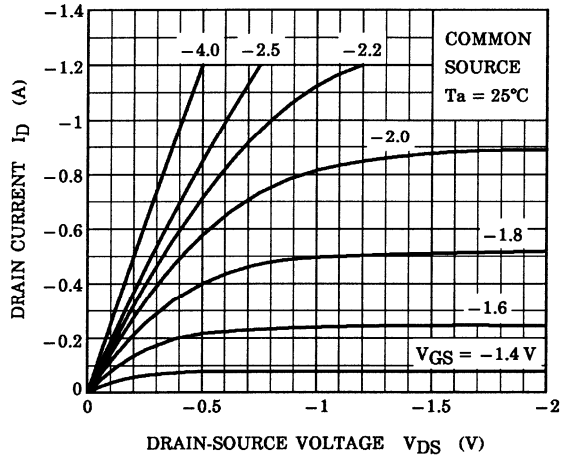
V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = −100 μA for this product. For normal switching operation, $V_{GS\ (ON)}$ requires higher voltage than V_{th} and $V_{GS\ (off)}$ requires lower voltage than V_{th}.

(Relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (ON)}$)

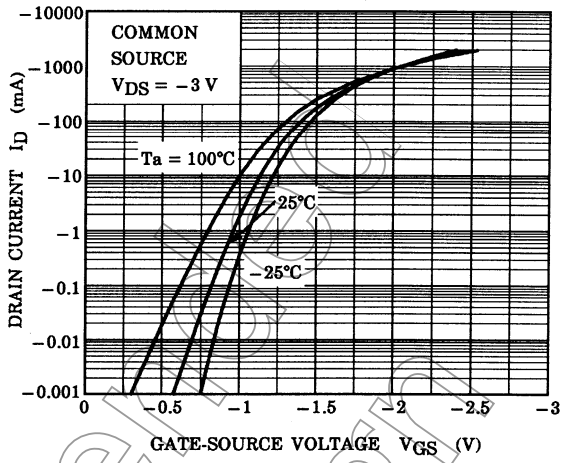
Please take this into consideration for using the device.

Not Recommended for New Design

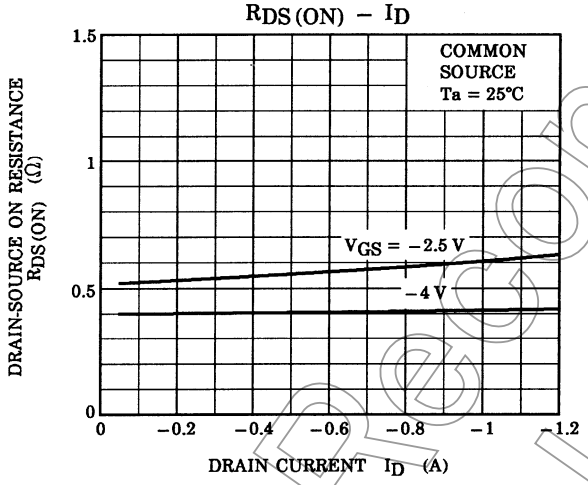
$I_D - V_{DS}$



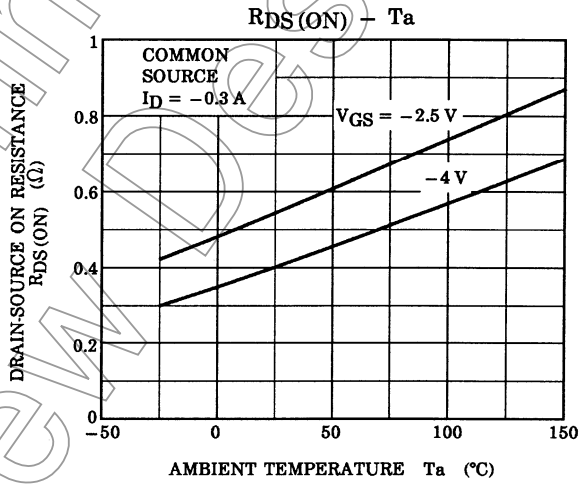
$I_D - V_{GS}$



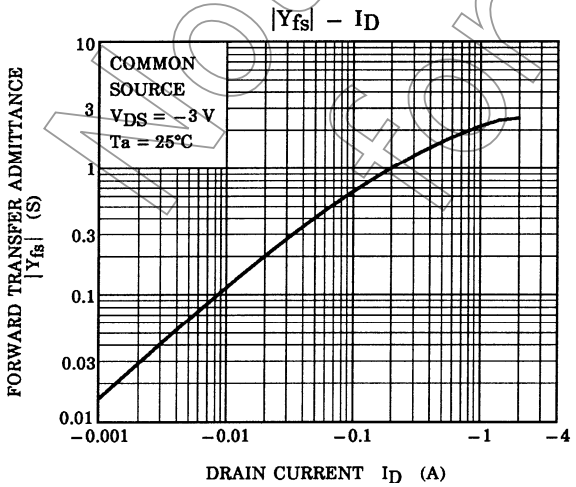
$R_{DS(ON)} - I_D$



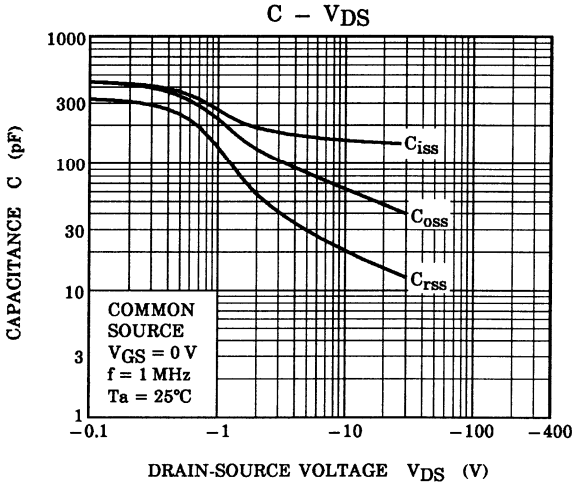
$R_{DS(ON)} - Ta$



$|Y_{fs}| - I_D$



$C - V_{DS}$



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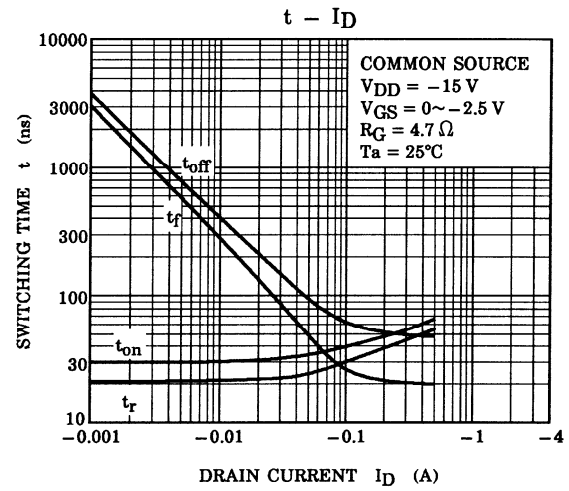

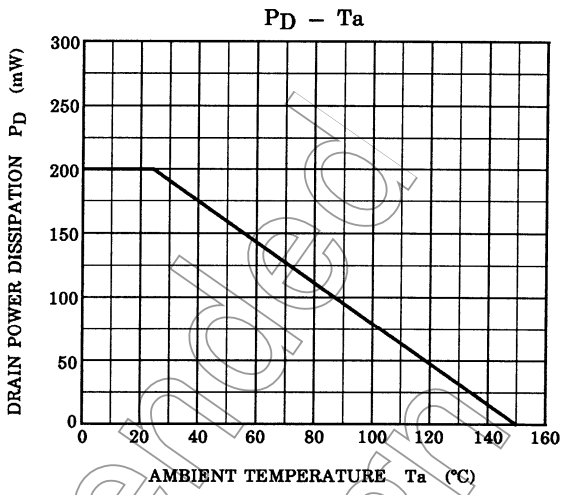

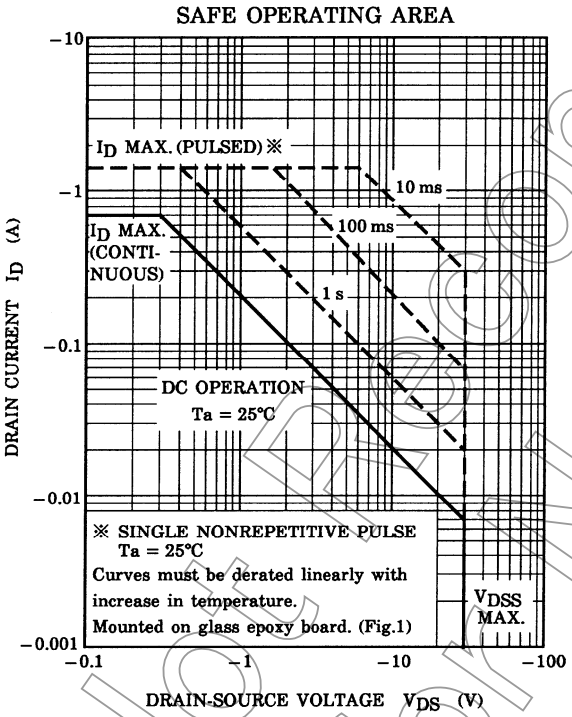

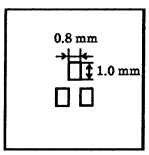

Figure 1 25.4 mm × 25.4 mm × 1.6 t (a Cu pad of 0.8 mm^2 area)

Not Recommended for New Design

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