OVERVIEW

The SM5002L series crystal oscillator module ICs fabricated in NPC's Molybdenum-gate CMOS. They comprise low-voltage low-current consumption oscillator circuits and output buffers. They incorporate built-in oscillation capacitance with superior frequency response to realize stable 3rd overtone oscillation without any external components.

FEATURES

- Oscillation frequency up to 100MHz
- 3rd overtone oscillation
- 2.7 to 3.6V supply voltage
- Capacitors C_G and C_D built-in
- Inverter amplifier feedback resistance built-in
- CMOS input level
- Output three-state function
- Standby function (oscillator stops)
- 3µA (typ) low standby current
- 8mA (V_{DD} = 3.0V) output drive capability
- Oscillator frequency output
- CMOS output duty level
- INHN pin pull-up resistance built-in
  - INHN = L: 2MΩ typ
  - INHN = H: 90kΩ typ
- 8-pin SOP (SM5002L×S)
- Chip form (CF5002L×)

SERIES CONFIGURATION

Version	Recommended operating frequency range[1] [MHz]	gm ratio	Built-in capacitance		R_{f1} [kΩ]	C_f [pF]	Output duty level	Output current [mA]	Standby function
			C_G [pF]	C_D [pF]					
CF5002LA SM5002LAS	30 to 40	1.0	8	15	5.6	22	CMOS	8	Yes
CF5002LB SM5002LBS	40 to 60	1.5	8	15	4.7	22	CMOS	8	Yes
CF5002LC SM5002LCS	50 to 70	1.5	8	10	3.9	22	CMOS	8	Yes
CF5002LD SM5002LDS	70 to 90	2.0	8	10	3.9	22	CMOS	8	Yes
CF5002LE SM5002LES	85 to 100	2.0	8	10	2.7	22	CMOS	8	Yes
CF5002LF SM5002LFS	25 to 30	1.0	10	15	8.5	22	CMOS	8	Yes

1. The recommended operating frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillator frequency band is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

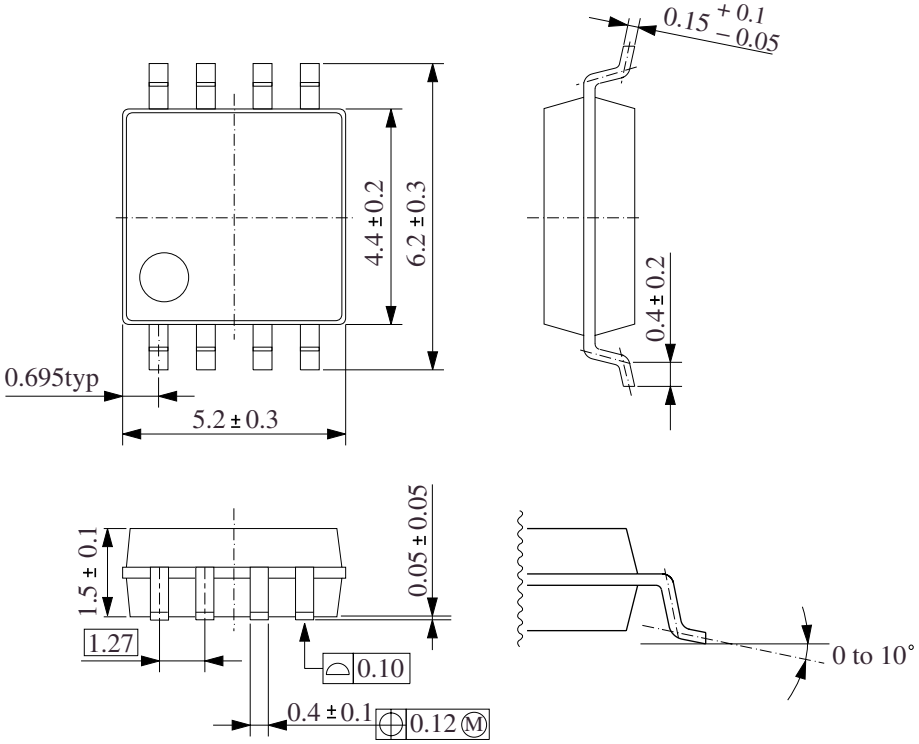
ORDERING INFORMATION

Device	Package
SM5002L×S	8-pin SOP
CF5002L×–1	Chip form
CF5002L×–2	

PACKAGE DIMENSIONS

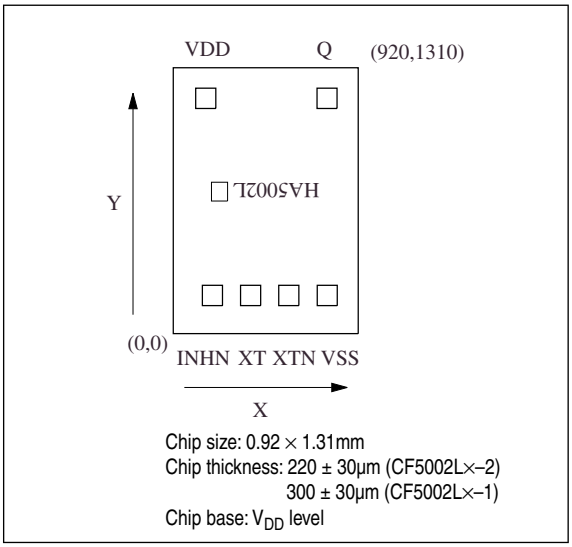
(Unit: mm)

• 8-pin SOP



PAD LAYOUT

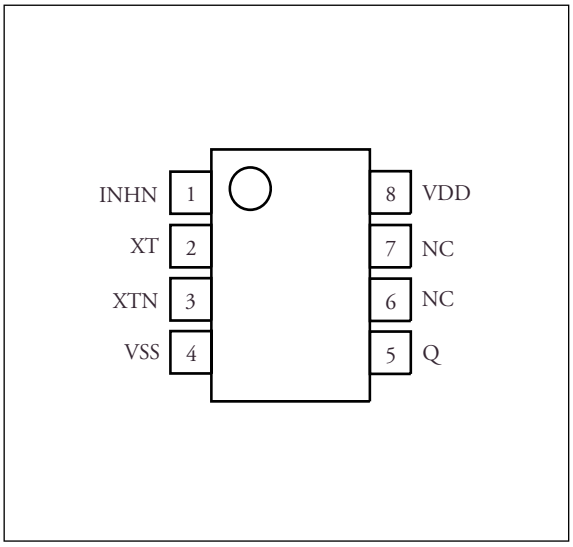
(Unit: µm)



Chip size: 0.92 × 1.31mm
Chip thickness: 220 ± 30µm (CF5002L×–2)
300 ± 30µm (CF5002L×–1)
Chip base: V_{DD} level

PINOUT

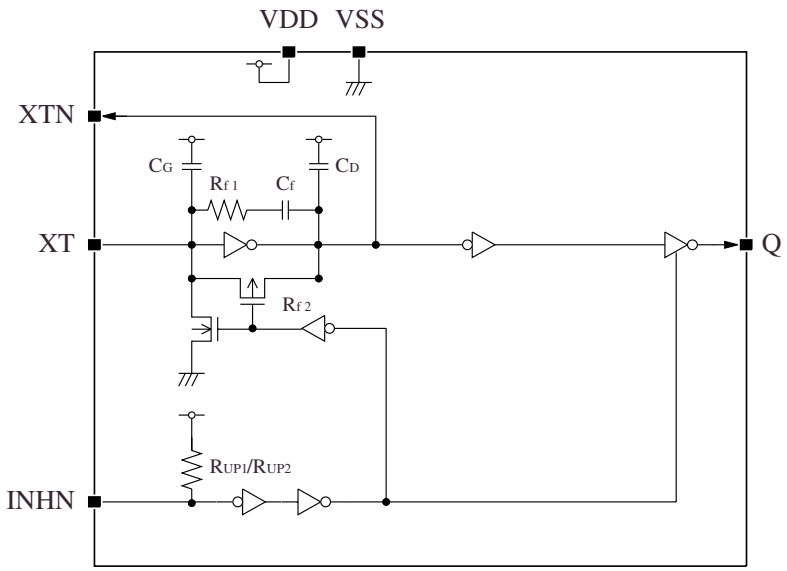
(Top view)



PIN DESCRIPTION and PAD DIMENSIONS

Number	Name	I/O	Description		Pad dimensions [µm]	
					X	Y
1	INHN	I	Output state control input. Oscillator stopped when LOW. Power-saving pull-up resistor built in		195	188
2	XT	I	Amplifier input.	Crystal oscillator connection pins. Crystal oscillator connected between XT and XTN	385	188
3	XTN	O	Amplifier output.		575	188
4	VSS	–	Ground		766	188
5	Q	O	Output. Output frequency. High impedance at standby operation		765	1159
6	NC	–	No connection		–	–
7	NC	–	No connection		–	–
8	VDD	–	Supply voltage		162	1159

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.5 to 7.0	V
Input voltage range	V_{IN}		–0.5 to V_{DD} + 0.5	V
Output voltage range	V_{OUT}		–0.5 to V_{DD} + 0.5	V
Operating temperature range	T_{opr}		–40 to 85	°C
Storage temperature range	T_{stg1}	Chip form	–65 to 150	°C
	T_{stg2}	8-pin SOP	–40 to 125	
Output current	I_{OUT}		25	mA
Power dissipation	P_D	Ta ≤ 85°C, 8-pin SOP	200	mW

Recommended Operating Conditions

CF5002L× series (Chip form)

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Units
			min	typ	max	
Supply voltage	V_{DD}	C_L ≤ 15pF, f ≤ 70MHz	2.7	–	3.6	V
		C_L ≤ 15pF, 70 < f ≤ 100MHz	3.0	–	3.6	V
		C_L ≤ 30pF, f ≤ 70MHz	3.0	–	3.6	V
Input voltage	V_{IN}		V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}		–20	–	80	°C

SM5002L×S series (8-pin SOP)

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Units
			min	typ	max	
Supply voltage	V_{DD}	C_L ≤ 15pF, f ≤ 50MHz	2.7	–	3.6	V
		C_L ≤ 15pF, 50 < f ≤ 70MHz	3.0	–	3.6	V
		C_L ≤ 30pF, f ≤ 50MHz	3.0	–	3.6	V
Input voltage	V_{IN}		V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}		–20	–	80	°C

Electrical Characteristics

V_{DD} = 2.7 to 3.6V, V_{SS} = 0V, Ta = –20 to 80°C, unless otherwise noted.

Parameter	Symbol	Conditions		Rating min	Rating typ	Rating max	Units
HIGH-level output voltage	V_{OH}	Q: Measurement cct 1, V_{DD} = 2.7V, I_{OH} = 8mA		2.2	2.4	–	V
LOW-level output voltage	V_{OL}	Q: Measurement cct 2, V_{DD} = 2.7V, I_{OL} = 8mA		–	0.3	0.4	V
Output leakage current	I_Z	Q: Measurement cct 2, INHN = LOW, V_{DD} = 3.6V	$V_{OH} = V_{DD}$	–	–	10	µA
			$V_{OL} = V_{SS}$	–	–	10	µA
HIGH-level input voltage	V_{IH}	INHN pin		$0.7V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	INHN pin		–	–	$0.3V_{DD}$	V
Current consumption	I_{DD}	INHN = open, Measurement cct 3, load cct 1, V_{DD} = 3.0 to 3.6V	SM5002LAS, CF5002LA SM5002LFS, CF5002LF C_L = 30pF, f = 30MHz	–	10	18	mA
			SM5002LBS, CF5002LB C_L = 30pF, f = 50MHz	–	15	25	mA
			SM5002LCS, CF5002LC C_L = 30pF, f = 70MHz	–	20	35	mA
			SM5002LDS, CF5002LD SM5002LES, CF5002LE C_L = 15pF, f = 100MHz	–	25	45	mA
Standby current	I_{ST}	INHN = LOW, Measurement cct 3		–	3	10	µA
INHN pull-up resistance	R_{UP1}	Measurement cct 4, INHN = LOW		0.4	–	4	MΩ
	R_{UP2}	Measurement cct 4, INHN = $0.7V_{DD}$		50	–	150	kΩ
AC feedback resistance	R_{f1}	Design value. A monitor pattern on a wafer is tested.	SM5002LAS, CF5002LA	4.7	5.6	6.5	kΩ
			SM5002LBS, CF5002LB	4.0	4.7	5.4	kΩ
			SM5002LCS, CF5002LC SM5002LDS, CF5002LD	3.3	3.9	4.5	kΩ
			SM5002LES, CF5002LE	2.2	2.7	3.2	kΩ
			SM5002LFS, CF5002LF	7.2	8.5	9.8	kΩ
DC feedback resistance	R_{f2}	Measurement cct 5		50	–	150	kΩ
AC feedback capacitance	C_f	Design value. A monitor pattern on a wafer is tested.		19.8	22	24.2	pF
Built-in capacitance	C_G	Design value. A monitor pattern on a wafer is tested.	SM5002LAS, CF5002LA SM5002LBS, CF5002LB SM5002LCS, CF5002LC SM5002LDS, CF5002LD SM5002LES, CF5002LE	7.2	8	8.8	pF
			SM5002LFS, CF5002LF	9	10	11	pF
	C_D		SM5002LAS, CF5002LA SM5002LBS, CF5002LB SM5002LFS, CF5002LF	13.5	15	16.5	pF
			SM5002LCS, CF5002LC SM5002LDS, CF5002LD SM5002LES, CF5002LE	9	10	11	pF

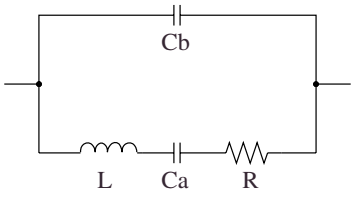
Switching Characteristics

V_{SS} = 0V, Ta = −20 to 80°C unless otherwise noted.

Parameter	Symbol	Conditions		Rating min	Rating typ	Rating max	Units
Output rise time	t_{r1}	Measurement cct 3, load cct 1, $0.1V_{DD} \rightarrow 0.9V_{DD}$	V_{DD} = 2.7 to 3.6V, C_L = 15pF	–	2	4	ns
	t_{r2}		V_{DD} = 3.0 to 3.6V, C_L = 30pF	–	2.5	5	ns
Output fall time	t_{f1}	Measurement cct 3, load cct 1, $0.9V_{DD} \rightarrow 0.1V_{DD}$	V_{DD} = 2.7 to 3.6V, C_L = 15pF	–	2	4	ns
	t_{f2}		V_{DD} = 3.0 to 3.6V, C_L = 30pF	–	2.5	5	ns
Output duty cycle[1]	DUTY	Measurement cct 3, load cct 1, Ta = 25°C, V_{DD} = 3.0V	SM5002LAS, SM5002LFS CF5002LA, CF5002LF C_L = 30pF, f = 30MHz	45	–	55	%
			SM5002LBS, CF5002LB C_L = 30pF, f = 50MHz	45	–	55	%
			SM5002LCS, CF5002LC C_L = 30pF, f = 70MHz	45	–	55	%
			SM5002LDS, SM5002LES C_L = 15pF, f = 100MHz	40	–	60	%
			CF5002LD, CF5002LE C_L = 15pF, f = 100MHz	45	–	55	%
Output disable delay time[2]	t_{PLZ}	Measurement cct 6, Ta = 25°C, V_{DD} = 2.7V, load $C_L \leq$ 15pF		–	–	100	ns
Output enable delay time[2]	t_{PZL}			–	–	100	ns

1. The duty cycle characteristic is checked the sample chips of each production lot.
2. Oscillator stop function is built-in. When INHN goes LOW, normal output stops. When INHN goes HIGH, normal output is not resumed until after the oscillator start-up time has elapsed.

Current consumption and Output waveform with NPC's standard crystal



f [MHz]	R [Ω]	L [mH]	Ca [fF]	Cb [pF]
30	18.62	16.24	1.733	5.337
50	22.17	7.40	1.370	4.105
70	25.42	4.18	1.254	5.170
100	16.60	3.56	0.726	5.394

FUNCTIONAL DESCRIPTION

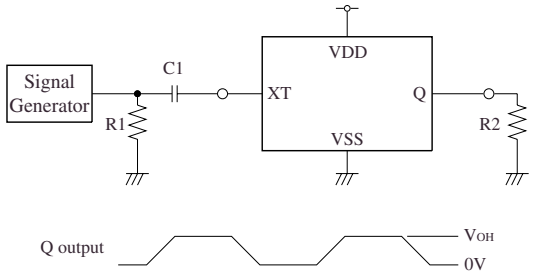
Standby Function

The oscillator stops when INHN goes LOW. When the oscillator stops, the oscillator output on Q goes high impedance.

INHN	Q	Oscillator
HIGH (or open)	f_O output frequency	Normal operation
LOW	High impedance	Stopped

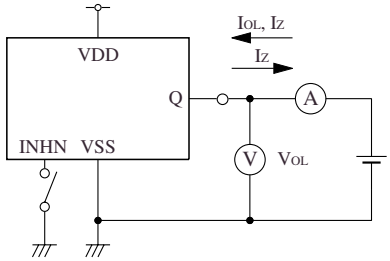
MEASUREMENT CIRCUITS

Measurement cct 1

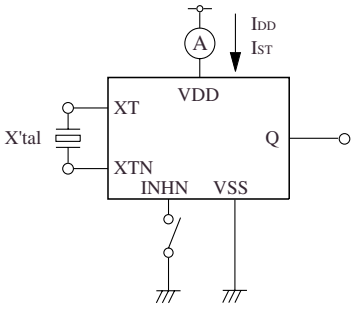


$2.5V_{P-P}$, 10MHz sine wave input signal
C1 : 0.001µF
R1 : 50Ω
R2 : 275Ω

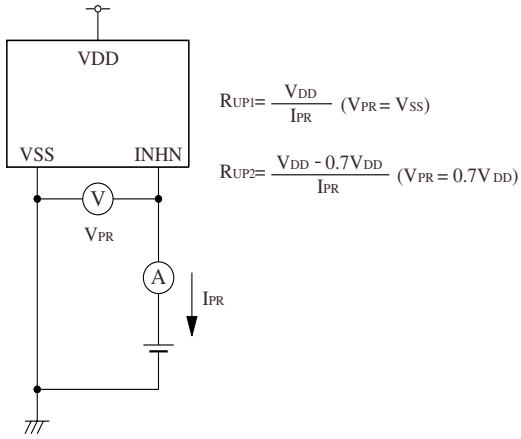
Measurement cct 2



Measurement cct 3



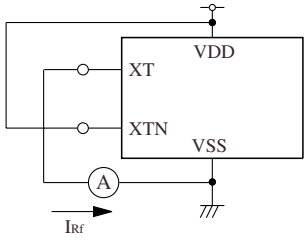
Measurement cct 4



$$R_{UP1} = \frac{V_{DD}}{I_{PR}} \quad (V_{PR} = V_{SS})$$

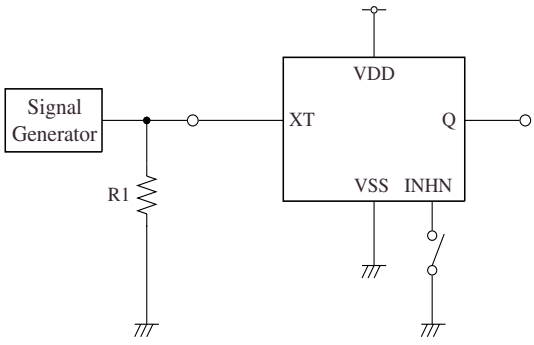
$$R_{UP2} = \frac{V_{DD} - 0.7V_{DD}}{I_{PR}} \quad (V_{PR} = 0.7V_{DD})$$

Measurement cct 5



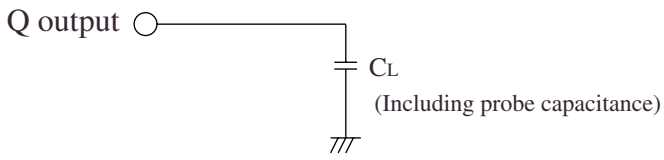
$$R_{f2} = \frac{V_{DD}}{I_{Rf}}$$

Measurement cct 6



R1 : 50Ω

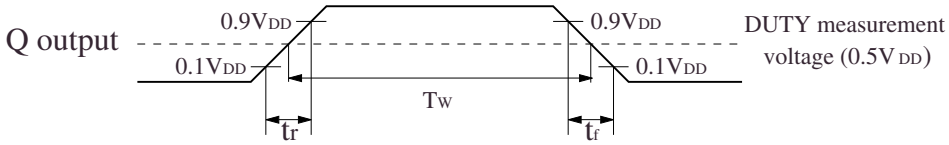
Load cct 1



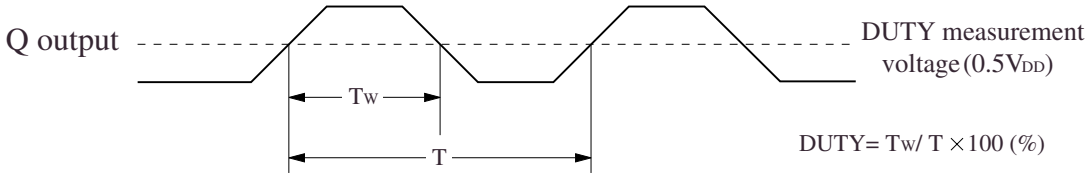
C_L = 15pF: t_{r1}, t_{f1} /DUTY, I_{DD} (70MHz < f ≤ 100MHz)
C_L = 30pF: t_{r2} , t_{f2} /DUTY, I_{DD} (f ≤ 70MHz)

Switching Time Measurement Waveform

Output duty level (CMOS)

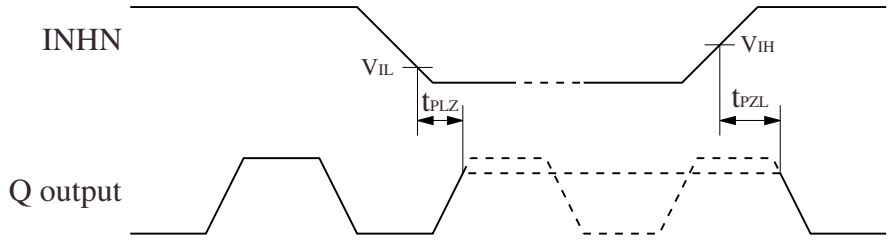


Output duty cycle (CMOS)



Output Enable/Disable Delay

The following figure shows the oscillator timing during normal operation. Note that when the device is in standby, the oscillator stops. When standby is released, the oscillator starts and stable oscillator output occurs after a short delay.



INHN inputwaveform tr = tf ≤ 10ns

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