

# RNA51xx Series

## CMOS system-RESET IC

REJ03D0505-0200

Rev.2.00

Sep 13, 2007

### General Description

The RNA51xx series provide system reset signal for microprocessor and electrical systems.

Threshold voltage is 1.4 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.4 V, 4.5 V, 4.6 V, 5.0 V and accuracy is  $\pm 1.0\%$ .

The reset output delay time can be set by external capacitor connected to CD pin.

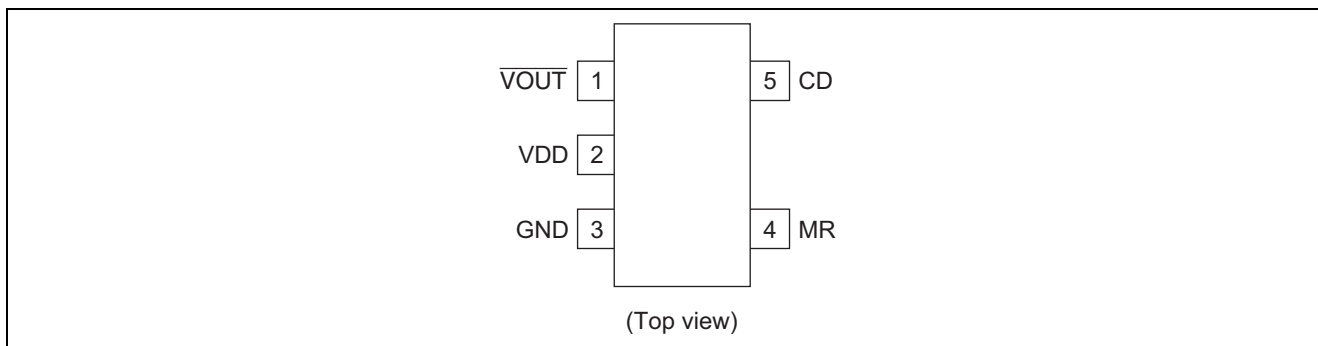
Manual reset input is available and input resistance is 2 M $\Omega$  typ.

This series have two output types (active-low CMOS output and active-low open-drain output).

### Features

- Threshold voltage: 1.4 V, 2.6 V, 2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 4.4 V, 4.5 V, 4.6 V, 5.0 V
- Threshold voltage accuracy:  $\pm 1.0\%$
- Threshold voltage hysteresis: 5% typ.
- Low supply current: 0.7  $\mu$ A typ.
- Capacitor-adjustable output delay time
- Manual reset
- $\overline{\text{VOUT}}$  CMOS output, or open-drain output
- 5-pin SOT-23 package
- Temperature range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

### Pin Arrangement



### Applications

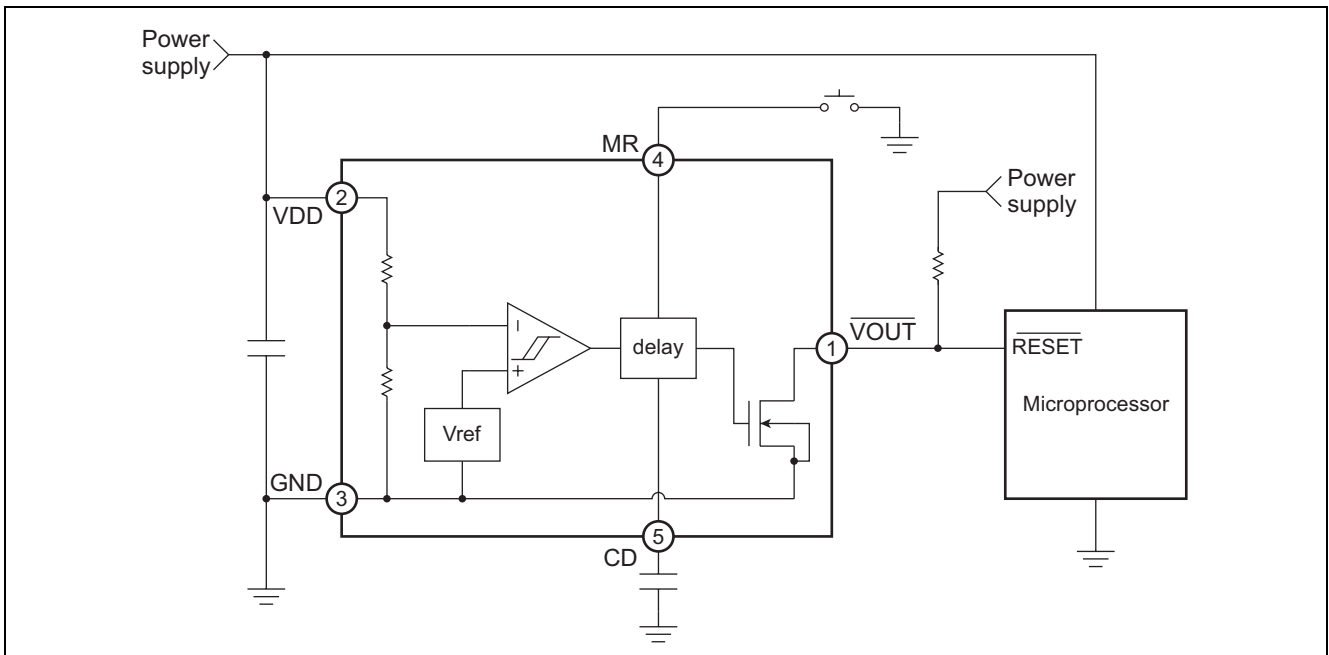
- Power supply voltage monitoring for microprocessors
- Battery-powered portable equipment
- Computers and notebook computers
- Wireless Communication Systems
- Digital still camera, digital video camera, PDA

## Product list

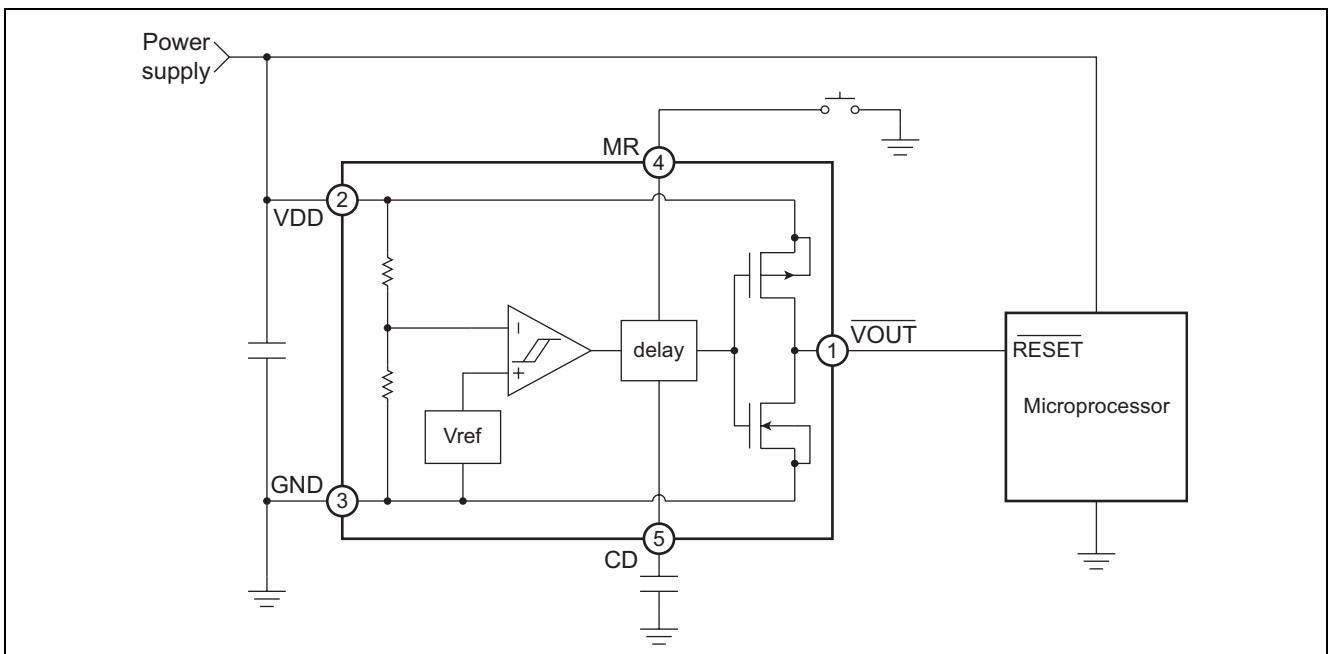
Threshold Voltage $-V_{TH}$ [V]	VOUT	
	Open-Drain output	CMOS output
1.4	—	RNA51B14FLP
2.6	RNA51A26FLP	—
2.7	RNA51A27FLP	RNA51B27FLP
2.8	RNA51A28FLP	—
2.9	RNA51A29FLP	—
3.0	RNA51A30FLP	—
3.1	RNA51A31FLP	—
4.4	RNA51A44FLP	—
4.5	RNA51A45FLP	—
4.6	RNA51A46FLP	—
5.0	—	RNA51B50FLP

## Functional block diagram & typical application circuit

### (1) RNA51Axx Products

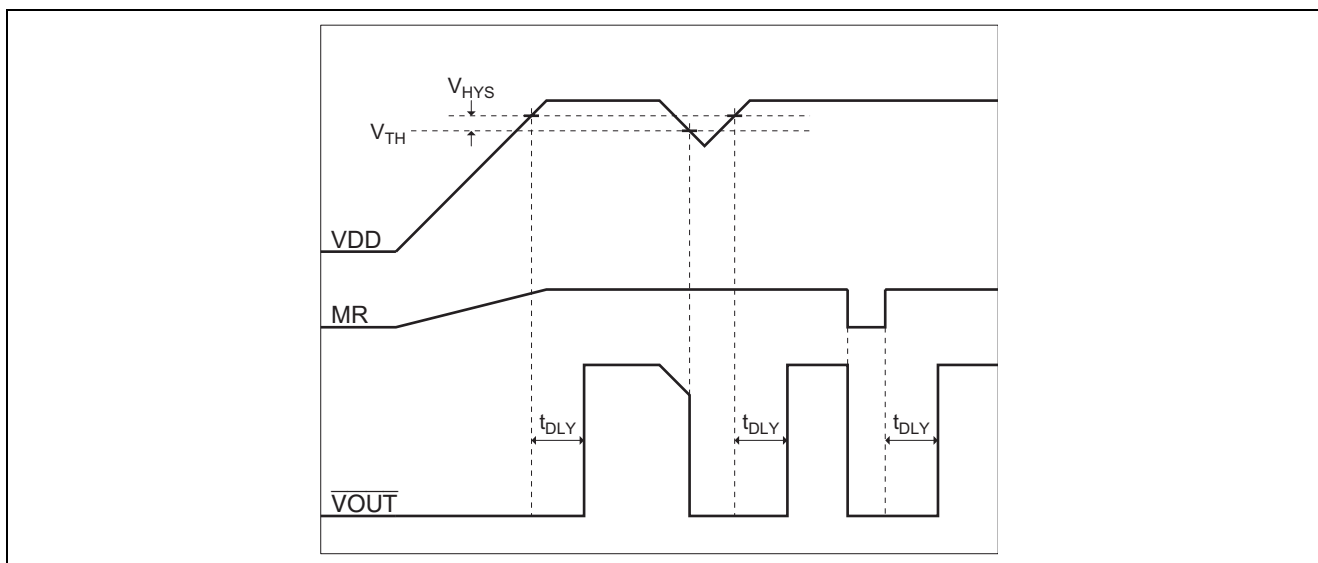


### (2) RNA51Bxx Products



- Notes:
1. It is good for stable operation to use a decoupling capacitor with excellent high frequency characteristics between VDD and GND pin.
  2. Capacitor value is determined by system conditions.

## Timing Diagram



## Absolute Maximum Ratings

### (1) RNA51Axx Products

Temperature condition Ta = 25°C

Item	Symbol	Pin	Ratings	Unit
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	6.0	V
Output voltage	V <sub>OUT</sub>	$\bar{V}_{OUT}$	-0.3 to 6.0	V
Input voltage	V <sub>IN</sub>	MR, MD	-0.3 to V <sub>DD</sub> +0.3	V
Output current	I <sub>OUT</sub>	V <sub>OUT</sub>	±50	mA
Continuous power dissipation	P <sub>D</sub>	—	120	mW
Operating temperature range	T <sub>OPR</sub>	—	-40 to +85	°C
Storage temperature range	T <sub>STG</sub>	—	-55 to +125	°C

### (2) RNA51Bxx Products

Temperature condition Ta = 25°C

Item	Symbol	Pin	Ratings	Unit
Supply voltage	V <sub>DD</sub>	V <sub>DD</sub>	6.0	V
Output voltage	V <sub>OUT</sub>	$\bar{V}_{OUT}$	-0.3 to V <sub>DD</sub> +0.3	V
Input voltage	V <sub>IN</sub>	MR, MD	-0.3 to V <sub>DD</sub> +0.3	V
Output current	I <sub>OUT</sub>	V <sub>OUT</sub>	±50	mA
Continuous power dissipation	P <sub>D</sub>	—	120	mW
Operating temperature range	T <sub>OPR</sub>	—	-40 to +85	°C
Storage temperature range	T <sub>STG</sub>	—	-55 to +125	°C

## Electrical characteristics

## (1) RNA51Axx Products

Temperature condition Ta = 25°C

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V <sub>DD</sub>	1.1	—	5.5	V	pull-up resistor = 470 kΩ V <sub>OUT</sub> ≤ 0.1×V <sub>DD</sub>
Supply current	I <sub>DD</sub>	—	0.7	4.2	μA	V <sub>DD</sub> = 5.5 V
Threshold voltage	-V <sub>TH</sub>	-V <sub>TH</sub> ×0.99	—	-V <sub>TH</sub> ×1.01	V	
Temperature coefficient of the threshold voltage (Reference value)	$\frac{\Delta(-V_{TH})}{-V_{TH} \cdot \Delta Ta}$	—	±100	—	ppm/°C	Ta = -40 to 85°C
Threshold voltage hysteresis	V <sub>HYS</sub>	-V <sub>TH</sub> ×3%	-V <sub>TH</sub> ×5%	-V <sub>TH</sub> ×8%	V	
VO <sub>UT</sub> low-level output current	I <sub>OL</sub>	0.2 3.4	1.2 7.0	—	mA	V <sub>OUT</sub> = 0.5 V V <sub>DD</sub> = 1.3 V V <sub>DD</sub> = 2.4 V (-V <sub>TH</sub> ≥ 2.7 V)
VO <sub>UT</sub> Output leakage current (open drain output)	I <sub>LEAK</sub>	—	—	0.1	μA	V <sub>DD</sub> = V <sub>OUT</sub> = 5.5 V
Delay time <sup>Note1</sup>	t <sub>DLY</sub>	10	20	35	ms	V <sub>DD</sub> = 1.1 to 5.5V, t <sub>TLH</sub> = 1 μs C <sub>D</sub> = 4.7 nF
MR Low-level input voltage <sup>Note2</sup>	V <sub>IL</sub>	—	—	V <sub>DD</sub> ×0.25	V	
MR High-level input voltage	V <sub>IH</sub>	V <sub>DD</sub> ×0.75	—	—	V	
MR internal pull-up resistance	R <sub>MR</sub>	1	2	7	MΩ	

## (2) RNA51Bxx Products

Temperature condition Ta = 25°C

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V <sub>DD</sub>	1.1	—	5.5	V	pull-up resistor = 470 kΩ V <sub>OUT</sub> ≤ 0.1×V <sub>DD</sub>
Supply current	I <sub>DD</sub>	—	0.7	4.2	μA	V <sub>DD</sub> = 5.5 V
Threshold voltage	-V <sub>TH</sub>	-V <sub>TH</sub> ×0.99	—	-V <sub>TH</sub> ×1.01	V	
Threshold voltage temperature dependency (Reference value for design)	$\frac{\Delta(-V_{TH})}{-V_{TH} \cdot \Delta Ta}$	—	±100	—	ppm/°C	Ta = -40 to 85°C
Threshold voltage hysteresis	V <sub>HYS</sub>	-V <sub>TH</sub> ×3%	-V <sub>TH</sub> ×5%	-V <sub>TH</sub> ×8%	V	
VO <sub>UT</sub> low-level output current	I <sub>OL</sub>	0.2 3.4	1.2 7.0	—	mA	V <sub>OUT</sub> = 0.5 V V <sub>DD</sub> = 1.3 V V <sub>DD</sub> = 2.4 V (-V <sub>TH</sub> ≥ 2.7 V)
VO <sub>UT</sub> High-level output current (CMOS output)	I <sub>OH</sub>	-1.4 -1.5	-2.7 -3.0	—	mA	V <sub>OUT</sub> = V <sub>DD</sub> -0.5 V V <sub>DD</sub> = 4.5 V (-V <sub>TH</sub> ≤ 4.0 V) V <sub>DD</sub> = 5.5 V
Delay time <sup>Note1</sup>	t <sub>DLY</sub>	10	20	35	ms	V <sub>DD</sub> = 1.1 to 5.5 V, t <sub>TLH</sub> = 1 μs C <sub>D</sub> = 4.7 nF
MR Low-level input voltage <sup>Note2</sup>	V <sub>IL</sub>	—	—	V <sub>DD</sub> ×0.25	V	
MR High-level input voltage	V <sub>IH</sub>	V <sub>DD</sub> ×0.75	—	—	V	
MR internal pull-up resistance	R <sub>MR</sub>	1	2	7	MΩ	

- Note: 1. Delay time is specified when charging starts in the condition that CD pin is completely discharged. When discharging of CD pin is not complete because of immediate stop and other reasons, the delay time is not guaranteed. Therefore, when passing of V<sub>DD</sub> pin input voltage immediately stops (the period of condition that V<sub>DD</sub> pin input voltage is lower than the detected voltage is short), discharging of external capacitor CD is inadequate, and the delay time becomes much shorter than the minimum guaranteed value. Be sure to fully check that there are no problems as the system.
2. Minimum value of low-pulse width to be input to MR pin depends on the value of external capacitor CD. Therefore, set the low-pulse width to be input to MR pin to the minimum input low-pulse width shown in figure 1 or more.

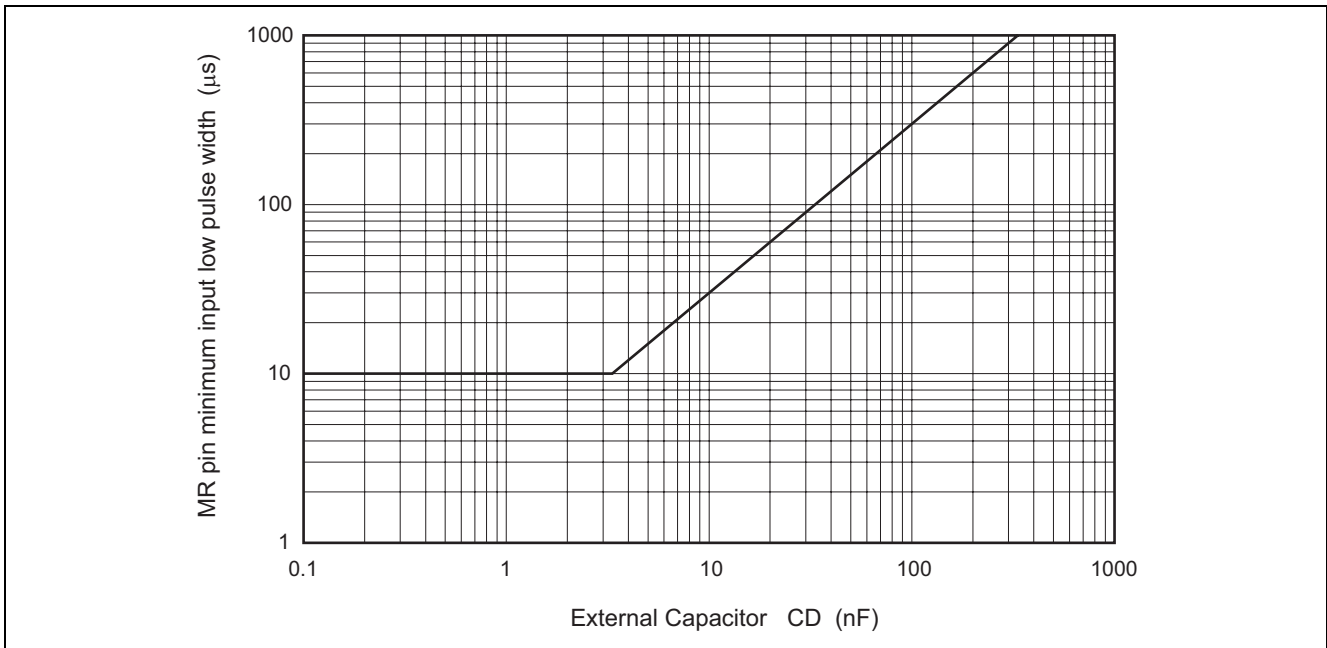


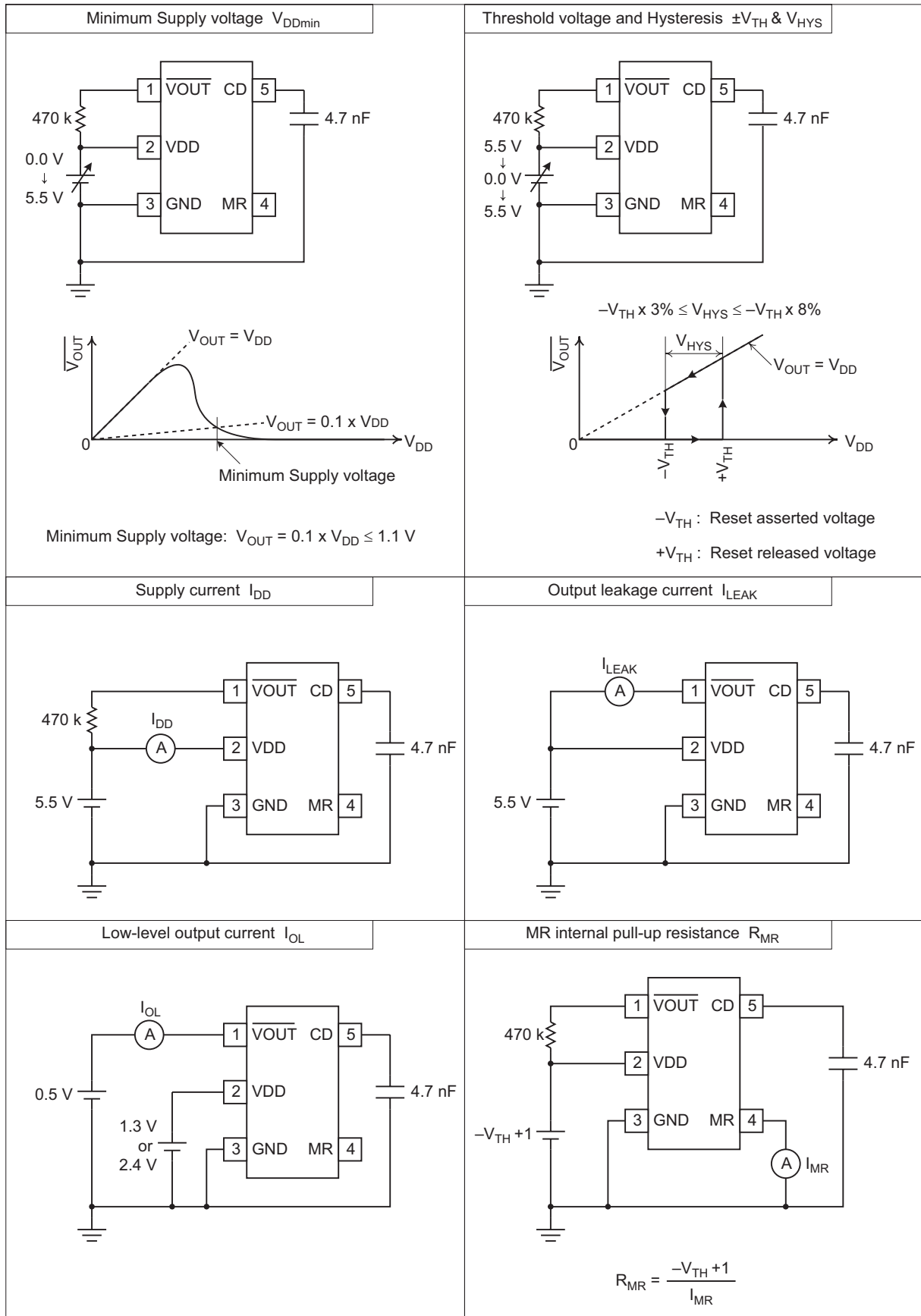
Figure 1 Dependence of MR pin minimum input low pulse width and external capacitor CD

Pin Description

PIN	NAME	FUNCTION
1	$\overline{VOUT}$	$\overline{VOUT}$ changes from high to low whenever VDD drops below $-V_{TH}$ . A pull-up resistor from 470 kΩ to 1 MΩ should be used on this pin for open-drain output.
2	VDD	Supply voltage and input for voltage detector. A decoupling capacitor with excellent high frequency characteristics should be placed near VDD pin and connected between VDD and GND pin.
3	GND	Ground
4	MR	Active-low Manual Reset Input. $\overline{VOUT}$ is low-level while MR is low. Once MR is disabling, $\overline{VOUT}$ turn to high-level after delay time. MR pin is internally pulled up to VDD through 2 MΩ.
5	CD	Connect capacitor between CD and GND pin to set programmable delay time. Ceramic capacitor from 100 pF to 0.1 µF is recommended.

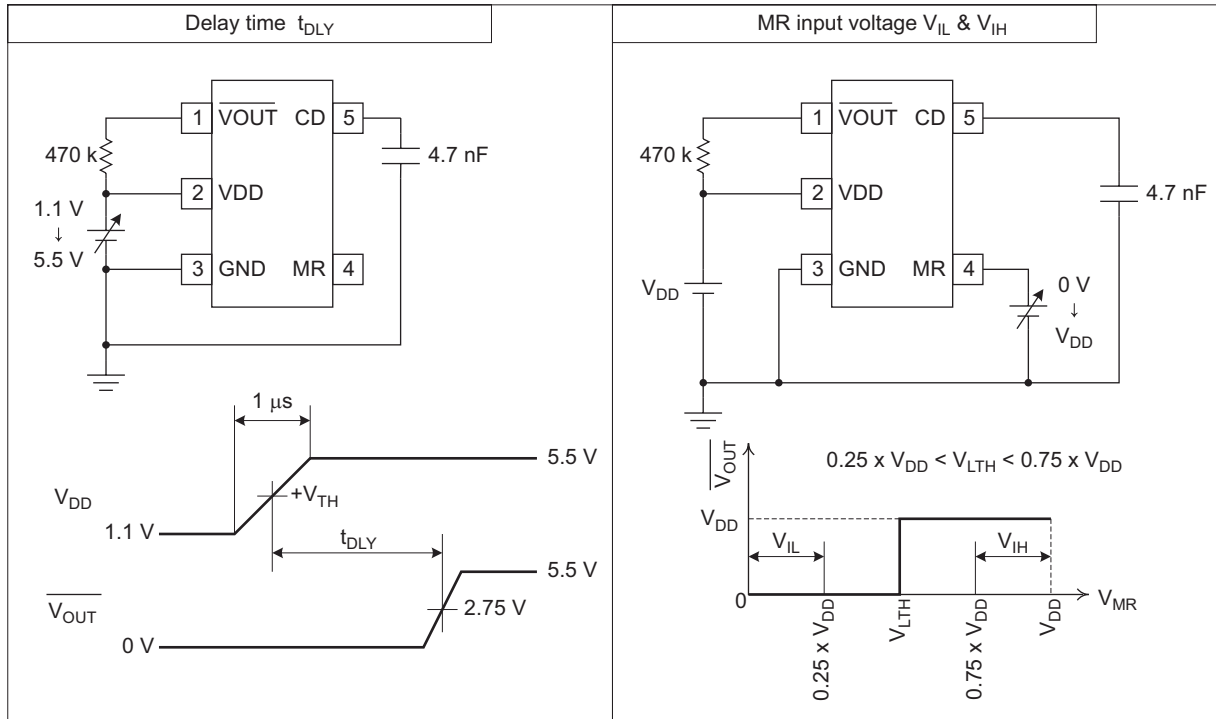
## Test Circuit

### (1) RNA51Axx Products



Test Circuit (Cont.)

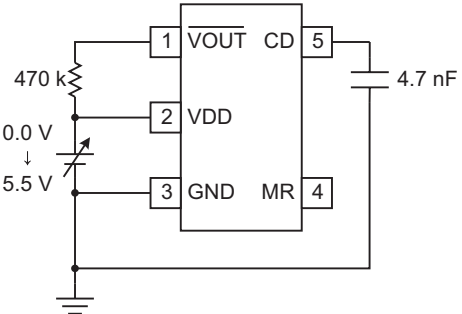
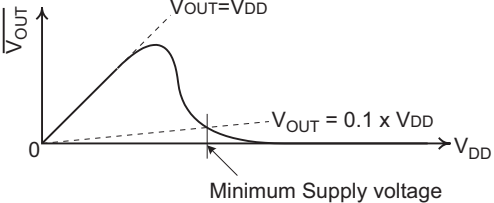
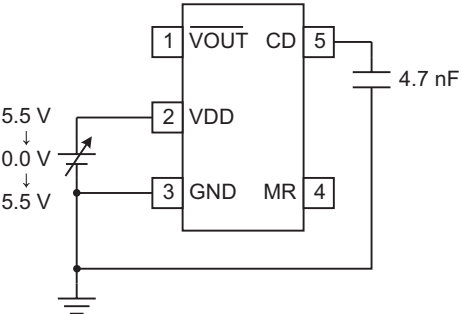
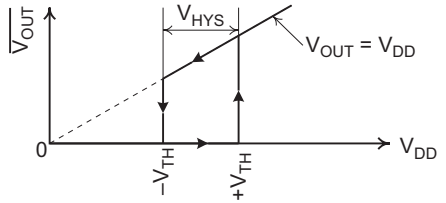
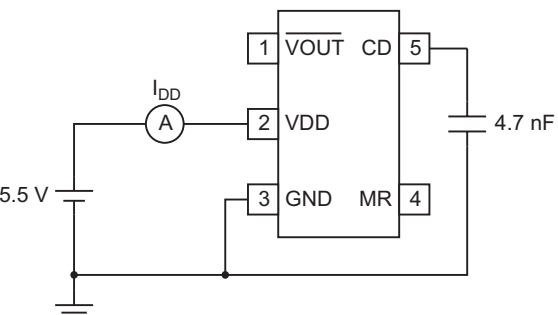
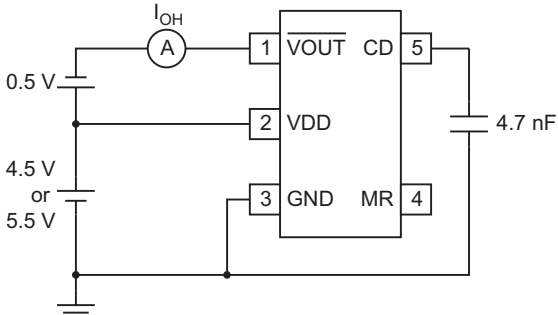
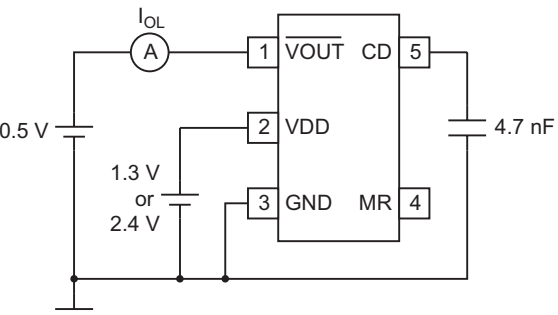
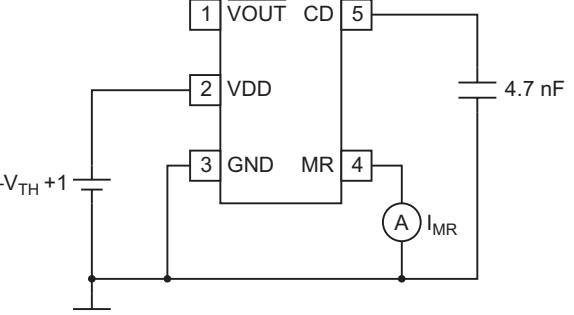
(1) RNA51Axx Products





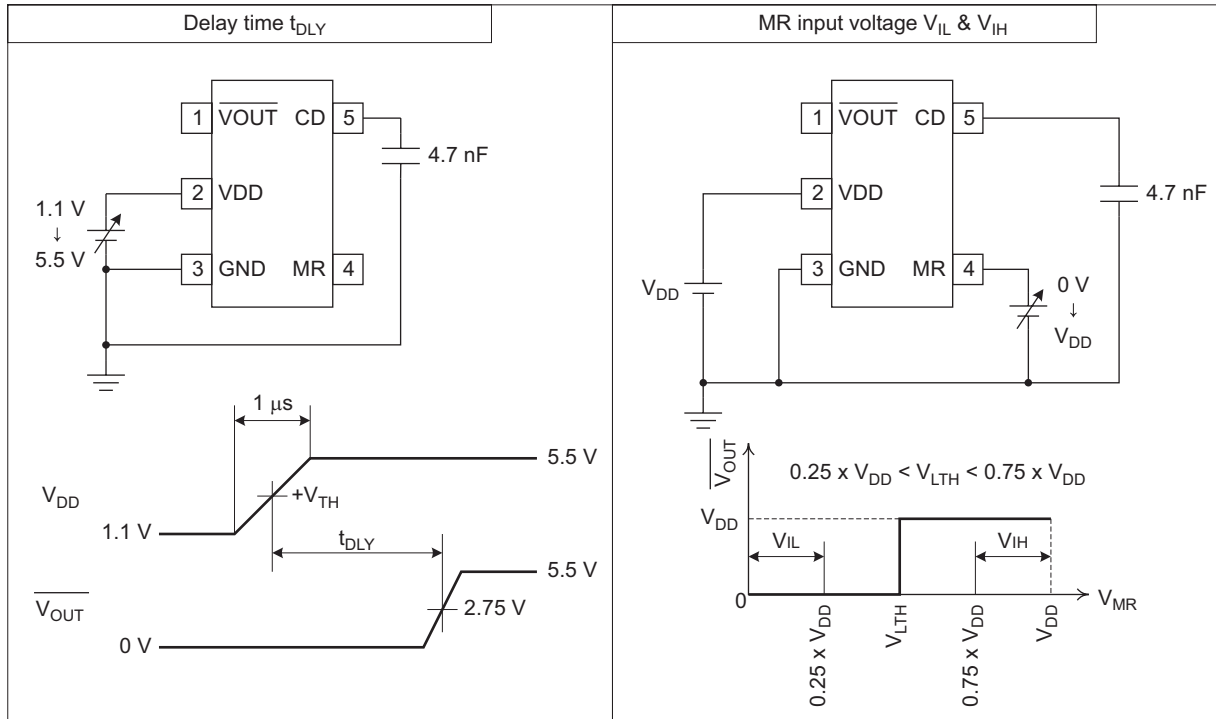
Test Circuit (Cont.)

(2) RNA51Bxx Products

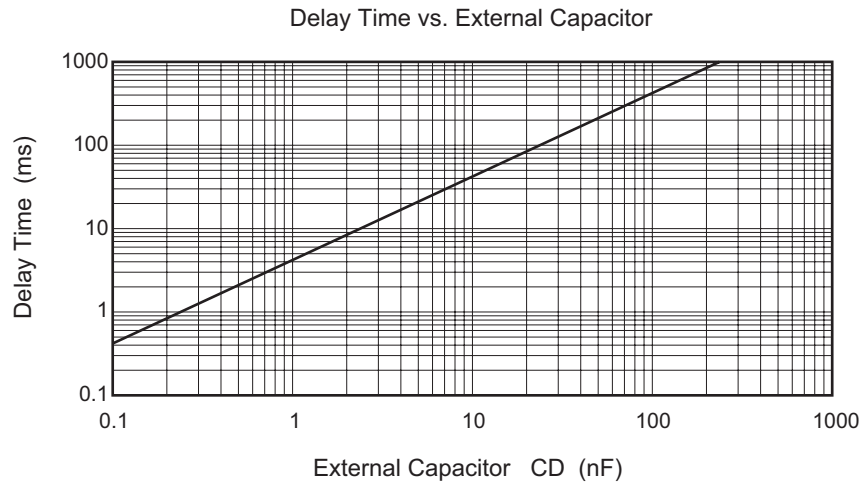
<p>Minimum Supply voltage <math>V_{DDmin}</math></p>   <p>Minimum Supply voltage: <math>V_{OUT} = 0.1 \times V_{DD} \leq 1.1 \text{ V}</math></p>	<p>Threshold voltage and Hysteresis <math>\pm V_{TH}</math> &amp; <math>V_{HYS}</math></p>   <p><math>-V_{TH} \times 3\% \leq V_{HYS} \leq -V_{TH} \times 8\%</math></p> <p><math>-V_{TH}</math>: Reset asserted voltage  <math>+V_{TH}</math>: Reset released voltage</p>
<p>Supply current <math>I_{DD}</math></p> 	<p>High-level output current <math>I_{OH}</math></p> 
<p>Low-level output current <math>I_{OL}</math></p> 	<p>MR internal pull-up resistance <math>R_{MR}</math></p>  <p><math>R_{MR} = \frac{-V_{TH} + 1}{I_{MR}}</math></p>

Test Circuit (Cont.)

(2) RNA51Bxx Products



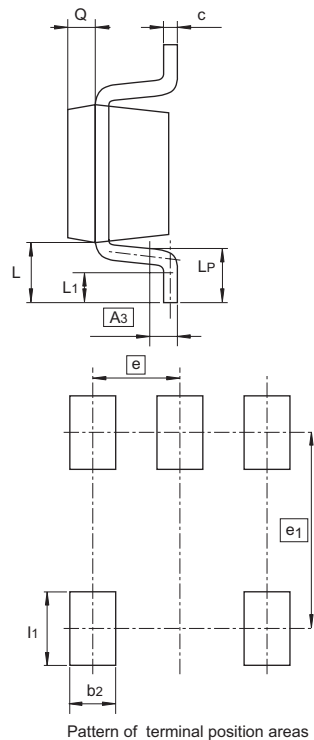
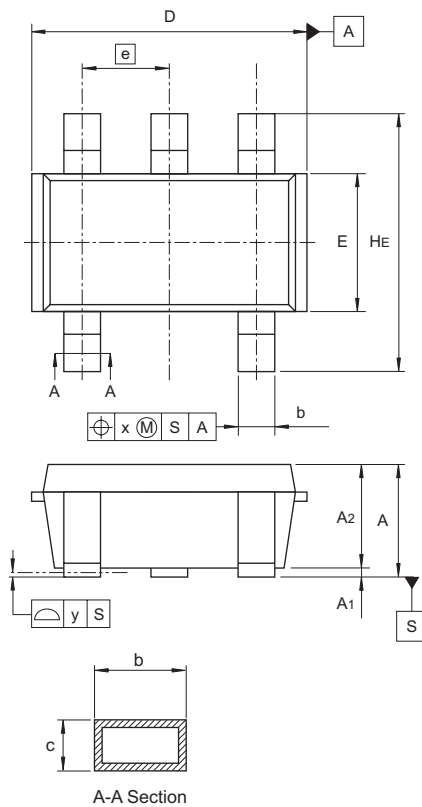
## Delay Time Graph



Note: This graph shows simulation results.

## Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
MPAK-5	SC-74A	PLSP0005ZB-A	MPAK-5 / MPAK-5V	0.015g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	1.0	—	1.4
A <sub>1</sub>	0	—	0.1
A <sub>2</sub>	1.0	1.1	1.3
A <sub>3</sub>	—	0.25	—
b	0.35	0.4	0.5
c	0.11	0.16	0.26
D	2.8	2.95	3.1
E	1.5	1.6	1.8
e	—	0.95	—
H <sub>E</sub>	2.5	2.8	3.0
L	0.3	—	0.7
L <sub>1</sub>	0.1	—	0.5
L <sub>P</sub>	0.2	—	0.6
x	—	—	0.05
y	—	—	0.05
b <sub>2</sub>	—	—	0.55
e <sub>1</sub>	—	2.15	—
l <sub>1</sub>	—	—	0.85
Q	—	0.3	—

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450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

**Renesas Technology Hong Kong Ltd.**  
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**  
10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology Singapore Pte. Ltd.**  
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**  
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510