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PREFACE

The information contained in this document should be considered preliminary. Although an effort has been made to keep the information accurate, there may be misleading or even incorrect statements made herein. The document is being written in parallel with actual chip development and, as such, it is subject to change. This Description is intended to be a living document, to be updated throughout the PCI 9054 design effort. It provides a broad technical overview of the PCI 9054.

The following is a list of additional documentation to provide the reader with more information about the PCI 9054 and related subjects:

- *PCI Local Bus Specification, Revision 2.1*
  PCI Special Interest Group
  5200 N.E. Elam Young Parkway, Hillsboro, OR, 97124-6497 USA
  503-696-2000, http://www.pcisig.com
- *PCI Hot-Plug Specification, Revision 1.0*
  PCI Special Interest Group
  5200 N.E. Elam Young Parkway, Hillsboro, OR, 97124-6497 USA
  503-696-2000, http://www.pcisig.com
- *PCI Power Management Interface Specification, Revision 1.0*, June 30, 1997
  PCI Special Interest Group
  5200 N.E. Elam Young Parkway, Hillsboro, OR, 97124-6497 USA
  503-696-2000, http://www.pcisig.com
- *PICMG 2.0, CompactPCI® Specification, Revision 2.1* or greater
  PCI Industrial Computer Manufacturers Group (PICMG)
  301 Edgewater Place, Suite 220, Wakefield, MA 01880, USA
  Tel: 781-224-1100, Fax: 617-224-1239, http://www.picmg.org
- *Intelligent I/O (I_2O) Architecture Specification Revision 1.5*
  I_2O Special Interest Group
  404 Balboa Street, San Francisco, CA 94118 USA
  Tel: 415-750-8352, Fax: 415-751-4829, http://www.i2osig.org

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REVISION HISTORY

Date	Revision	Comment
09/16/97	0.3	Revise version 0.2 Red Book to include PCI 9054 special functions.
01/21/98	0.9	Added special functions: • Power Management functionality • Vital Product Data (VPD) functionality • CompactPCI Hot Swap functionality • PCI Hot Plug • MPC850 or MPC860 Operation mode • 176-pin PQFP and 225-pin PBGA pinouts Portions of the CompactPCI *Specification* used for the CompactPCI Hot Swap section.
02/13/98	0.9	Incorporated changes from January and February review meetings.
06/26/98	0.91	Incorporated engineering feedback and PCI 9054 flier text. Updated Local timing specifications.
09/02/98	0.92	Changed title to “data book” and removed references to inches in Table 14-1 and Table 14-2. Added serial EEPROM information to Table 1-4. Added information to BB# description in Table 1-5 and Table 12-7. Changed TA# information for Direct Slave and DMA modes in Section 2.2.4.1. Added cross-references to other sections for Bust Forever mode in Table 2-8 and Table 2-9. Added burst information to Section 2.2.5.1. Added VPD information relating to long serial EEPROM loads to Section 2.4.2.1. Added “Register Bits Affected” information to Table 2-20 and Table 2-21. Added port size information to Table 3-3. Changed DMA PCI DAC information in Section 3.5.1. Added Section 5.5.2.1, “Block DMA PCI Dual Address Cycle.” Added Section 5.5.3.1, “Scatter/Gather DMA PCI Dual Address Cycle.” Changed captions for Figure 1-3, Figure 5-16, and Figure 5-17. Added recommendation to not assert EOT# during a descriptor load on the Local Bus to Section 3.5.9 and Section 5.5.9. Clarified INTCSR[11]=0 information in Section 6.3.1.2. Added additional VPD information to Section 10, Section 10.1, and Section 10.1.4. Changed PCIBAR register information and corrected the serial EEPROM information for 3Ch in Table 11-2. Changed the PCI:0Ch and LOC:8Ch information in Table 11-3. Changed the Read information from “Yes” to “PCI” in Table 11-40 through Table 11-43 (PVPDCNTL, PVPD_NEXT, PVPDAD, and PVPDATA). Changed CNTRL[27] description to “Reserved” in Table 11-73. Swapped pinouts for TSIZ[0:1] and LBE[3:2]#. M Mode—TSIZ0 is now pin 92 (PQFP) and pin N14 (PBGA). TSIZ1 is now pin 91 (PQFP) and pin P15 (PBGA). C and J Modes—LBE3# is now pin 92 (PQFP) and pin N14 (PBGA). LBE2# is now pin 91 (PQFP) and pin P15 (PBGA). Corrected minor typographical errors.

Date	Revision	Comment
11/12/98	1.0	Augmented entire book by separating M mode and C and J modes into their own sections. Changed “negate” to “de-assert”. Changed “Half Word” to “Word” and “Word” to “Lword” in M mode sections. Changed “driven” to “asserted” in multiple tables. Added a slash to “Direct Master/Target Abort.” Added “PCI” to “Dual Address Cycle” text references. Changed “PCI command 7h” to “PCI command code = 7h”. Updated timing diagrams for all modes. Changed “Arbitration” to “Control Access” in Scatter/Gather DMA Mode from Local-to-PCI Bus figure captions. Corrected inputs and outputs for DMA 0/1 Local and PCI FIFOs in the PCI 9054 Internal Block Diagram. Changed “Local Initialization” and “Serial EEPROM” section descriptions. Added new Section 1.5, “PCI 9054 Data Assignment Convention.” Split Signal listings into PCI and Local signals in Table 1-5 and Table 1-6. Added exception for MWI mode to Sections 2.1.2 and 4.1.2. Changed assertion and bus ownership information in Sections 2.2.1 and 4.2.1. Local Bus cycle description changed in Sections 2.2.2 and 4.2.2. Additional changes to Section 4.2.2 added regarding use of BLAST#. Added New Capabilities function support information, Sections 2.4.2.3 and 4.4.2.3. Added Hot Swap Next Capability Pointer information to Table 2-21 and Table 4-21. Changed Serial EEPROM Memory map information in Figure 2-5 and Figure 4-5. Updated Response to FIFO Full or Empty information in Table 3-1 and Table 5-1. Corrected references to Local Configuration and PCI Configuration DMA registers in Sections 3.1.2 and 5.1.2. Added Master Enable (PCICR) and PCI Command Code (CNTRL) to bullet list in Sections 3.4.1 and 5.4.1. Added Continuous Burst information to Section 3.4.1.3 (M mode only). Added Lword information to FIFO description in Sections 3.4.3 and 5.4.2. Miscellaneous changes made to DMA Operation information in Sections 3.5–3.5.2 and 5.5–5.5.2. Changed DMA descriptor “Note” text in Sections 3.5.3 and 5.5.3. Added new Sections 3.5.3.2 and 5.5.3.2, “DMA Clear Count Mode.” Changed current descriptor and Channel Done bit text in Sections 3.5.6, 5.5.6, and 6.3.1.7. Descriptor Pointer and Memory Descriptor Block(s) text changes applied to Figure 3-16, Figure 3-17, Figure 5-16, and Figure 5-17. Changed sections describing “End of Transfer (EOT#) Input” and “Local Bus Latency and Pause Timers” to third-level headings. Moved “DMA Arbitration” section to appear after “End of Transfer (EOT#) Input.” Added “Direct Master” to “Read Ahead mode” text and changed “Multiple-Cycle reads” to “Burst-Cycle reads” and “are set” to “are asserted” to the “Read” portion of Sections 3.4.1.3 and 5.4.1.3. Added DMA Local Bus Timer information to Sections 3.5.11 and 5.5.11. Removed text describing generation of a new ADS# from Section 4.2.5.1. Changed “End of Chain bits are programmed” to “End of Chain bits are detected” in Sections 3.5.3 and 5.5.3. Changed Doorbell register information in Figure 6-1. Swapped sequence of Sections 6.3 and 6.4. Applied significant revisions to Section 8, including the addition of System Changes Power Mode and Wake-Up Request examples. Combined “Hot Swap Switch” and “Status LED” sections into new Section 9.1.2.2.1, “Ejector Switch and Blue LED.” Added new content to section. Corrected register “Value after Reset” values in Section 11. Revised timing information in Table 13-6 through Table 13-9, AC Electrical Characteristics for Local inputs and outputs. Corrected information for B9, C6, D10, and P6 in PBGA Pinout, Table 14-3. Added new Section 15, “Ordering Instructions.”

PCI 9054

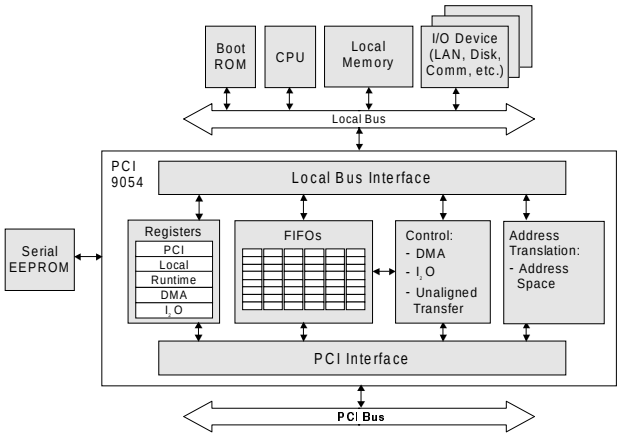
PCI I/O Accelerator

November 1998
Version 1.0

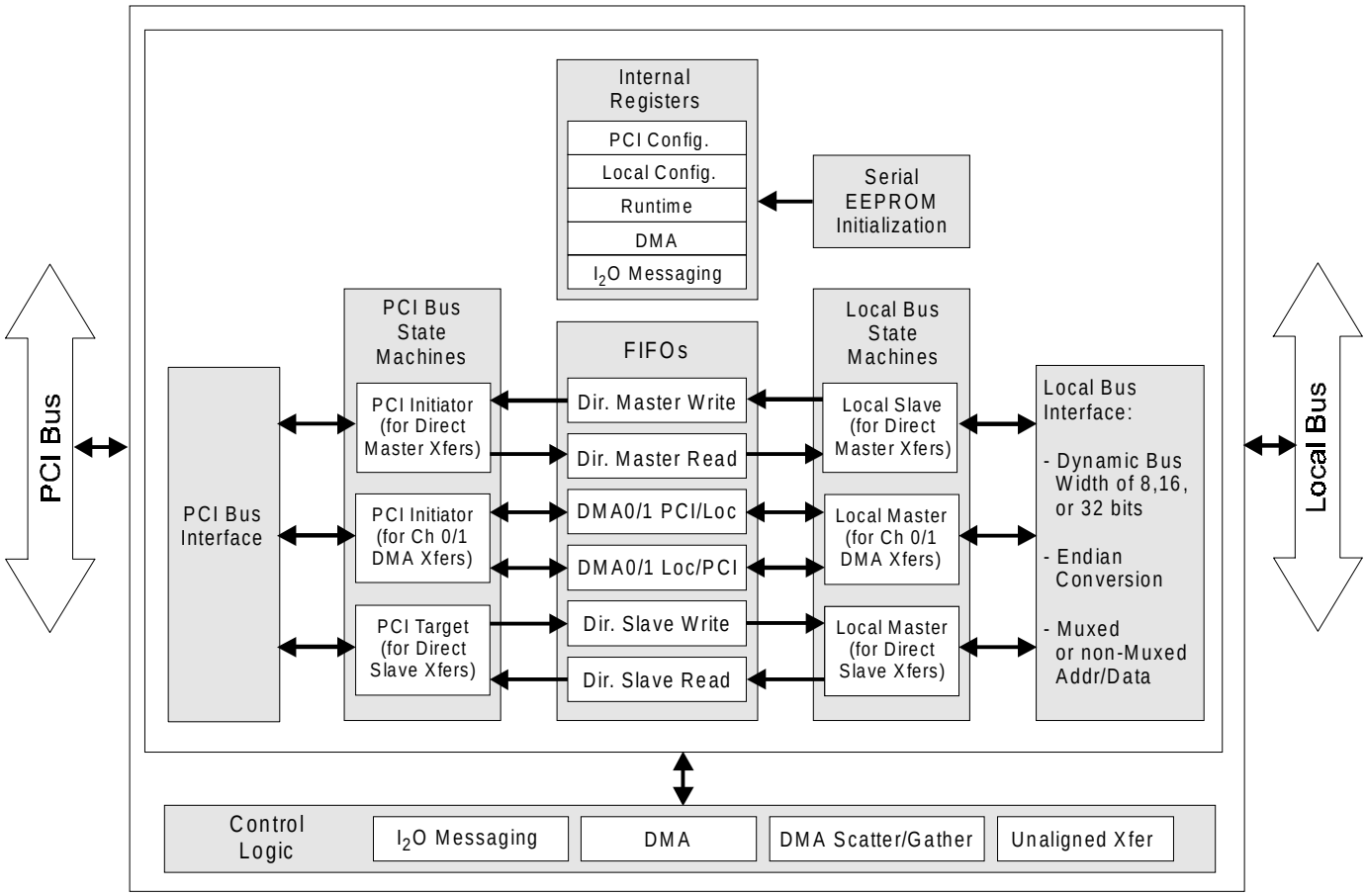
I_2O Compatible, CompactPCI Hot Swap Friendly
PCI Bus Master Interface Chip
for Adapters and Embedded Systems

FEATURES

- PCI Specification version 2.2 (v2.2) compliant 32-bit, 33-MHz Bus Master Interface Controller with PCI Power Management features for adapters and embedded systems
- General Purpose Bus Master Interface featuring advanced Data Pipe Architecture™ technology, which includes two DMA engines, programmable Target and Initiator Data Transfer modes and PCI messaging functions
- PCI v2.2 Vital Product Data (VPD) configuration support
- PCI Dual Address Cycle (DAC) support
- PCI Hot Plug and CompactPCI Hot Swap compliant
- I_2O™ v1.5-Ready Messaging Unit
- Two independent DMA channels for Local Bus memory to and from PCI Host Bus Data transfers
- Supports Type 0 and Type 1 Configuration cycles
- Programmable Burst Management
- Programmable Interrupt Generator
- Six programmable FIFOs for zero wait state burst operation
- PCI ⇔ Local Data transfers up to 132 MB/s
- 3.3V, 5V tolerant PCI and Local signaling supports Universal PCI Adapter designs, 3.3V core, low-power CMOS in 176-pin PQFP and 225-pin PBGA
- Supports Local Bus Direct-Connect to MPC850 or MPC860 Power QUICC, Intel i960 family and IBM PPC401 CPUs and similar bus protocol devices
- Programmable Local Bus runs up to 50 MHz and supports non-multiplexed 32-bit address/data, multiplexed 32-bit, and slave accesses of 8-, 16-, or 32-bit Local Bus devices
- Serial EEPROM interface
- Three PCI-to-Local Address spaces
- Programmable Local Bus wait states
- Programmable prefetch counter
- Local Bus runs asynchronously to the PCI Bus
- Eight 32-bit Mailbox and two 32-bit Doorbell registers
- Performs Big Endian ⇔ Little Endian conversion
- PCI-to-Local Delayed Read mode
- Local-to-PCI Deferred Read mode (M mode only)
- Flexible 3.3V, 5V Tolerant Local Bus operation up to 50 MHz
- Industrial Temp Range operation



Typical Adapter Block Diagram



PCI 9054 Internal Block Diagram

1. COMPANY AND PRODUCT BACKGROUND

PLX Technology, Inc., the world leader in PCI-to-Local Bus I/O accelerator chips, supports more than 500 OEM customers in a wide variety of PCI applications. Customer applications include PC workstations and servers, PCI add-in boards, embedded PCI communication systems (such as routers and switches), and industrial PCI implementations (such as CompactPCI, PMC, and Passive Backplane PCI).

PLX Technology, Inc., is an active participant in industry standard committees, including the PCI SIG®, I_2O SIG®, and PICMG®, and maintains active developer technology and cross-marketing partnerships with industry leaders, such as Intel, IBM, Hewlett-Packard, Motorola, Integrated Systems, WindRiver, and others.

Focused on providing complete solutions for PCI implementations, PLX provides design assistance to customers in the form of Reference Design kits and Software Development kits. Depending upon the application, these kits may include reference boards, API libraries, software debug tools, and sample device drivers with source, enabling customers to quickly bring new designs to production. New tools, application notes, FAQs, and information updates are constantly added to our website (www.plxtech.com) for the convenience of PLX customers. Our expertise and total solutions for the PCI interface allow customers to focus on adding value in their designs without worrying about the complexities of implementing PCI, I_2O, and CompactPCI.

1.1 PCI 9054 I/O Accelerator

The PCI 9054, a 32-bit 33-MHz PCI Bus Master I/O Accelerator, is the most advanced general-purpose bus Master device available. It offers a robust PCI Specification v2.2 implementation enabling Burst transfers up to 132 MB/second. The PCI 9054 incorporates the industry leading PLX Data Pipe Architecture™ technology, including DMA engines, programmable PCI Initiator and Target Data-Transfer modes, and PCI messaging functions.

1.2 Data Pipe Architecture Technology

1.2.1 Dual DMA Channels

- Dual independent channels provide flexible prioritization scheme
- Programmable Burst length, including unlimited burst
- Direct hardware control of DMA
  - Demand mode DMA operation
  - Block mode or Scatter/Gather operation
  - End of Transfer (EOT) signal
- Shuttle mode DMA channel support provides automatic invalidation of used DMA descriptors
- Unaligned transfer support
- Supports PCI Bus Mastering from the Local Slave-only devices
- Scatter/Gather list management
  - Descriptors can be found in PCI Bus memory or in Local Bus memory
  - Allows independent Scatter/Gather ring management

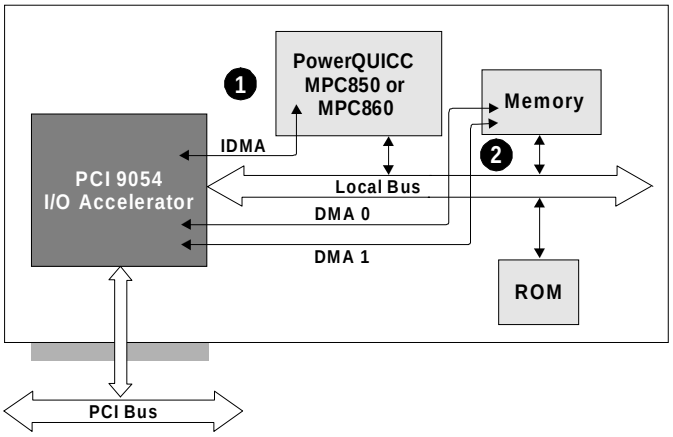


Figure 1-1. High-Performance MPC850 or MPC860 PowerQUICC Adapter Design

1.2.2 PCI Initiator (Direct Master)

- Type 0 and Type 1 Configuration cycles
- Supports all PCI Memory and I/O cycles
- Initiator Read prefetching
- Burst length control-programmable threshold pointer
- Unaligned transfer control
- Big/Little Endian conversion

1.2.3 PCI Target (Direct Slave)

- Multiple independent address spaces
- Dynamic Local Bus width control
- Target Read prefetching
- Big/Little Endian conversion
- Local Bus priority control
- PCI Latency Timer

1.2.4 PCI Messaging

- Complete Messaging Unit with mailbox and doorbell registers
- Queue management pointers that can be used for message passing under the I_2O protocol or a custom protocol

1.3 PCI 9054 PCI Applications

1.3.1 High Performance Motorola MPC850 or MPC860 PowerQUICC Designs

A key application for the PCI 9054 is Motorola MPC850- or MPC860-based adapters for telecom and networking applications. These applications include high performance communications such as WAN/LAN controller cards, high-speed modem cards, Frame Relay cards, and routers and switches. The PCI 9054 simplifies designs by providing an industry-leading enhanced direct-connect interface to the MPC850 or MPC860 processor. The flexible PCI 9054 3.3V, 5V tolerant I/O buffers, combined with a Local Bus operation up to 50 MHz, is ideally suited for current and future PowerQUICC processors. The PCI 9054 also provides support for the MPC850 or MPC860 IDMA channel for movement of data between the internal MPC850 or MPC860 I/O and the PCI Bus. In addition, the PCI 9054 also makes use of the advanced Data Pipe Architecture technology, allowing unlimited Burst capability, as shown in Figure 1-1.

1. For PowerQUICC IDMA operation, the PCI 9054 transfers data to the PCI Bus under the control of the IDMA handshake protocol.
2. At the same time, the PCI 9054 Data Pipe Architecture technology DMA can be operated bidirectionally, with the PCI 9054 as the Master for both buses, to manage transfers of data from the Local Bus to the PCI Bus or from the PCI Bus to the Local Bus. This is a prime example of how the PCI 9054 provides superior general purpose Bus Master performance and provides designers using the PowerQUICC processor with greater flexibility in implementing multiple simultaneous I/O transfers. The PCI 9054 has unlimited bursting capability, which enhances any MPC850 or MPC860 PowerQUICC design.

1.3.2 High Performance CompactPCI Adapter Designs

Another key application for the PCI 9054 is CompactPCI adapters for telecom and networking applications. These applications include high performance communications such as WAN/LAN controller cards, high-speed modem cards, Frame Relay cards, and telephony cards for telecom switches and remote-access systems.

The PCI 9054 has integrated key features to enable live-insertion of Hot Swap CompactPCI adapters. The PCI 9054 PICMG v2.1-compatible Hot Swap *Friendly* PCI interface includes both Hot Swap *Capable* and Hot Swap *Friendly* features.

1.3.2.1 Hot Swap Capable

- PCI Specification v2.1 or better
- Tolerant of Vcc from early power
- Tolerant of asynchronous reset
- Tolerant of precharge voltage
- Limited I/O pin leakage at precharge voltage

1.3.2.2 Hot Swap Friendly

- Incorporates the Hot Swap Control/Status register (HS_CSR)
- Incorporates an Extended Capability Pointer (ECP) mechanism
- Incorporates added resources for software control of ENUM#, the ejector switch, and the status LED, which indicates insertion and removal to the user

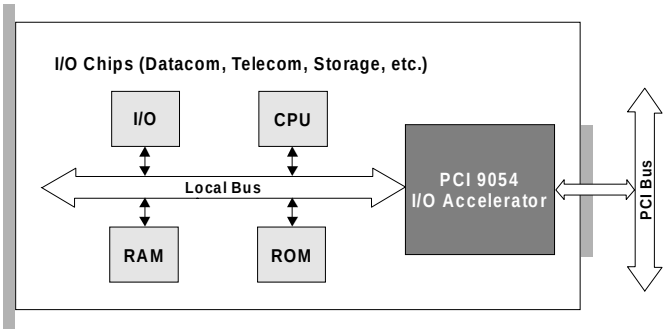


Figure 1-2. High-Performance CompactPCI Adapter

1.3.3 PCI Bus Embedded Host Design

Another application for the PCI 9054 is PCI Host-embedded system designs, such as network switches and routers, printer engines, set-top boxes, and industrial equipment. In this configuration, the PCI 9054 Data Pipe Architecture technology allows high-performance transfer modes. In addition, the PCI 9054 supports both Type 0 and Type 1 PCI Configuration cycles that allow the PCI 9054 to configure other PCI devices or cards in the system.

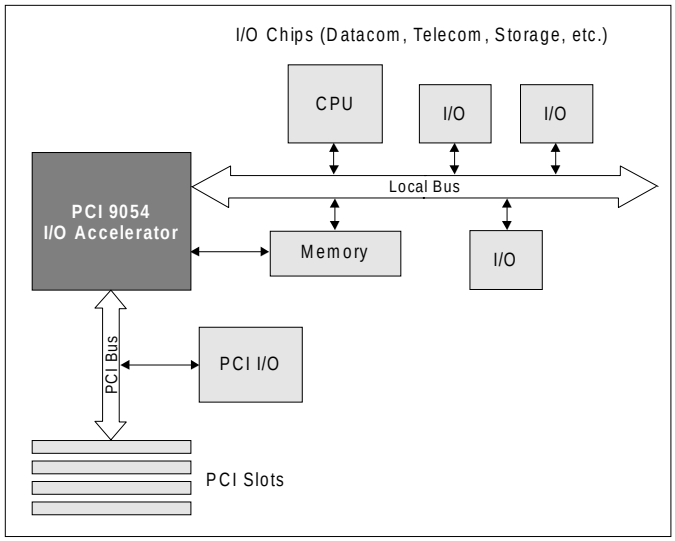


Figure 1-3. High-Performance Embedded Adapter

1.4 PCI 9054 Major Features

PCI v2.1 and v2.2 Compliant. Compliant with all aspects of PCI Specification v2.1 and v2.2, including PCI Power Management features. Supports four power states for PCI Power Management functions—D_0, D_1, D_2, and D_{3hot}—and the Power Management Event interrupt (PME#).

VPD Support. Fully supports the Vital Product Data (VPD) PCI extension, which provides an alternate access method other than Expansion ROM for VPD.

PCI Dual-Address Cycle (DAC) Support (64-bit Address Space). Supports PCI Dual Address Cycle beyond the low 4-GB Address space. PCI DAC can be used during PCI 9054 PCI Bus Master operation (DMA, Direct Master).

PCI Hot Plug and CompactPCI Hot Swap Compliant. Compliant with PCI Hot Plug and CompactPCI Hot Swap adapter specifications.

I_2O Ready Messaging Unit. Incorporates the I_2O Ready Messaging Unit, which enables the adapter or embedded system to communicate with other I_2O-supported devices. The I_2O Messaging Unit is fully compatible with the PCI extension of I_2O Specification v1.5.

Dual Independently Programmable DMA Controllers with Programmable FIFOs. Provides two independently programmable DMA controllers with shared programmable FIFOs. Each channel supports Block and Scatter/Gather DMA modes, as well as End of Transfer (EOT) mode. The PCI 9054 supports Demand Mode DMA for DMA Channel 0.

PCI Host Capability. In Direct Master mode, the PCI 9054 can assert Type 1 and Type 0 PCI Configuration cycles.

Six Programmable FIFOs for Zero Wait State Burst Operation.

Table 1-1. FIFO Depth

FIFO	Length
Direct Master Read	16 Lwords
Direct Master Write	32 Lwords
Direct Slave Read	16 Lwords
Direct Slave Write	32 Lwords
DMA Read	32 Lwords
DMA Write	32 Lwords

PCI ⇔ Local Data Transfers up to 132 MB/sec.

5 Volt Tolerant Operation. The PCI 9054 requires 3.3V Vcc. It provides 3.3V signaling with 5V I/O tolerance on both the PCI and Local Buses.

Local Bus Direct Interface. Supports Local Bus direct interface to the Motorola MPC850 or MPC860 family, the Intel i960 family, the IBM PPC401 family, and other similar bus-protocol devices.

Programmable Local Bus. Runs up to 50 MHz and supports non-multiplexed 32-bit address/data, multiplexed 32-bit, and Slave accesses of 8-, 16-, or 32-bit Local Bus devices.

Serial EEPROM Interface. Contains an optional serial EEPROM interface (optional only if a Local processor is being used) that can be used to load configuration information. This is useful for loading information that is unique to a particular adapter (such as the Network ID or the Vendor ID).

Three PCI-to-Local Address Spaces. The PCI 9054 supports three PCI-to-Local Address spaces when the PCI 9054 is in PCI Target or PCI Slave mode. These spaces (Space 0, Space 1, and Expansion ROM spaces) allow any PCI Bus Master to access the Local Memory spaces with programmable wait states, bus width, burst capabilities, and so forth.

Programmable Prefetch Counter. The PCI 9054 can be programmed to prefetch data during Direct Slave and Direct Master prefetches (known or unknown size). To perform burst reads, prefetching must be enabled. The prefetch size can be programmed to match the Master burst length, or can be used as Read Ahead mode data. The PCI 9054 reads single data (8, 16, or 32 bit) if the Master initiates a single cycle; otherwise, the PCI 9054 prefetches the programmed size.

Mailbox Registers. Contains eight 32-bit Mailbox registers that may be accessed from the PCI or Local Bus.

Doorbell Registers. Includes two 32-bit doorbell registers. One asserts interrupts from the PCI Bus to the Local Bus. The other asserts interrupts from the Local Bus to the PCI Bus.

Big/Little Endian Conversion. Supports dynamic switching between Big Endian (Address Invariance) and Little Endian (Data Invariance) operations for Direct Slave, Direct Master, DMA, and internal register accesses on the Local Bus.

The PCI 9054 supports on-the-fly Endian conversion for Space 0, Space 1, and Expansion ROM space. The Local Bus can be Big/Little Endian by using the BIGEND# input pin or programmable internal register configuration. When BIGEND# is asserted, it overrides the internal register configuration during Direct Master and internal register accesses on the Local Bus.

Note: *The PCI Bus is always Little Endian.*

Programmable Local Bus Modes. The PCI 9054 is a PCI Bus Master interface chip that connects a PCI Bus to one of three Local Bus types (M, C, or J mode), selected through mode pins.

The PCI 9054 may be connected to any Local Bus with a similar design with little or no glue logic. Table 1-2 lists the three modes.

Table 1-2. Programmable Local Bus Modes

Mode	Description
M	32-bit address/32-bit data, non-multiplexed direct connect interface to MPC850 or MPC860
C	32-bit address/32-bit data, non-multiplexed
J	32-bit address/32-bit data, multiplexed

Clock. The Local Bus interface runs from a Local clock to provide the necessary internal clocks. This clock runs asynchronously to the PCI clock.

Read Ahead Mode. Supports Read Ahead mode, where prefetched data can be read from the PCI 9054 internal Direct Slave Read FIFO instead of from the Local Bus. The address must be subsequent to the previous address and 32-bit aligned (next address = current address + 4). This feature allows for increased bandwidth and reduced data latency.

M Mode of Operation. The PCI 9054 is designed with a seamless interface to the Motorola MPC850 or MPC860 RISC processors. The PCI 9054 communicates with the MPC850 or MPC860 using five possible Data-Transfer modes:

- Configuration Register Access
- Direct Master Operation
- Direct Slave Operation
- DMA Operation
- IDMA/SDMA Operation

C and J Modes of Operation. The PCI 9054 is designed with a seamless interface to the Intel i960 and the IBM PPC401 family RISC processors. The PCI 9054 communicates with these processors using four possible Data-Transfer modes:

- Configuration Register Access
- Direct Master Operation
- Direct Slave Operation
- DMA Operation

Interrupt Generator. Can assert PCI and Local interrupts from external and internal sources.

Unaligned DMA Transfer Support. Can transfer data on any byte-boundary combination of the PCI and Local Address spaces.

Keep Bus Mode (M Mode). The PCI 9054 can be programmed to keep the PCI Bus by generating wait state(s) if the Direct Master Write FIFO becomes full. The PCI 9054 can also be programmed to keep the Local Bus (BB# asserted) if the Direct Slave Write FIFO becomes empty or the Direct Slave Read FIFO becomes full. The Local Bus is dropped in either case when the Local Bus Latency Timer is enabled and expires.

Keep Bus Mode (C and J Modes). The PCI 9054 can be programmed to keep the PCI Bus by generating wait state(s) if the Direct Master Write FIFO becomes full. The PCI 9054 can also be programmed to keep the Local Bus (LHOLD asserted) if the Direct Slave Write FIFO becomes empty or the Direct Slave Read FIFO becomes full. The Local Bus is dropped in either case when the Local Bus Latency Timer is enabled and expires.

New Capabilities Structure. Supports New Capabilities registers to define additional capabilities of the PCI functions.

Posted Memory Writes. Supports the Posted Memory Writes (PMW) for maximum performance and to avoid potential deadlock situations.

RST# Timing. Supports response to first configuration accesses after de-assertion of RST# under 2^{25} clocks.

Subsystem ID and Subsystem Vendor ID. Contains Subsystem ID and Subsystem Vendor ID in the PCI Configuration Register Space in addition to System and Vendor IDs. The PCI 9054 also contains a permanent Vendor ID (10B5h) and Device ID (9054h).

Direct Bus Master. Supports PCI accesses from a Local Bus Master. Burst transfers are supported for memory-mapped devices and single-transfers are supported for memory-mapped and I/O devices. The PCI 9054 also supports PCI Bus interlock (LOCK#) cycles.

Direct Slave. Supports Burst Memory-Mapped and Single I/O-Mapped accesses to the Local Bus. The Read and Write FIFOs enable high-performance bursting.

1.5 PCI 9054 Data Assignment Convention

Table 1-3 describes the PCI 9054 data assignment convention.

Table 1-3. PCI 9054 Data Assignment Convention

Data Width	PCI 9054 Convention
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	Lword

1.6 PCI 9050/9080 Compatibility

1.6.1 Pin Compatibility

The PCI 9054 is ***not*** pin compatible with the PCI 9080 ***nor*** with the PCI 9050.

1.6.2 Register Compatibility

All registers implemented in the PCI 9080 are implemented in the PCI 9054. The PCI 9054 includes many new bit definitions and several new registers. Refer to Section 11.1 for details.

The PCI 9054 is ***not*** register-compatible with the PCI 9050.

1.7 PCI 9054, PCI 9080, and PCI 9050 Comparison

Table 1-4. Comparison of PCI 9054, PCI 9080, and PCI 9050

Feature	PCI 9054	PCI 9080	PCI 9050
Package Size/Type	176 PQFP, 225 PBGA	208 PQFP	160 PQFP
Number of DMA Channel(s)	2	2	0
Local Address Spaces	3	3	5
Direct Master Mode	Yes	Yes	No
Mailbox Registers	Eight 32-bit	Eight 32-bit	Eight 32 bit
Doorbell Registers	Two 32-bit	Two 32-bit	Two 32 bit
Number of FIFOs	6	8	—
FIFO Depth—Direct Slave Write and Direct Master Write	32 Lwords (128 bytes)	32 Lwords (128 bytes)	—
FIFO Depth—Direct Slave Read and Direct Master Read	16 Lwords (64 bytes)	16 Lwords (64 bytes)	2
FIFO Depth—DMA Channel 0	32 Lwords (128 bytes) Single bidirectional Read/Write FIFO	32 Lwords (128 bytes) Read and Write FIFOs	N/A
FIFO Depth—DMA Channel 1	16 Lwords (64 bytes) Single bidirectional Read/Write FIFO	16 Lwords (64 bytes) Read and Write FIFOs	N/A
LLOCKo# Pin for Lock Cycles	Yes	Yes	Yes
WAIT# Pin for Wait State Generation	Yes	Yes	No
BPCLKo Pin; Buffered PCI Clock	No	Yes	Yes
DREQ0# and DACK0# Pins for Demand Mode DMA Support	Yes (1 channel only)	Yes	No
Register Addresses	Identical to the PCI 9080 except the PCI 9054 has additional registers related to added functionality	—	—
Big Endian ⇔ Little Endian Conversion	Yes	Yes	Yes
PCI Specification v2.1 Deferred Reads	Yes	Yes	Yes
PCI Specification v2.2 PCI Power Management, PCI Hot Plug Compliant, CompactPCI Hot Swap Compliant	Yes	No	No
PCI v2.2 VPD Support	Yes	No	No
Programmable Prefetch Counter	Yes	Yes	Yes
Memory Write and Invalidate Cycle	Yes	Yes	No
Additional Device and Vendor ID Registers	Yes	Yes	No
I_2O Messaging Unit	Yes	Yes	No
Core and Local Bus Vcc	3.3V	5V	5V
PCI Bus Vcc	3.3V	3.3/5V	5V
3.3V Tolerant PCI Bus and Local Bus Signaling	Yes	Yes (if PCI Vcc is 3.3V)	No
5V Tolerant PCI Bus and Local Bus Signaling	Yes	Yes (if PCI Vcc is 5V)	Yes
Serial EEPROM Support	2-kilobit, 4-kilobit devices	1-kilobit, 2-kilobit devices	—
Serial EEPROM Read Control	Reads allowed via Vital Product Data Function (refer to Section 10)	Reads allowed via Serial EEPROM Control Register (CNTRL)	1-kilobit device

1.8 PCI 9054 Signal Listing (M, C, or J Modes)

Table 1-5. PCI 9054 PCI Signal Listing (M, C, or J Modes)

Symbol	Bus Mode	Signal Name	Total Pins	Function
AD[31:0]	All	Address and Data	32	All multiplexed on the same PCI pins. The Bus transaction consists of an Address phase, followed by one or more Data phases. The PCI 9054 supports both Read and Write bursts.
C/BE[3:0]#	All	Bus Command and Byte Enables	4	All multiplexed on the same PCI pins. During the Address phase of a transaction, defines the bus command. During the Data phase, used as byte enables. Refer to the PCI spec for further detail if needed.
DEVSEL#	All	Device Select	1	When actively driven, indicates the driving device has decoded its address as the Target of the current access. As an input, indicates whether any device on the bus is selected.
FRAME#	All	Cycle Frame	1	Driven by the current Master to indicate beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, Data transfers continue. When FRAME# is de-asserted, the transaction is in the final Data phase.
GNT#	All	Grant	1	Indicates to the agent that access to the bus is granted. Every Master has its own REQ# and GNT#.
IDSEL	All	Initialization Device Select	1	Used as a chip select during Configuration Read and Write transactions.
INTA#	All	Interrupt A	1	PCI Interrupt request.
IRDY#	All	Initiator Ready	1	Indicates ability of the initiating agent (Bus Master) to complete the current Data phase of the transaction.
LOCK#	All	Lock	1	Indicates an atomic operation that may require multiple transactions to complete.
PAR	All	Parity	1	Even parity across AD[31:0] and C/BE[3:0]#. All PCI agents require parity generation. PAR is stable and valid one clock after the Address phase. For Data phases, PAR is stable and valid one clock after either IRDY# is asserted on a Write transaction or TRDY# is asserted on a Read transaction. Once PAR is valid, it remains valid until one clock after current Data phase completes.
PCLK	All	Clock	1	Provides timing for all transactions on PCI and is an input to every PCI device. The PCI 9054 operates up to 33 MHz.
PERR#	All	Parity Error	1	Reports data parity errors during all PCI transactions, except during a special cycle.
PME#	All	Power Management Event	1	Wake-up event interrupt.
REQ#	All	Request	1	Indicates to arbiter that this agent must use the bus. Every Master has its own GNT# and REQ#.
RST#	All	Reset	1	Used to bring PCI-specific registers, sequencers, and signals to a consistent state.
SERR#	All	Systems Error	1	Reports address parity errors, data parity errors on the Special Cycle command, or any other system error where the result is catastrophic.
STOP#	All	Stop	1	Indicates the current Target is requesting that the Master stop the current transaction.
TRDY#	All	Target Ready	1	Indicates ability of the Target agent (selected device) to complete the current Data phase of the transaction.

Table 1-6. PCI 9054 Local Signal Listing (M, C, or J Modes)

Symbol	Bus Mode	Signal Name	Total Pins	Function
ADS#	C, J	Address Strobe	1	Indicates valid address and start of new Bus access. Asserted for first clock of Bus access.
ALE	J	Address Latch Enable	1	Asserted during Address phase and de-asserted before Data phase and before next LCLK rising edge.
BB#	M	Bus Busy	1	As an input, the PCI 9054 monitors this signal to determine whether an external Master has ended a Bus cycle. As an output, the PCI 9054 asserts this signal after an external arbiter has granted ownership of the Local Bus and BB# is inactive from another Master. Signal requires an external pull-up resistor value of 510Ω be applied to guarantee a fast transition to the inactive state when the PCI 9054 relinquishes ownership of the Local Bus.
BDIP#	M	Burst Data in Progress	1	As an input, driven by the Bus Master during a Burst transaction. The Master de-asserts before the last Data phase on the bus. As an output, driven by the PCI 9054 during the Data phase of a Burst transaction. The PCI 9054 de-asserts before the last Burst Data phase on the bus.
BG#	M	Bus Grant	1	Asserted by the Local Bus arbiter in response to BR#. Indicates the requesting Master is next.
BI#	M	Burst Inhibit	1	Whenever BR# is asserted, indicates that the Target device does not support Burst transactions.
BIGEND#/ WAIT#	All M	Big Endian Select WAIT input/output Select (*WAIT# is available at this location only in M mode)*	1	Multiplexed input/output pin. Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. Big Endian Byte order for Direct Master transfers or Configuration register accesses is also programmable through the Configuration registers. If wait is selected, then PCI 9054 issues WAIT# when it is a Master on the Local Bus and has internal wait states setup. As a Slave, the PCI 9054 accepts WAIT# as an input from the Bus Master.
BLAST#	C, J	Burst Last	1	Signal driven by the current Local Bus Master to indicate the last transfer in a Bus access.
BR#	M	Bus Request	1	Asserted by the Master to request use of the Local Bus. The Local Bus arbiter asserts BG# when the Master is next in line for bus ownership.
BREQi	C, J	Bus Request	1	Asserted to indicate a Local Bus Master requires the bus. If enabled through the PCI 9054 Configuration registers, the PCI 9054 releases the bus during a DMA transfer if this signal is asserted.
BREQo	C, J	Bus Request Out	1	Asserted to indicate the PCI 9054 requires the bus to perform a Direct Slave PCI-to-Local Bus access while a Direct Master access is pending on the Local Bus. Can be used with external logic to assert backoff to a Local Bus Master. Operational parameters are set up through the PCI 9054 Configuration registers.

Table 1-6. PCI 9054 Local Signal Listing (M, C, or J Modes) (continued)

Symbol	Bus Mode	Signal Name	Total Pins	Function
BTERM#	C, J	Burst Terminate	1	As input to the PCI 9054: For processors that burst up to four Lwords. If the Bterm Mode bit is disabled through the PCI 9054 Configuration registers, the PCI 9054 also bursts up to four Lwords. If enabled, the PCI 9054 continues to burst until a BTERM# input is asserted. BTERM# is a Ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9054 programmable wait state generator. As output from the PCI 9054: Asserted, along with READY#, to request break up of a burst and start of a new Address cycle (PCI Aborts only).
BURST#	M	Burst	1	As an input, driven by the Master along with address and data indicating a Burst transfer is in progress. As an output, driven by the PCI 9054 along with address and data indicating a Burst transfer is in progress.
CCS#	All	Configuration Register Select	1	Internal PCI 9054 registers are selected when CCS# is asserted low.
DACK0#	All			*See USERi/DACK0#/LLOCKi#.*
DEN#	J	Data Enable	1	Used in conjunction with DT/R# to provide control for data transceivers attached to the Local Bus.
DMPAF	All			*See MDREQ#/DMPAF/EOT#.*
DP[0:3]	M	Data Parity	4	Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for writes or reads to the PCI 9054. Parity is asserted for reads from or writes by the PCI 9054.
DP[3:0]	C, J			
DREQ0#	All			*See USERo/DREQ0#/LLOCKo#.*
DT/R#	J	Data Transmit/Receive	1	Used in conjunction with DEN# to provide control for data transceivers attached to the Local Bus. When asserted, indicates the PCI 9054 receives data.
EECS	All	Serial EEPROM Chip Select	1	Serial EEPROM Chip Select.
EEDI/EEDO	All	Serial EEPROM Data IN/ Serial EEPROM Data OUT	1	Multiplexed Write/Read data to serial EEPROM pin.
EESK	All	Serial DataClock	1	Serial EEPROM clock pin.
ENUM#	All	Enumeration	1	Interrupt output asserted when an adapter using PCI 9054 has been freshly inserted or is ready to be removed from a PCI slot.
EOT#	All			*See MDREQ#/DMPAF/EOT#.*

Table 1-6. PCI 9054 Local Signal Listing (M, C, or J Modes) (continued)

Symbol	Bus Mode	Signal Name	Total Pins	Function
LA[28:2]	J	Local Address Bus	27	Carries the middle 27 bits of the physical address bus. During bursts, it is incremented to indicate successive Data cycles. The lowest two bits, LA[3:2], carry the Word address of the 32-bit Memory address. All bits are incremented during a Burst access.
LA[0:31]	M	Address Bus	32	Carries the 32 bits of the physical Address Bus.
LA[31:2]	C	Address Bus	30	Carries the upper 30 bits of physical Address Bus. During bursts, LA[31:2] increment to indicate successive Data cycles.
LAD[31:0]	J	Address/Data Bus	32	During an Address phase, the bus carries the upper 30 bits of the physical Address Bus. During a Data phase, the bus carries 32 bits of data.
LBE[3:0]#	C	Byte Enables	4	Encoded, based on the bus-width configuration, as follows: **32-Bit Bus**: The four byte enables indicate which of the four bytes are active during a Data cycle: BE3# Byte Enable 3—LD[31:24] BE2# Byte Enable 2—LD[23:16] BE1# Byte Enable 1—LD[15:8] BE0# Byte Enable 0—LD[7:0] **16-Bit Bus:** BE3#, BE1# and BE0# are encoded to provide BHE#, LA1, and BLE#, respectively: BE3# Byte High Enable (BHE#)—LD[15:8] BE2# not used BE1# Address bit 1 (LA1) BE0# Byte Low Enable (BLE#)—LD[7:0] **8-Bit Bus:** BE1# and BE0# are encoded to provide LA1 and LA0, respectively: BE3# not used BE2# not used BE1# Address bit 1 (LA1) BE0# Address bit 0 (LA0)

Table 1-6. PCI 9054 Local Signal Listing (M, C, or J Modes) (continued)

Symbol	Bus Mode	Signal Name	Total Pins	Function
LBE[3:0]#	J	Byte Enables	4	Encoded, based on the bus-width configuration, as follows: **32-Bit Bus:** The four byte enables indicate which of the four bytes are active during a Data cycle: BE3# Byte Enable 3—LAD[31:24] BE2# Byte Enable 2—LAD[23:16] BE1# Byte Enable 1—LAD[15:8] BE0# Byte Enable 0—LAD[7:0] **16-Bit Bus:** BE3#, BE1# and BE0# are encoded to provide BHE#, LAD1, and BLE#, respectively: BE3# Byte High Enable (BHE#)—LAD[15:8] BE2# not used BE1# Address bit 1 (LAD1) BE0# Byte Low Enable (BLE#)—LAD[7:0] **8-Bit Bus:** BE1# and BE0# are encoded to provide LAD1 and LAD0, respectively: BE3# not used BE2# not used BE1# Address bit 1 (LAD1) BE0# Address bit 0 (LAD0)
LCLK	All	Local processor Clock	1	Local clock input.
LD[0:31]	M	Data Bus	32	Carries 8-, 16-, or 32-bit data quantities, depending upon bus-width configuration. All Master accesses to the PCI 9054 are 32 bits only.
LD[31:0]	C			
LEDon/ LEDin	All	LEDon/LEDin	1	As an output, acts as the Hot Swap board indicator LED. As an input, monitors the CompactPCI board latch status.
LFRAME#	All	PCI Buffered FRAME# Signal	1	Could be used to monitor PCI Bus activity. *Available only on the PBGA package.*
LHOLD	C, J	Hold Request	1	Asserted to request use of the Local Bus. The Local Bus arbiter asserts LHOLDA when control is granted.
LHOLDA	C, J	Hold Acknowledge	1	Asserted by the Local Bus arbiter when control is granted in response to LHOLD. Bus should not be granted to the PCI 9054 unless requested by LHOLD.
LINT#	All	Local Interrupt	1	As an input to the PCI 9054, when asserted low, causes a PCI interrupt. As an output, a synchronous level output that remains asserted as long as an interrupt condition exists. If edge level interrupt is required, disabling and then enabling Local interrupts through INTCSR creates an edge if an interrupt condition still exists or a new interrupt condition occurs.
LLOCKi#	All			*See USERi/DACK0#/LLOCKi#.*
LLOCKo#	All			*See USERo/DREQ0#/LLOCKo#.*
LRESETo#	All	Local Bus Reset Out	1	Asserted when the PCI 9054 chip is reset. Can be used to drive RESET# input of a Local processor.

Table 1-6. PCI 9054 Local Signal Listing (M, C, or J Modes) (continued)

Symbol	Bus Mode	Signal Name	Total Pins	Function
LSERR#	C, J	System Error Interrupt Output	1	Synchronous level output asserted when the PCI Bus Target Abort bit is set (PCISR[11]=1) or Received Master Abort bit is set (PCISR[13]=1). If edge level interrupt is required, disabling and then enabling LSERR# interrupts through the interrupt/control status creates an edge if an interrupt condition still exists or a new interrupt condition occurs.
LW/R#	C, J	Write/Read	1	Asserted low for reads and high for writes.
MDREQ#/ DMPAF/ EOT#	M All All	IDMA Data Transfer Request *(MDREQ# is available at this location in M mode only)* Direct Master Programmable Almost Full End of Transfer for Current DMA Channel	1	Multiplexed input or output pin. MDREQ#: IDMA M mode Data transfer request start. Always asserted, indicating Data transfer should start. De-asserted only when the Direct Master FIFO becomes full. Programmable through a Configuration register. DMPAF: Direct Master Write FIFO Almost Full status output. Programmable through a Configuration register. EOT#: Terminates the current DMA transfer. ***Note:*** *EOT# serves as a general purpose EOT. Before asserting EOT#, user should be aware of DMA channel activity.*
MODE[1:0]	All	Bus Mode	2	Selects the PCI 9054 bus operation mode: Mode 0 / Mode 1 / Bus Mode 1 / 1 / M 1 / 0 / J 0 / 1 / Reserved 0 / 0 / C
RD/WR#	M	Read/Write	1	Asserted high for reads and low for writes.
READY#	C, J	Ready Input/Output	1	When the PCI 9054 is a Bus Master, indicates that Read data on the bus is valid or that a Write Data transfer is complete. Used in conjunction with the PCI 9054 programmable wait state generator. When a Local Bus access is made to the PCI 9054, indicates that Read data on the bus is valid or that a Write Data transfer is complete.
RETRY#	M	Retry	1	Driven by the PCI 9054 when it is a Slave to indicate a Local Master must back off and restart the cycle. In Deferred Read mode, indicates the Master should return for requested data.

Table 1-6. PCI 9054 Local Signal Listing (M, C, or J Modes) (continued)

Symbol	Bus Mode	Signal Name	Total Pins	Function
TA#	M	Transfer Acknowledge	1	As an input, when a Local Bus access is made to the PCI 9054, indicates a Write Data transfer can complete or that Read data on the bus is valid. As an output, when the PCI 9054 is a Bus Master, indicates a Write Data transfer is complete or that Read data on the bus is valid.
TEA#	M	Transfer Error Acknowledge	1	Driven by the Target device, indicating an error condition has occurred during a Bus cycle.
TEST	All	Test Pin	1	Pulled high for test and low for normal operation. When pulled high: All outputs except USERo/DREQ0#/LLOCKo# and LEDon/LEDin are placed in tri-state. USERo/DREQ0#/LLOCKo# provide NANDTREE output.
TS#	M	Address Strobe	1	Indicates the valid address and start of new Bus access. Asserted for the first clock of a Bus access.
TSIZ[0:1]	M	Transfer Size	2	Driven by current Master along with the address, indicating the data-transfer size. Refer to Section 3.4.3.5.3 for more information.
	All		1	Multiplexed input/output pin.
USERi/		User Input		USERi: General-purpose input that can be read by way of the PCI 9054 Configuration registers.
DACK0#/		Demand Mode DMA Acknowledge		DACK0#: When a channel is programmed through the Configuration registers to operate in Demand mode, this output indicates a DMA transfer is being executed. DACK0# corresponds to PCI 9054 DMA Ch 0.
LLOCKi#		Local Lock Input		LLOCKi#: Indicates an atomic operation that may require multiple transactions to complete. Used by the PCI 9054 for direct Local access to the PCI Bus.
	All		1	Multiplexed input/output pin.
USERo/		User Output		USERo: General-purpose output controlled from the PCI 9054 Configuration registers.
DREQ0#/		Demand DMA Request		DREQ0#: When a channel is programmed through the Configuration registers to operate in Demand mode, this input serves as a DMA request. DREQ0# corresponds to PCI 9054 DMA Ch 0.
LLOCKo#		Local Lock Output		LLOCKo#: Indicates an atomic operation for a Direct Slave PCI-to-Local Bus access may require multiple transactions to complete.

Table 1-6. PCI 9054 Local Signal Listing (M, C, or J Modes) (continued)

Symbol	Bus Mode	Signal Name	Total Pins	Function
VDD	All	Power (+3.3V)	15	Three-volt power supply pins for core and I/O buffers. Liberal .01 µF to .1 µF decoupling capacitors should be placed near the PCI 9054.
VSS	All	Ground	12	Ground pins.
WAIT#	C, J	Wait Input/Output	1	As an input, can be asserted to cause the PCI 9054 to insert wait states for Local Direct Master accesses to the PCI Bus. Can be thought of as a Ready input from an external Master for Direct Master accesses. As an output, asserted by the PCI 9054 when internal wait state generator causes wait states. Can be thought of as an output providing PCI 9054 Ready status.
WAIT#	M			*See BIGEND#/WAIT#.*

2. M MODE BUS OPERATION

2.1 PCI Bus Cycles

The PCI 9054 is compliant with PCI Specification v2.2. Refer to PCI Specification v2.2 for specific PCI Bus functions.

2.1.1 PCI Target Command Codes

As a Target, the PCI 9054 allows access to the PCI 9054 internal registers and the Local Bus, using the commands listed in Table 2-1.

All Read or Write accesses to the PCI 9054 can be Byte, Word, or Lword (longword) accesses, defined as 32 bit. All memory commands are aliased to basic memory commands. All I/O accesses to the PCI 9054 are decoded to an Lword boundary. Byte enables are used to determine which bytes are read or written. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

Table 2-1. PCI Target Command Codes

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)
Memory Read Multiple	1100 (Ch)
PCI Dual Address Cycle	1101 (Dh)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

2.1.2 PCI Master Command Codes

The PCI 9054 can access the PCI Bus to perform DMA or Direct Master Local-to-PCI Bus transfers. During a Direct Master or DMA transfer, the command code assigned to the PCI 9054 internal register location (CNTRL[15:0]) is used as the PCI command code (except for Memory Write and Invalidate mode for DMA cycles where (DMPBAM[9]=1). Table 2-2 through Table 2-5 list various PCI Master Command codes.

Notes: *Programmable internal registers determine PCI command codes when the PCI 9054 is the Master.*

DMA cannot perform I/O or configuration accesses.

2.1.2.1 DMA Master Command Codes

DMA controllers of the PCI 9054 can assert the Memory cycles listed in Table 2-2.

Table 2-2. DMA Master Command Codes

Command Type	Code (C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
PCI Dual Address Cycle	1101 (Dh)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

2.1.2.2 Direct Local-to-PCI Command Codes

For direct Local-to-PCI Bus accesses, the PCI 9054 asserts the cycles listed in Table 2-3 through Table 2-5.

Table 2-3. Local-to-PCI Memory Access

Command Type	Code (C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
PCI Dual Address Cycle	1101 (Dh)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

Table 2-4. Local-to-PCI I/O Access

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)

Table 2-5. Local-to-PCI Configuration Access

Command Type	Code (C/BE[3:0]#)
Configuration Memory Read	1010 (Ah)
Configuration Memory Write	1011 (Bh)

2.1.3 PCI Arbitration

The PCI 9054 asserts REQ# to request the PCI Bus. The PCI 9054 can be programmed using the PCI Request Mode bit (MARBR[23]) to de-assert REQ# when it asserts FRAME# during a Bus Master cycle, or to keep REQ# asserted for the entire Bus Master cycle. The PCI 9054 always de-asserts REQ# for a minimum of two PCI clocks between Bus Master ownership that includes a Target disconnect.

The Direct Master Write Delay bits (DMPBAM[15:14]) can be programmed to delay the PCI 9054 from asserting PCI REQ# during a Direct Master Write cycle. DMPBAM can be programmed to wait 0, 4, 8, or 16 PCI Bus clocks after the PCI 9054 has received its first Write data from the Local Bus Master and is ready to begin the PCI Write transaction. This function is useful in applications where a Local Master is bursting and a Local Bus clock is slower than the PCI Bus clock. This allows Write data to accumulate in the PCI 9054 Direct Master Write FIFO, which provides for better use of the PCI Bus.

2.2 Local Bus Cycles

The PCI 9054 interfaces a PCI Host bus to several Local Bus types, as listed in Table 2-6 and Table 2-7. It operates in one of three modes, selected through MODE[1:0] (PQFP—Pins 157 and 156; PBGA—Pins B7 and E8), corresponding to three bus types—M, J, and C.

Table 2-6. Local Bus Types (176-Pin PQFP)

Pin 157	Pin 156	Mode	Bus Type
1	1	M	32-bit non-multiplexed
1	0	Reserved	—
0	1	J	32-bit multiplexed
0	0	C	32-bit non-multiplexed

Table 2-7. Local Bus Types (225-Pin PBGA)

Pin B7	Pin E8	Bus Mode	Bus Type
1	1	M	32-bit non-multiplexed
1	0	Reserved	—
0	1	J	32-bit multiplexed
0	0	C	32-bit non-multiplexed

In M mode, the PCI 9054 provides a direct connection to the MPC850 or MPC860 address and data lines, regardless of the Little Endian or Big Endian mode of the PCI 9054.

2.2.1 Local Bus Arbitration

The PCI 9054 asserts BR# to request the Local Bus. It owns the Local Bus when BG# is asserted. Upon receiving BG#, the PCI 9054 waits for BB# to be de-asserted. The PCI 9054 then asserts BB# at the next rising edge of the Local clock after acknowledging BB# is de-asserted (no other device is acting as the Local Bus Master). The PCI 9054 continues to assert BB# while acting as the Local Bus Master (*that is*, it holds the bus until instructed to release BB#) when the Local Bus Latency Timer is enabled and expires (MARBR[7:0]).

Note: *The Local Bus Pause Timer applies only to DMA operation. It does* ***not*** *apply to Direct Slave operation.*

2.2.2 Direct Master

Local Bus cycles can be Single or Burst cycles. As a Local Bus Target, the PCI 9054 allows access to the PCI 9054 internal registers and the PCI Bus.

Local Bus Direct Master accesses to the PCI 9054 must be for a 32-bit nonpipelined bus. Non-32-bit Direct Master accesses to the PCI 9054 require simple external logic.

2.2.3 Direct Slave

The PCI Bus Master reads from and writes to the Local Bus (the PCI 9054 is a PCI Bus Target and a Local Bus Master).

2.2.4 Wait State Control

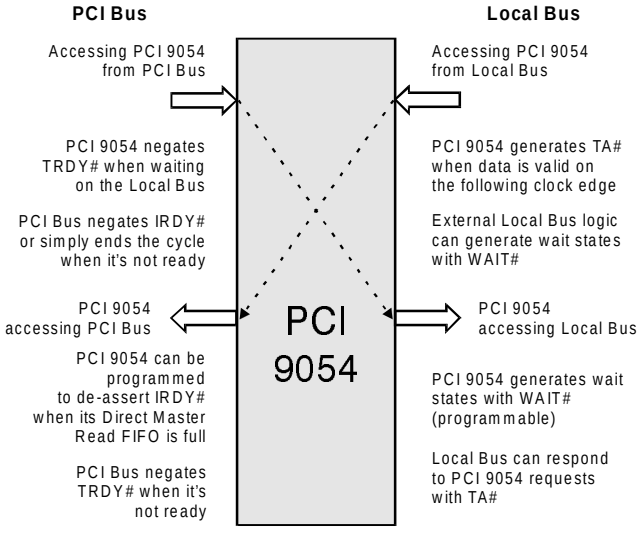


Figure 2-1. Wait States

Note: *The figure represents a sequence of Bus cycles.*

The TA# signal has no effect until the wait state counter is 0. TA# can then be used to introduce additional wait states.

2.2.4.1 Wait States—Local Bus

In Direct Master mode and when accessing the PCI 9054 registers, the PCI 9054 acts as a Local Bus Slave. The PCI 9054 asserts external wait states with the TA# signal.

In Direct Slave and DMA modes, the PCI 9054 acts as a Local Bus Master. The Internal Wait States bit(s) (LBRD0[21:18, 5:2], (LBRD1[5:2]), DMAMODE0[5:2], and/or DMAMODE1[5:2]) can be used to program the number of internal wait states between the first address-to-data (and subsequent data-to-data in Burst mode).

In Direct Slave and DMA modes, if TA# is enabled, it continues the Data transfer, regardless of the wait state counter.

In Direct Slave and DMA modes, the TA# signal has no effect until the wait state counter—(LBRD0[21:18, 5:2]), (LBRD1[5:2]), (DMAMODE0[5:2]), and/or (DMAMODE1[5:2])—reaches zero. TA# then controls the number of wait states by being de-asserted in the middle of the data transaction.

2.2.4.2 Wait States—PCI Bus

The PCI Bus Master throttles IRDY# and the PCI Bus Slave throttles TRDY# to insert PCI Bus wait state(s).

2.2.5 Burst Mode and Continuous Burst Mode (Bterm "Burst Terminate" Mode)

Note: *In the following sections, Bterm refers to the PCI 9054 internal register bit, and BTERM# refers to the PCI 9054 external signal.*

2.2.5.1 Burst and Bterm Modes

Table 2-8. Burst and Bterm on the Local Bus

Mode	Burst	Bterm	Result
Single Cycle	0	0	One TS# per data (default).
Single Cycle	0	1	One TS# per data.
Burst-4	1	0	One TS# per four data (recommended for MPC850 or MPC860).
Burst Forever	1	1	Direct Slave or DMA—One TS# per Burst data or until BI# is asserted (refer to Section 2.2.5.2.1).

Note: *BI# is supported in Burst-4 mode. Refer to the MPC850 or MPC860 data manual.*

On the Local Bus, BTERM# is not supported, but the Bterm bit can be used to gain maximum performance and data throughput.

- If the Burst Mode bit is enabled, but the Bterm Mode bit is disabled, then the PCI 9054 bursts four Lwords. BDIP# is de-asserted at the last Lword transfer before its completion (LA[3:2]=11) and a new TS# is asserted at the first Lword (LA[3:2]=00) of the next burst.
- If the Burst Mode and Bterm Mode bits are both enabled, then the PCI 9054 bursts until the transfer counter counts to "0", the Local Latency Timer is enabled and expires, the EOT function is introduced, or DREQ0# is de-asserted during DMA transactions. For Direct Slave transactions, the PCI 9054 bursts until BI# is asserted, implying a new TS# is required, or the Local Latency Timer is enabled and expires. BDIP# output is not supported in this case.

Notes: *If Address Increment is disabled, the DMA transaction bursts beyond four Lwords.*

If the Bterm Mode bit is disabled, the PCI 9054 performs the following:

- ***32-bit Local Bus****—Bursts up to four Lwords*
- ***16-bit Local Bus****—Bursts up to two Lwords*
- ***8-bit Local Bus****—Bursts up to one Lword*

In every case, it performs four transactions.

2.2.5.2 Burst-4 Lword Mode

If the Burst Mode bit is enabled and the Bterm Mode bit is disabled, bursting can start only on a 16-byte boundary and continue up to the next 16-byte address boundary. After data before the boundary is transferred, the PCI 9054 asserts a new Address cycle (TS#).

Table 2-9. Burst-4 Lword Mode

Bus Width	Burst
32 bit	Four Lwords or up to a quad Lword boundary (LA3, LA2 = 11)
16 bit	Eight words or up to a quad Lword boundary (LA2, LA1 = 11)
8 bit	Sixteen bytes or up to a quad Lword boundary (LA1, LA0 = 11)

2.2.5.2.1 Continuous Burst Mode (Bterm "Burst Terminate" Mode)

If both the Burst and Bterm Mode bits are enabled, the PCI 9054 can operate beyond the Burst-4 Lword mode.

Bterm mode enables the PCI 9054 to perform long bursts to special external M-mode interface devices that

can accept bursts of longer than four Lwords. The PCI 9054 asserts one Address cycle and continues to burst data. The external address is incremented during bursts. If a device requires a new Address cycle, it can assert BI# input anywhere after the first Data phase to cause the PCI 9054 to assert a new Address cycle (TS#). The BI# input acknowledges the current Data transfer and requests that a new Address cycle be asserted (TS#), for the next Data transfer. If the Bterm Mode bit is enabled, the PCI 9054 de-asserts BURST# only if its Read FIFO is full, its Write FIFO is empty, or if a transfer is complete.

For continuous bursts greater than four Lwords, the BURST# signal should be used to qualify the end of the Burst transaction. The BDIP# output signal is not driven in this situation.

During Burst Forever Write transactions in M mode, the PCI 9054 passes all bytes from the PCI Bus to the Local Bus, if C/BE# begins to toggle on the nonquad-aligned address by keeping TSIZ[0:1] at a constant value of 0 and issues TS# for the toggled address. However, if C/BE# toggles on the quadword-aligned address, the PCI 9054 begins the Local Bus Burst and toggles TSIZ[0:1], along with TS#, for all data that follows when a burst resumes. It is recommended to keep all bytes enabled during a PCI Write Burst transaction.

2.2.5.3 Partial Lword Accesses

Lword accesses in which not all byte enables are asserted will be broken into Single-Cycle accesses. Burst start addresses can be any Lword boundary. If the Burst Start Address in a Direct Slave or DMA transfer is not aligned to an Lword boundary, the PCI 9054 first performs a Single cycle. It then starts to burst on the Lword boundary if there is remaining data that is not a whole Lword during DMA (*for example*, it will result in a Single cycle at the end).

2.2.6 Local Bus Read Accesses

For all Single-Cycle Local Bus Read accesses, the PCI 9054 reads only bytes corresponding to byte enables requested by the PCI Initiator. For all Burst Read cycles, the PCI 9054 can be programmed to

- Prefetch
- Perform Read Ahead mode
- Generate internal wait states
- Enable external wait control (TA# input)
- Enable type of Burst mode to perform

2.2.7 Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Bus Master or the PCI 9054 DMA controller are written.

2.2.8 Direct Slave Accesses to 8- or 16-Bit Local Bus

Direct PCI access to an 8- or 16-bit Local Bus results in the PCI Bus Lword being broken into multiple Local Bus transfers. For each transfer, byte enables are encoded to provide Local Address bits LA[1:0].

2.2.9 Local Bus Data Parity

Generation or use of Local Bus data parity is optional. Signals on the data parity pins do not affect operation of the PCI 9054. The PCI Bus parity checking and generation is independent of the Local Bus parity checking and generation. PCI Bus parity checking may result in assertion of PERR#, a PCI Bus system error (SERR#), or other means of PCI Bus transfer termination as a result of the parity error on the PCI data address, command code, and byte enables. The Local Bus Parity Check is passive and only provides parity information to the Local processor during Direct Master, Direct Slave, and DMA transfers.

There is one data parity pin for each byte lane of the PCI 9054 data bus (DP[0:3]). “Even data parity” is asserted for each lane during Local Bus reads from the PCI 9054 and during PCI 9054 Master writes to the Local Bus.

Even data parity is checked during Local Bus writes to the PCI 9054 and during PCI 9054 reads from the Local Bus. Parity is checked for each byte lane with an asserted byte enable. If a parity error is detected, TEA# is asserted in the Clock cycle following the data being checked.

2.3 Big Endian/Little Endian

2.3.1.1 PCI Bus Little Endian Mode

PCI Bus is a Little Endian bus (*that is*, the address is invariant and data is Lword-aligned to the lowermost byte lane).

Table 2-10. PCI Bus Little Endian Byte Lanes

Byte Number	Byte Lane
0	AD[7:0]
1	AD[15:8]
2	AD[23:16]
3	AD[31:24]

2.3.1.2 Local Bus Big/Little Endian Mode

The PCI 9054 Local Bus can be programmed to operate in Big or Little Endian mode**.**

Table 2-11. Byte Number and Lane Cross-Reference

Byte Number		Byte Lane
Big Endian	Little Endian	
3	0	LD[31:24]
2	1	LD[23:16]
1	2	LD[15:8]
0	3	LD[7:0]

Table 2-12. Big/Little Endian Program Mode

BIGEND# Pin	BIGEND Register (1=Big, 0=Little)	Endian Mode
0	0	Big
0	1	Big
1	0	Little
1	1	Big

Table 2-13 lists registers for information about the following cycles.

Table 2-13. Cycles Reference Tables

Cycles	Register Bits
Local access to the Configuration registers	BIGEND[0]
Direct Master, Memory, and I/O	BIGEND[1]
Direct Slave	BIGEND[2], Space 0, and BIGEND[3], Expansion ROM

In Big Endian mode, the PCI 9054 transposes data byte lanes. Data is transferred as listed in Table 2-14 through Table 2-18.

2.3.1.3 32-Bit Local Bus—Big Endian Mode

Data is Lword aligned to uppermost byte lane (Address Invariance).

Table 2-14. Upper Lword Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

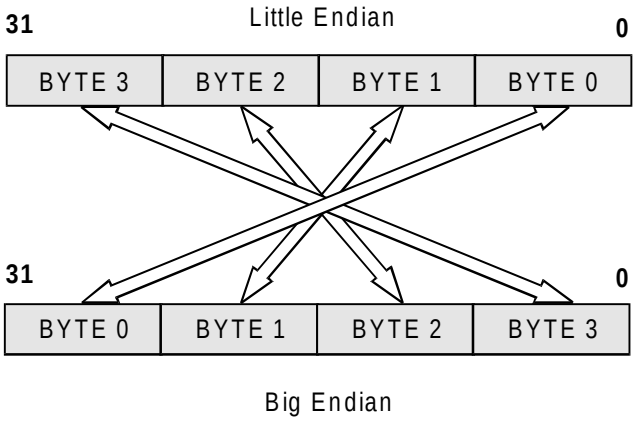


Figure 2-2. Big/Little Endian—32-Bit Local Bus

2.3.1.4 16-Bit Local Bus—Big Endian Mode

For a 16-bit Local Bus, the PCI 9054 can be programmed to use upper or lower word lanes.

Table 2-15. Upper Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
Second Transfer	Byte 2 appears on Local Data [31:24]
	Byte 3 appears on Local Data [23:16]

Table 2-16. Lower Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [15:8]
	Byte 1 appears on Local Data [7:0]
Second Transfer	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

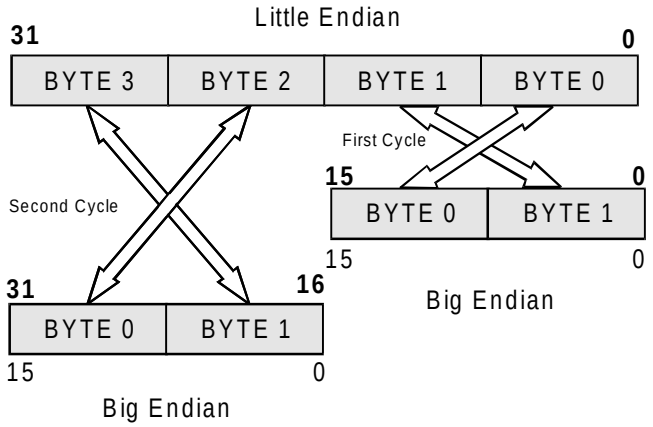


Figure 2-3. Big/Little Endian—16-Bit Local Bus

2.3.1.5 8-Bit Local Bus—Big Endian Mode

For an 8-bit Local Bus, the PCI 9054 can be programmed to use upper or lower byte lanes.

Table 2-17. Upper Byte Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24]
Second transfer	Byte 1 appears on Local Data [31:24]
Third transfer	Byte 2 appears on Local Data [31:24]
Fourth transfer	Byte 3 appears on Local Data [31:24]

Table 2-18. Lower Byte Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [7:0]
Second Transfer	Byte 1 appears on Local Data [7:0]
Third Transfer	Byte 2 appears on Local Data [7:0]
Fourth Transfer	Byte 3 appears on Local Data [7:0]

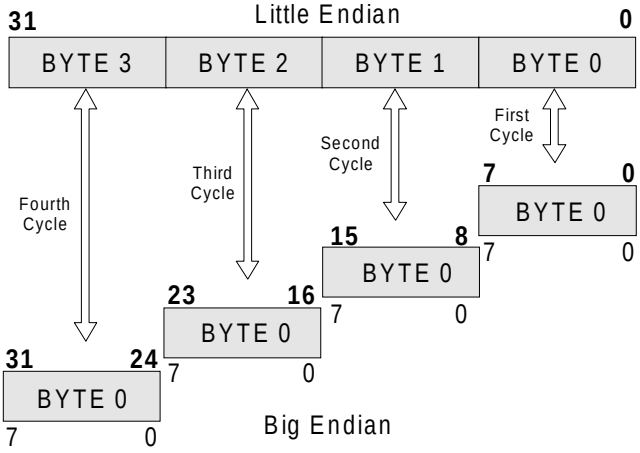


Figure 2-4. Big/Little Endian—8-Bit Local Bus

2.3.1.6 Local Bus Big/Little Endian Mode Accesses

For each of the following transfer types, the PCI 9054 Local Bus can be independently programmed to operate in Little Endian or Big Endian mode:

- Local Bus accesses to the PCI 9054 Configuration registers
- Direct Slave PCI accesses to Local Address Space 0
- Direct Slave PCI accesses to Local Address Space 1
- Direct Slave PCI accesses to Expansion ROM
- DMA Channel 0 accesses to the Local Bus
- DMA Channel 1 accesses to the Local Bus
- Direct Master Accesses to the PCI Bus

For Local Bus accesses to the Internal Configuration registers and Direct Master accesses, use BIGEND# to dynamically change the Endian mode.

Notes: *The PCI Bus is always Little Endian.*

Only byte lanes are swapped, not individual bits.

2.4 Serial EEPROM

Functional operation described can be modified through the PCI 9054 programmable internal registers.

2.4.1 Vendor and Device ID Registers

Three Vendor and Device ID registers are supported:

- **PCIIDR**—Contains the normal Device and Vendor IDs. Can be loaded from the serial EEPROM or Local processor(s).
- **PCISVID**—Contains the Subsystem and Subvendor IDs. Can be loaded from the serial EEPROM or Local processor(s).
- **PCIHIDR**—Contains the (hardcoded) PLX Vendor and Device IDs.

2.4.1.1 Serial EEPROM Initialization

During serial EEPROM initialization, the PCI 9054 responds to PCI Target accesses with a Retry. During serial EEPROM initialization, the PCI 9054 responds to a Local processor access by delaying acknowledgement of the cycle (TA#).

2.4.1.2 Local Initialization

The PCI 9054 issues a Retry to all PCI accesses until the Local Init Status bit (LMISC[2]) is set. This bit can be programmed three different ways:

1. By the Local processor, through the Local Configuration register.
2. By the serial EEPROM, during a serial EEPROM load, if the Local processor does not set this bit or if this bit is missing.
3. If the Local processor and/or the serial EEPROM are missing, the serial EEPROM remains blank and the PCI 9054 reverts to the default values and sets this bit (refer to Table 2-19).

2.4.2 Serial EEPROM Operation

After reset, the PCI 9054 attempts to read the serial EEPROM to determine its presence. An active start bit set to 0 indicates a serial EEPROM is present. The PCI 9054 supports 93CS56L (2 kilobit) or 93CS66L (4 kilobit). (Refer to manufacturer's data sheet for the particular serial EEPROM being used.) The first Lword is then checked to verify that the serial EEPROM is programmed. If the first Lword (32 bits) is all ones, a blank serial EEPROM is present. If the first Lword (32 bits) is all zeros, no serial EEPROM is present. For both conditions, the PCI 9054 reverts to the default

values. (Refer to Table 2-19.) CNTRL[28] is set to 1 if programmed (real or random data if a serial EEPROM is detected).

The 3.3V serial EEPROM clock (EESK) is derived from the PCI clock. The PCI 9054 generates the serial EEPROM clock by internally dividing the PCI clock by 132.

Table 2-19. Serial EEPROM Guidelines

Local Processor	Serial EEPROM	System Boot Condition
None	None	The PCI 9054 uses default values. The EEDI/EEDO pin must be **pulled low**—a 1 K-ohm resistor is required (rather than pulled high, which is typically done for this pin). If PCI 9054 detects all zeros, it reverts to default values.
None	Programmed	Boot with serial EEPROM values. The Local Init Status bit (LMISC[2]) must be set by the serial EEPROM.
None	Blank	The PCI 9054 detects a blank device and reverts to default values.
Present	None	The Local processor programs the PCI 9054 registers, then sets the Local Init Status bit (LMISC[2]=done). ***Note:*** *Some systems may hang if Direct Slave reads and writes take a long time (during initialization, the PCI Host also performs Direct Slave accesses). The value of the PCI Target Retry Delay Clocks (LBRD0[31:28]) may resolve this problem.*
Present	Programmed	Load serial EEPROM, but the Local processor can reprogram the PCI 9054. Either the Local processor or the serial EEPROM must set the Local Init Status bit (LMISC[2]=done).
Present	Blank	The PCI 9054 detects a blank serial EEPROM and reverts to default values. ***Notes:*** *In some systems, the Local processor may be too late to reconfigure the PCI 9054 registers before the BIOS configures the PCI 9054.* *The serial EEPROM can be programmed through the PCI 9054 after the system boots in this condition.*

The serial EEPROM can be read or written from the PCI or Local Buses. The Serial EEPROM Control Register bits (CNTRL[28:24]) control the PCI 9054 pins that enable reading or writing of serial EEPROM data bits. (Refer to manufacturer's data sheet for the particular serial EEPROM being used.)

The serial EEPROM can also be read or written, using the VPD function (refer to Section 10).

The PCI 9054 has two serial EEPROM load options:

- **Long Load Mode**—Default. The PCI 9054 loads 17 Lwords from the Serial EEPROM and the Extra Long Load bit (LBRD0[25])
- **Extra Long Load Mode**—The PCI 9054 loads 22 Lwords if the Serial EEPROM and the Extra Long Load bit (LBRD0[25]) is set to 1 during a Long Load

2.4.2.1 Long Serial EEPROM Load

The registers listed in Table 2-20 are loaded from the serial EEPROM after a reset is de-asserted if the Serial EEPROM Extra Long Load bit is not set (LBRD0[25]=0). The serial EEPROM is organized in words (16 bit). The PCI 9054 first loads the Most Significant Word bits (MSW[31:16]), starting from the most significant bit ([31]). The PCI 9054 then loads the Least Significant Word bits (LSW[15:0]), starting again from the most significant bit ([15]). Therefore, the PCI 9054 loads the Device ID, Vendor ID, class code, and so forth.

The serial EEPROM values can be programmed using a Data I/O programmer. The values can also be programmed using the PCI 9054 VPD function (refer to Section 10) or through the Serial EEPROM Control register (CNTRL).

The CNTRL register allows programming of the serial EEPROM, one bit at a time. To read back the value from the serial EEPROM, the Vital Product Data (VPD) function should be utilized. With full utilization of VPD, the designer can perform reads and writes from/to the serial EEPROM, 32 bits at a time. Values should be programmed in the order listed in Table 2-20. The 34, 16-bit words listed in the table are stored sequentially in the serial EEPROM.

Table 2-20. Long Serial EEPROM Load Registers

Serial EEPROM Offset	Description	Register Bits Affected
0h	Device ID	PCIIDR[31:16]
2h	Vendor ID	PCIIDR[15:0]
4h	Class Code	PCICCR[23:8]
6h	Class Code / Revision	PCICCR[7:0] / PCIREV[7:0]
8h	Maximum Latency / Minimum Grant	PCIMLR[7:0] / PCIMGR[7:0]
Ah	Interrupt Pin / Interrupt Line Routing	PCIIPR[7:0] / PCIILR[7:0]
Ch	MSW of Mailbox 0 (User Defined)	MBOX0[31:16]
Eh	LSW of Mailbox 0 (User Defined)	MBOX0[15:0]
10h	MSW of Mailbox 1 (User Defined)	MBOX1[31:16]
12h	LSW of Mailbox 1 (User Defined)	MBOX1[15:0]
14h	MSW of Range for PCI-to-Local Address Space 0	LAS0RR[31:16]
16h	LSW of Range for PCI-to-Local Address Space 0	LAS0RR[15:0]
18h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[31:16]
1Ah	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[15:0]
1Ch	MSW of Mode/DMA Arbitration Register	MARBR[31:16]
1Eh	LSW of Mode/DMA Arbitration Register	MARBR[15:0]
20h	MSW of Serial EEPROM Write-Protected Address	PROT_AREA[15:0]
22h	LSW of Local Miscellaneous Control Register / LSW of Local Bus Big/Little Endian Descriptor Register	LMISC[7:0] / BIGEND[7:0]
24h	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]
26h	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]
28h	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[31:16]
2Ah	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[15:0]
2Ch	MSW of Bus Region Descriptors for PCI-to-Local Accesses	LBRD0[31:16]
2Eh	LSW of Bus Region Descriptors for PCI-to-Local Accesses	LBRD0[15:0]
30h	MSW of Range for Direct Master-to-PCI	DMRR[31:16]
32h	LSW of Range for Direct Master-to-PCI	DMRR[15:0]
34h	MSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[31:16]
36h	LSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[15:0]
38h	MSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[31:16]
3Ah	LSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[15:0]
3Ch	MSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[31:16]
3Eh	LSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[15:0]
40h	MSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[31:16]
42h	LSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[15:0]

2.4.2.2 Extra Long Serial EEPROM Load

The registers listed in the Local Address Space 0/Expansion ROM Bus Region Descriptor register (LBRD0) are loaded from serial EEPROM after a reset is de-asserted if the Serial EEPROM Extra Long Load bit is set (LBRD0[25]=1). The serial EEPROM is organized in words (16 bit). The PCI 9054 first loads the Most Significant Word bits ([31:16]), starting from the most significant bit ([31]). It then loads the Least Significant Word bits ([15:0]), restarting from the most significant bit ([15]). Therefore, the PCI 9054 loads Device ID, Vendor ID, class code, and so forth.

The serial EEPROM values can be programmed using a Data I/O programmer. The values can also be programmed using the PCI 9054 VPD function or through the Serial EEPROM Control register (CNTRL). Values should be programmed in the order listed in Table 2-21. The 44 16-bit words listed in Table 2-20 and Table 2-21 should be stored sequentially in the serial EEPROM.

Table 2-21. Extra Long Serial EEPROM Load Registers

Serial EEPROM Offset	Description	Register Bits Affected
44h	Subsystem ID	PCISID[15:0]
46h	Subsystem Vendor ID	PCISVID[15:0]
48h	MSW of Range for PCI-to-Local Address Space 1 (1 MB)	LAS1RR[31:16]
4Ah	LSW of Range for PCI-to-Local Address Space 1 (1 MB)	LAS1RR[15:0]
4Ch	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[31:16]
4Eh	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[15:0]
50h	MSW of Bus Region Descriptors (Space 1) for PCI-to-Local Accesses	LBRD1[31:16]
52h	LSW of Bus Region Descriptors (Space 1) for PCI-to-Local Accesses	LBRD1[15:0]
54h	MSW of Hot Swap Control	Reserved
56h	LSW of Hot Swap Control / Hot Swap Next Capability Pointer	HS_NEXT[7:0] / HS_CNTL[7:0]

2.4.2.3 New Capabilities Function Support

The New Capabilities Function Support includes PCI Power Management, Hot Swap, and VPD features, as listed in Table 2-22.

Table 2-22. New Capabilities Function Support Features

New Capability Function	PCI Register Offset Location
First (Power Management)	40'h, if the New Capabilities Function Support bit (PCISR[4]) is enabled (PCISR[4] is enabled, by default).
Second (Hot Swap)	48'h, which is pointed to from PMNEXT[7:0].
Third (VPD)	4C'h, which is pointed to from HS_NEXT[7:0]. Because PVPD_NEXT[7:0] defaults to zero, this indicates that VPD is the last New Capability Function Support feature of the PCI 9054.

2.4.2.4 Recommended Serial EEPROMs

The PCI 9054 is designed to use either a 2-kilobit (NM93CS56L or compatible) or 4-kilobit (NM93CS66L or compatible) device.

Note: *The PCI 9054 does not support serial EEPROMs that do not support sequential reads and writes (such as the NM93C56L).*

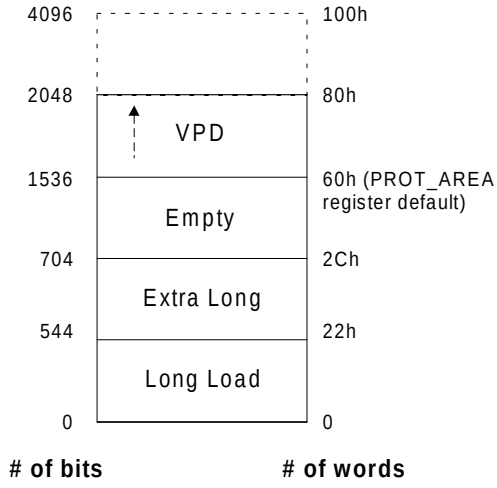


Figure 2-5. Serial EEPROM Memory Map

2.4.2.5 Serial EEPROM Initialization

During serial EEPROM initialization, the PCI 9054 responds to PCI Target accesses with a Retry. During serial EEPROM initialization, the PCI 9054 responds to a Local processor access by delaying acknowledgement of the cycle (TA#).

2.4.3 Internal Register Access

The PCI 9054 provides several internal registers, which allow for maximum flexibility in the bus interface design and performance. These registers are accessible from the PCI and Local Buses and include the following:

- PCI Configuration registers
- Local Configuration registers
- DMA registers
- Mailbox registers
- PCI-to-Local and Local-to-PCI Doorbell registers
- Messaging Queue registers (I_2O)
- Power Management registers
- Hot Swap registers
- VPD registers

Figure 2-6 illustrates how these registers are accessed.

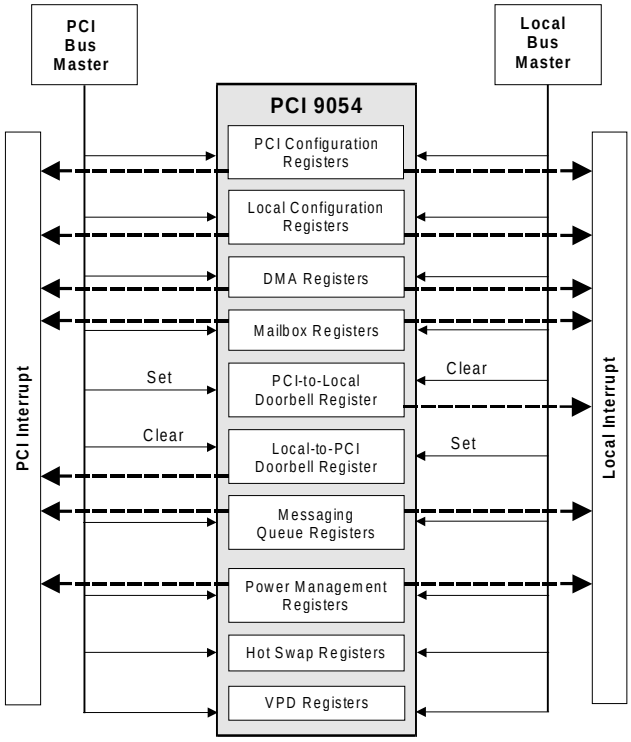


Figure 2-6. PCI 9054 Internal Register Access

2.4.3.1 PCI Bus Access to Internal Registers

The PCI 9054 PCI Configuration registers can be accessed from the PCI Bus with a Configuration Type 0 cycle.

All other PCI 9054 internal registers can be accessed by a Memory cycle, with the PCI Bus address that matches the base address specified in PCI Base Address 0 (PCIBAR0[31:8]) for the PCI 9054 Memory-Mapped Configuration register. These registers can also be accessed by an I/O cycle, with the PCI Bus address matching the base address specified in PCI Base Address 1 for the PCI 9054 I/O-Mapped Configuration register.

All PCI Read or Write accesses to the PCI 9054 registers can be Byte, Word, or Lword accesses. All PCI Memory accesses to the PCI 9054 registers can be Burst or Non-Burst accesses. The PCI 9054 responds with a PCI disconnect for all Burst I/O accesses (PCIBAR1[31:8]) to the PCI 9054 Internal registers.

2.4.3.2 Local Bus Access to Internal Registers

The Local processor can access all PCI 9054 internal registers through an external chip select. The PCI 9054 responds to a Local Bus access when the PCI 9054 Configuration Chip Select input (CCS#) is asserted low. Figure 2-7 illustrates how the Configuration Chip Select logic works.

Note: *CCS# must be decoded while TS# is low.*

Accesses must be for a 32-bit non-pipelined bus.

Local Read or Write accesses to the PCI 9054 internal registers can be Byte, Word, or Lword accesses. Local accesses to the PCI 9054 internal registers can be Burst or Non-Burst accesses.

The PCI 9054 TA# signal indicates that Data transfer is complete.

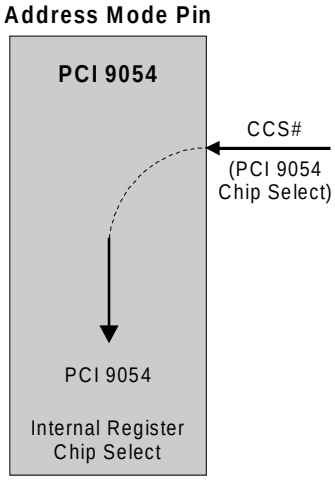
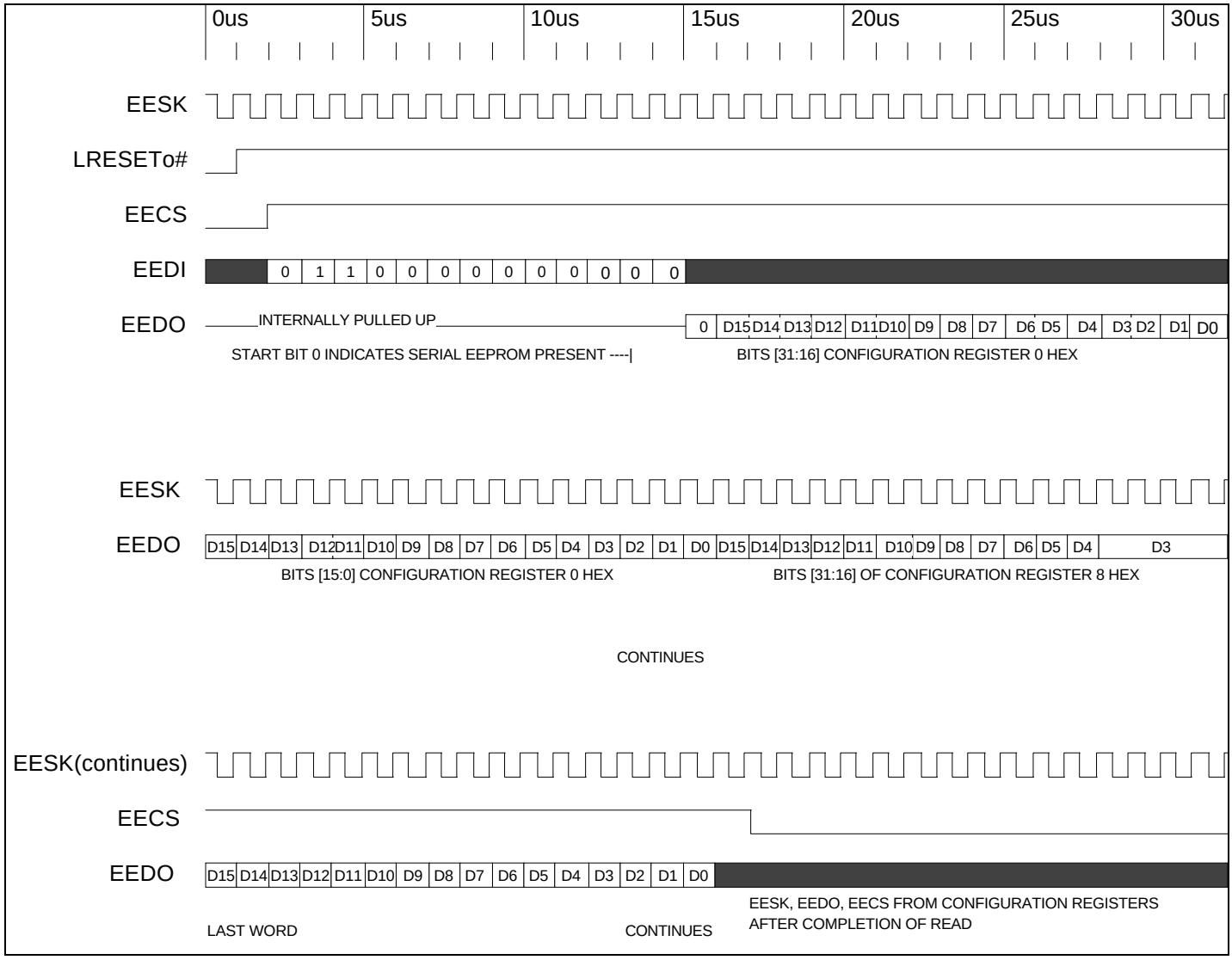
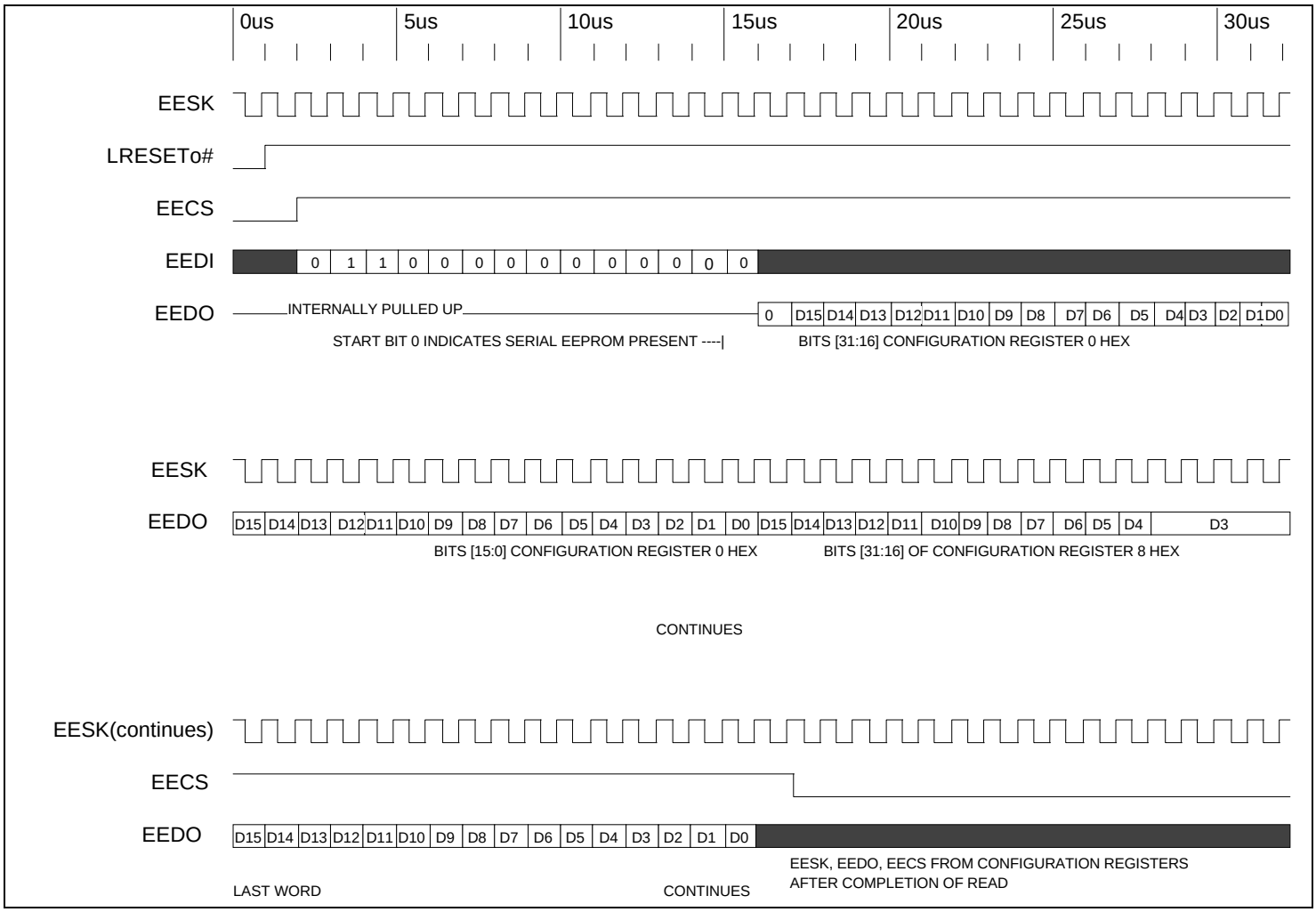


Figure 2-7. Address Decode Mode

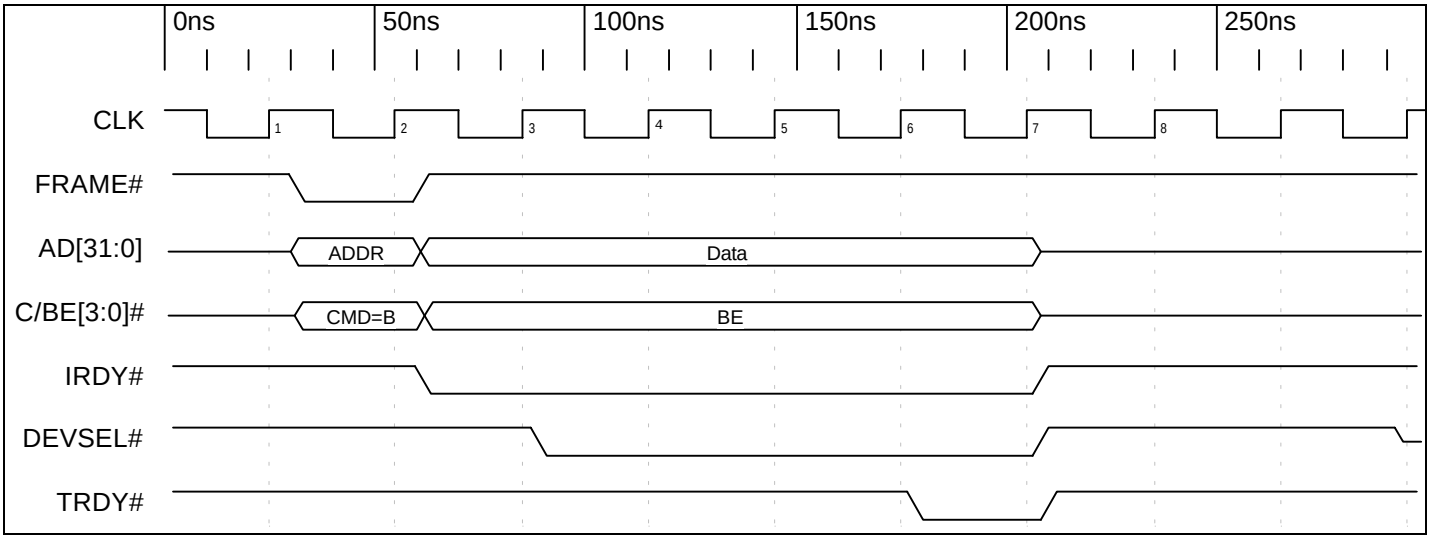
2.4.4 Serial EEPROM Timing Diagrams



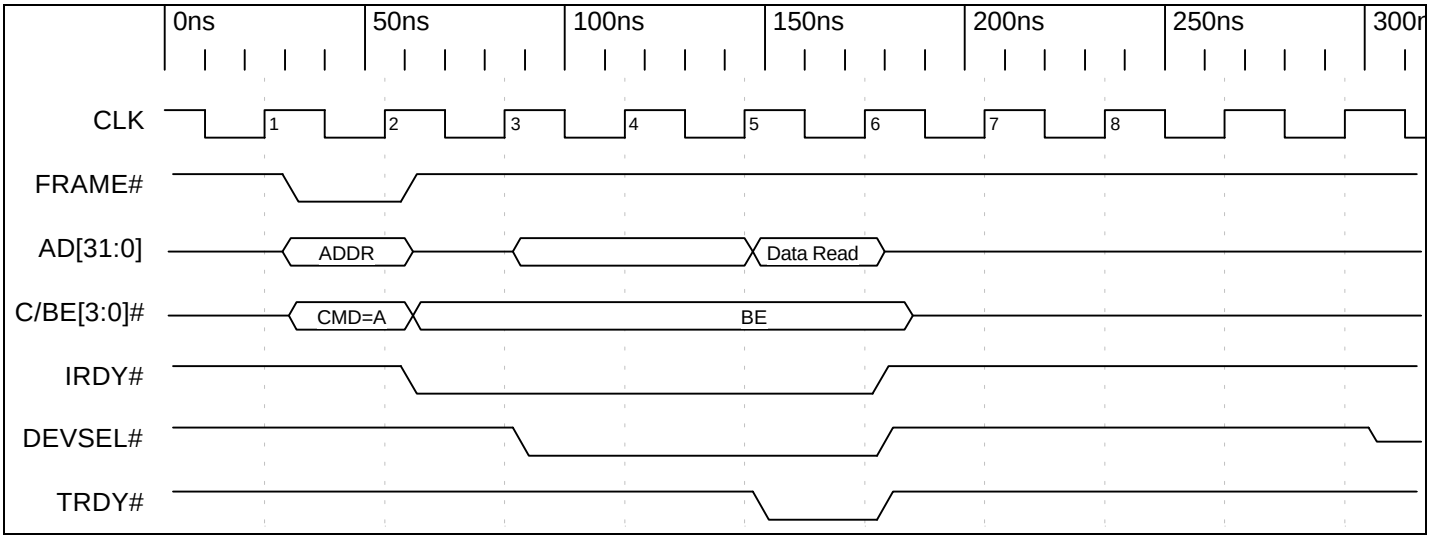
Timing Diagram 2-1. Initialization from Serial EEPROM (2K)



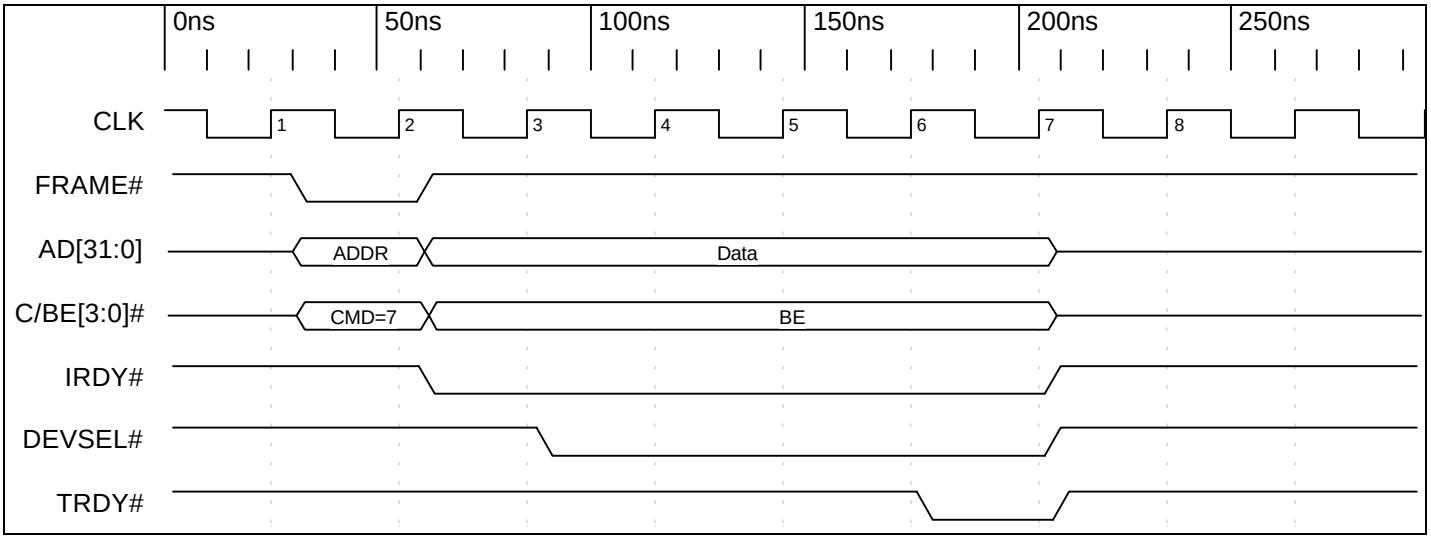
Timing Diagram 2-2. Initialization from Serial EEPROM (4K)



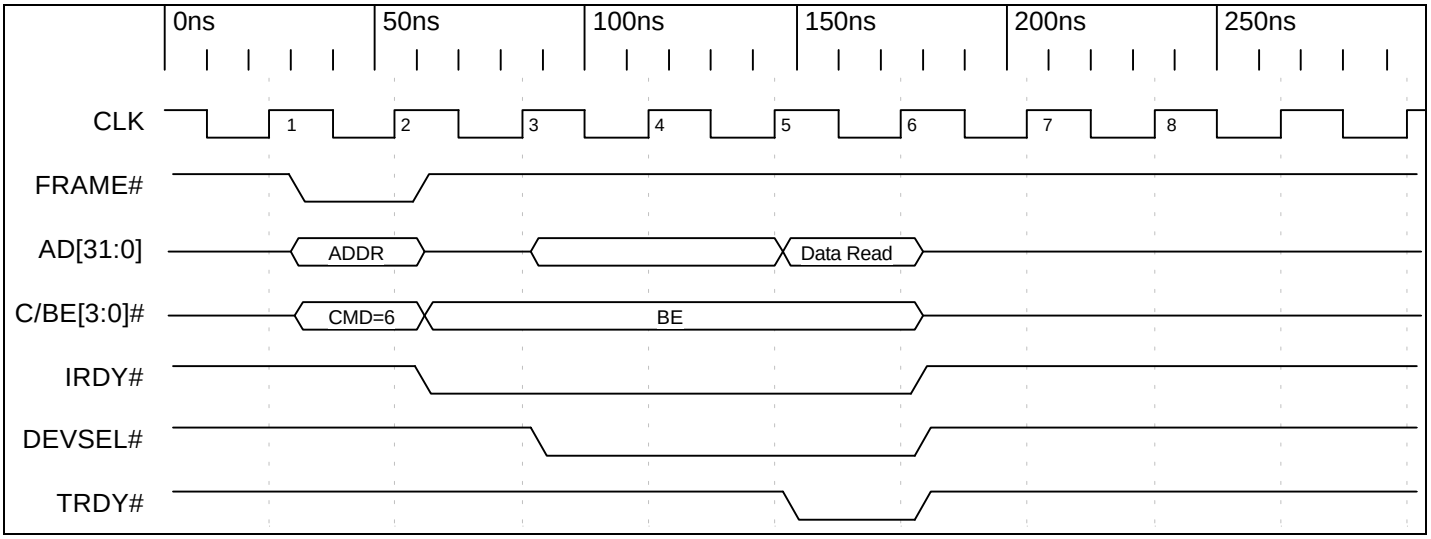
Timing Diagram 2-3. PCI Configuration Write to PCI Configuration Register



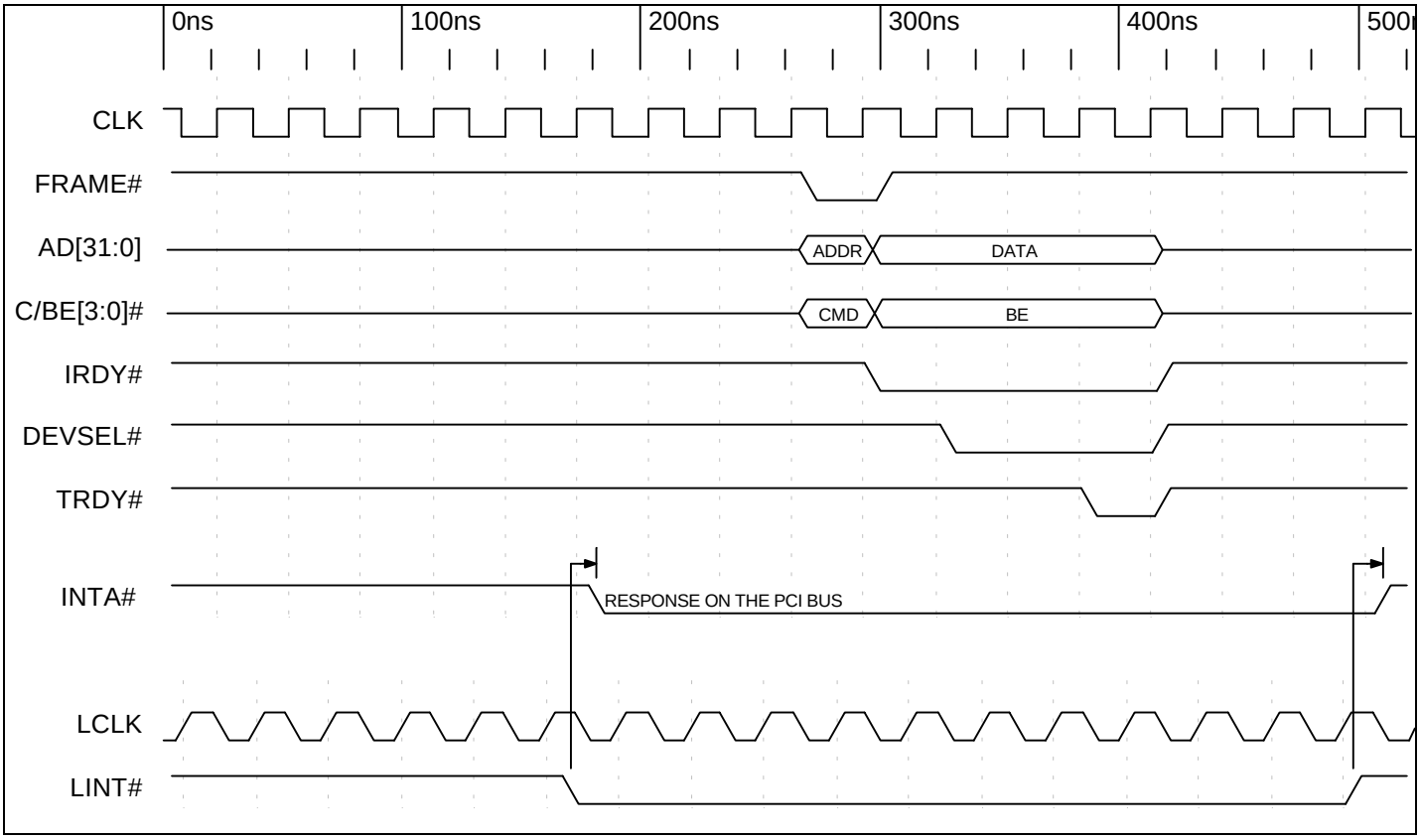
Timing Diagram 2-4. PCI Configuration Read to PCI Configuration Register



Timing Diagram 2-5. PCI Memory Write to Local Configuration Register



Timing Diagram 2-6. PCI Memory Read to Local Configuration Register



Timing Diagram 2-7. Local Interrupt Asserting PCI Interrupt

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3. M MODE FUNCTIONAL DESCRIPTION

The functional operation described here can be modified through the PCI 9054 programmable internal registers.

3.1 Reset Operation

3.1.1 PCI Bus Input RST#

PCI Bus RST# input pin is a PCI Host reset. It causes all PCI Bus outputs to float, resets the entire PCI 9054 and causes the Local reset LRESETo# signal to be asserted.

3.1.2 Software Reset

A Host on the PCI Bus can set the PCI Adapter Software Reset bit (CNTRL[30]=1) to reset the PCI 9054 and assert LRESETo# output. All Local Configuration registers are reset; however, the PCI Configuration DMA and Shared Runtime registers and the Local Init Status bit (LMISC[2]) are not reset. When the Software Reset bit (CNTRL[30]) is set, the PCI 9054 responds to PCI accesses, but not to Local Bus accesses. The PCI 9054 remains in this reset condition until the PCI Host clears the bit. The serial EEPROM is reloaded if the Reload Configuration Registers bit is set (CNTRL[29]=1).

Note: *The Local Bus cannot clear this reset bit because the Local Bus is in a reset state, even if the Local processor does not use LRESETo# to reset.*

3.2 PCI 9054 Initialization

The PCI 9054 Configuration registers can be programmed by an optional serial EEPROM and/or by a Local processor, as listed in Table 2-19. The serial EEPROM can be reloaded by setting the Reload Configuration Registers bit (CNTRL[29]).

The PCI 9054 retries all PCI cycles until the Local Init Status bit is set to “done” (LMISC[2]=1).

Note: *The PCI Host processor can also access Internal Configuration registers after the Local Init Status bit is set.*

If a PCI Host is present, the Master Enable, Memory Space, and I/O Space bits (PCICR[2:0]) are programmed by that Host after initialization completes (LMISC[2]=1).

3.3 Response to FIFO Full or Empty

Table 3-1 lists the response of the PCI 9054 to full and empty FIFOs.

3.4 Direct Data Transfer Modes

The PCI 9054 supports three direct transfer modes:

- **Direct Master**—Local CPU accesses PCI memory or I/O
- **Direct Slave**—PCI Master accesses Local memory or I/O
- **DMA**—PCI 9054 DMA controller reads/writes PCI memory to/from Local memory

3.4.1 Direct Master Operation (Local Master-to-PCI Target)

The PCI 9054 supports a direct access of the PCI Bus by the Local processor or an intelligent controller. Master mode must be enabled in the PCI Command register. The following registers define Local-to-PCI accesses:

- Direct Master Memory and I/O Range (DMRR)
- Local Base Address for Direct Master-to-PCI Memory (DMLBAM)
- Local Base Address for Direct Master-to-PCI I/O and Configuration (DMLBAI)
- PCI Base Address (DMPBAM)
- Direct Master Configuration (DMCFGA)
- Direct Master PCI Dual Address Cycles (DMDAC)
- Master Enable (PCICR)
- PCI Command Code (CNTRL)

Table 3-1. Response to FIFO Full or Empty

Mode	Direction	FIFO	PCI Bus	Local Bus
Direct Master Write	Local-to-PCI	Full	Normal	De-assert TA#, RETRY# [1]
		Empty	De-assert REQ# (off the PCI Bus)	Normal
Direct Master Read	PCI-to-Local	Full	De-assert REQ# or throttle IRDY#[2]	Normal
		Empty	Normal	De-assert TA#
Direct Slave Write	PCI-to-Local	Full	Disconnect or throttle TRDY# [4]	Normal
		Empty	Normal	De-assert BB# [3]
Direct Slave Read	Local-to-PCI	Full	Normal	De-assert BB# [3]
		Empty	Throttle TRDY# [4]	Normal
DMA	Local-to-PCI	Full	Normal	De-assert BB# [3]
		Empty	De-assert REQ#	Normal
	PCI-to-Local	Full	De-assert REQ#	Normal
		Empty	Normal	De-assert BB# [3]

Notes:

1 *Issue RETRY# depends upon the Direct Master Write FIFO Almost Full RETRY# Output Enable bit (LMISC[6]).*

2 *Throttle IRDY# depends upon the Direct Master PCI Read Mode bit (DMPBAM[4]).*

3 *BB# de-assert depends upon the Local Bus Direct Slave Release Bus Mode bit (MARBR[21]).*

4 *Throttle TRDY4 depends upon the Direct Slave Write mode bit (LBRD0[27]).*

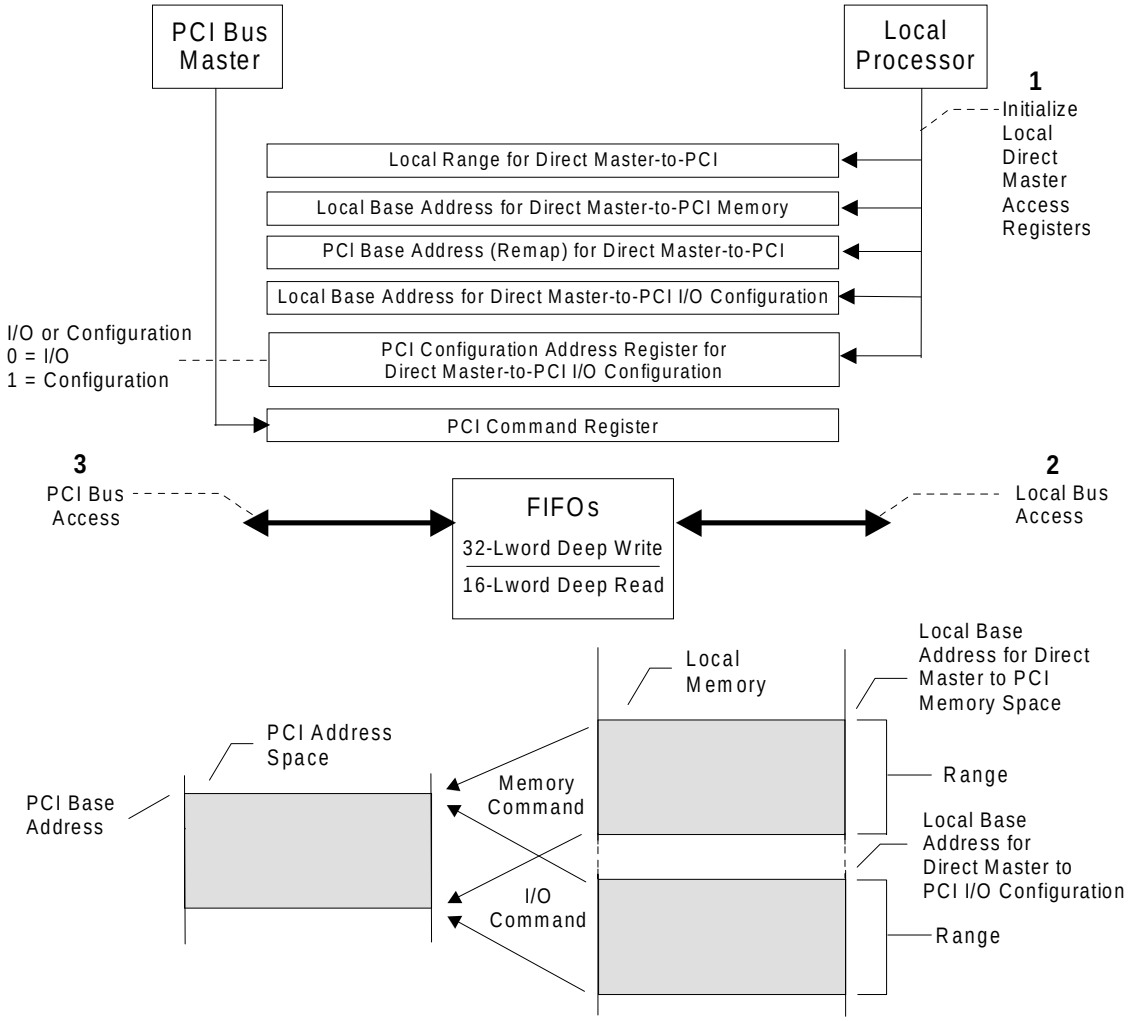


Figure 3-1. Direct Master Access of the PCI Bus

3.4.1.1 Direct Master Memory and I/O Decode

The Range register and the Local Base Address specifies the Local Address bits to use for decoding a Local-to-PCI access (Direct Master). The range of Memory or I/O space must be a power of 2 and the Range register value must be the inverse of the range value. In addition, the Local Base Address must be a multiple of the range value.

Any Local Master Address starting from the Direct Master Local Base Address (Memory or I/O) to the range value is recognized as a Direct Master access by the PCI 9054. All Direct Master cycles are then decoded as PCI Memory, I/O, or Configuration Type 0 or 1. Moreover, a Direct Master Memory or I/O cycle is remapped according to the Remap register value. The Remap Register value must be a multiple of the Direct Master Range value (not the Range register value).

The PCI 9054 can only accept Memory cycles from a Local processor. The Local Base Address and/or the range determine whether PCI Memory or PCI I/O transactions occur.

3.4.1.2 Direct Master FIFOs

For Direct Master Memory access to the PCI Bus, the PCI 9054 has a 32-Lword (128-byte) Write FIFO and a 16-Lword (64-byte) Read FIFO. The FIFOs enable the

Local Bus to operate independent of the PCI Bus and allows high-performance bursting on the PCI and Local Buses. In a Direct Master write, the Local processor (Master) writes data to the PCI Bus (Slave). In a Direct Master read, the Local processor (Master) reads data from the PCI Bus (Slave). The FIFOs that function during a Direct Master write and read are illustrated in Figure 3-2 and Figure 3-3.

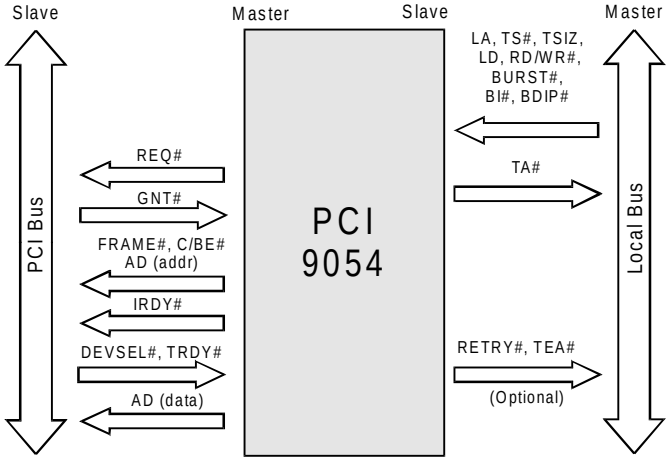


Figure 3-2. Direct Master Write

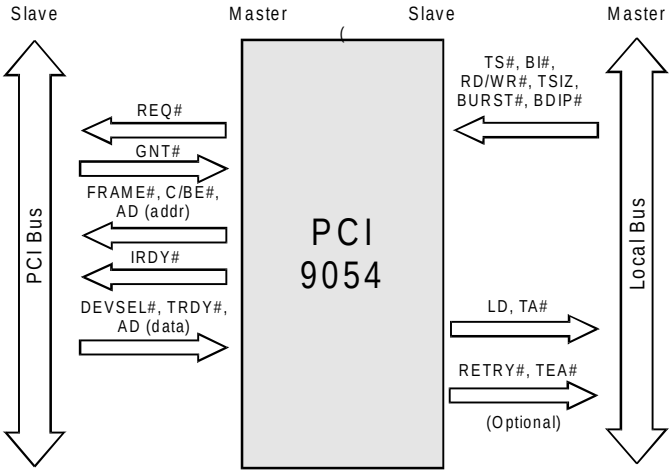


Figure 3-3. Direct Master Read

Note: *The figures represent a sequence of Bus cycles.*

3.4.1.3 Direct Master Memory Access

The MPC850 or MPC860 transfers data through a Single or Burst Read/Write Memory transaction, or through SDMA channels to the PCI 9054 and PCI Bus. The MPC850 or MPC860 IDMA/SDMA accesses to the PCI 9054 appear as Direct Master operations. Refer to Section 3.4.2 for more information.

Transactions are initiated by the MPC850 or MPC860 (a Local Bus Master) when the memory address on the Local Bus matches the Memory space decoded for Direct Master operations. Upon a Local Bus Read, the PCI 9054 becomes a PCI Bus Master, arbitrates for the PCI Bus, and reads data from the PCI Target directly into the Direct Master Read FIFO. When sufficient data is placed into the FIFO, it asserts the Transfer Acknowledge (TA#) signal onto the Local Bus to indicate that the requested data is on the Local Bus.

The Local processor can read or write to PCI memory. The PCI 9054 converts the Local Read/Write access. The Local Address space starts from Direct Master Local Base Address up to the range. Remap (PCI Base Address) defines PCI starting address.

An MPC850 or MPC860 Single cycle causes a Single-Cycle PCI transaction. An MPC850 or MPC860 Burst cycle asserts a Burst PCI Cycle transaction. Bursts are limited to 16 bytes (four Lwords) in the MPC850 or MPC860.

The PCI 9054 supports bursts beyond the 1-byte boundary (Continuous Burst) when the BDIP# input signal remains asserted beyond a 16-byte boundary by an external Local Bus Master. To finish, continuing burst and the external Master should de-assert the BDIP# signal on the last Data phase.

Writes—Upon a Local Bus Write, the Local Bus Master writes data to the Direct Master Write FIFO. When the first data is in the FIFO, the PCI 9054 becomes the PCI Bus Master, arbitrates for the PCI Bus, and writes data to the PCI Target device. The PCI 9054 continues to accept writes and returns TA# until the Write FIFO is full. It then holds off TA# until space becomes available in the Write FIFO. A programmable Direct Master "almost full" status output is provided (MDREQ#/ DMPAF/EOT#). The PCI 9054 asserts RETRY# whenever the Direct Master Write FIFO is full, implying that the Local Master can relinquish the bus and finish the Write operation at a later time (LMISC[6]).

Reads—PCI 9054 holds off TA# while gathering an Lword from the PCI Bus. Programmable Prefetch modes are available if prefetch is enabled: prefetch, 4, 8, 16, or continuous until the Direct Master cycle ends. The Read cycle is terminated when the Local BDIP# input is de-asserted. Unused Read data is flushed from the FIFO.

The PCI 9054 does not prefetch Read data for single cycle Direct Master reads (Local BURST# input is not asserted during the first Data phase). In this case, the PCI 9054 reads a single PCI Lword unless Direct Master Read Ahead mode is enabled.

For Direct Master Single-Cycle reads, the PCI 9054 sets the corresponding PCI Bus byte enables from the Local Bus address and the TSIZ[0:1] signal.

For Burst-Cycle reads, the PCI 9054 reads entire Lwords (all PCI Bus byte enables are asserted).

If the Direct Master Prefetch Limit bit is enabled (DMPBAM[11]=1), the PCI 9054 does not prefetch past a 4-kilobit boundary. Also, the Local Bus must not cross a 4-kilobit boundary during a Burst read.

The PCI 9054 never prefetches beyond the region specified for Direct Master accesses.

3.4.1.4 Direct Master I/O Configuration Access

When a Local Direct Master I/O access to the PCI Bus occurs, the PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration Enable bit (DMCFGA[31]) determines whether an I/O or Configuration access is to be made to the PCI Bus.

Local Burst accesses are broken into single PCI I/O address/Data cycles. The PCI 9054 does not prefetch Read data for I/O and configuration reads.

For Direct Master I/O or Configuration cycles, the PCI 9054 asserts the same PCI Bus byte enables as set on the Local Bus.

3.4.1.5 Direct Master I/O

If the Configuration Enable bit is cleared (DMCFGA[31]=0), a single I/O access is made to the PCI Bus. The Local Address, Remapped Decode Address Bits, and Local byte enables are encoded to provide the address and are output with an I/O read or write command during a PCI Address cycle.

When the I/O Remap Select bit is set (DMPBAM[13]=1), the PCI Address bits [31:16] are forced to 0 for the 64-kilobit I/O address limit.

For writes, data is loaded into the Write FIFO and TA# is returned to the Local Bus. For reads, the PCI 9054 holds off TA# while receiving an Lword from the PCI Bus.

3.4.1.6 RETRY# Capability

3.4.1.6.1 Direct Master Write FIFO Full

The PCI 9054 supports the Direct Master Write FIFO full condition. When enabled (LMISC[6]=1), the PCI 9054 asserts the RETRY# signal to the Local Bus Master to relinquish ownership of the bus and return to finish the initial write at a later time.

In a Direct Master Write FIFO full condition, the PCI 9054 asserts the RETRY# signal. Otherwise, the Direct Master Write transfer goes through successfully.

3.4.1.6.2 Direct Master Delayed Read

The PCI 9054 supports Deferred Direct Master Read transactions. When the M Mode Direct Master Deferred Read Enable bit is set (LMISC[4]=1), the PCI 9054 asserts RETRY# and prefetches Read data every time the Local Master requests a read. During a PCI data prefetch, the Local Master is capable of doing other transactions and free to return for requested data at a later time. When Deferred Direct Master Read mode is disabled, the Local Master must “keep” the Local Bus and wait for the requested data (TA# is not asserted until data is available to the Local Bus).

3.4.1.7 Direct Master Configuration (PCI Configuration Type 0 or Type 1 Cycles)

If the Configuration Enable bit (DMCFGA[31]) is set, a Configuration access is made to the PCI Bus. In addition to enabling configuration of this bit, the user must provide all register information. The Register Number and Device Number bits (DMCFGA[7:2] and DMCFGA[15:11], respectively) must be modified and a new Configuration Read/Write cycle must be performed before accessing other registers or devices.

If the PCI Configuration Address register selects a Type 0 command, bits [10:0] of the register are copied to address bits [10:0]. Bits [15:11] (device number) are translated into a single bit being set in the PCI Address bits [31:11]. The PCI Address bits [31:11] can be used as a device select. For a Type 1 command, bits [23:0] are copied from the register to bits [23:0] of the PCI address. The PCI Address bits [31:24] are set to 0. A configuration read or write command code is output with the address during the PCI Address cycle (refer to the DMCFGA register).

For writes, Local data is loaded into the Write FIFO and TA# is returned. For reads, the PCI 9054 holds off TA# while gathering an Lword from the PCI Bus.

3.4.1.7.1 Direct Master Configuration Cycle Example

To perform a Type 0 Configuration cycle to PCI device on AD[21]:

1. The PCI 9054 must be configured to allow Direct Master access to the PCI Bus. The PCI 9054 must also be set to respond to I/O Space accesses. These bits must be set (PCICR[2:0]=111b).

   In addition, Direct Master memory and I/O access must be enabled (DMPBAM[1:0]=11).

2. The Local Memory map selects the Direct Master range. For this example, use a range of 1 MB:

   1 MB = 2^{20} = 000FFFFFh

   The value to program into the Range register is the inverse of 000FFFFFh (FFF00000h):

   DMRR = FFF00000h

3. The Local Memory map determines the Local Base Address for the Direct Master-to-PCI I/O Configuration register. For this example, use 40000000h:

   DMLBAI = 40000000h

4. The PCI Address (Remap) for Direct Master-to-PCI Memory register must enable the Direct Master I/O access. The Direct Master I/O Access Enable bit must be set (DMPBAM[1]=1).

5. The user must know which PCI device and PCI Configuration register the PCI Configuration cycle is accessing. This example assumes the IDSEL signal of the Target PCI device is connected to AD[21] (logical device #10=0Ah). Also access PCIBAR0 (the fourth register, counting from 0; use Table 11-2 for reference). Set DMCFGA[31, 23:0] as follows:

Bit	Description	Value
1:0	Configuration Type 0.	00b
7:2	Register Number. Fourth register. Must program a "4" into this value, beginning with bit 2.	000100b
10:8	Function Number.	000b
15:11	Device Number n-11, where n is the value in AD[n]=21-11 = 10.	01010b
23:16	Bus Number.	00000000b
31	Configuration Enable.	1

   After these registers are configured, a simple Local Master Memory cycle to the I/O base address is necessary to generate a PCI Configuration Read or Write cycle. Offset to the base address is not necessary because the register offset for the read or write is specified in the Configuration register. The PCI 9054 takes the Local Bus Master Memory cycle and checks for the Configuration Enable bit (DMCFGA[31]). If set, the PCI 9054 converts the current cycle to a PCI Configuration cycle, using the DMCFGA register and the Write/Read signal (RD/WR#).

   The Register Number and Device Number bits (DMCFGA[7:2] and DMCFGA[15:11], respectively) must be modified and a new Configuration Read/Write cycle must be performed before accessing other registers or devices.

3.4.1.8 Direct Master PCI Dual Address Cycle

The PCI 9054 supports PCI Dual Address Cycle (DAC) when it is a PCI Bus Master using the DMADAC0 and DMADAC1 registers for Block DMA transactions. Scatter/Gather DMA can utilize the DAC function via the DMADAC0 and DMADAC1 registers or DMAMODE0[18] AND DMAMODE1[18]. The DAC command is used to transfer a 64-bit address to devices that support 64-bit addressing when the address is above the 4-GB Address space. The PCI 9054 performs a DAC within two PCI clock periods, where the first PCI address is a Lo-Addr, with the command (C/BE[3:0]#) "D", and the second PCI address is a Hi-Addr, with the command (C/BE[3:0]#) "6" or "7", depending upon whether it is a PCI Read or PCI Write cycle.

3.4.1.9 Direct Master/Target Abort

The PCI 9054 Direct Master/Target Abort logic enables a Local Bus Master to perform a Direct Master Bus poll of devices to determine whether devices exist (typically when the Local Bus performs Configuration cycles to the PCI Bus). When a PCI Master device attempts to access and does not receive DEVSEL# within six PCI clocks, it results in a Master Abort. The Local Bus Master must clear the Received Master Abort bit or Target Abort bit (PCISR[13 or 11]=0, respectively) and continue by processing the next task.

3.4.1.9.1 Direct Master/Target Abort

If a PCI Master, Target Abort, or Retry Time-Out is encountered during a transfer, the PCI 9054 asserts TEA# if enabled [(INTCSR[1:0]=1), which can be used as a Non-Maskable Interrupt (NMI)]. If a Local Bus Master is waiting for TA#, it is asserted along with TEA#. The interrupt handler of the Local Bus Master can take the appropriate application-specific action. It can then clear the Target Abort bit (PCISR[11]) to clear the TEA# interrupt and re-enable Direct Master transfers.

If a Local Bus Master is attempting a Burst read from a nonresponding PCI device (Master/Target Abort), it receives TA# and BI# for the first cycle only. In addition, the PCI 9054 asserts TEA# if the Enable Local Bus LSERR# bits are enabled (INTCSR[1:0], which can be used as an NMI). If the Local processor cannot terminate its Burst cycle, it may cause the Local processor to hang. The Local Bus must then be reset from the PCI Bus. If the Local Bus Master cannot terminate its cycle with TEA# output, it should not perform Burst cycles when attempting to determine whether a PCI device exists.

3.4.1.10 Direct Master Memory Write and Invalidate

The PCI 9054 can be programmed to perform Memory Write and Invalidate cycles to the PCI Bus for Direct Master transfers, as well as DMA transfers (refer to Section 3.5.4). The PCI 9054 supports Memory Write and Invalidate transfers for cache line sizes of 8 or 16 Lwords. Size is specified in the System Cache Line Size bits (PCICLSR[7:0]). If a size other than 8 or 16 is specified, the PCI 9054 performs Write transfers rather than Memory Write and Invalidate transfers.

Direct Master Memory Write and Invalidate transfers are enabled when the Invalidate Enable bit (DMPBAM[9]) and the Memory Write and Invalidate Enable bit (PCICR[4]) are set.

In Memory Write and Invalidate mode, if the start address of the Direct Master transfer is on a cache line boundary, the PCI 9054 waits until the number of Lwords required for the specified cache line size are written from the Local Bus before starting a PCI Memory Write and Invalidate access. This ensures a complete cache line write can complete in one PCI Bus ownership.

If the start address is not on a cache line boundary, the PCI 9054 starts a normal PCI Write access (PCI command code = 7h). The PCI 9054 terminates a cycle at a cache line boundary if it is performing a normal write or if it is performing a Memory Write and Invalidate cycle and another cache line of data is not available. If an entire cache line is available by the time PCI 9054 regains use of the PCI Bus, the PCI 9054 resumes Memory Write and Invalidate cycles. Otherwise, it continues with a normal write. If a Target disconnects before a cache line is completed, the PCI 9054 completes the remainder of that cache line, using normal writes.

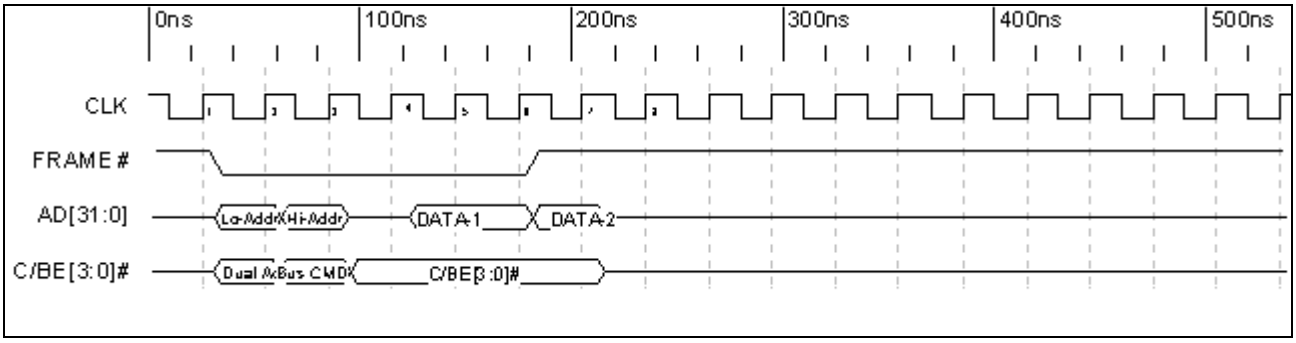


Figure 3-4. Dual Address Timing

3.4.2 IDMA/SDMA Operation

3.4.2.1 IDMA Operation

The PCI 9054 supports the MPC850 or MPC860 Independent DMA (IDMA) mode, using the MDREQ# signal and operating in Direct Master mode. In M mode, this signal is connected to the MPC850 or MPC860 DREQ[1:0] input pins. After programming the MPC850 or MPC860 IDMA channel, the PCI 9054 uses Direct Master mode to transfer data between the PCI Bus and the MPC850 or MPC860 internal dual-port RAM (or external memory). The data count is controlled by the IDMA Byte counter and throttled by the PCI 9054 MDREQ# signal. When the PCI 9054 FIFO is nearly full, MDREQ# is de-asserted to the MPC850 or MPC860, indicating that it should inhibit transferring further data (the FIFO threshold count in the PCI 9054 must be set to a value of at least five Lwords below the full capacity of the FIFO—27 Lwords) (DMPBAM[10, 8:5]). The Retry function can be used to communicate to the Local Bus Master that it should relinquish ownership of the Local Bus.

Note: *The Direct Master Write FIFO Retry Enable bit (LMISC[6]) can be disabled to prevent the assertion of the RETRY# signal.*

In IDMA reads (PCI 9054 to the Local Bus), the MDREQ# signal is always asserted (indicating data is available), although the Read FIFO is empty. Any Local Bus read of the PCI Bus causes the PCI 9054 to become a PCI Bus Master and fill the Direct Master Read FIFO buffer. When sufficient data is in the FIFO, the PCI 9054 completes the Local Bus cycle by asserting Transfer Acknowledge (TA#).

After the IDMA has transferred all required bytes (MPC850 or MPC860 Byte counter decrements to zero), the MPC850 or MPC860 generate an internal interrupt, which in turn should execute the code to disable the IDMA channel (the MDREQ# input signal may still be asserted by the PCI 9054). The SDACK[1:0] signal from the MPC850 or MPC860 is not used by the PCI 9054 (no connection).

Refer to Section 3.4.1 for more information about Direct Master Data transfers.

3.4.2.2 SDMA Operation

The PCI 9054 supports the MPC850 or MPC860 Serial DMA (SDMA) mode, using Direct Master mode. No handshake signals are required to perform the SDMA operation.

The Retry function can be used to communicate to the Local Bus Master it should relinquish ownership of the Local Bus. The Direct Master Write FIFO Retry Enable bit (LMISC[6]) can be disabled to prevent assertion of the RETRY# signal.

Note: *The Direct Master Write FIFO can be programmed to identify the full status condition (DMPBAM[10, 8:5]). The FIFO Full Status Flag is in MARBR[30].*

3.4.3 Direct Slave Operation (PCI Master-to-Local Bus Access)

The PCI 9054 supports both Burst Memory-Mapped Transfer accesses and I/O-Mapped, Single-Transfer accesses to the Local Bus from the PCI Bus through a 16-Lword (64-byte) Direct Slave Read FIFO and a 32-Lword (128-byte) Direct Slave Write FIFO. The PCI Base Address registers are provided to set up the location of the adapter in the PCI memory and the I/O space. In addition, Local mapping registers allow address translation from the PCI Address Space to the Local Address Space. Three spaces are available:

- Space 0
- Space 1
- Expansion ROM space

Expansion ROM space is intended to support a bootable ROM device for the Host.

For Single Cycle Direct Slave reads, the PCI 9054 reads a single Local Bus Lword or partial Lword. The PCI 9054 disconnects after one transfer for all Direct Slave I/O accesses.

For the highest data-transfer rate, the PCI 9054 supports posted writes and can be programmed to prefetch data during a PCI Burst read. The Prefetch size, when enabled, can be from one to 16 Lwords or until the PCI Bus stops requesting. When the PCI 9054 prefetches, if enabled, it drops the Local Bus after reaching the prefetch counter. In Continuous Prefetch mode, the PCI 9054 prefetches as long as FIFO space is available and stops prefetching when the PCI Bus terminates the request. If Read prefetching is disabled, the PCI 9054 disconnects after one Read transfer.

In addition to Prefetch mode, the PCI 9054 supports Read Ahead mode (refer to Section 3.4.3.3).

Each Local space can be programmed to operate in an 8--, 16-, or 32-bit Local Bus width. The PCI 9054 has an internal wait state generator and external wait state input, TA#. TA# can be disabled or enabled with the Internal Configuration registers.

With or without wait state(s), the Local Bus, independent of the PCI Bus, can

- Burst as long as data is available (Continuous Burst mode)
- Burst four Lwords at a time (recommended)
- Perform a Continuous Single cycle

A Burst cycle from the PCI Bus through the PCI 9054 asserts an MPC850 or MPC860 Burst transaction if the following is true:

- The address is quad-Lword aligned,
- A FIFO contains at least four Lwords, and
- All PCI Bus byte enables are set for writes only and ignored for reads

3.4.3.1 Direct Slave Lock

The PCI 9054 supports direct PCI-to-Local-Bus exclusive accesses (locked atomic operations). A PCI-locked operation to the Local Bus results in the entire address Space 0, Space 1, and Expansion ROM space being locked until they are released by the PCI Bus Master. Locked operations are enabled or disabled with the Direct Slave LOCK# Enable bit (MARBR[22]) for PCI-to-Local accesses.

3.4.3.2 Direct Slave PCI v2.1 Delayed Read Mode

The PCI 9054 can be programmed through the PCI Specification v2.1 Mode bit (MARBR[24]=1) to perform delayed reads, as specified in PCI Specification v2.1.

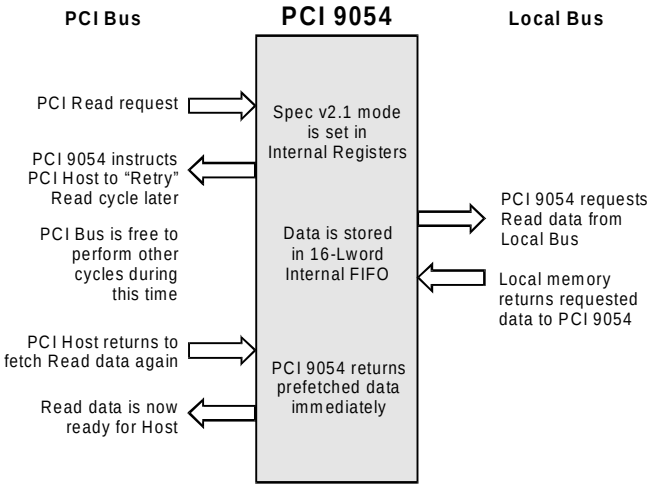


Figure 3-5. Direct Slave PCI v2.1 Delayed Reads

Note: *The figure represents a sequence of Bus cycles.*

In addition to delayed reads, the PCI 9054 supports the following PCI Specification v2.1 functions:

- No write while a read is pending (PCI Retry for reads)
- Write and flush pending read

3.4.3.3 Direct Slave PCI Read Ahead Mode

The PCI 9054 also supports Read Ahead mode, where prefetched data can be read from the internal FIFO of the PCI 9054 instead of from the Local Bus. The address must be subsequent to the previous address and 32-bit aligned (next address = current address + 4). Read Ahead mode functions with or without PCI Delayed Read mode.

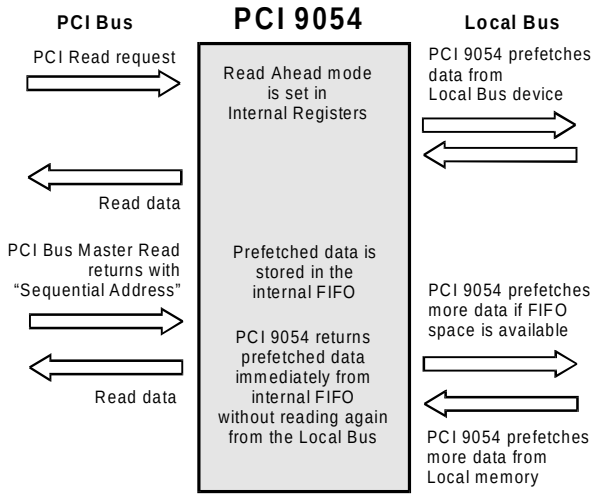


Figure 3-6. Direct Slave PCI 9054 Read Ahead Mode

Note: *The figure represents a sequence of Bus cycles.*

3.4.3.4 Direct Slave Transfer

Transactions are initiated by a PCI Bus Master addressing the Memory space decoded for the Local Bus. Upon a PCI Read/Write, the PCI 9054 becomes a Local Bus Master and arbitrates for the Local Bus.

The PCI 9054 then reads data into the Direct Slave Read FIFO or writes data to the Local Bus.

The Direct Slave or Direct Master pre-empts DMA; however, the Direct Slave does not pre-empt the Direct Master (refer to Section 3.4.4.1).

The PCI 9054 can be programmed to "keep" the PCI Bus by generating a wait state(s) and de-asserting TRDY# if the Write FIFO becomes full. The PCI 9054

can also be programmed to "keep" the Local Bus and continue asserting BB# if the Direct Slave Write FIFO becomes empty or the Direct Slave Read FIFO becomes full. In either case, the Local Bus is dropped when the Local Bus Latency Timer is enabled and expires (MARBR[7:0]).

For Direct Slave writes, the PCI Bus writes data to the Local Bus. Direct Slave is the "Command from the PCI Host," which has the highest priority.

For Direct Slave reads, the PCI Bus Master reads data from the Local Bus Slave.

The PCI 9054 supports on-the-fly Endian conversion for Space 0, Space 1, and Expansion ROM space. The Local Bus can be Big/Little Endian (Address/Data Invariance) by using the programmable internal register configuration.

Note: *The PCI Bus is always Little Endian.*

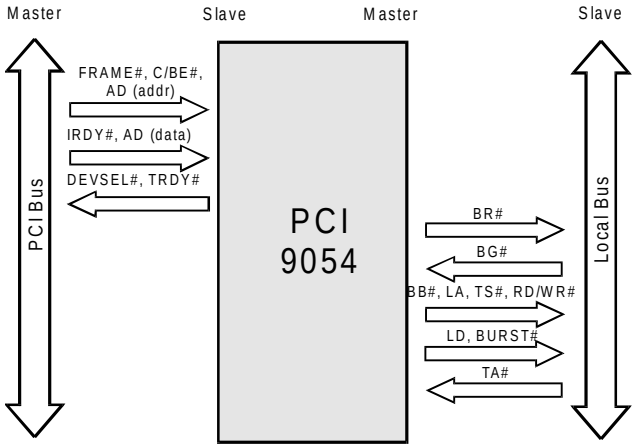


Figure 3-7. Direct Slave Write

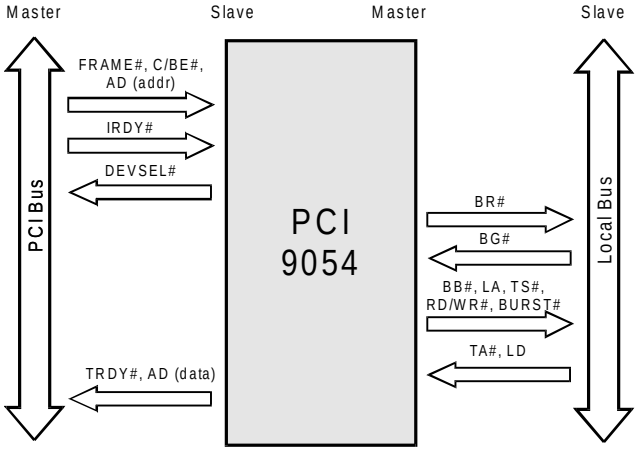


Figure 3-8. Direct Slave Read

Note: *The figures represent a sequence of Bus cycles.*

During Direct Slave transactions, the MPC850 or MPC860 user has the option to use the PCI 9054 for maximum Burst transfers, using the BTERM# Input Enable bit(s) (LBRD0[23,7], LBRD1[7], and DMAMODE0[7]).

In Direct Slave transfers, each Direct Slave space (Space 0, Space 1, and Expansion ROM) has its own BTERM# Input Enable bit (the BTERM# input signal becomes the BI# signal in M mode). Space 0 is in LBRD0[7], Space 1 is in LBRD1[7], and Expansion ROM is in LBRD0[23].

When the Bterm Mode bit is enabled, the PCI 9054 continues to burst on the Local Bus until the BI# signal is asserted for one CLK cycle any time after the next Data phase, implying a new Address cycle (TS#) is needed if there is more data to transfer.

When the Bterm Mode bit is enabled and the BI# signal is asserted, the PCI 9054 asserts TS# every 16 bytes or until BI# is de-asserted (whichever occurs first).

If the Bterm Mode bit is disabled and the BI# signal is asserted on the first Data phase, Single-Cycle transfers are performed.

Table 3-2. Direct Slave Burst Mode Cycle Detection

Burst Enable Bit	BTERM# Input Enable Bit	BI# Signal	Result
1	0	Not asserted	Burst 16 bytes (MPC850 or MPC860 compatible)
1	0	Asserted during first Data phase	Single cycle
1	1	Asserted	Burst until BI# is asserted for one CLK cycle
0	X	X	Single cycle

Caution: *The MPC850 and MPC860 do not support bursting more than 16 bytes. The BTERM# Input Enable bits should be set only for Local Bus Masters that support continuous bursting.*

Note: *"X" is "Don't Care."*

The PCI 9054 supports Local Bus error conditions using TEA#. TEA# may be asserted by a device on the Local Bus, either before or simultaneously with TA#. In either case, the PCI 9054 tries to complete the current transaction by transferring data and then asserting TS# for every address that follows, waiting for another TA# or TEA# to be issued (used to flush Direct Slave FIFOs). After acknowledging TEA# is asserted, the PCI 9054 asserts PCI SERR# and sets an error flag, using the Signaled System Error bit (PCISR[14]=1). When set, this

indicates a catastrophic error occurred on the Local Bus. SERR# may be masked off by resetting the TEA# Input Interrupt Mask bit (LMISC[5]=0).

The PCI 9054 Local Bus Latency Timer (MARBR[7:0]) can be used to better utilize the Local Bus.

3.4.3.5 Direct Slave PCI-to-Local Address Mapping

Note: *Not applicable in I_2O mode.*

Three Local Address spaces—Space 0, Space 1, and Expansion ROM—are accessible from the PCI Bus. Each is defined by a set of three registers:

- Local Address Range (LAS0RR, LAS1RR, and/or EROMRR)
- Local Base Address (LAS0BA, LAS1BA, and/or EROMBA)
- PCI Base Address (PCIBAR2, PCIBAR3, and/or PCIERBAR)

A fourth register, the Bus Region Descriptor register for PCI-to-Local Accesses (LBRD0 and/or LBRD1), defines the Local Bus characteristics for the Direct Slave regions (refer to Figure 3-9).

Each PCI-to-Local Address space is defined as part of reset initialization, as described in Section 3.4.3.5.1. These Local Bus characteristics can be modified at any time before actual data transactions.

3.4.3.5.1 Direct Slave Local Bus Initialization

Range—Specifies which PCI Address bits to use for decoding a PCI access to Local Bus space. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits that must be included in decode and 0 to all others.

Remap PCI-to-Local Addresses into a Local Address Space—Bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor—Specifies the Local Bus characteristics.

3.4.3.5.2 Direct Slave PCI Initialization

After a PCI reset, the software determines how much address space is required by writing all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9054 returns zeroes (0) in the Don't Care Address bits, effectively specifying the address space required. The PCI software then maps the Local Address space into the PCI Address space by programming the PCI Base Address register. (Refer to Figure 3-9.)

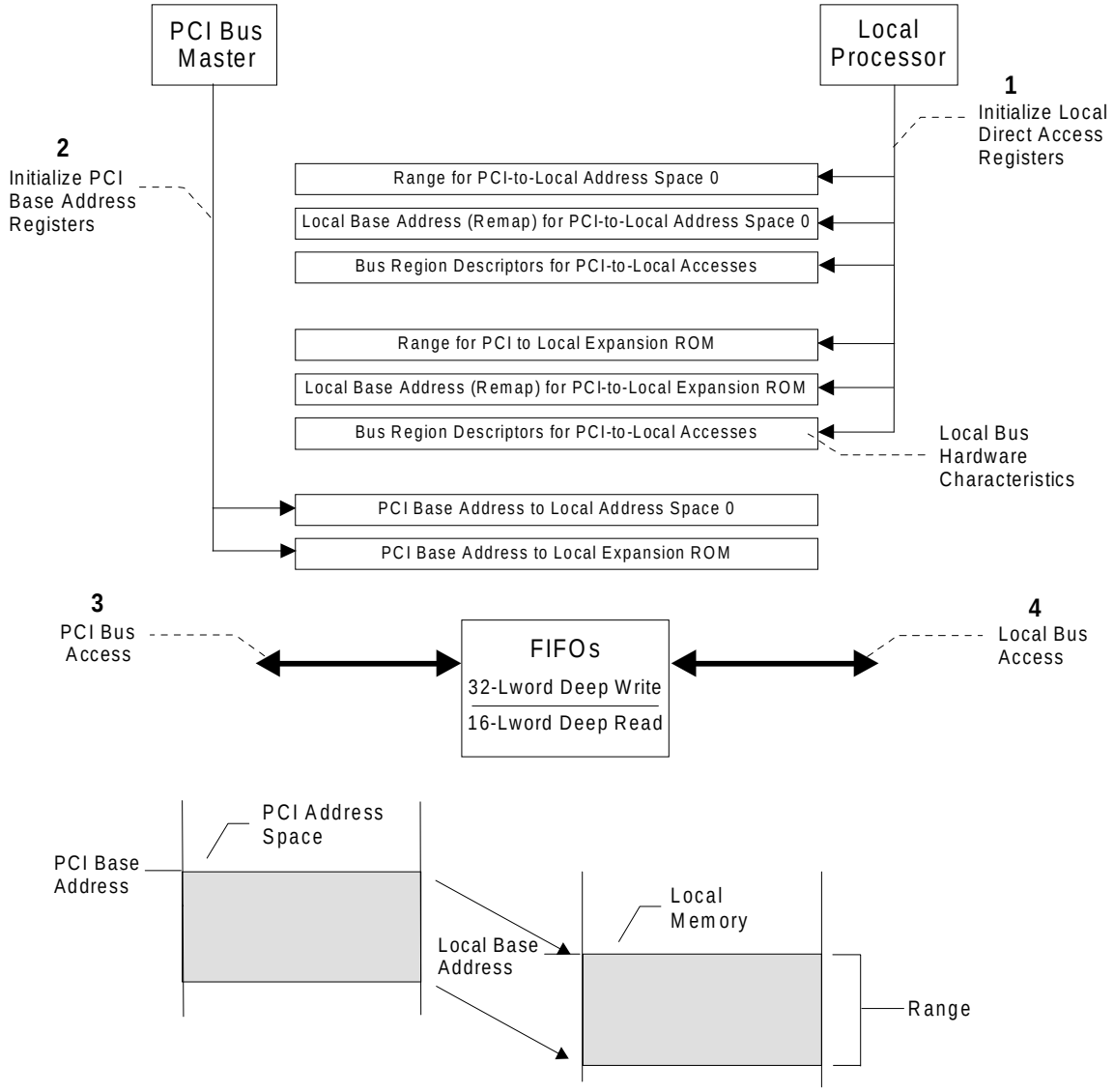


Figure 3-9. Direct Slave Access of the Local Bus

3.4.3.5.3 Direct Slave Transfer Size

The TSIZ[0:1] pins correspond to the data-transfer size on the Local Bus.

Table 3-3. Data Bus TSIZ[0:1] Contents for Write Cycles

Transfer Size	TSIZ		Address		External Data Bus Pattern For 32-, 16-, and 8-Bit Port Sizes			
			LA30	LA31	LD[0:7]	LD[8:15]	LD[16:23]	LD[24:31]
Byte	0	1	0	0	OP0	—	—	—
	0	1	0	1	OP1	OP1	—	—
	0	1	1	0	OP2	—	OP2	—
	0	1	1	1	OP3	OP3	—	OP3
Word	1	0	0	0	OP0	OP1	—	—
	1	0	1	0	OP2	OP3	OP2	OP3
Lword	0	0	0	0	OP0	OP1	OP2	OP3

Table 3-4. Data Bus TSIZ[0:1] Requirements for Read Cycles

Transfer Size	TSIZ		Address		32-Bit Port Size				16-Bit Port Size		8-Bit Port Size
			LA30	LA31	LD[0:7]	LD[8:15]	LD[16:23]	LD[24:31]	LD[0:7]	LD[8:15]	LD[0:7]
Byte	0	1	0	0	OP0	—	—	—	OP0	—	OP0
	0	1	0	1	—	OP1	—	—	—	OP1	OP1
	0	1	1	0	—	—	OP2	—	OP2	—	OP2
	0	1	1	1	—	—	—	OP3	—	OP3	OP3
Word	1	0	0	0	OP0	OP1	—	—	OP0	OP1	OP0
	1	0	1	0	—	—	OP2	OP3	OP2	OP3	OP2
Lword	0	0	0	0	OP0	OP1	OP2	OP3	OP0	OP1	OP0

3.4.3.5.3.1 Direct Slave Example

A 1 MB Local Address Space, 12300000h through 123FFFFFh, is accessible from the PCI Bus at PCI addresses 78900000h through 789FFFFFh.

a. Local initialization software sets the Range and Local Base Address registers as follows:

- **Range**—FFF00000h (1 MB, decode the upper 12 PCI Address bits)
- **Local Base Address (remap)**—123XXXXXh, (Local Base Address for PCI-to-Local accesses) [Space Enable bit(s) must be set to be recognized by the PCI Host (LAS0BA[0]=1, LAS1BA[0]=1)]

b. PCI Initialization software writes all ones to the PCI Base Address, then reads it back again.

- The PCI 9054 returns a value of FFF00000h. The PCI software then writes to the PCI Base Address register(s).
- **PCI Base Address**—789XXXXXh (PCI Base Address for Access to the Local Address Space registers, PCIBAR2 and PCIBAR3).

For a PCI Direct access to the Local Bus, the PCI 9054 has a 32-Lword (128-byte) Write FIFO and a 16-Lword (64-byte) Read FIFO. The FIFOs enable the Local Bus to operate independent of the PCI Bus. The PCI 9054 can be programmed to return a Retry response or to throttle TRDY# for any PCI Bus transaction attempting to write to the PCI 9054 Local Bus when the FIFO is full.

For PCI Read transactions from the Local Bus, the PCI 9054 holds off TRDY# while gathering data from the Local Bus. For Read accesses mapped to PCI Memory space, the PCI 9054 prefetches up to 16 Lwords (has Continuous Prefetch mode) from the Local Bus. Unused Read data is flushed from the FIFO. For Read accesses mapped to PCI I/O space, the PCI 9054 does not prefetch Read data. Rather, it breaks each read of a Burst cycle into a Single Address/Data cycle on the Local Bus.

The PCI Target Retry Delay Clocks bits (LBRD0[31:28]) can be used to program the period of time in which the PCI 9054 holds off TRDY#. The PCI 9054 issues a Retry to the PCI Bus Transaction Master when the programmed time period expires. This occurs when the PCI 9054 cannot gain control of the Local Bus and return TRDY# within the programmed time period.

3.4.3.6 Direct Slave Priority

Direct Slave accesses have a higher priority than DMA accesses, thereby preempting DMA transfers. During a DMA transfer, if the PCI 9054 detects a pending Direct Slave access, it releases the Local Bus within two Data transfers. The PCI 9054 resumes operation after the Direct Slave access completes.

When the PCI 9054 DMA controller owns the Local Bus, its BR# output and BG# input are asserted. When a Direct Slave access occurs, the PCI 9054 releases the Local Bus within two Lword transfers by de-asserting BB# and floating the Local Bus outputs. After the PCI 9054 acknowledges that BG# is de-asserted, it requests the Local Bus for a Direct Slave transfer by asserting BR#. When the PCI 9054 receives BG#, it drives the bus and performs the Direct Slave transfer. Upon completing a Direct Slave transfer, the PCI 9054 releases the Local Bus by de-asserting BB# and floating the Local Bus outputs. After the PCI 9054 acknowledges that BG# is de-asserted and the Local Bus Pause Timer is set to zero, it requests a DMA transfer from the Local Bus by re-asserting BR#. When it receives BG#, it drives the bus and continues the DMA transfer.

3.4.4 Deadlock Conditions

Deadlock can occur when a PCI Bus Master must access the PCI 9054 Local Bus at the same time a Master on the PCI 9054 Local Bus must access the PCI Bus.

There are two types of deadlock:

- **Partial Deadlock**—A Local Bus Master is performing a Direct Bus Master access to a PCI Bus device other than the PCI Bus device concurrently trying to access the Local Bus
- **Full Deadlock**—A Local Bus Master is performing a Direct Bus Master access to the same PCI Bus device concurrently trying to access the Local Bus

This applies only to Direct Master and Direct Slave accesses through the PCI 9054. Deadlock does not occur in transfers through the PCI 9054 DMA channels or the PCI 9054 internal registers (such as mailboxes).

For partial deadlock, the PCI access to the Local Bus times out (the PCI Target Retry Delay Clock (LBRD0[31:28]), which is programmable through the Local Bus Region Descriptor register) and the PCI 9054 responds with a PCI Retry. The PCI Specification requires that a PCI Master release its request for the PCI Bus (de-assert REQ#) for a minimum of two PCI clocks after receiving a Retry. This allows the PCI Bus arbiter to grant the PCI Bus to the PCI 9054 so that it can complete its Direct Master access and free up the

Local Bus. Possible solutions are described in the following sections for cases in which the PCI Bus arbiter does not function as described (PCI Bus architecture dependent), waiting for a time out is undesirable, or a full deadlock condition exists.

For full deadlock, the only solution is to back off the Local Bus Master.

3.4.4.1 Backoff

The PCI 9054 Local RETRY# signal indicates whether a possible deadlock condition exists. The PCI 9054 starts the Backoff timer (programmable through registers) when it detects one of the following conditions:

- A PCI Bus Master is attempting to access memory or an I/O device on the Local Bus and is not gaining access (*for example*, BG# is not received).
- A Local Bus Master is performing a Direct Bus Master Read access to the PCI Bus. Or, a Local Bus Master is performing a Direct Bus Master Write access to the PCI Bus and the PCI 9054 Direct Master Write FIFO cannot accept another Write cycle.

If the Local Bus Backoff Enable bit is enabled (EROMBA[4]=1) and expires and the PCI 9054 has not received BG#, the PCI 9054 asserts RETRY#. External bus logic can use this signal to perform backoff.

The Backoff cycle is device/bus architecture dependent. The external logic (arbiter) can assert the necessary signals to cause the Local Bus Master to release the Local Bus (backoff). After the Local Bus Master backs off, it can grant the bus to the PCI 9054 by asserting BG#.

Once RETRY# is asserted, TA# for current Data cycle is never asserted (the Local Bus Master must perform a backoff). When the PCI 9054 detects BG#, it proceeds with the PCI Master-to-Local-Bus access. When this access completes and the PCI 9054 releases the Local Bus, external logic can then release the backoff and the Local Bus Master can resume the cycle interrupted by the Backoff cycle. The PCI 9054 Write FIFO retains all data acknowledged (*that is*, last data for which TA# was asserted).

After the backoff condition ends, the Local Bus Master restarts the last cycle with TS#. For writes, data following TS# should be the data the PCI 9054 did not acknowledge prior to the Backoff cycle (*for example*, the last data for which TA# is not asserted).

All PCI Read cycles completed before the Local Bus was backed off remain in the Direct Master Read FIFO. Therefore, if the Local Bus Master returns with the same last cycle, the cycle is acknowledged with the data currently in the FIFO (the FIFO data is not read twice). A new PCI read is performed if the resumed Local Bus cycle is not the same as the Backed Off cycle.

3.4.4.1.1 Software/Hardware Solution for Systems without Backoff Capability

For adapters that do not support backoff, a possible deadlock solution is as follows.

PCI Host software, external Local Bus hardware, general purpose output USERo and general purpose input USERi can be used by the PCI Host software to prevent deadlock. USERo can be asserted to request that the external arbiter not grant the bus to any Local Bus Master except the PCI 9054. Status output from the Local arbiter can be connected to the general purpose input USERi to indicate that no Local Bus Master owns the Local Bus, or the PCI Host to determine that no Local Bus Master that currently owns the Local Bus can read input. The PCI Host can then perform Direct Slave access. When the Host finishes, it de-asserts USERo.

3.4.4.1.2 Preempt Solution

For devices that support preempt, USERo can be used to preempt the current Local Bus Master device. When USERo is asserted, the current Local Bus Master device completes its current cycle and releases the Local Bus, de-asserting BB#.

3.4.4.2 Software Solutions to Deadlock

Both PCI Host and Local Bus software can use a combination of mailbox registers, doorbell registers, interrupts, direct Local-to-PCI accesses and direct PCI-to-Local accesses to avoid deadlock.

3.5 M Mode DMA Operation

The PCI 9054 supports two independent DMA channels capable of transferring data from the:

- Local-to-PCI Bus
- PCI-to-Local Bus

Each channel consists of a DMA and a dedicated, bidirectional FIFO. Both channels support Block transfers, and Scatter/Gather transfers, with or without End of Transfer (EOT#). Only DMA Channel 0 supports Demand mode DMA transfers. Master mode must be enabled with the Master Enable bit (PCICR[2]) before the PCI 9054 can become a PCI Bus Master. In addition, both DMA channels can be programmed to

- Operate in 8-, 16-, or 32-bit Local Bus width
- Use zero to 15 internal wait states (Local Bus)
- Enable/disable internal wait states (Local Bus)
- Enable/disable Local Bus Burst capability
- Limit Local Bus bursts to four (BTERM# enable/disable)
- Hold Local address constant (Local Target is FIFO) or increment
- Perform PCI Memory Write and Invalidate (command code = Fh) or normal PCI Memory Write (command code = 7h)
- Pause Local transfer with/without BLAST# (DMA Fast/Slow termination)
- Assert PCI interrupt (INTA#) or Local interrupt (LINT#) when DMA transfer is complete or Terminal Count is reached during Scatter/Gather DMA mode transfers
- Operate in DMA Clear Count mode (only if the descriptor is in Local memory)

The PCI 9054 also supports PCI Dual Address with the upper 32-bit registers (DMADAC0 and DMADAC1).

The Local Bus Latency Timer determines the number of Local clocks the PCI 9054 can burst data before relinquishing the Local Bus. The Local Pause Timer sets how soon the DMA channel can request the Local Bus.

3.5.1 DMA PCI Dual Address Cycle

The PCI 9054 supports PCI Dual Address Cycle (DAC) when it is a PCI Bus Master using the DMDAC register for Direct Master transactions. The DAC command is used to transfer a 64-bit address to devices that support 64-bit addressing when the address is not in the low 4-GB Address space. The PCI 9054 performs a DAC within two PCI clock periods, where the first PCI address is a Lo-Addr with the command (C/BE[3:0]#) “D” and the second PCI address will be a Hi-Addr with the command (C/BE[3:0]#) “6” or “7”, depending upon it being a PCI Read or a PCI Write cycle. Whenever the DMDAC register contains a value of 0x00000000, the PCI 9054 performs a Single Address Cycle (SAC) on the PCI Bus. (Refer to Figure 3-10.)

3.5.2 Block DMA Mode

The Host processor or the Local processor sets the Local and PCI starting addresses, transfer byte count, and transfer direction. The Host or Local processor then sets the DMA Start bit to initiate a transfer. The PCI 9054 arbitrates the PCI and Local Buses and transfers data. Once the transfer completes, the PCI 9054 sets the Channel Done bit(s) (DMACSR0[4]=1 and/or DMACSR1[4]=1) and, if enabled, asserts an interrupt(s) (DMAMODE0[10] and/or DMAMODE1[10]) to the Local processor or the PCI Host (programmable). The Channel Done bit(s) can be polled, instead of interrupt generation, to indicate the DMA transfer status.

DMA registers are accessible from the PCI and Local Buses (refer to Figure 3-10).

During DMA transfers, the PCI 9054 is a Master on both the PCI and Local Buses. For simultaneous access, Direct Slave or Direct Master has a higher priority than DMA.

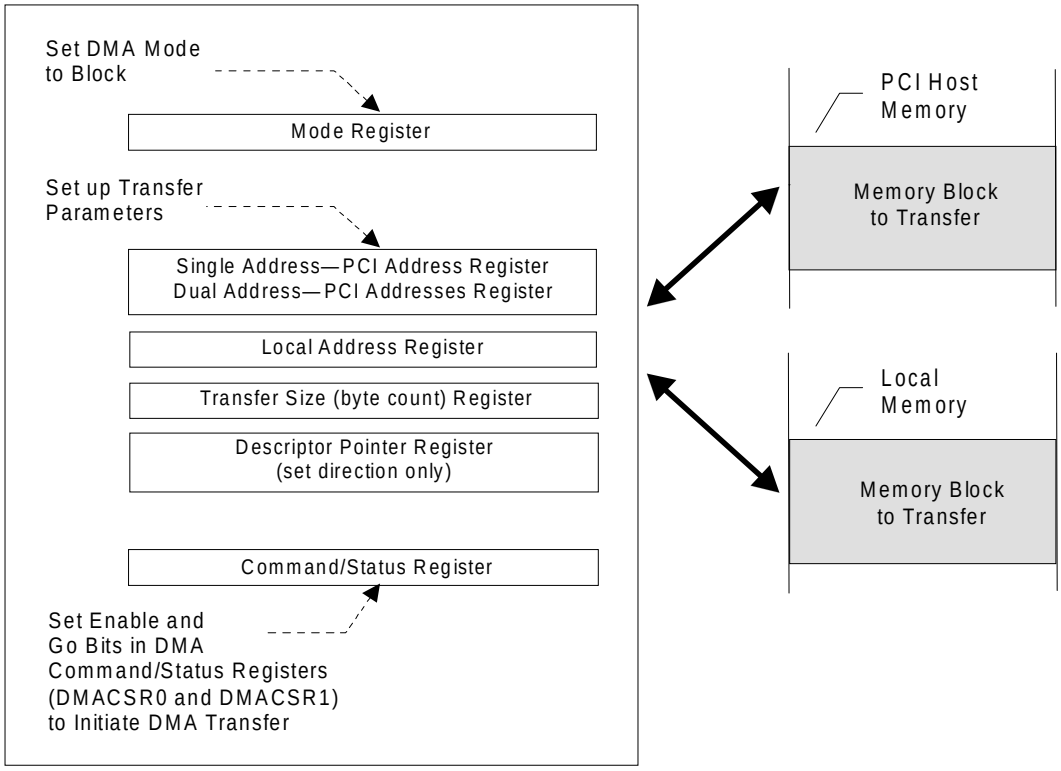


Figure 3-10. Block DMA Mode Initialization (Single Address or Dual Address PCI)

The PCI 9054 releases the PCI Bus if one of the following conditions occur (refer to Figure 3-11 and Figure 3-12):

- FIFO is full (PCI-to-Local Bus)
- FIFO is empty (Local-to-PCI Bus)
- Terminal count is reached
- PCI Bus Latency Timer expires (PCILTR[7:0])—normally programmed by the Host PCI BIOS—and PCI GNT# de-asserts
- PCI Host asserts STOP#

The PCI 9054 releases the Local Bus if one of the following conditions occurs:

- FIFO is empty (PCI-to-Local Bus)
- FIFO is full (Local-to-PCI Bus)
- Terminal count is reached
- Local Bus Latency Timer is enabled and expires (MARBR[7:0])
- Special cycle BI# input is asserted
- Direct Slave request is pending

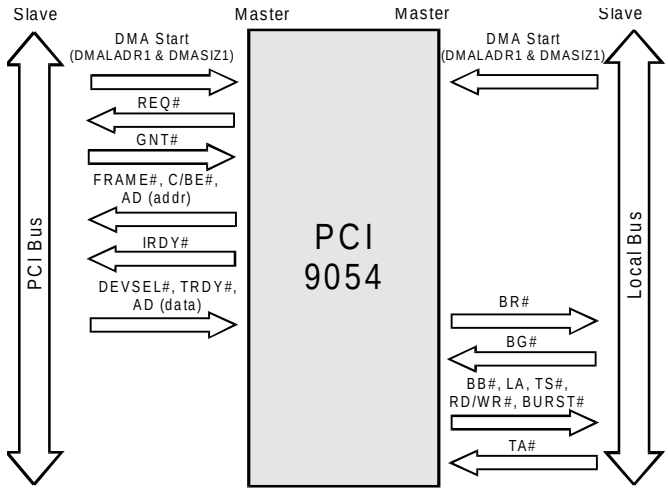


Figure 3-11. DMA, PCI-to-Local Bus

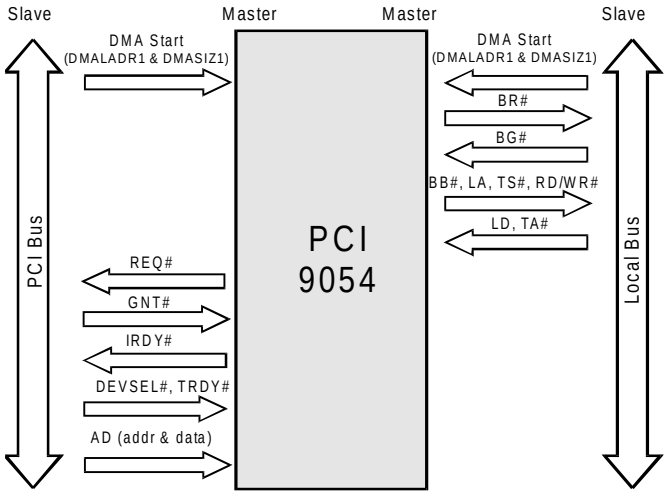


Figure 3-12. DMA, Local-to-PCI Bus

Note: *The figures represent a sequence of Bus cycles.*

During DMA transactions, users have the option of using the Burst Forever BTERM# Input Enable bit(s) (DMAMODE0[7] and/or DMAMODE1[7]) if the External Memory Controller is provided. Used in conjunction with the Fast/Slow Terminate Mode Select bit(s) (DMAMODE0[15] and/or DMAMODE1[15]).

Table 3-5. DMA

BTERM# Input Enable Bit(s)	Fast/Slow Terminate Mode Select Bit(s)	PCI 9054 BDIP# Output
Enabled (1)	Disabled (1)	BDIP# is not asserted. Burst forever or until BI# asserts for one CLK cycle.
Enabled (1)	Enabled (0)	
Disabled (0)	Disabled (1)	BDIP# is not asserted. Burst forever.
Disabled (0)	Enabled (0)	BDIP# is asserted by the PCI 9054. Burst up to 16 bytes
		(MPC850 or MPC860 compatible).

Table 3-6. Normal DMA with EOT Function

BTERM# Enable Bit(s)	Fast/Slow Terminate Mode Select Bit(s)	PCI 9054 BDIP# Output
Enabled (1)	Disabled (1)	BDIP# is not asserted. Immediate transfer terminated by EOT#.
Enabled (1)	Enabled (0)	
Disabled (0)	Disabled (1)	
Disabled (0)	Enabled (0)	BDIP# is asserted by the PCI 9054. Transfers up to the nearest 16-byte boundary, then terminates (MPC850 or MPC860 compatible).

Note: *If the Burst Enable bit is set to 0, the PCI 9054 performs Single-Cycle transfers on the Local Bus.*

3.5.2.1 Block DMA PCI Dual Address Cycle

The PCI 9054 supports the DAC feature in Block DMA mode. Whenever the DMADAC0 or DMADAC1 registers contain a value of 0x00000000, the PCI 9054 performs a Single Address Cycle (SAC) on the PCI Bus. Any other value causes a Dual Address to appear on the PCI Bus. (Refer to Figure 3-13.)

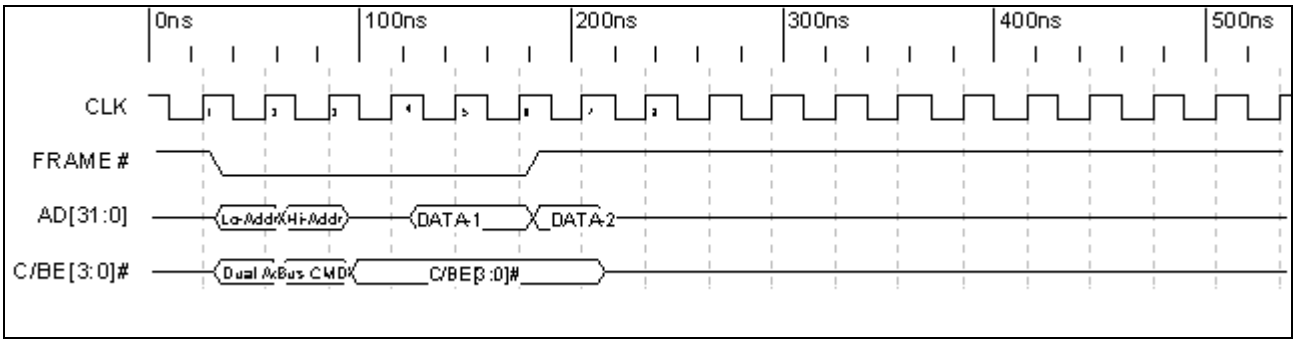


Figure 3-13. Dual Address Timing

3.5.3 Scatter/Gather DMA Mode

In Scatter/Gather DMA mode, the Host processor or Local processor sets up descriptor blocks in Local or Host memory composed of PCI and Local addresses, transfer count, transfer direction, and address of next descriptor block (refer to Figure 3-14 and Figure 3-15). The Host or Local processor then

- Enables the Scatter/Gather mode bit(s) (DMAMODE0[9]=1 and/or DMAMODE1[9]=1)
- Sets up the address of initial descriptor block in the PCI 9054 Descriptor Pointer register(s) (DMADPR0 and/or DMADPR1)
- Initiates the transfer by setting a control bit(s) (DMACSR0[1:0] and/or DMACSR1[1:0])

The PCI 9054 loads the first descriptor block and initiates the Data transfer. The PCI 9054 continues to load descriptor blocks and transfer data until it detects the End of Chain bit(s) (DMADPR0[1] and/or DMADPR1[1]) is set (these bits are part of each descriptor). When the End of Chain bit(s) is detected, the PCI 9054 completes the current descriptor block and sets the DMA Done bit(s) (DMACSR0[4] and/or DMACSR1[4]). If the End of Chain bit(s) are detected, the PCI 9054 asserts a PCI interrupt (INTA#) and/or Local interrupt (LINT#).

The PCI 9054 can also be programmed to assert PCI or Local interrupts after each descriptor is loaded, then finish transferring.

If Scatter/Gather descriptors are in Local memory, the DMA controller can be programmed to clear the transfer size at completion of each DMA, using the DMA Clear Count Mode bit(s) (DMAMODE0[16] and/or DMAMODE1[16]).

Notes: *In Scatter/Gather DMA mode, the descriptor includes the PCI and Local Address Space, transfer size, and next descriptor pointer. It also includes a DAC value if DMADPR0[18] and/or DMAMODE1[I8] is enabled. Otherwise, the register value is used. The Descriptor Pointer register(s) (DMADPR0 and/or DMADPR1) contains end of chain (bit 1), direction of transfer (bit 3), next descriptor address (bits [31:4]), interrupt after terminal count (bit 2), and next descriptor location (bit 0) bits.*

The Local Bus width must be the same as Local memory bus width.

A DMA descriptor can be on the Local memory or the PCI memory, or both (for example, one descriptor on Local memory, another descriptor on PCI memory and vice-versa).

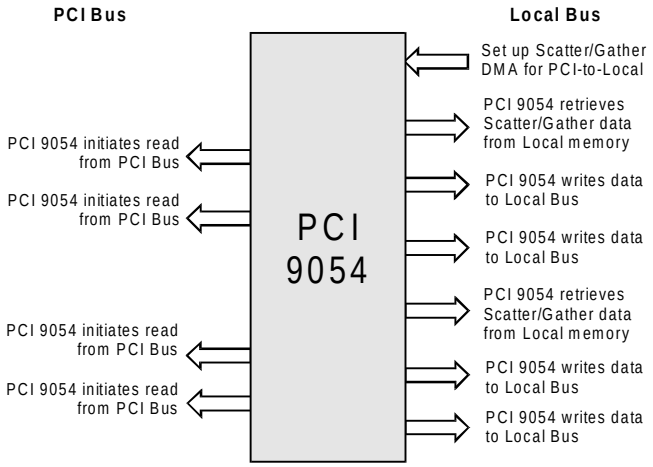


Figure 3-14. Scatter/Gather DMA Mode from PCI-to-Local Bus (Control Access from the Local Bus)

Note: *The figure represents a sequence of Bus cycles.*

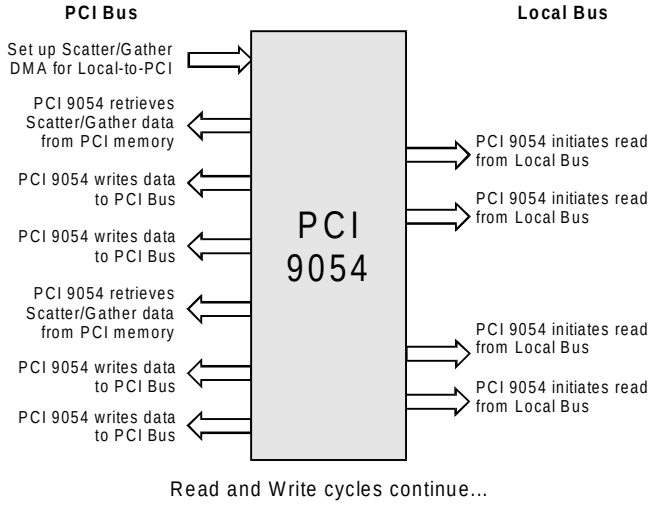


Figure 3-15. Scatter/Gather DMA Mode from Local-to-PCI Bus (Control Access from the PCI Bus)

Note: *The figure represents a sequence of Bus cycles.*

3.5.3.1 Scatter/Gather DMA PCI Dual Address Cycle

The PCI 9054 supports the DAC feature in Scatter/Gather DMA mode for Data transfers only. The descriptor blocks should reside below the 4-GB Address space. The PCI 9054 offers three different options of how PCI DAC Scatter/Gather DMA is utilized. Assuming the descriptor blocks are located on the PCI Bus:

- DMADAC0 and/or DMADAC1 contain(s) a non-zero value. DMAMODE0[18] and/or DMAMODE1[18] is set to 0. The PCI 9054 performs a Single Address Cycle (SAC) four-Lword descriptor block load from PCI memory and DMA transfer with DAC on the PCI Bus. (Refer to Figure 3-16.)
- DMADAC0 and/or DMADAC1 contain(s) an 0x00000000 value. DMAMODE0[18] and/or DMAMODE1[18] is set to 1. The PCI 9054 performs a SAC five-Lword descriptor block load from PCI memory and DMA transfer with DAC on the PCI Bus. (Refer to Figure 3-17.)
- DMADAC0 and/or DMADAC1 contain(s) a non-zero value. DMAMODE0[18] and/or DMAMODE1[18] is set to 1. The PCI 9054 performs a SAC five-Lword descriptor block load from PCI memory and DMA transfer with DAC on the PCI Bus. The fifth descriptor overwrites the value of the DMADAC0 and/or DMADAC1 register. (Refer to Figure 3-17.)

3.5.3.2 DMA Clear Count Mode

The PCI 9054 supports DMA Clear Count mode (Write-Back feature, DMAMODE0[16] and DMAMODE1[16]). This feature allows users to control the data transfer blocks during Scatter/Gather DMA operations. The PCI 9054 clears the Transfer Size descriptor to zero by writing to a descriptor-memory location at the end of each transfer chain. This feature works only if DMA descriptors are on the Local Bus.

3.5.4 DMA Memory Write and Invalidate

The PCI 9054 can be programmed to perform Memory Write and Invalidate cycles to the PCI Bus for DMA transfers, as well as Direct Master transfers (refer to Section 3.4.1.10). The PCI 9054 supports Memory Write and Invalidate transfers for cache line sizes of 8 or 16 Lwords. Size is specified in the System Cache Line Size bits (PCICLSR[7:0]). If a size other than 8 or 16 is specified, the PCI 9054 performs Write transfers rather than Memory Write and Invalidate transfers.

DMA Memory Write and Invalidate transfers are enabled when the DMA controller Memory Write and Invalidate Enable bit(s) (DMAMODE0[13] and/or DMAMODE1[13]) and the Memory Write and Invalidate Enable bit (PCICR[4]) are set.

In Memory Write and Invalidate mode, the PCI 9054 waits until the number of Lwords required for specified cache line size are read from the Local Bus before starting the PCI access. This ensures a complete cache line write can complete in one PCI Bus ownership. If a Target disconnects before a cache line completes, the PCI 9054 completes the remainder of that cache line, using normal writes before resuming Memory Write and Invalidate transfers. If a Memory Write and Invalidate cycle is in progress, the PCI 9054 continues to burst if another cache line is read from the Local Bus before the cycle completes. Otherwise, the PCI 9054 terminates the burst and waits for the next cache line to be read from the Local Bus. If the final transfer is not a complete cache line, the PCI 9054 completes the DMA transfer, using normal writes.

3.5.4.1 DMA Abort

DMA transfers can be aborted, in addition to the EOT# signal, as follows:

1. Set the Channel Enable bit(s) (DMACSR0[0]=1 and/or DMACSR1[0]=1).
2. Set the Channel Start bit(s) (DMACSR0[1]=1 and/or DMACSR1[1]=1).
3. Clear the DMA Channel Enable bit(s) (DMACSR0[0]=0 and/or DMACSR1[0]=0).
4. Abort DMA by setting the Channel Abort bit(s) (DMACSR0[2]=1 and/or DMACSR1[2]=1).
5. Wait until the Channel Done bit(s) is set (DMACSR0[4]=1 and/or DMACSR1[4]=1).

Note: *One to two Data transfers occur after the Abort bit is set. Aborting when no DMA cycles are in progress causes the next DMA to abort.*

3.5.5 DMA Priority

The DMA Channel Priority bit (MARBR[20:19]) can be used to specify the following priorities:

- Rotating (MARBR[20:19]=00)
- DMA Channel 0 (MARBR[20:19]=01)
- DMA Channel 1 (MARBR[20:19]=10)

3.5.6 DMA Channel 0/1 Interrupts

A DMA channel can assert a PCI Bus or Local Bus interrupt when done (transfer complete) or after a transfer is complete for the current descriptor in Scatter/Gather DMA mode. The DMA Channel Interrupt Select bit(s) determine whether to assert a PCI (DMAMODE0[17]=1 and/or DMAMODE1[17]=1) or Local (DMAMODE0[17]=0 and/or DMAMODE1[17]=0) interrupt. The Local or PCI processor can read the DMA Channel 0 Interrupt Active bits to determine whether a DMA Channel 0 (INTCSR[21]) or DMA Channel 1 (INTCSR[22]) interrupt is pending.

The Channel Done bit(s) (DMACSR0[4] and/or DMACSR1[4]) can be used to determine whether an interrupt is:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt

The Done Interrupt Enable bit(s) (DMAMODE0[10] and/or DMAMODE1[10]) enable a Done interrupt. In Scatter/Gather DMA mode, a bit in the Next Descriptor Pointer register of the channel (loaded from Local memory) specifies whether to assert an interrupt at the end of the transfer for the current descriptor.

A DMA Channel interrupt is cleared by the Channel Clear Interrupt bit(s) (DMACSR0[3]=1 and/or DMACSR1[3]=1).

3.5.7 DMA Data Transfers

The PCI 9054 DMA controller can be programmed to transfer data from the Local Bus to the PCI Bus or from the PCI Bus to the Local Bus.

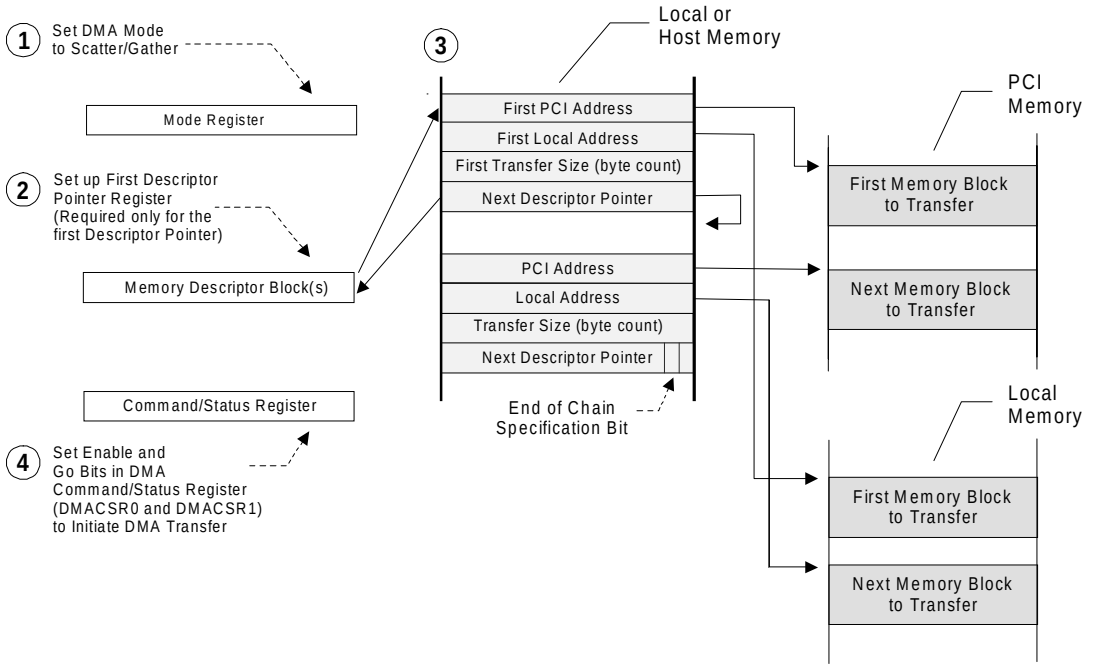


Figure 3-16. Scatter/Gather DMA Mode Descriptor Initialization [PCI SAC/DAC PCI Address (DMADAC0, DMADAC1) Register Dependent]

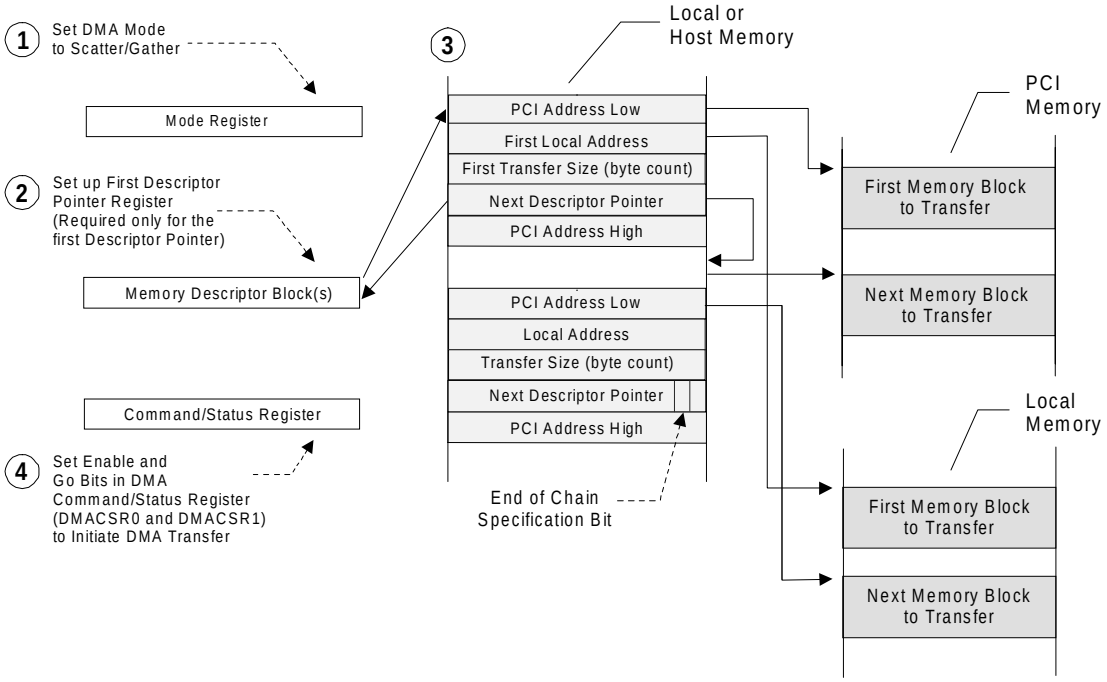


Figure 3-17. Scatter/Gather DMA Mode Descriptor Initialization [DAC PCI Address (DMAMODE0[18], DMAMODE1[18]) Descriptor Dependent]

3.5.7.1 Local-to-PCI Bus DMA Transfer

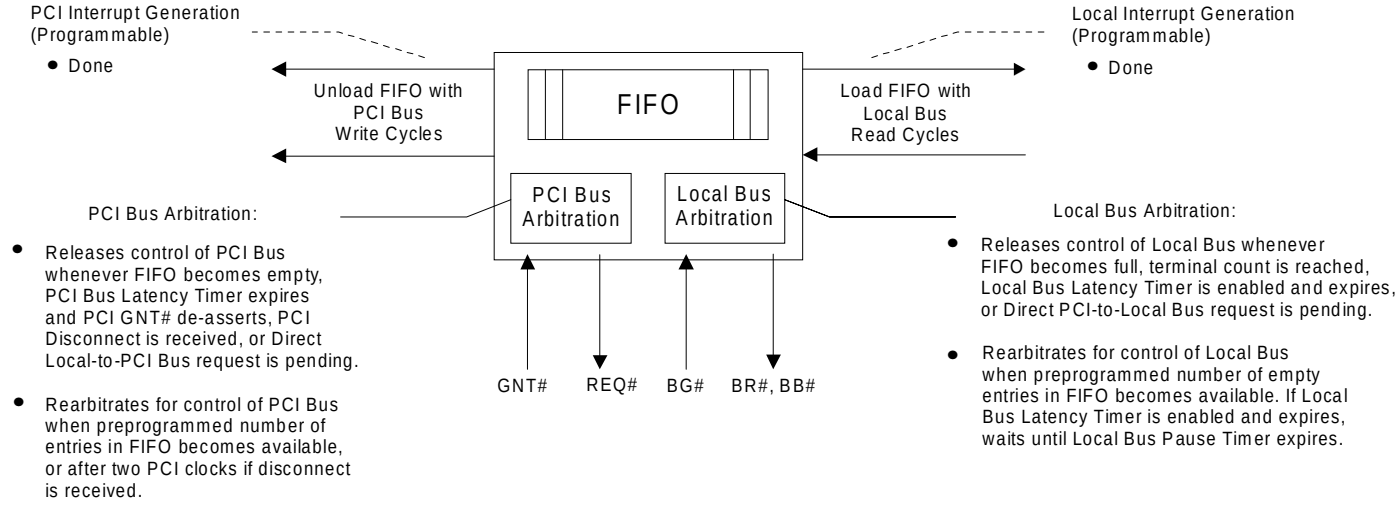


Figure 3-18. Local-to-PCI Bus DMA Data Transfer Operation

3.5.7.2 PCI-to-Local Bus DMA Transfer

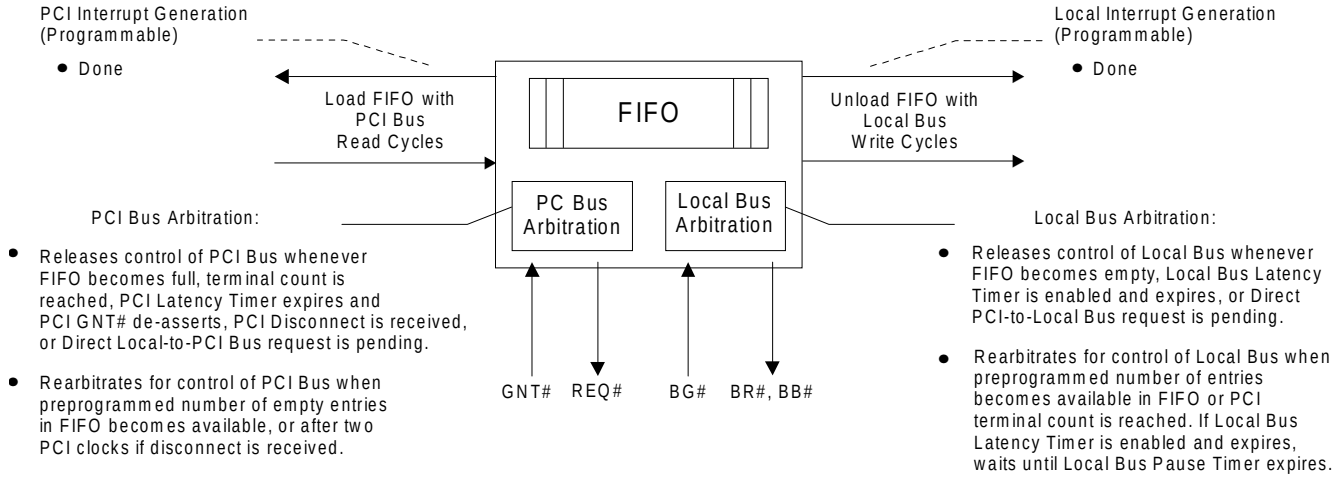


Figure 3-19. PCI-to-Local Bus DMA Data Transfer Operation

3.5.7.3 DMA Local Bus Error Condition

The PCI 9054 supports Local Bus error conditions with the TEA# signal. TEA# may be asserted by a device on the Local Bus, either before or simultaneously with TA#. In either case, the PCI 9054 attempts to finish the current transaction by transferring data and then asserting TS# for every address that follows, waiting for another TA# or TEA# to be issued to flush the FIFOs. After sensing TEA# is asserted, the PCI 9054 asserts PCI SERR# and sets the Signaled System Error bit (PCISR[14], indicating a catastrophic error occurred on the Local Bus. SERR# may be masked by resetting the TEA# Input Interrupt Mask bit (LMISC[5]=0).

The PCI 9054 Local Bus Latency Timer (MARBR[7:0]), as well as the Local Bus Pause Timer (MARBR[15:8]), can be used to better utilize the Local Bus.

3.5.7.4 DMA Unaligned Transfers

For unaligned Local-to-PCI transfers, the PCI 9054 reads a partial Lword from the Local Bus. It continues to perform a Single-Cycle read (Lwords) from the Local Bus until the nearest 16-byte boundary. If the Burst Mode bit is enabled, the PCI 9054 bursts thereafter. Lwords are assembled, aligned to the PCI Bus address, and loaded into the FIFO until the nearest 16-byte boundary.

For PCI-to-Local transfers, Lwords are read from the PCI Bus and loaded into the FIFO. On the Local Bus, Lwords are assembled from the FIFO, aligned to the Local Bus address and single-cycle written to the Local Bus until the nearest 16-byte boundary. If burst functionality is enabled, the PCI 9054 bursts thereafter.

3.5.8 Demand Mode DMA, Channel 0

The Fast/Slow Terminate Mode Select bit(s) (DMAMODE0[15] and/or DMAMODE1[15]) determines the number of Lwords to transfer after the DMA controller DREQ0# input is de-asserted.

If BDIP# output is not required to be de-asserted before the last Lword of a DMA transfer (bit [15]=1), the DMA controller releases the data bus after it receives an external TA# or the internal wait state counter decrements to 0 for the current Lword. If the DMA controller is currently bursting data, which is not the last Data phase for the burst, BDIP# is not asserted before the last Lword of the DMA transfer.

If BDIP# output must be de-asserted before the last Lword of the DMA transfer (bit [15]=0), the DMA controller continues transferring data up to the nearest 16-byte boundary. If DREQ0# is de-asserted during the Address phase of the first transfer in PCI 9054 Local Bus ownership (TS#, BG# asserted), the DMA controller completes a 16-byte transfer. If DREQ0# is de-asserted during a Data-Transfer phase, one Lword before the last 16-byte transfer, the PCI 9054 finishes the transfer and performs an additional 16-byte transfer to satisfy BDIP# de-assertion protocol. (Refer to Table 3-7.)

Table 3-7. Demand Mode DMA, Channel 0

BTERM# Input Enable Bit(s)	Fast/Slow Terminate Mode Select Bit(s)	PCI 9054 BDIP# Output
Enabled (1)	Disabled (1)	BDIP# is not asserted. Immediate transfer terminated by EOT#.
Enabled (1)	Enabled (0)	
Disabled (0)	Disabled (1)	
Disabled (0)	Enabled (0)	BDIP# asserted by the PCI 9054. Transfers up to the nearest 16-byte boundary, then terminates (MPC850 or MPC860 compatible).

3.5.9 End of Transfer (EOT#) Input

The DMA EOT# Enable bit(s) (DMAMODE0[14] and DMAMODE1[14]) determines the number of Lwords to transfer after a DMA controller asserts EOT# input. EOT# input should be asserted only when the PCI 9054 owns a bus. (Refer to Table 3-8.)

If BDIP# output is not required to be de-asserted before the last Lword of the DMA transfer (DMAMODE0[15]=1 and/or DMAMODE1[15]=1), and the DMA EOT# Enable bit(s) is set (DMAMODE0[14]=1 and/or DMAMODE1[14]=1), the DMA controller releases the data bus and terminates DMA after receiving an external TA# signal. Or, the internal wait state counter decrements to 0 for the current Lword when EOT# is asserted.

If BDIP# output must be de-asserted before the last Lword of the DMA transfer (DMAMODE0[15]=0 and/or DMAMODE1[15]=0), the DMA controller transfers data up to the nearest 16-byte boundary if EOT# is asserted and enabled (DMAMODE0[14]=1 and/or DMAMODE1[14]=1).

If EOT# is asserted during the Data-Transfer phase one Lword before the last 16-byte transfer, the PCI 9054 completes the transfer and performs an additional 16-byte transfer to satisfy the BDIP# de-assertion protocol.

The DMA controller terminates a transfer on an Lword boundary after EOT# is asserted. For an 8-bit bus, the PCI 9054 terminates after transferring the last byte for the Lword. For a 16-bit bus, the PCI 9054 terminates after transferring the last word for the Lword. In Single-Cycle mode (burst disabled), the transfer is terminated at the four-Lword boundary.

During the descriptor loading on the Local Bus, assertion of EOT# causes a complete descriptor load and no subsequent Data transfer; however, this is not recommended. This has no effect when the descriptor is loaded from the PCI Bus.

Table 3-8. Any DMA Transfer Channel 0/1 with EOT Functionality

BTERM# Enable Bit(s)	Fast/Slow Terminate Mode Select Bit(s)	PCI 9054 BDIP# Output
Enabled (1)	Disabled (1)	BDIP# is not asserted. Immediate transfer terminated by EOT# or paused by DREQ#.
Enabled (1)	Enabled (0)	
Disabled (0)	Disabled (1)	
Disabled (0)	Enabled (0)	BDIP# asserted by the PCI 9054. Transfers up to the nearest 16-byte boundary, then terminates (MPC850 or MPC860 compatible).

3.5.10 DMA Arbitration

The PCI 9054 asserts BR# when it needs to be the Local Bus Master. Upon receiving BG#, the PCI 9054 waits for BB# to be de-asserted. The PCI 9054 then asserts BB# at the next rising edge of the Local clock after acknowledging BB# is de-asserted (no other device is acting as Local Bus Master). The PCI 9054 continues to assert BB# while acting as the Local Bus Master (*that is*, it holds the bus until instructed to release BB#) under the following conditions:

- Local Bus Latency Timer is enabled and expires (MARBR[7:0])
- Direct Slave access is pending
- EOT# input is received (if enabled)

The DMA controller releases control of the PCI Bus when one of the following conditions occurs:

- FIFOs are full or empty
- PCI Bus Latency Timer expires (PCILTR[7:0])—and loses the PCI GNT# signal
- Target disconnect response is received

The DMA controller de-asserts its PCI Bus request (REQ#) for a minimum of two PCI clocks.

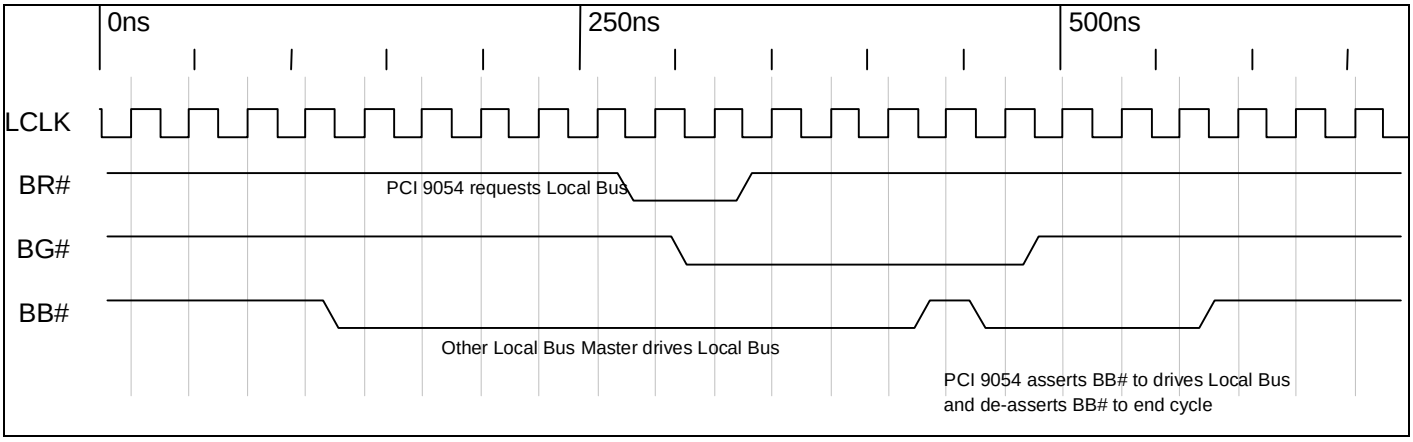
3.5.11 Local Bus Latency and Pause Timers

The Local Bus Latency and Pause Timers are programmable with the Mode/DMA Arbitration register (MARBR[7:0, 15:8]). If the Local Bus Latency Timer is enabled and expires (MARBR[7:0]), the PCI 9054 completes an Lword transfer up to the nearest 16-byte boundary and releases the Local Bus, de-asserting BB#. After the programmable Pause Timer expires (MARBR[15:8]), it arbitrates for the bus by asserting BR#. When it receives BG#, it asserts BB# and continues to transfer until the FIFO is empty for a Local-to-PCI transfer or full for a PCI-to-Local transfer.

The DMA transfer could be paused by writing a 0 to the Channel Enable bit. To acknowledge the disable, the PCI 9054 gets at least one data from the bus before it stops. However, this is not recommended during a burst.

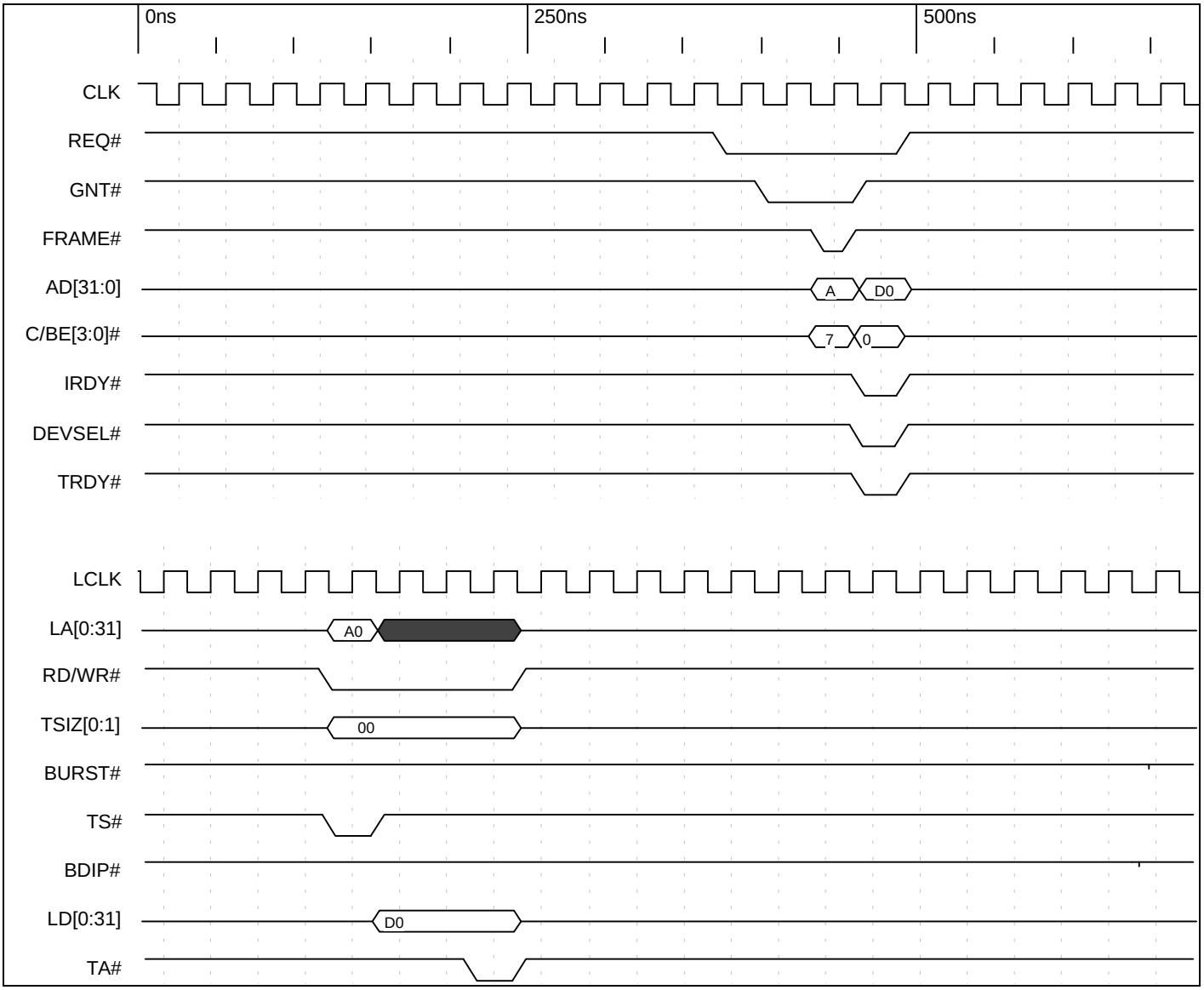
The DMA Local Bus Timer starts after the Local Bus is granted to the PCI 9054 and the Local Pause Timer starts after BB# is de-asserted.

3.6 M Mode Timing Diagrams

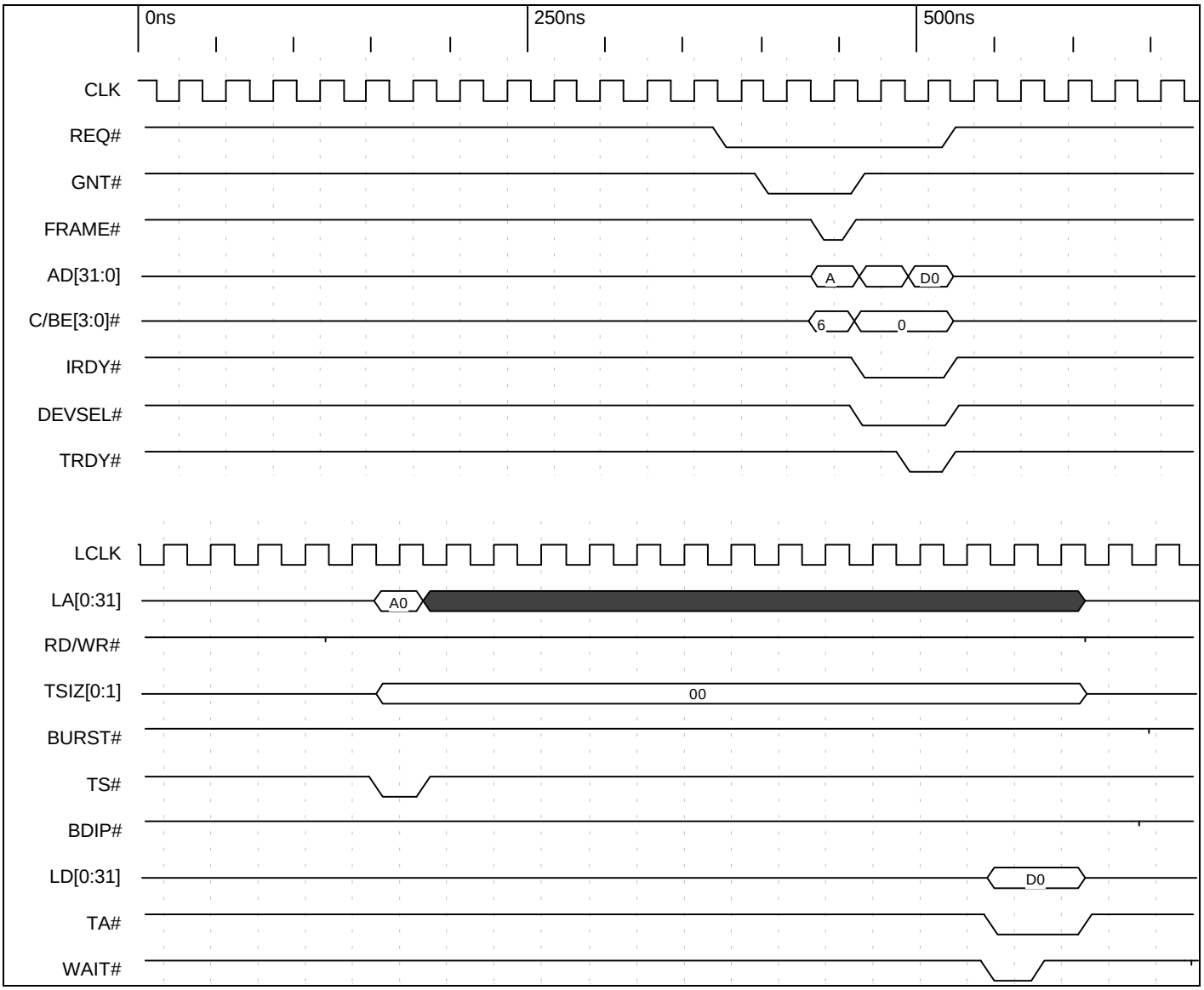


Timing Diagram 3-1. Local Bus Arbitration (BR#, BG#, BB#, etc.)

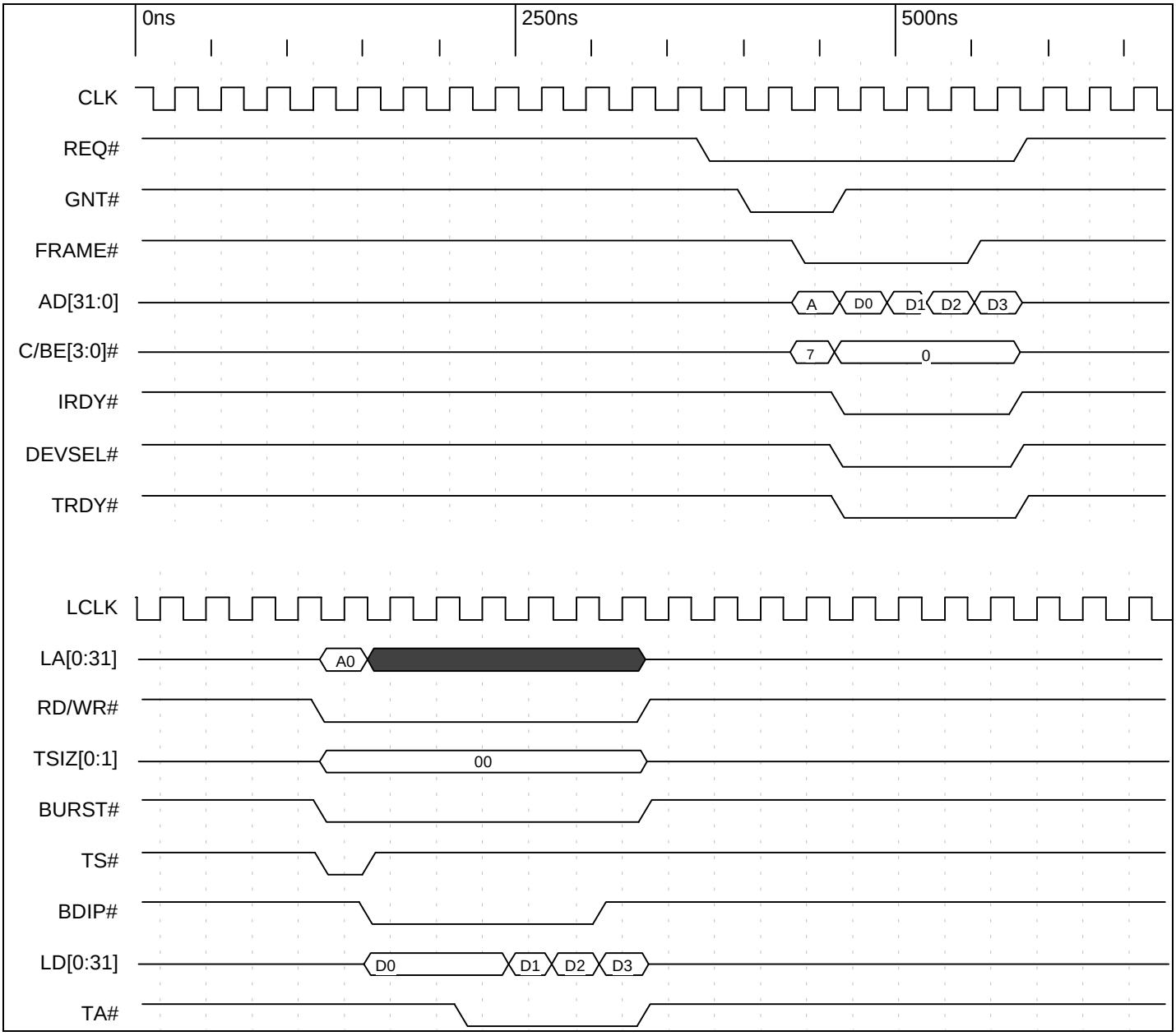
3.6.1 M Mode Direct Master



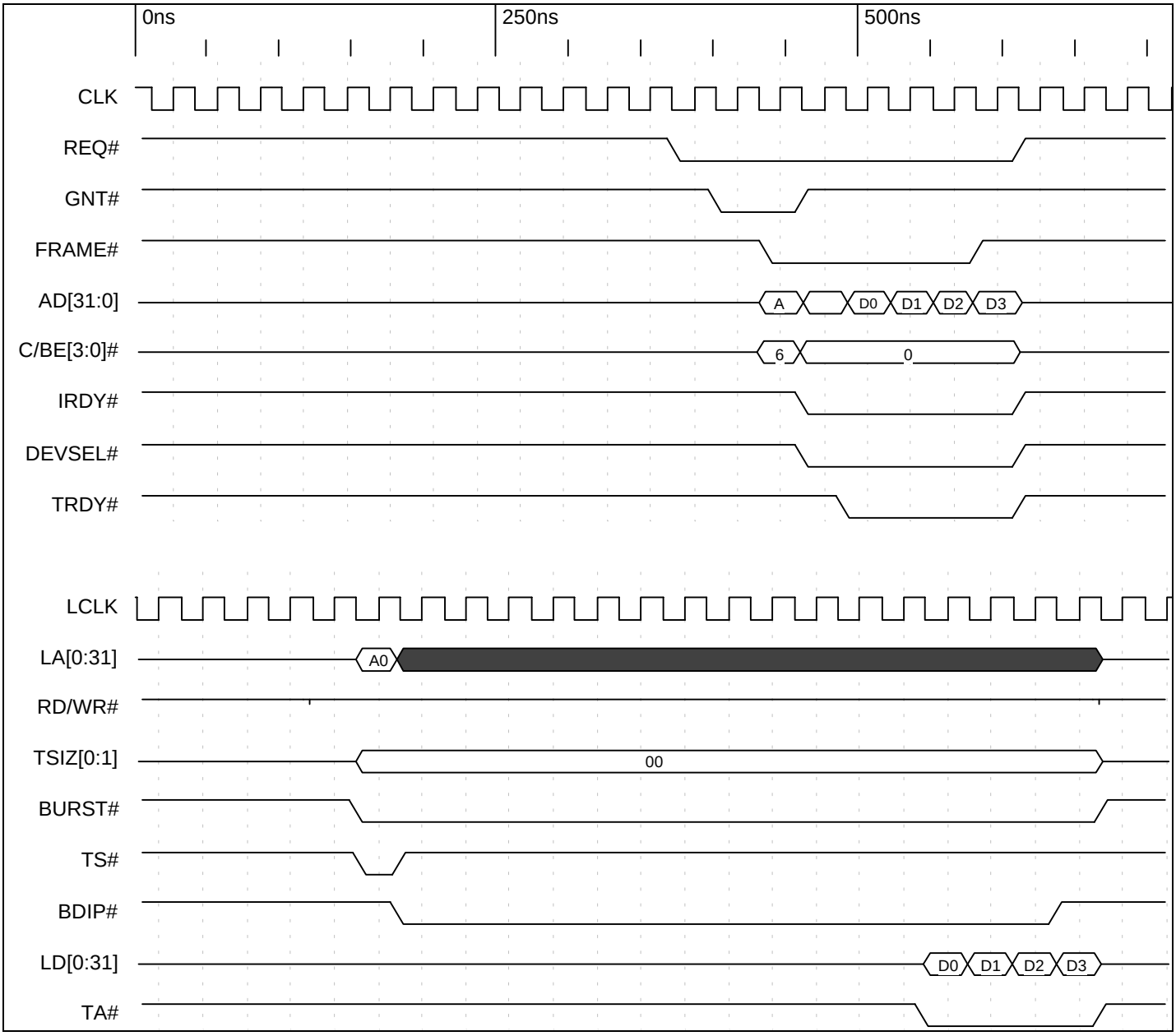
Timing Diagram 3-2. Direct Master Single Write Cycle, Zero Wait States



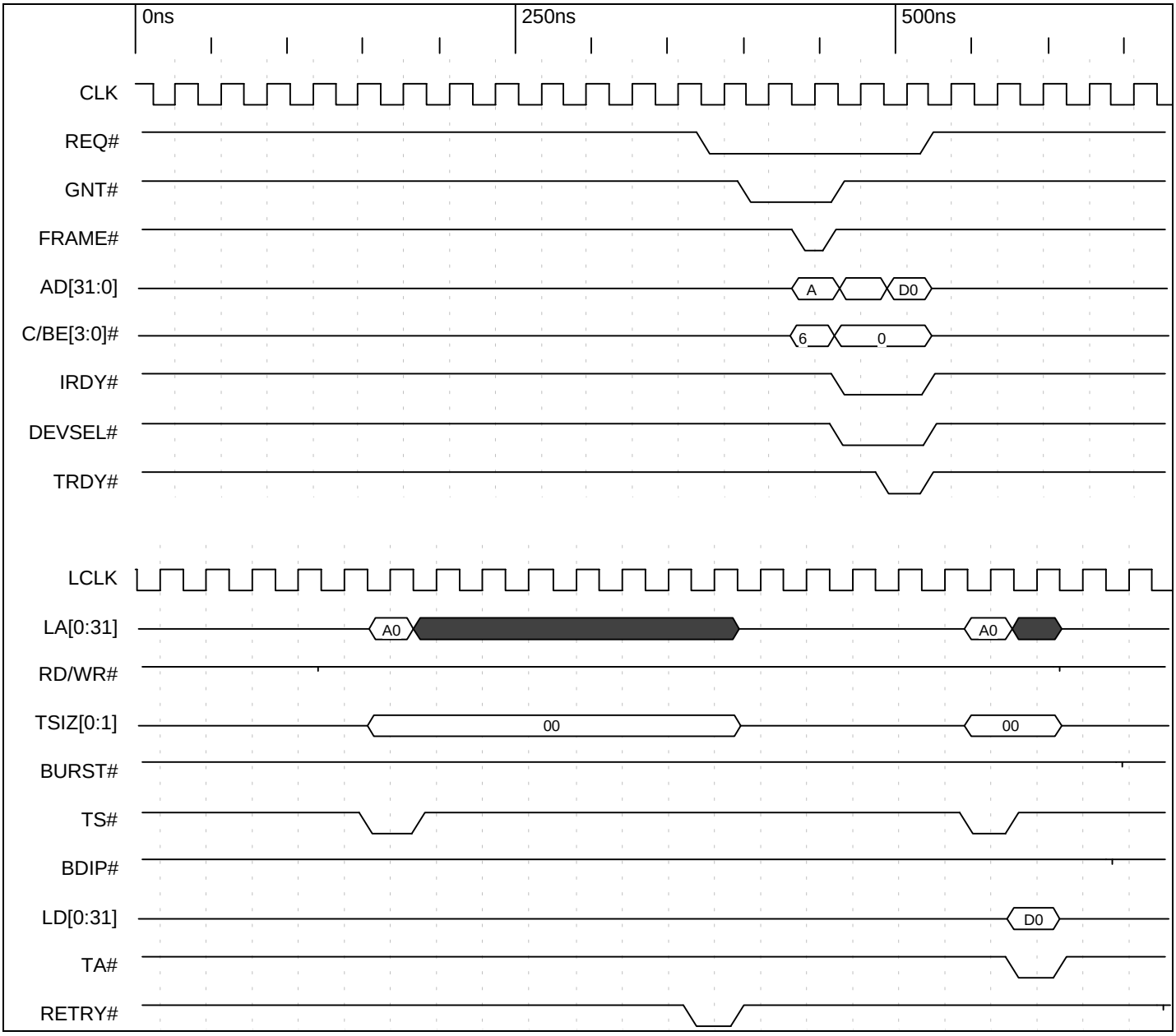
Timing Diagram 3-3. Direct Master Single Read Cycle, One Wait State (WAIT# Asserted for One Clock)



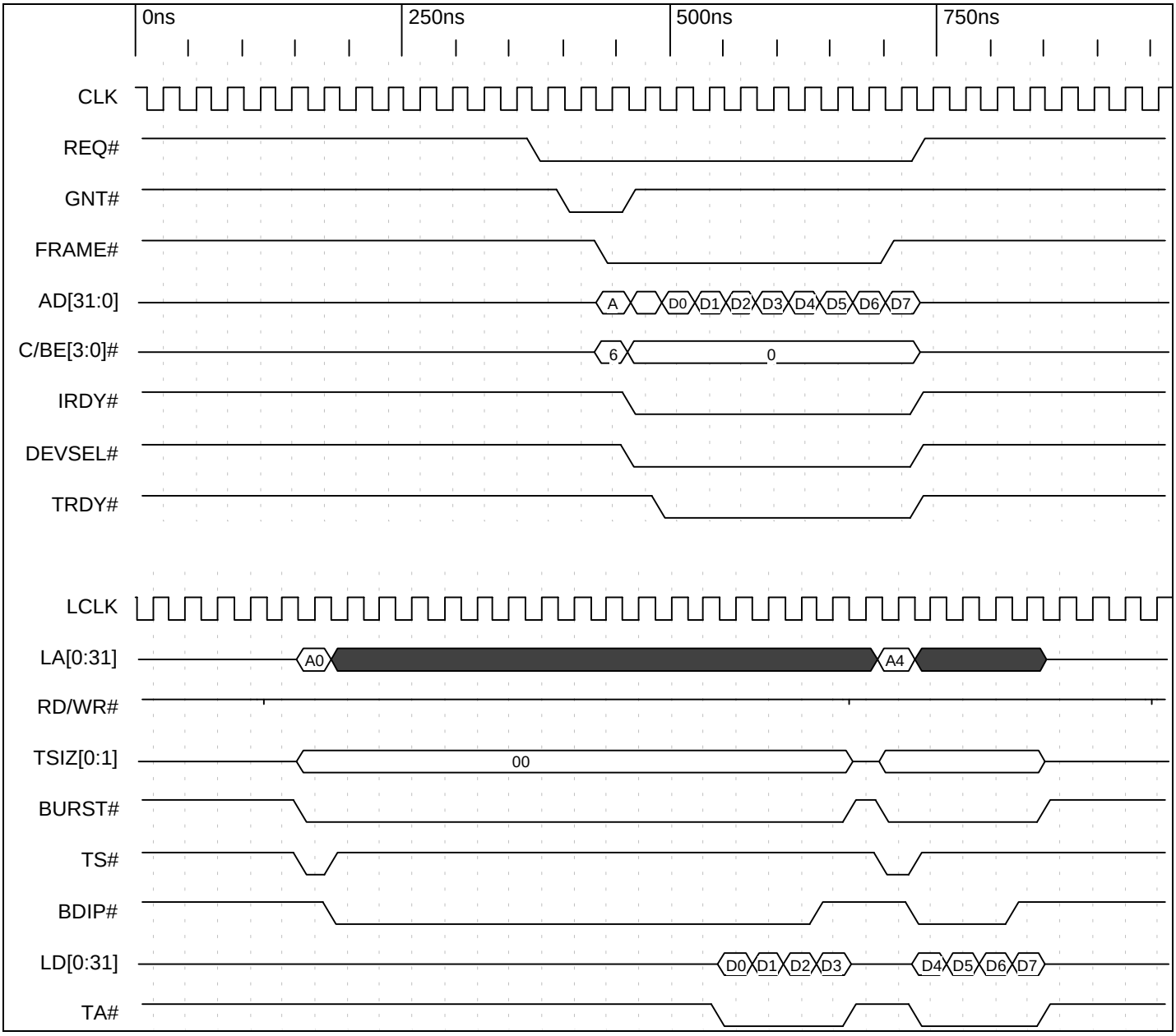
Timing Diagram 3-4. Direct Master Burst Write Cycle of Four Lwords, Zero Wait States



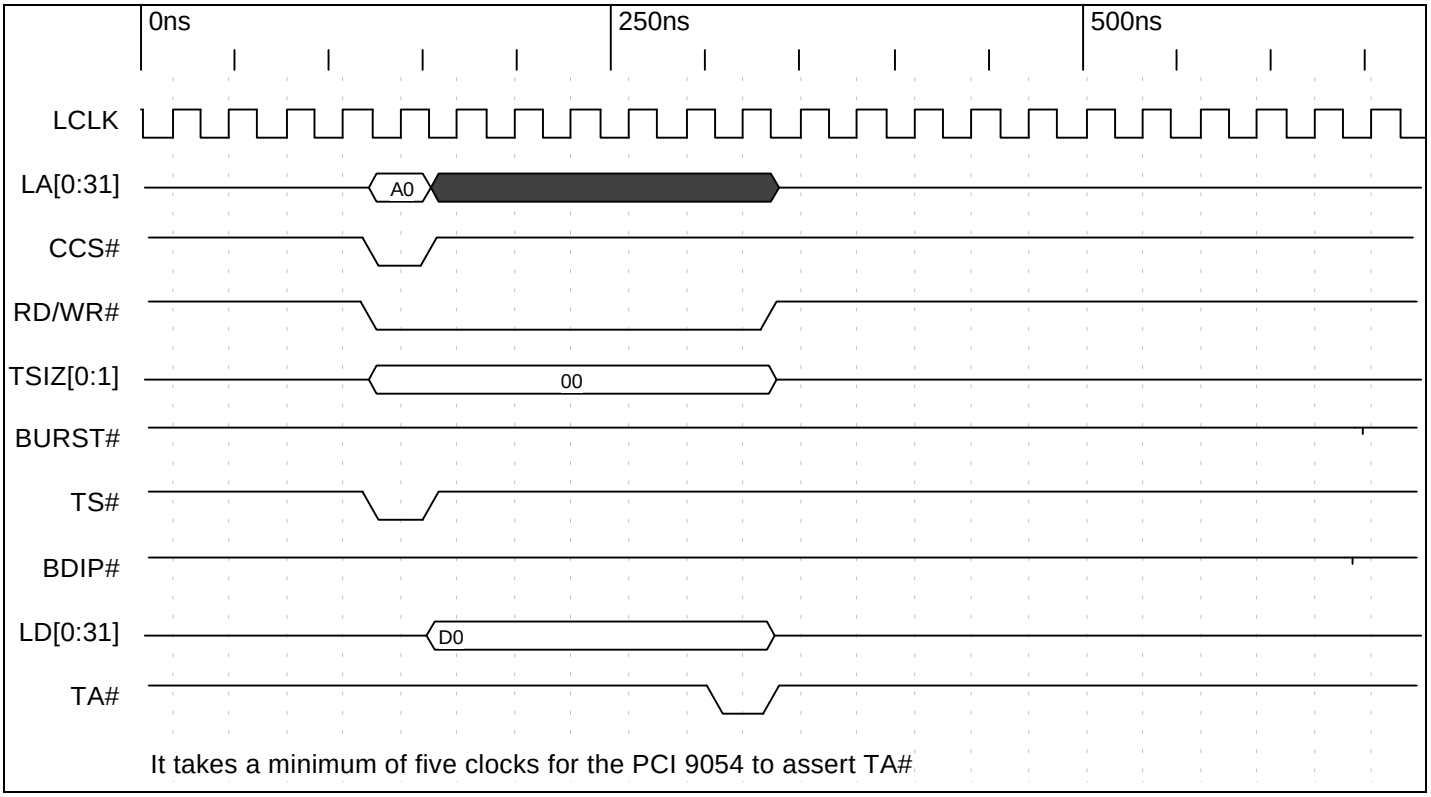
Timing Diagram 3-5. Direct Master Burst Read Cycle of Four Lwords, Zero Wait States



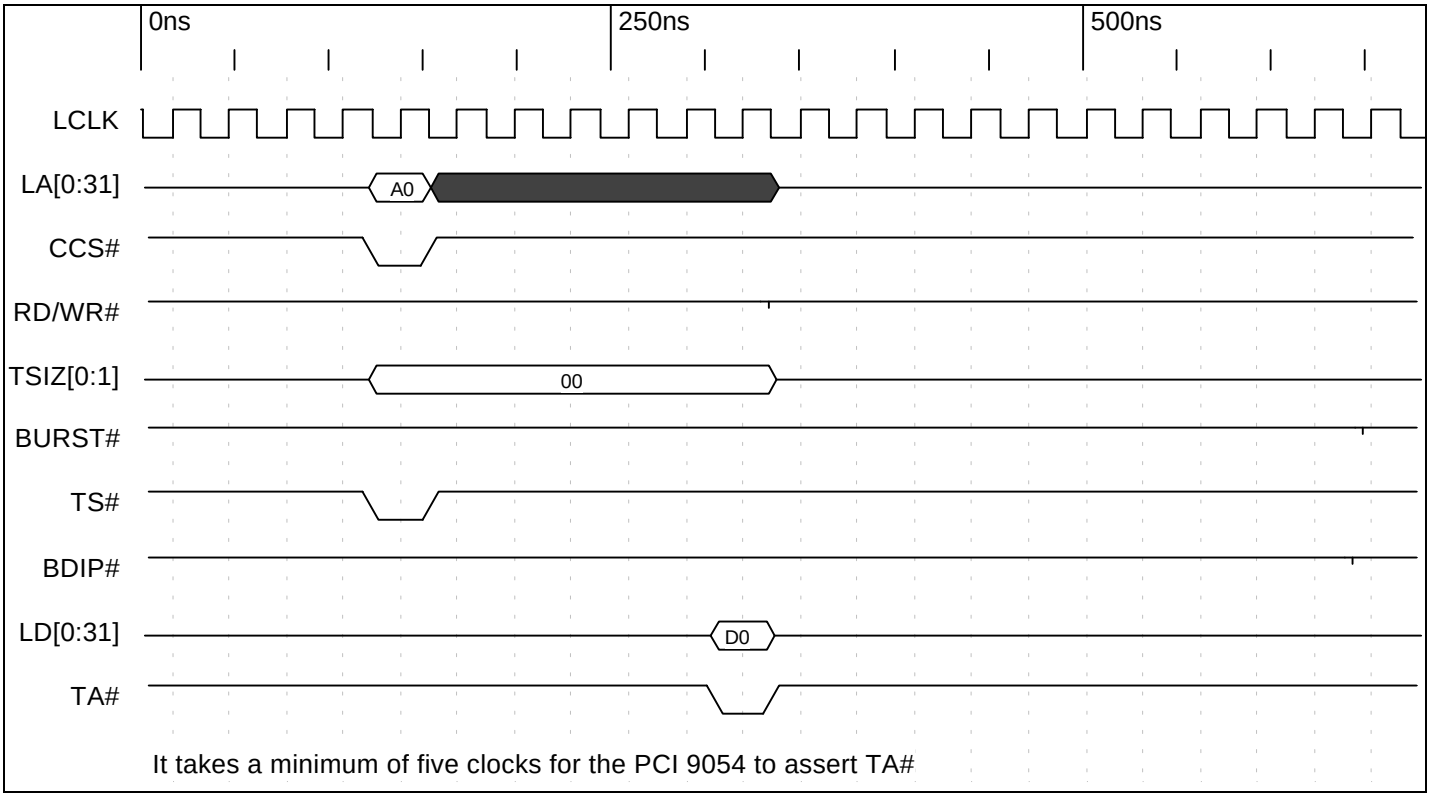
Timing Diagram 3-6. Direct Master Deferred Read Mode (RETRY#)



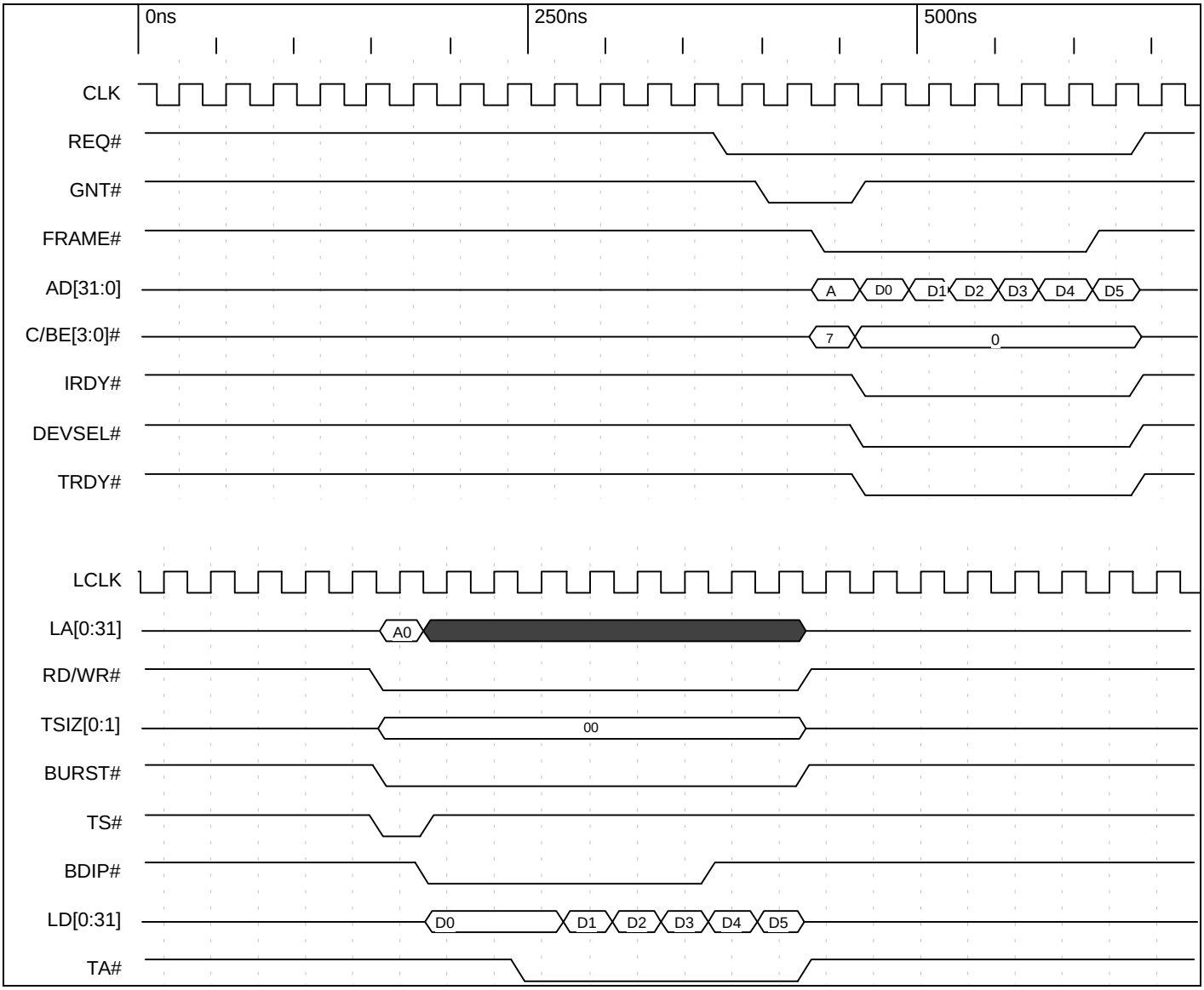
Timing Diagram 3-7. Direct Master Burst Read with Read Ahead Mode (Prefetch Counter Set to Eight Lwords)



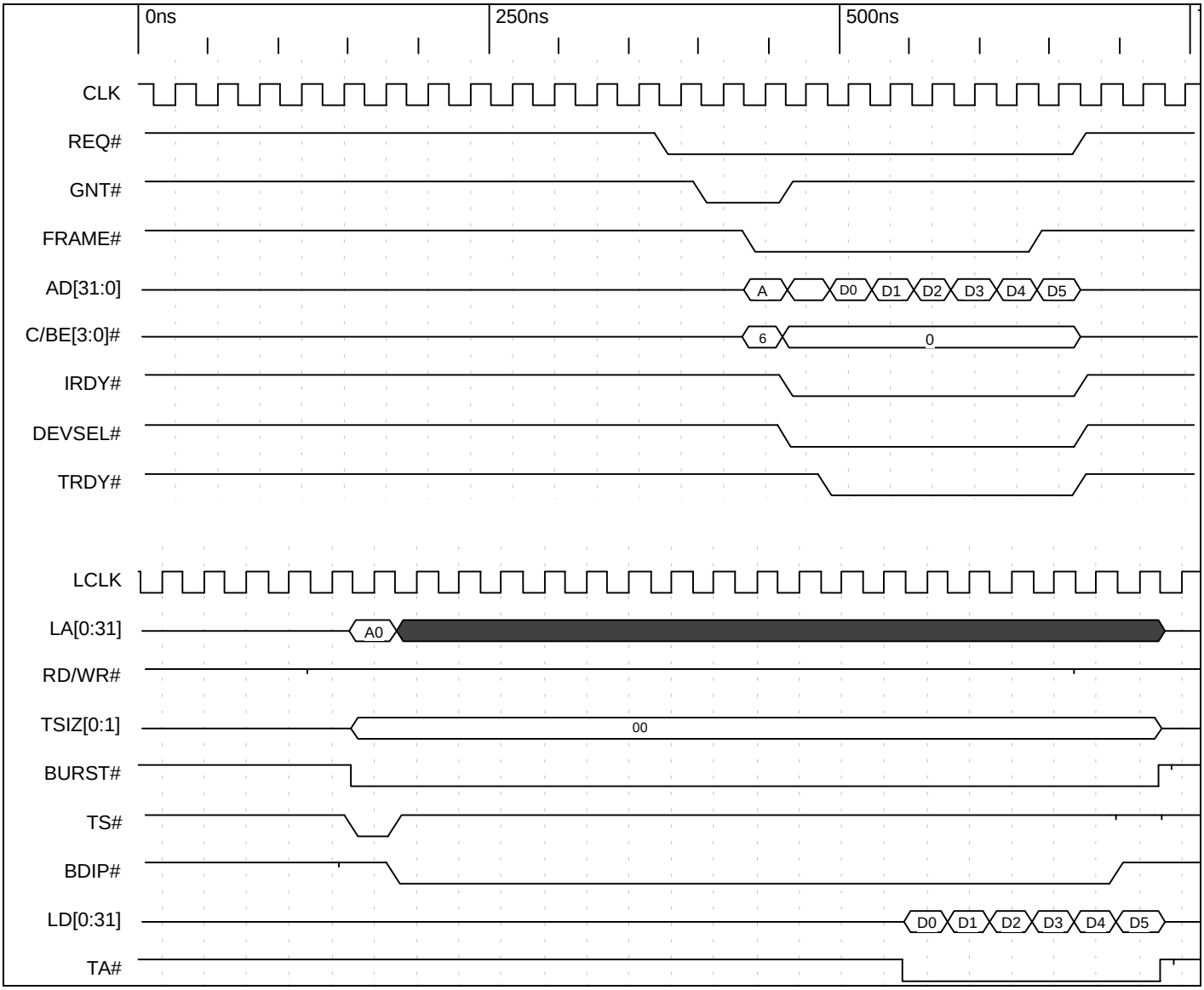
Timing Diagram 3-8. Local Configuration Write to Configuration Register



Timing Diagram 3-9. Local Configuration Read from Configuration Register

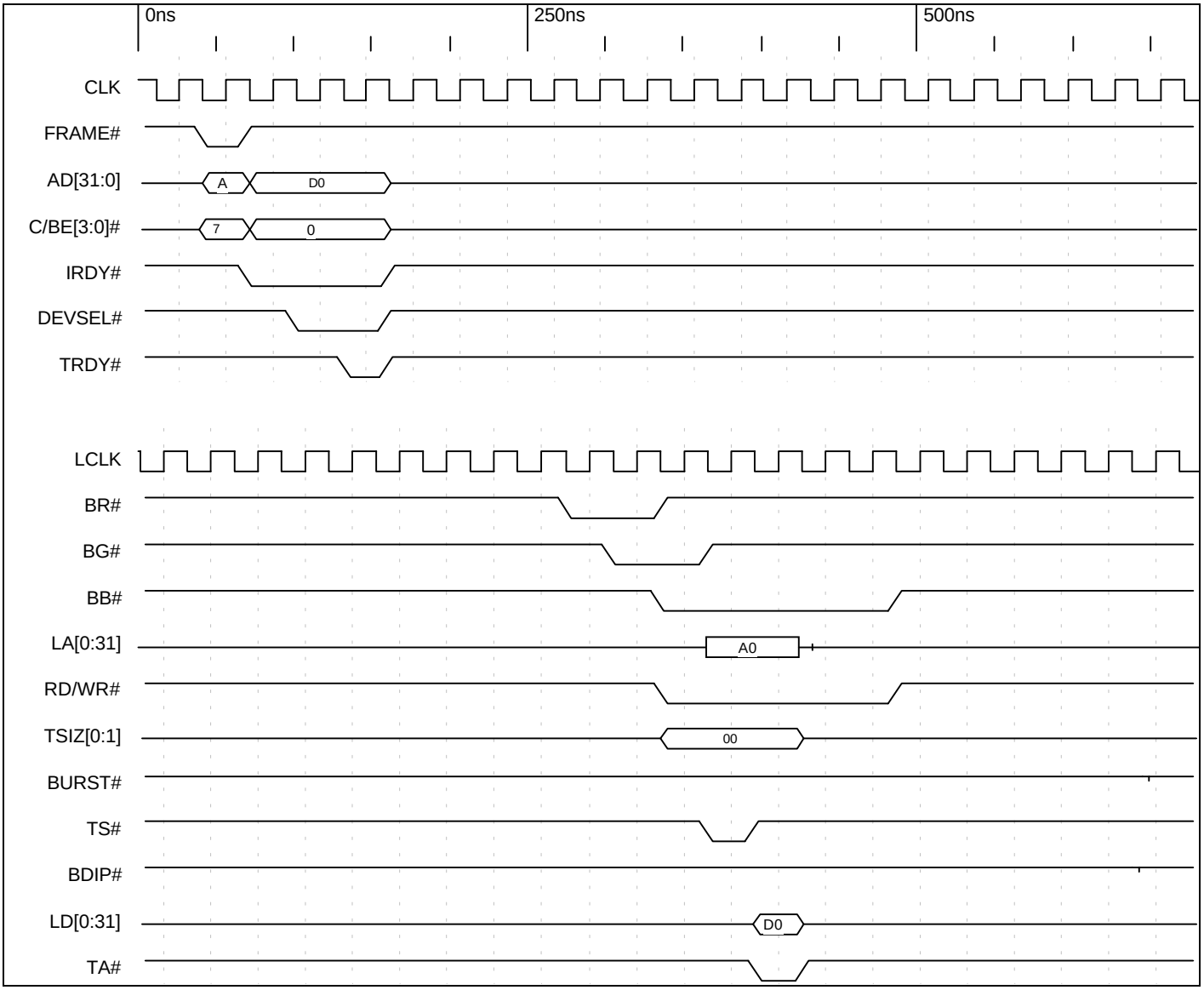


Timing Diagram 3-10. Direct Master Burst Write of Six Lwords Beyond MPC860 Protocol

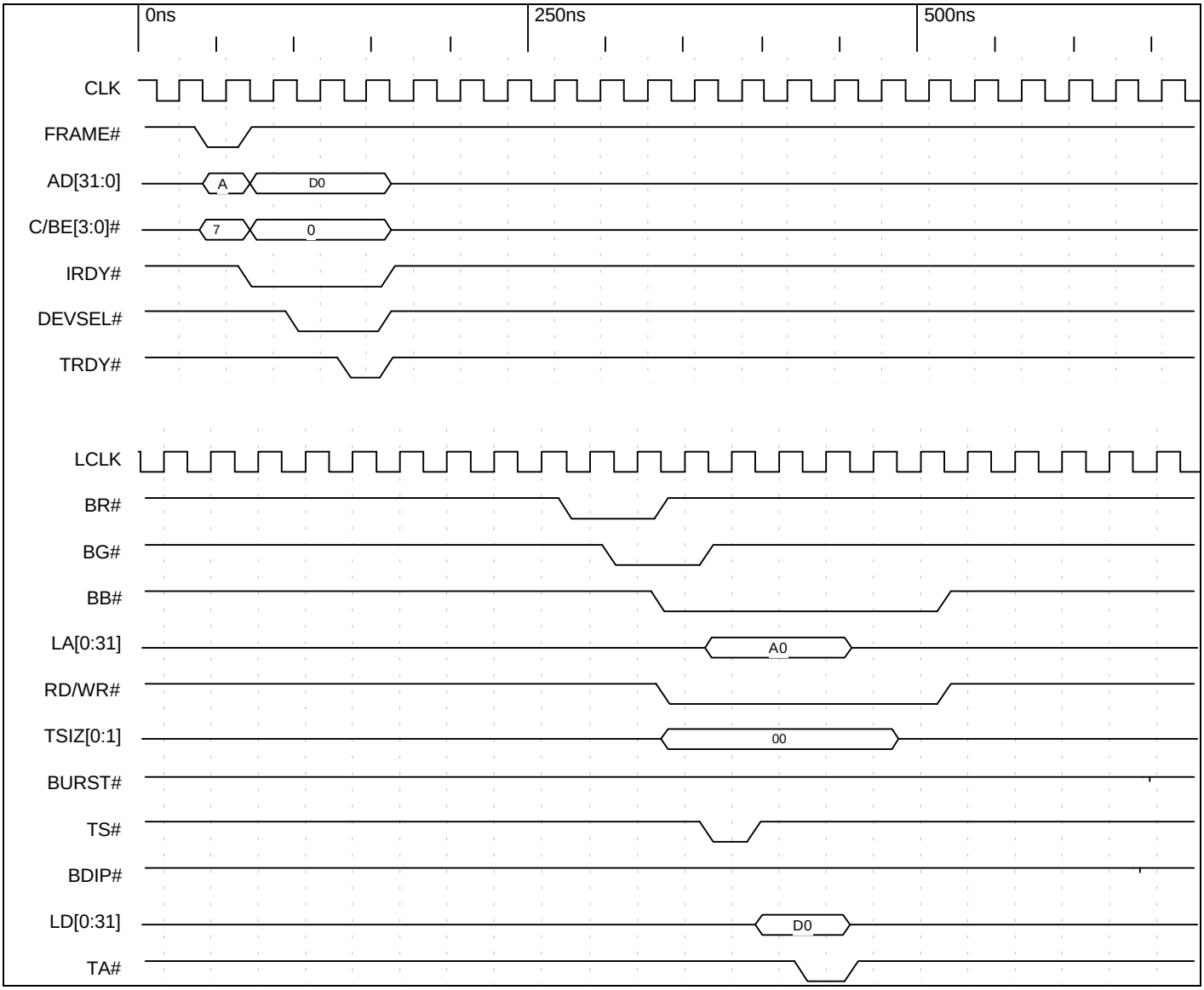


Timing Diagram 3-11. Direct Master Burst Read of Six Lwords Beyond MPC860 Protocol

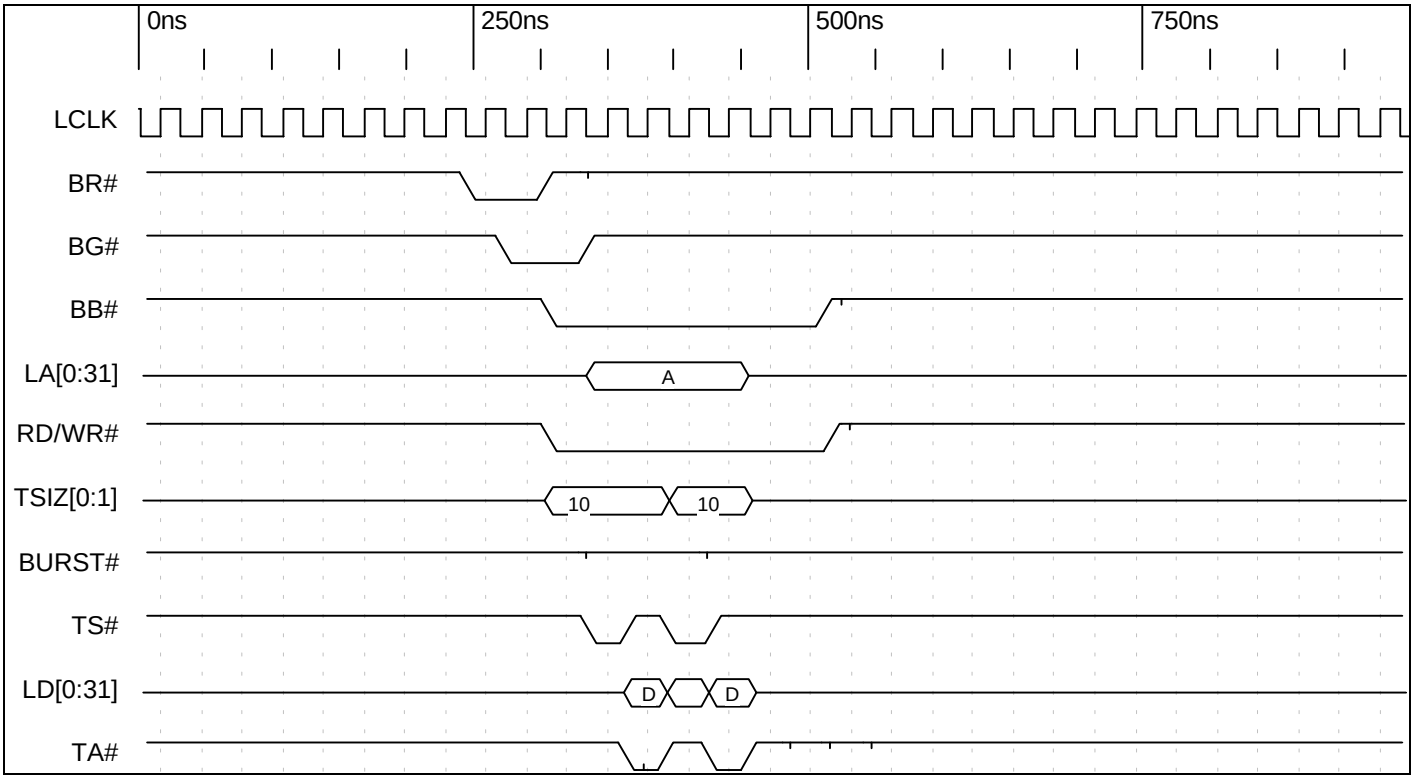
3.6.2 M Mode Direct Slave



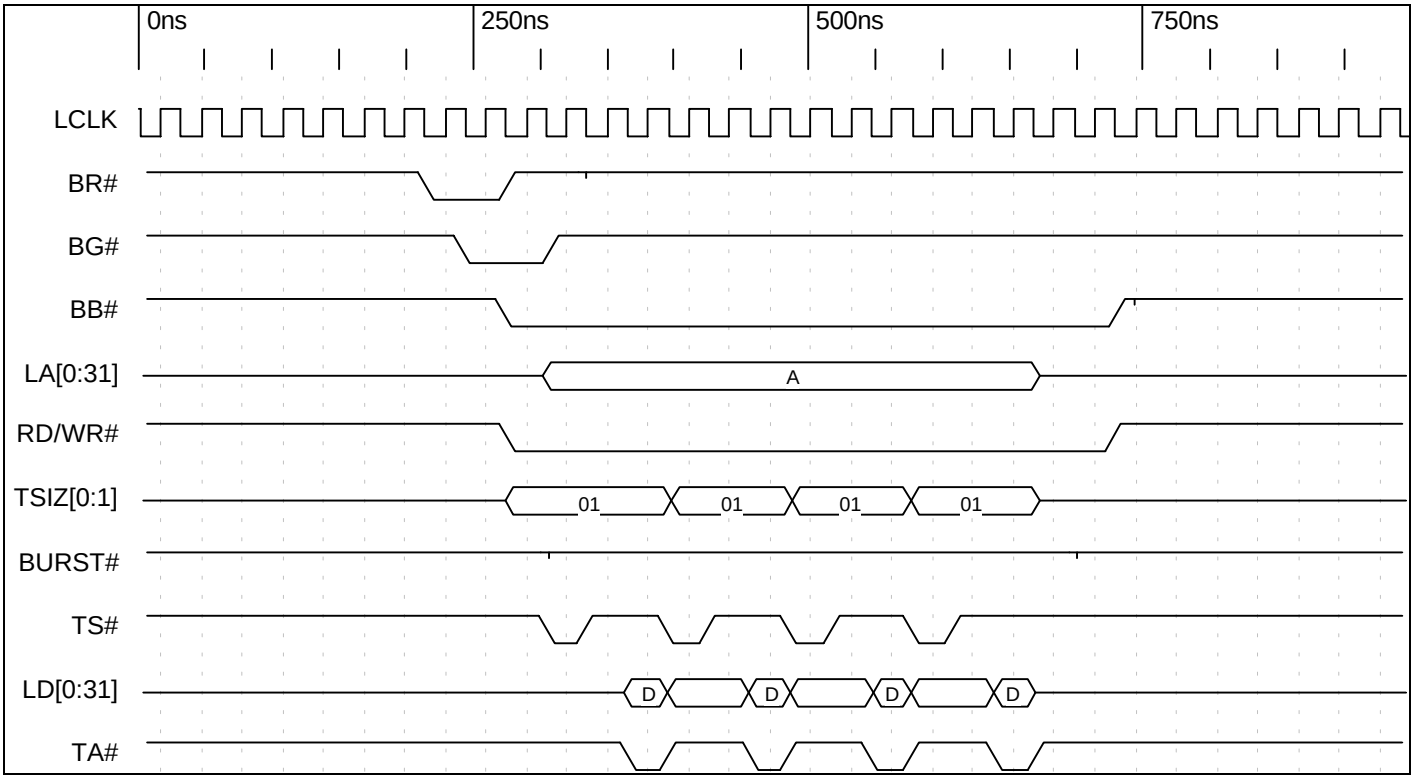
Timing Diagram 3-12. Direct Slave Single Write Cycle, Zero Wait States



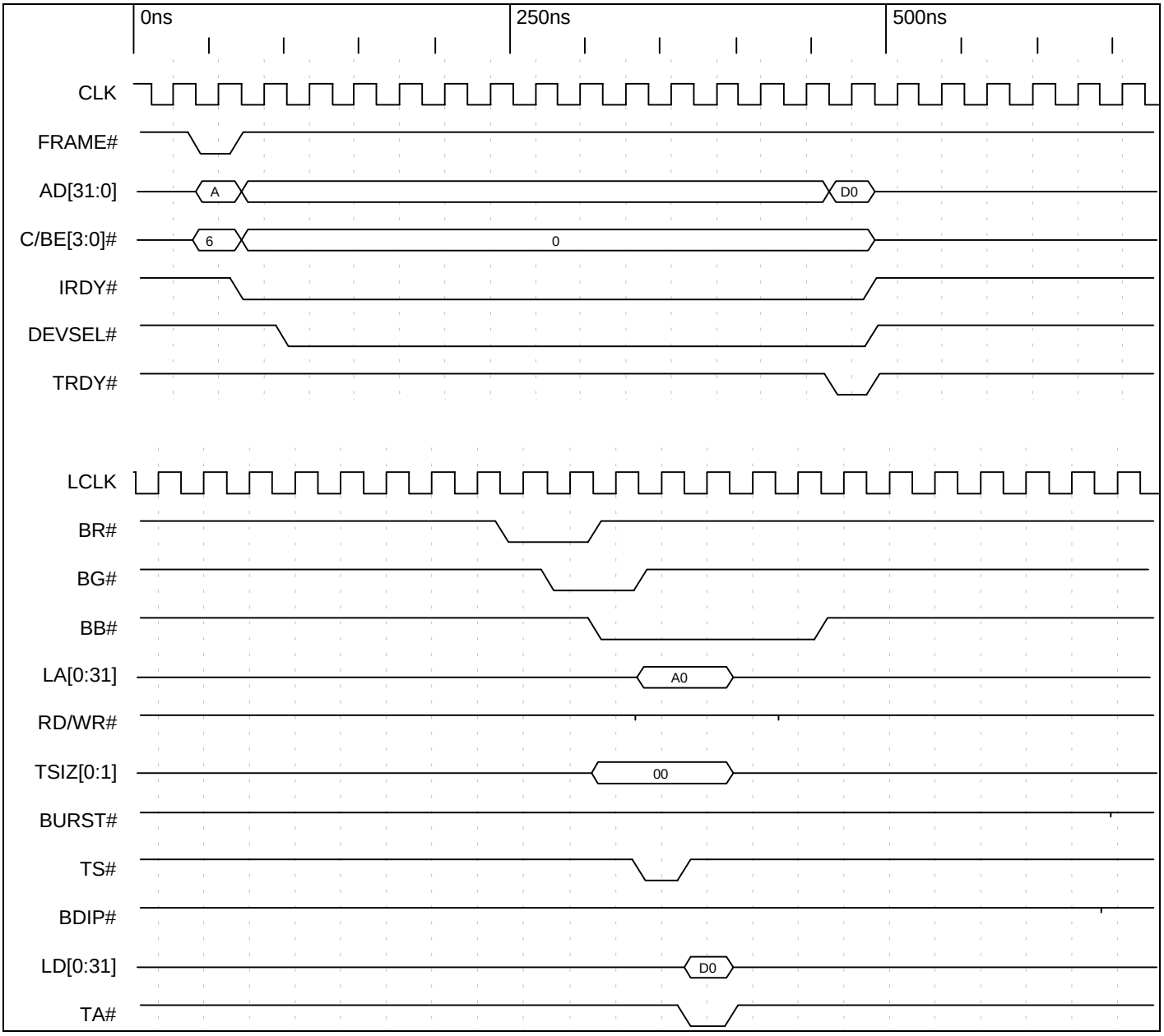
Timing Diagram 3-13. Direct Slave Single Write Cycle, One Wait State by Delaying TA#



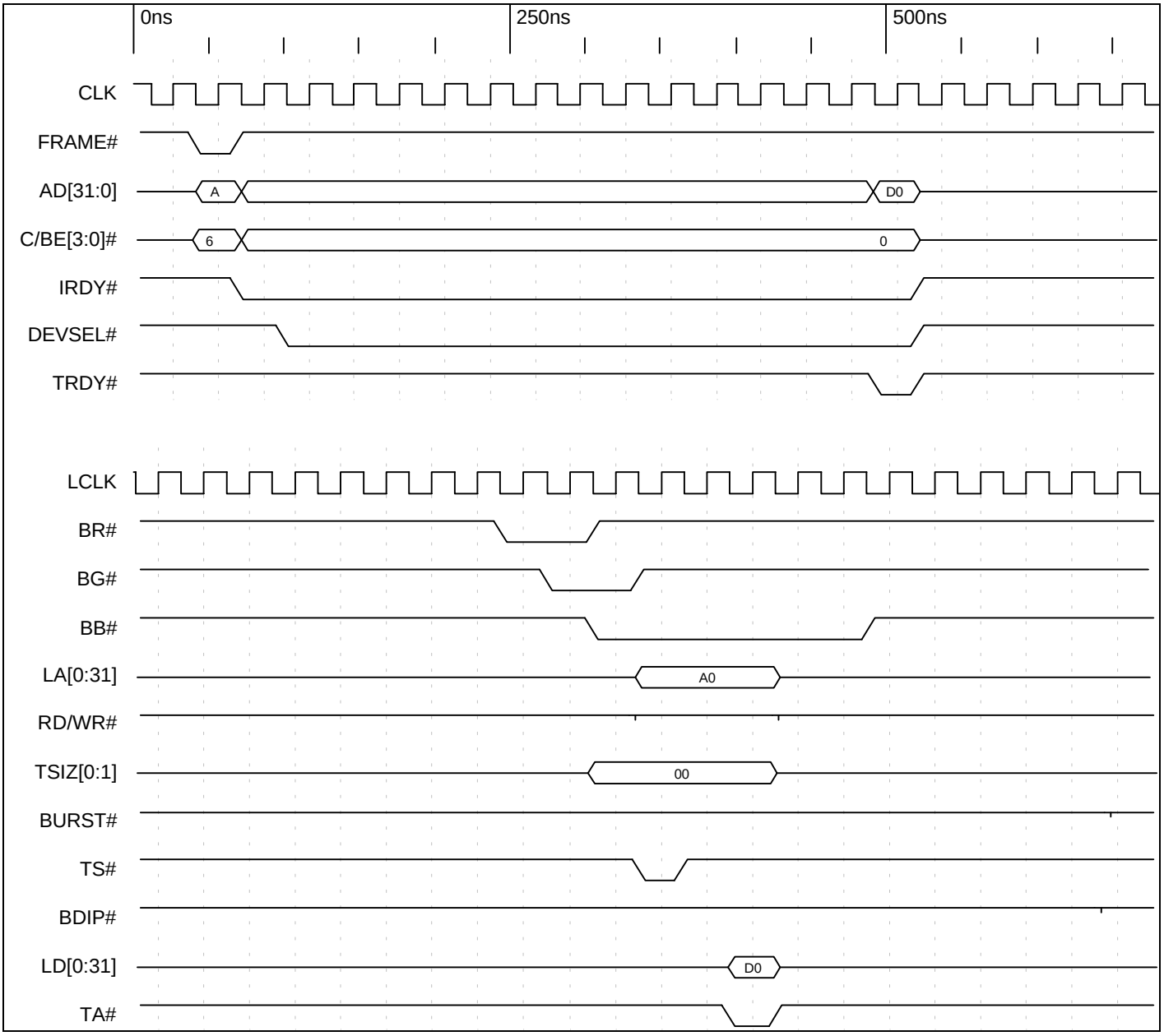
Timing Diagram 3-14. Local Bus Single Write Cycle, Zero Wait States, Burst Enabled, 16-Bit Local Bus



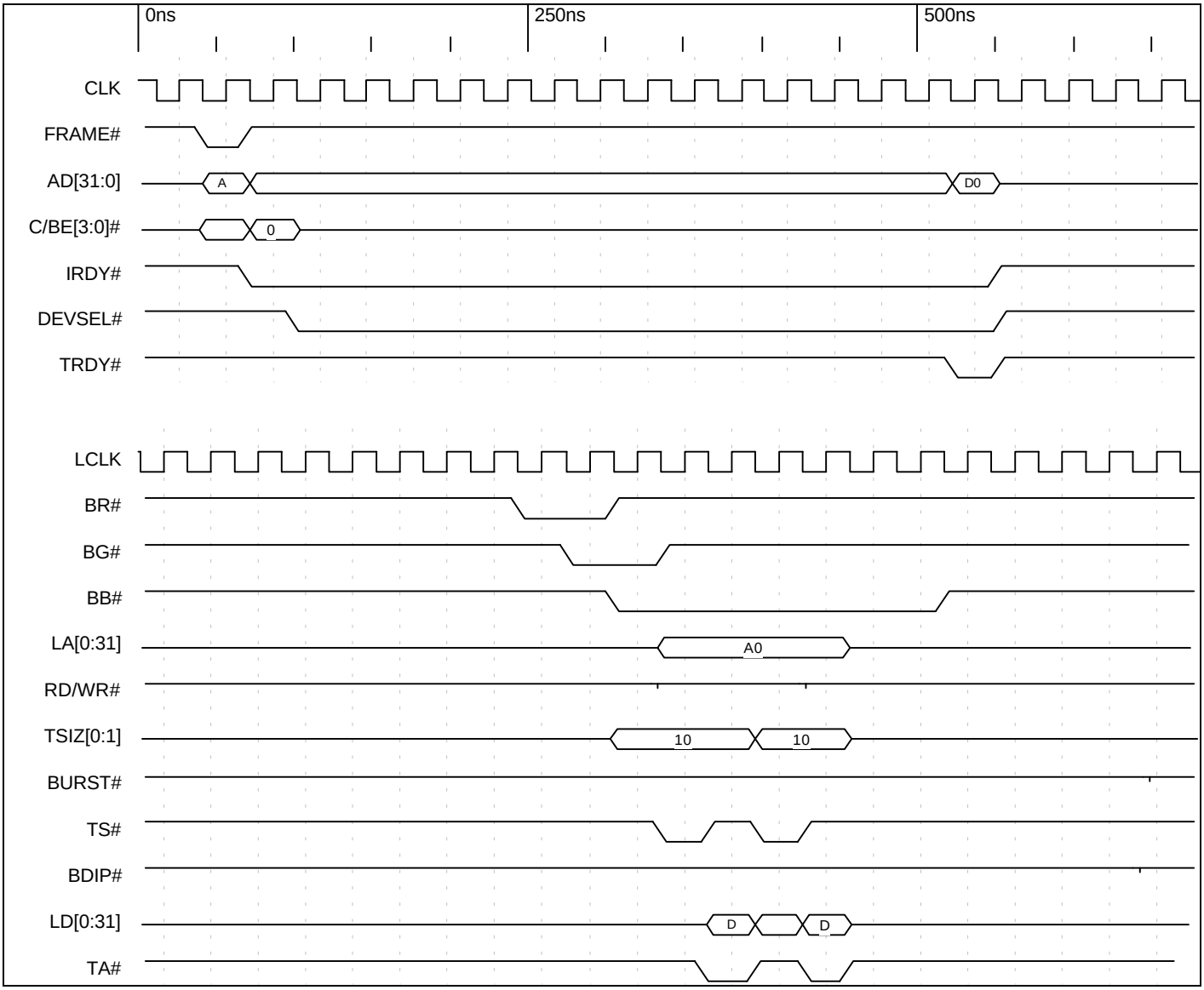
Timing Diagram 3-15. Local Bus Single Write Cycle, One Wait State, Burst Disabled, 8-Bit Local Bus



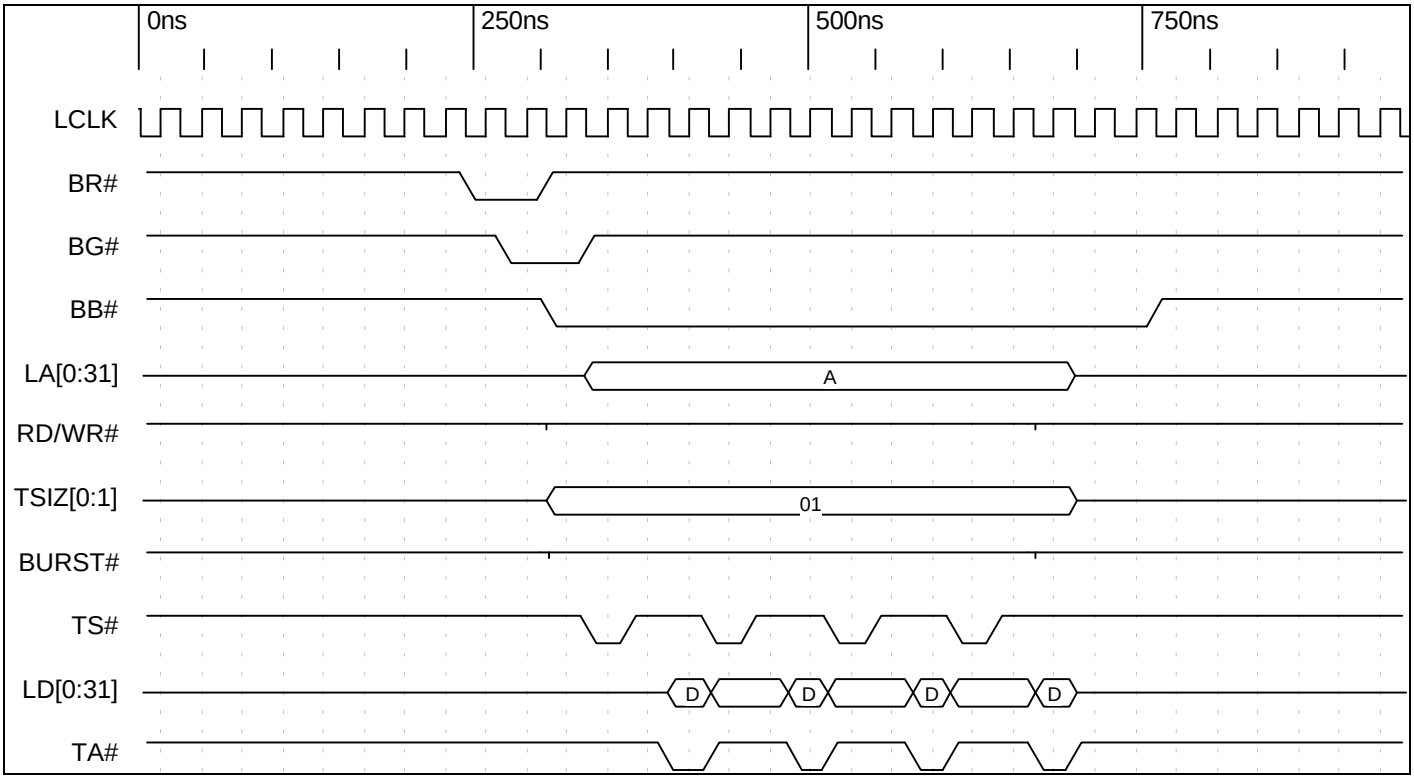
Timing Diagram 3-16. Direct Slave Single Read Cycle, Zero Wait States



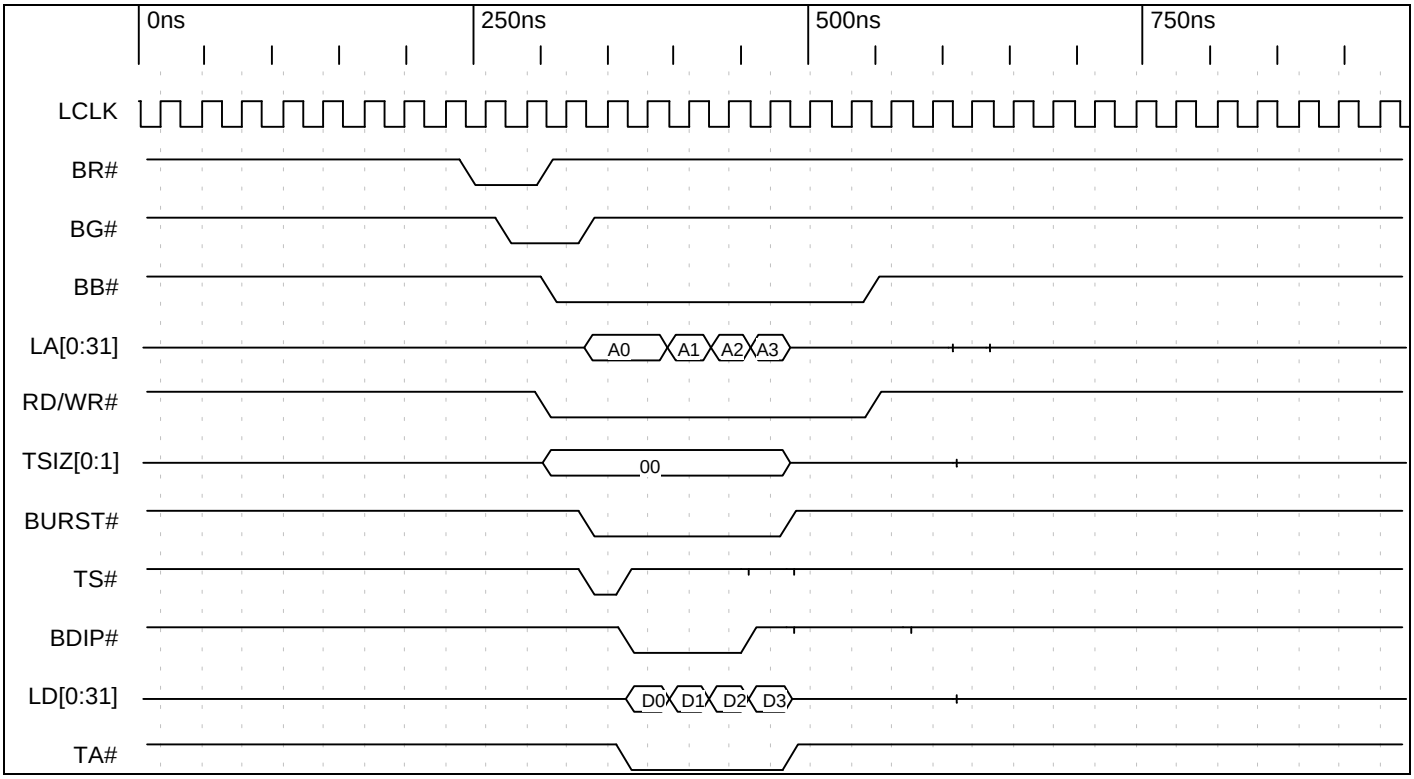
Timing Diagram 3-17. Direct Slave Single Read Cycle, One Wait State Using TA#



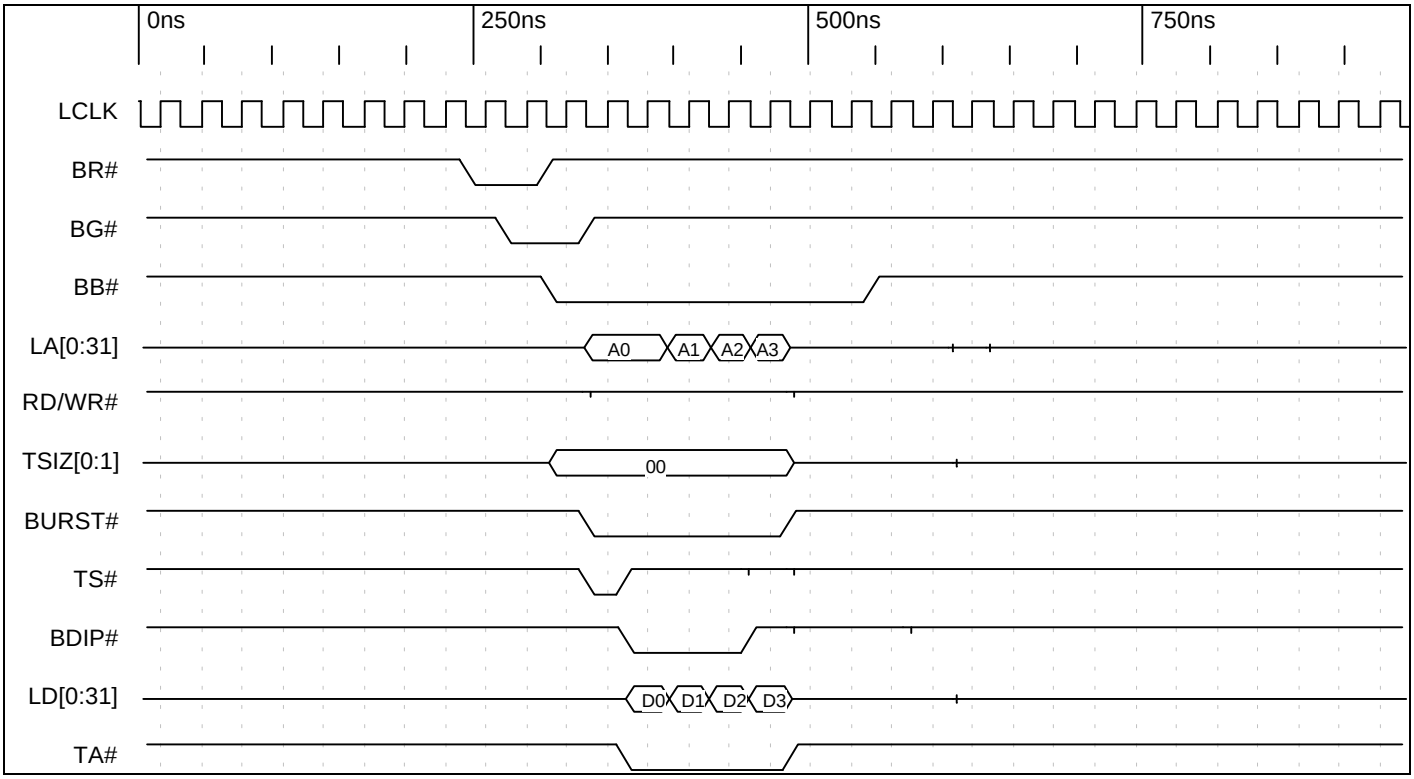
Timing Diagram 3-18. Direct Slave Single Read Cycle, Zero Wait States, 16-Bit Bus



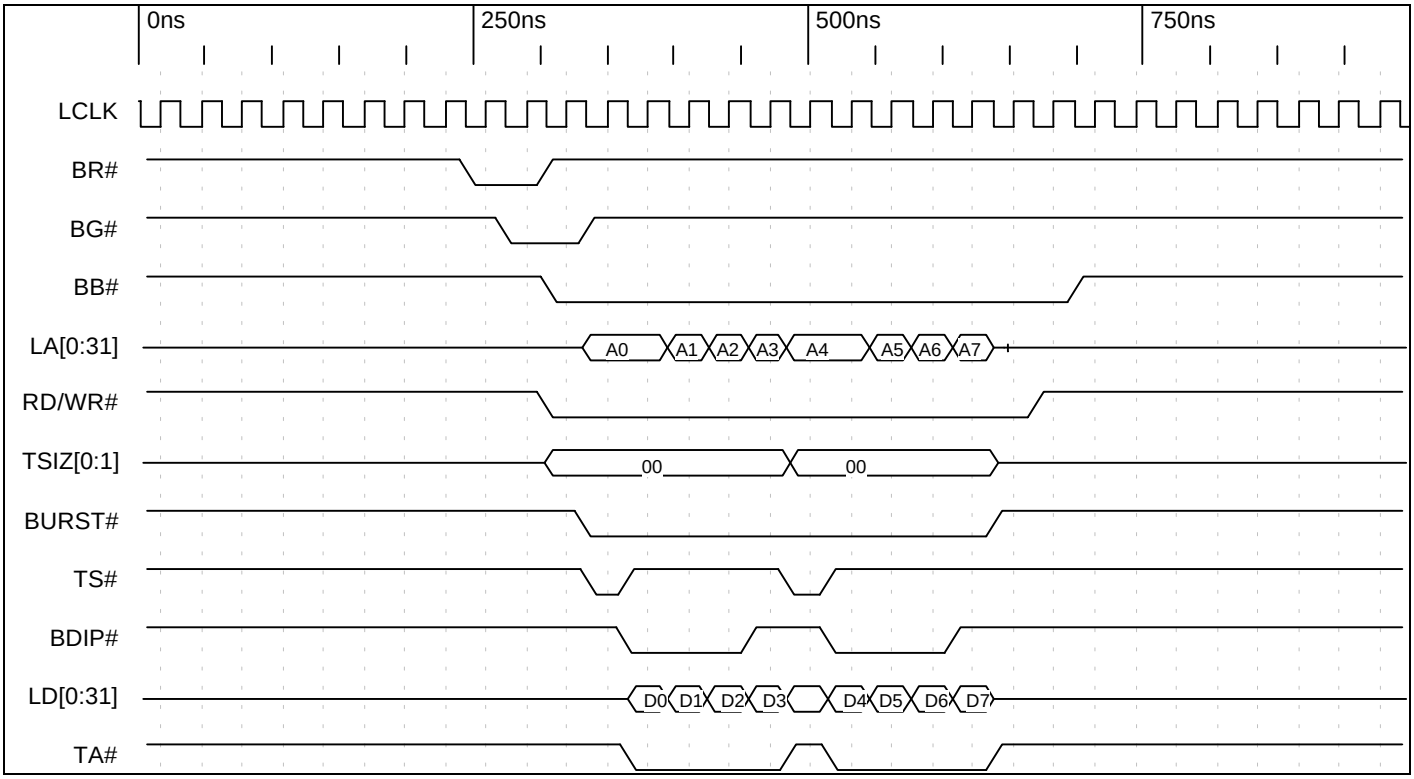
Timing Diagram 3-19. Direct Slave Single Read Cycle, One Wait State, Burst Disabled, 8-Bit Local Bus



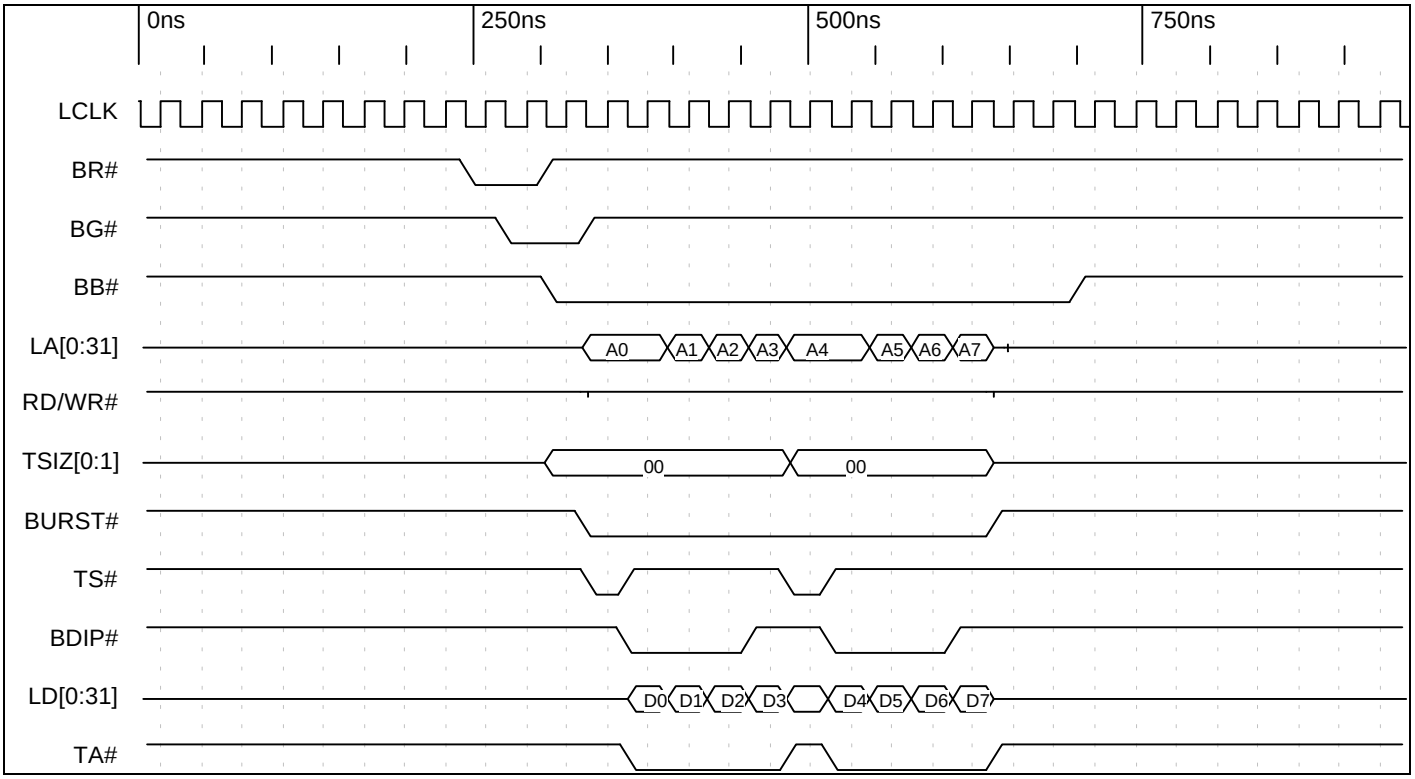
Timing Diagram 3-20. Direct Slave Burst Write Cycle of Four Lwords, Bterm Disabled, Burst Enabled



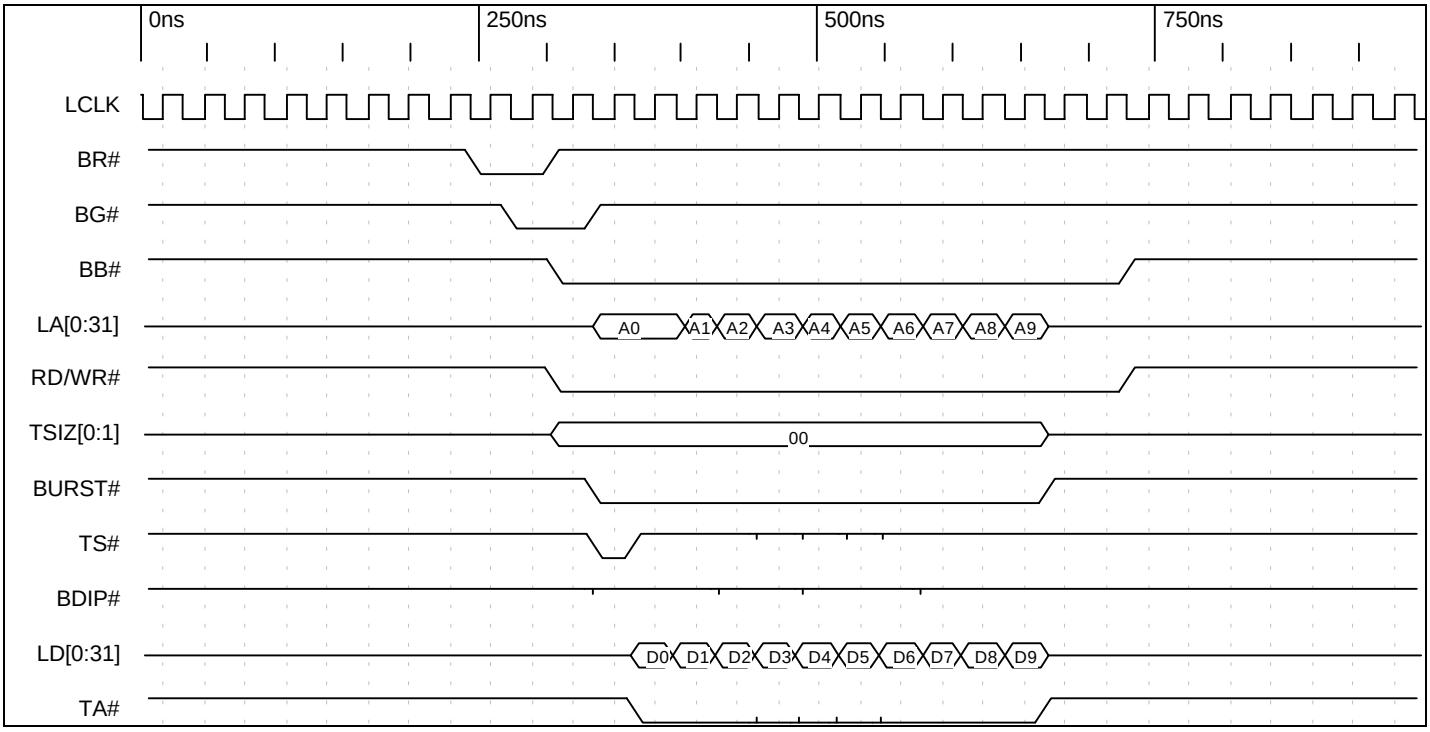
Timing Diagram 3-21. Direct Slave Burst Read Cycle of Four Lwords, Bterm Disabled, Burst Enabled



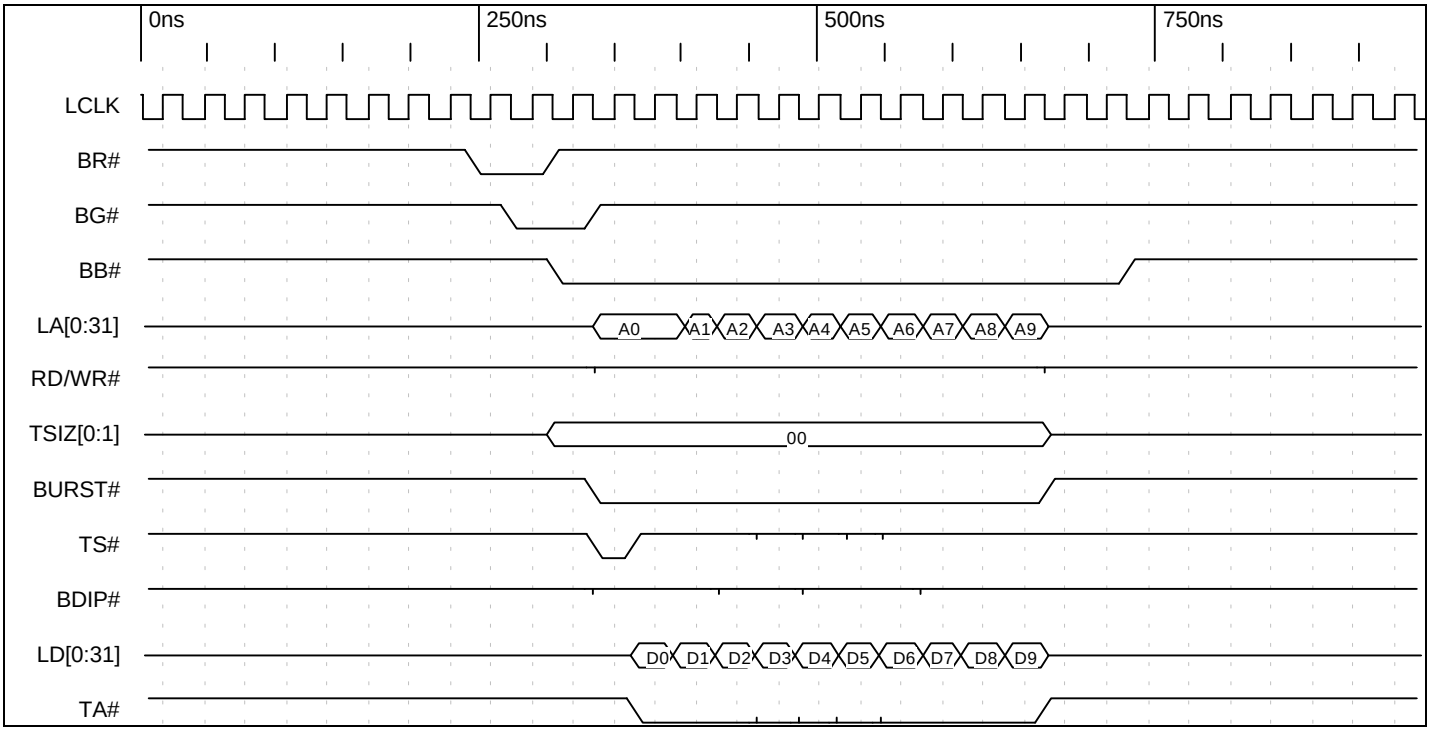
Timing Diagram 3-22. Direct Slave Burst Write Cycle of Eight Lwords, Bterm Disabled, Burst Enabled



Timing Diagram 3-23. Direct Slave Burst Read Cycle of Eight Lwords, Bterm Disabled, Burst Enabled

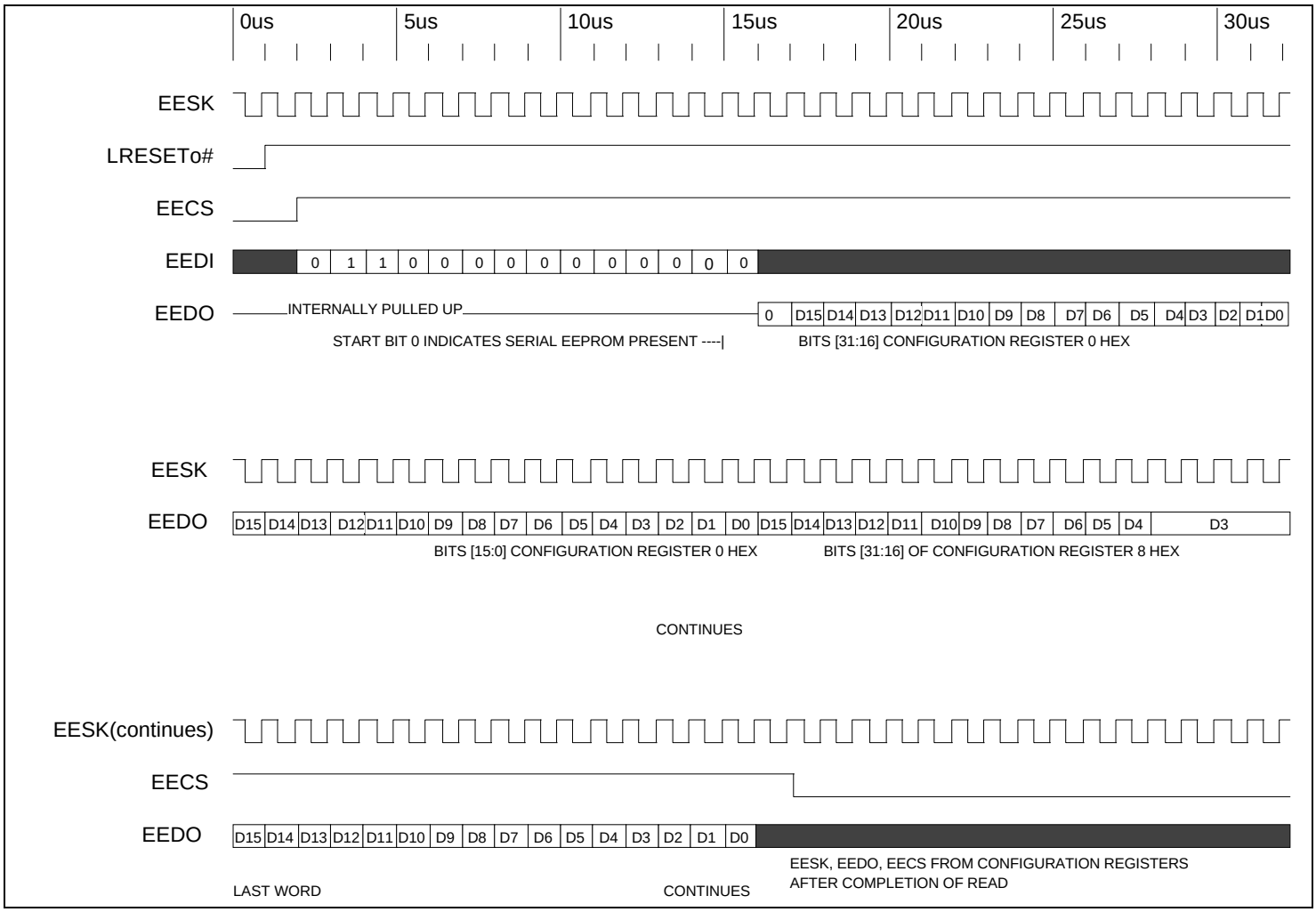


Timing Diagram 3-24. Direct Slave Burst Write Cycle of 10 Lwords, Zero Wait States Beyond MPC860 Protocol, Bterm Enabled, Burst Enabled

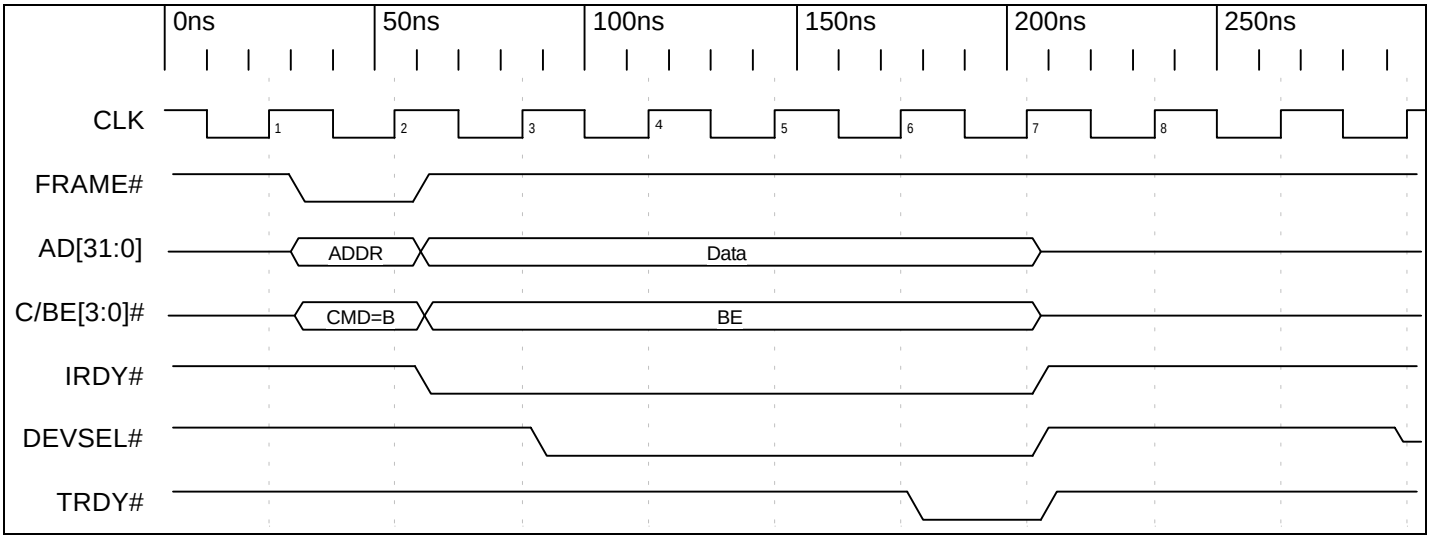


Timing Diagram 3-25. Direct Slave Burst Read Cycle of 10 Lwords, Zero Wait States Beyond MPC860 Protocol, Bterm Enabled, Burst Enabled

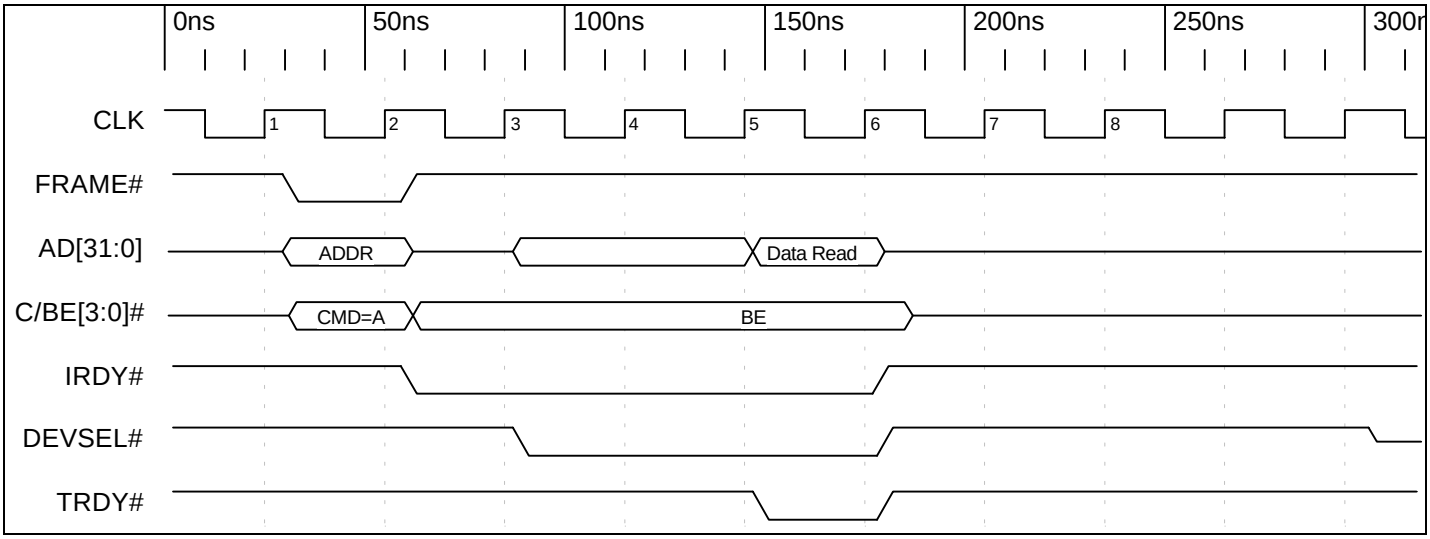
Timing Diagram 3-26. Initialization from Serial EEPROM (2K)



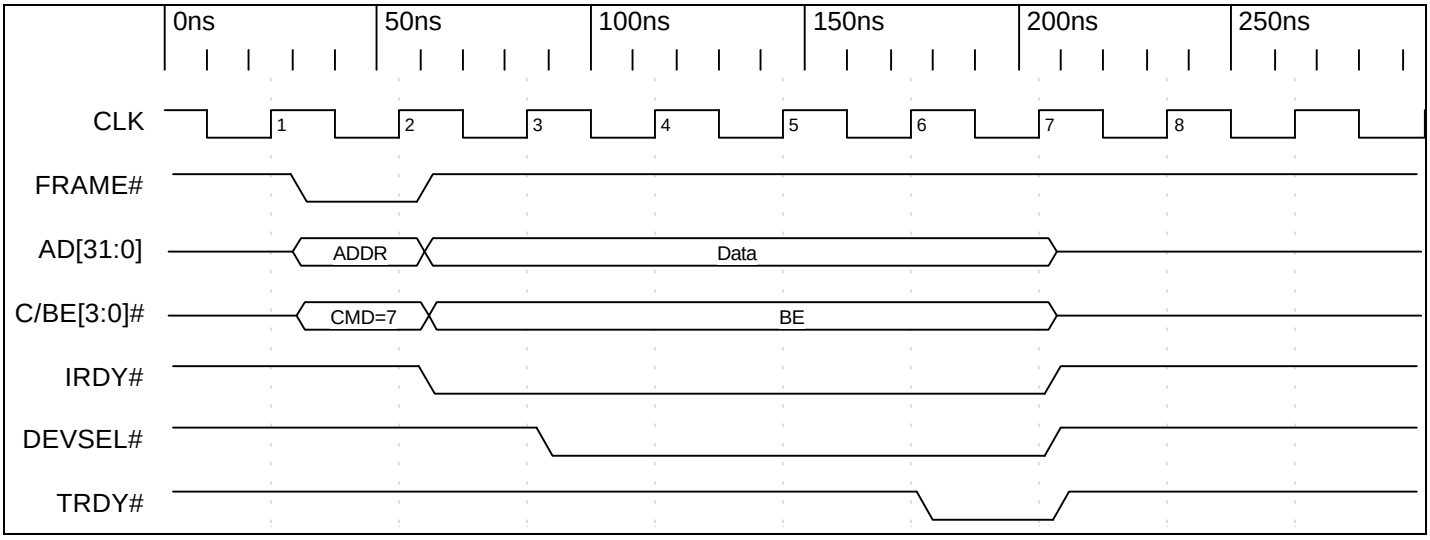
Timing Diagram 3-27. Initialization from Serial EEPROM (4K)



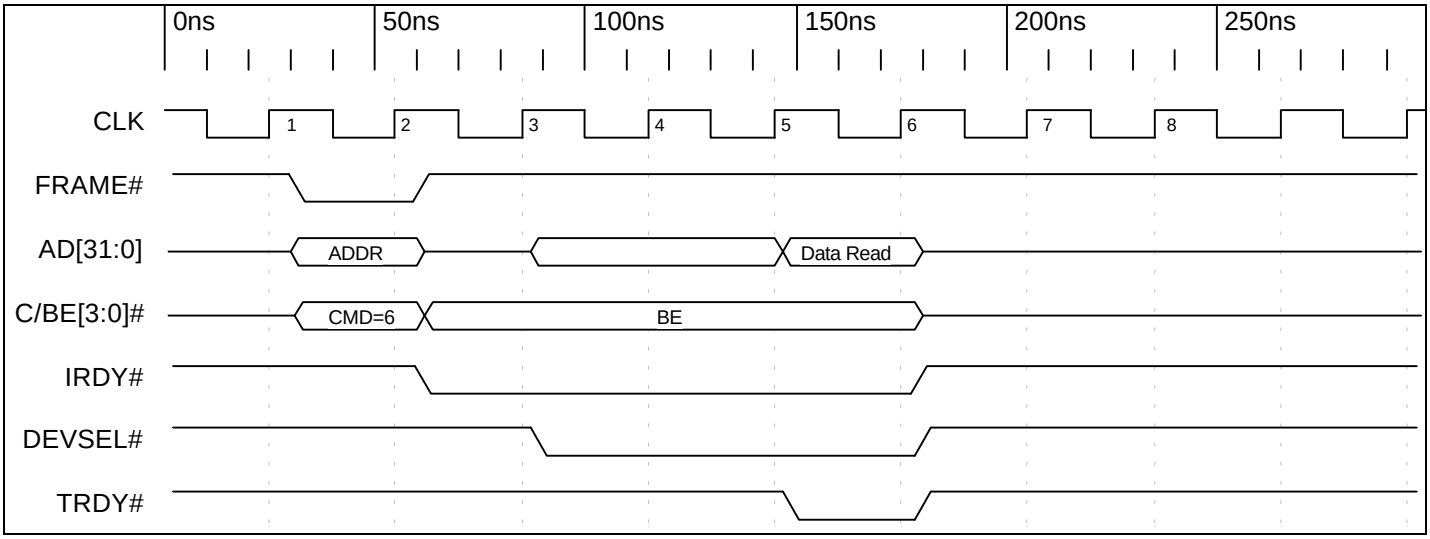
Timing Diagram 3-28. PCI Configuration Write to PCI Configuration Register



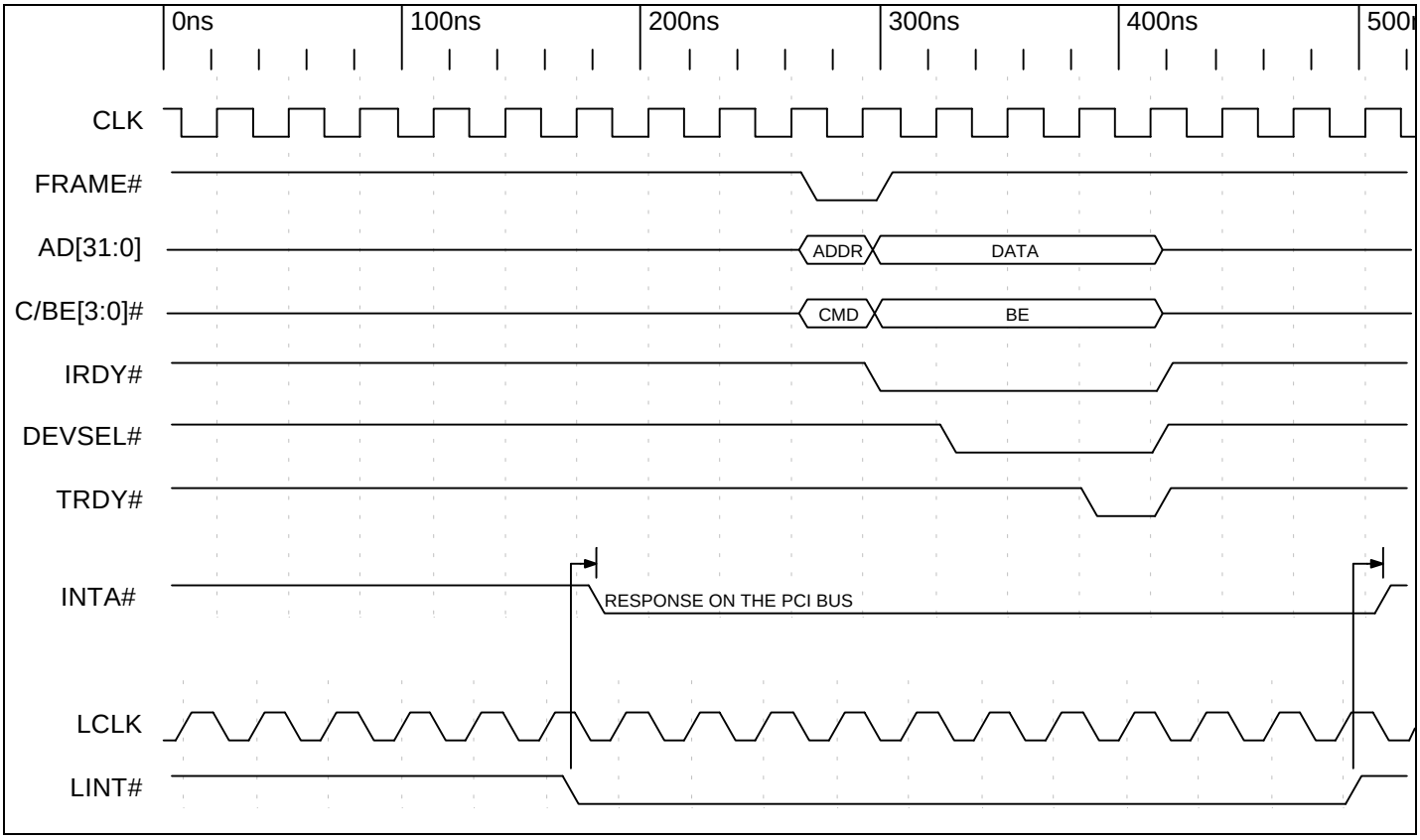
Timing Diagram 3-29. PCI Configuration Read to PCI Configuration Register



Timing Diagram 3-30. PCI Memory Write to Local Configuration Register

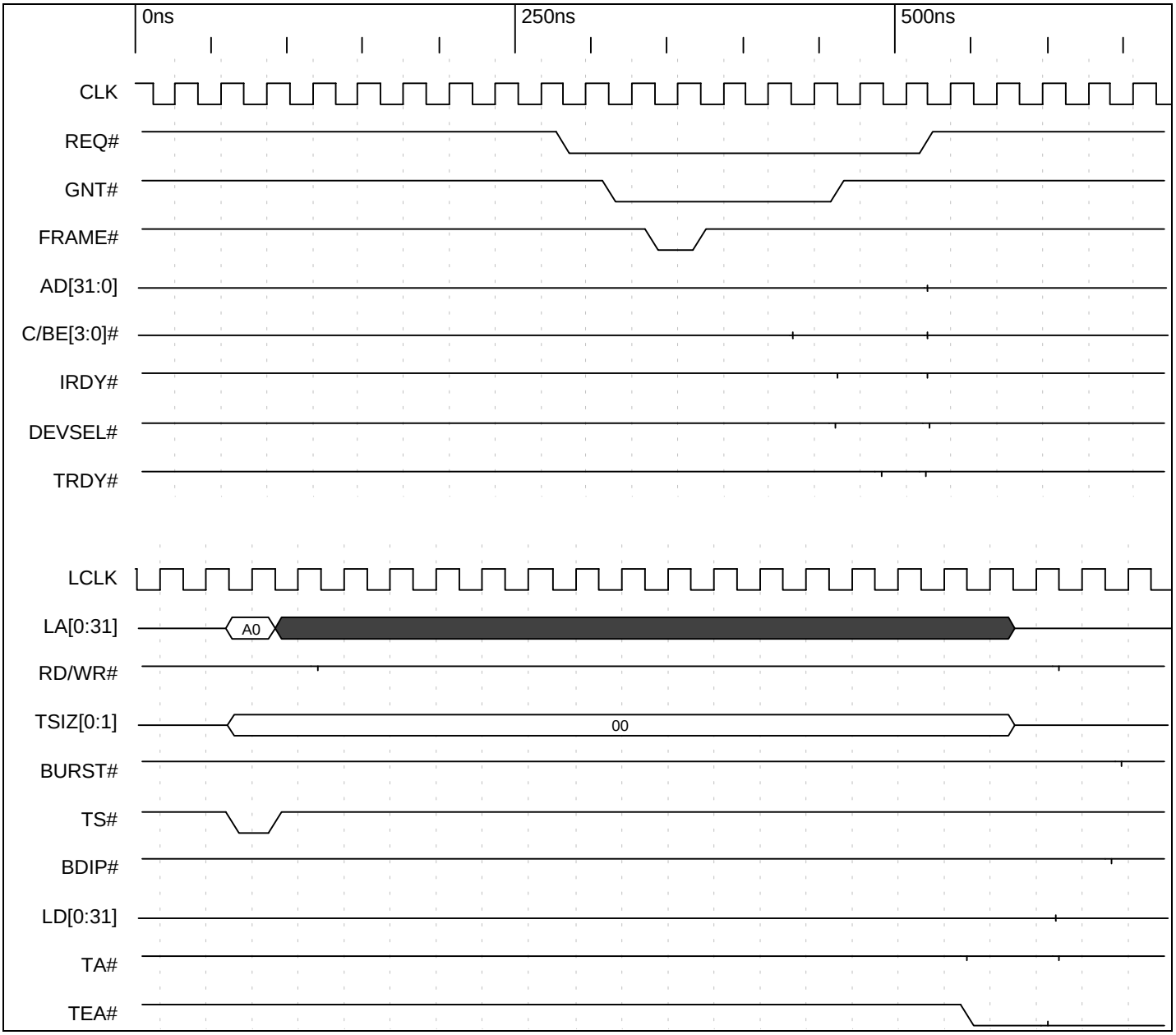


Timing Diagram 3-31. PCI Memory Read to Local Configuration Register

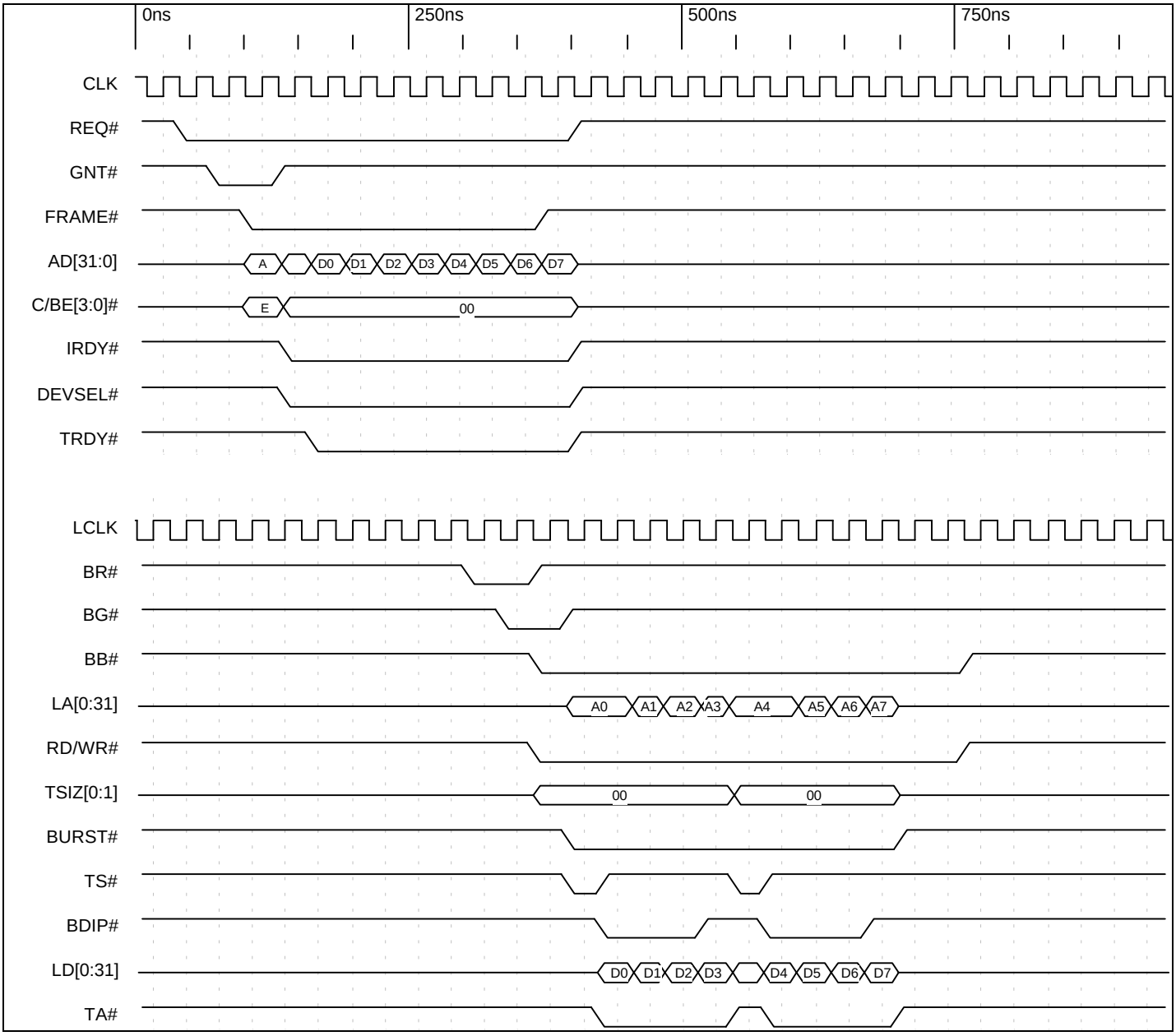


Timing Diagram 3-32. Local Interrupt Asserting PCI Interrupt

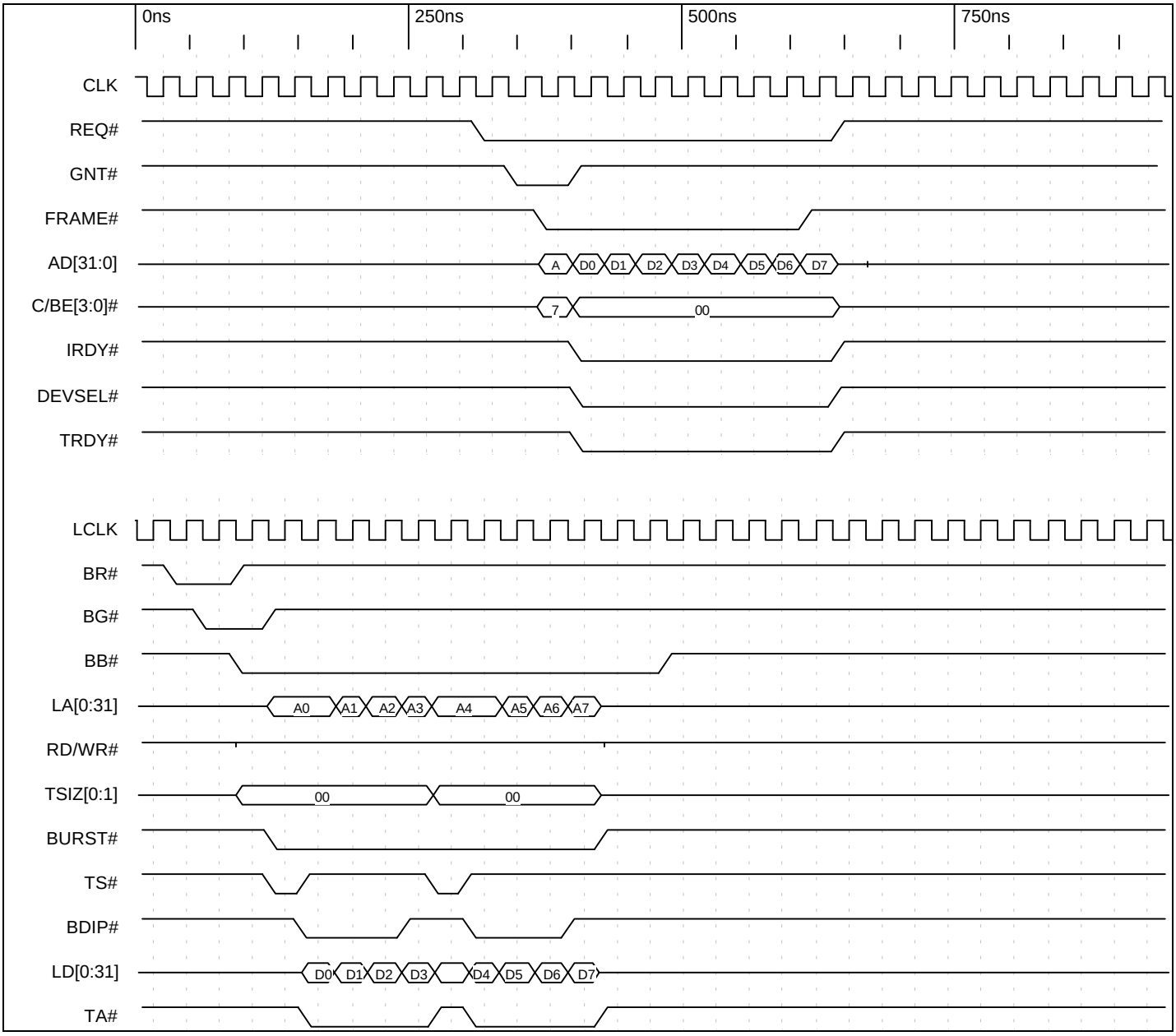
3.6.3 M Mode DMA



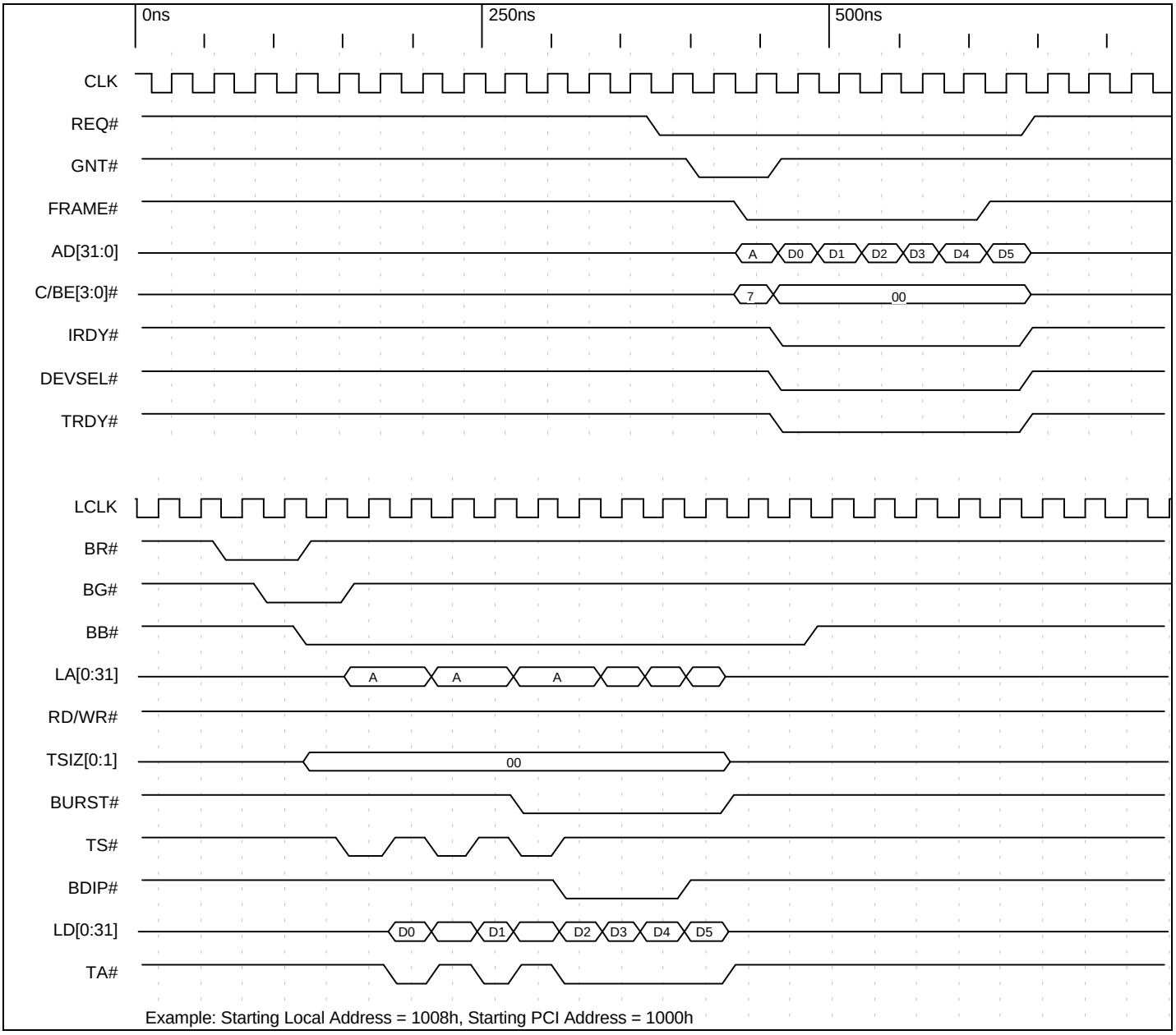
Timing Diagram 3-33. Master Abort Condition During Direct Master Read Cycle Causes TEA#



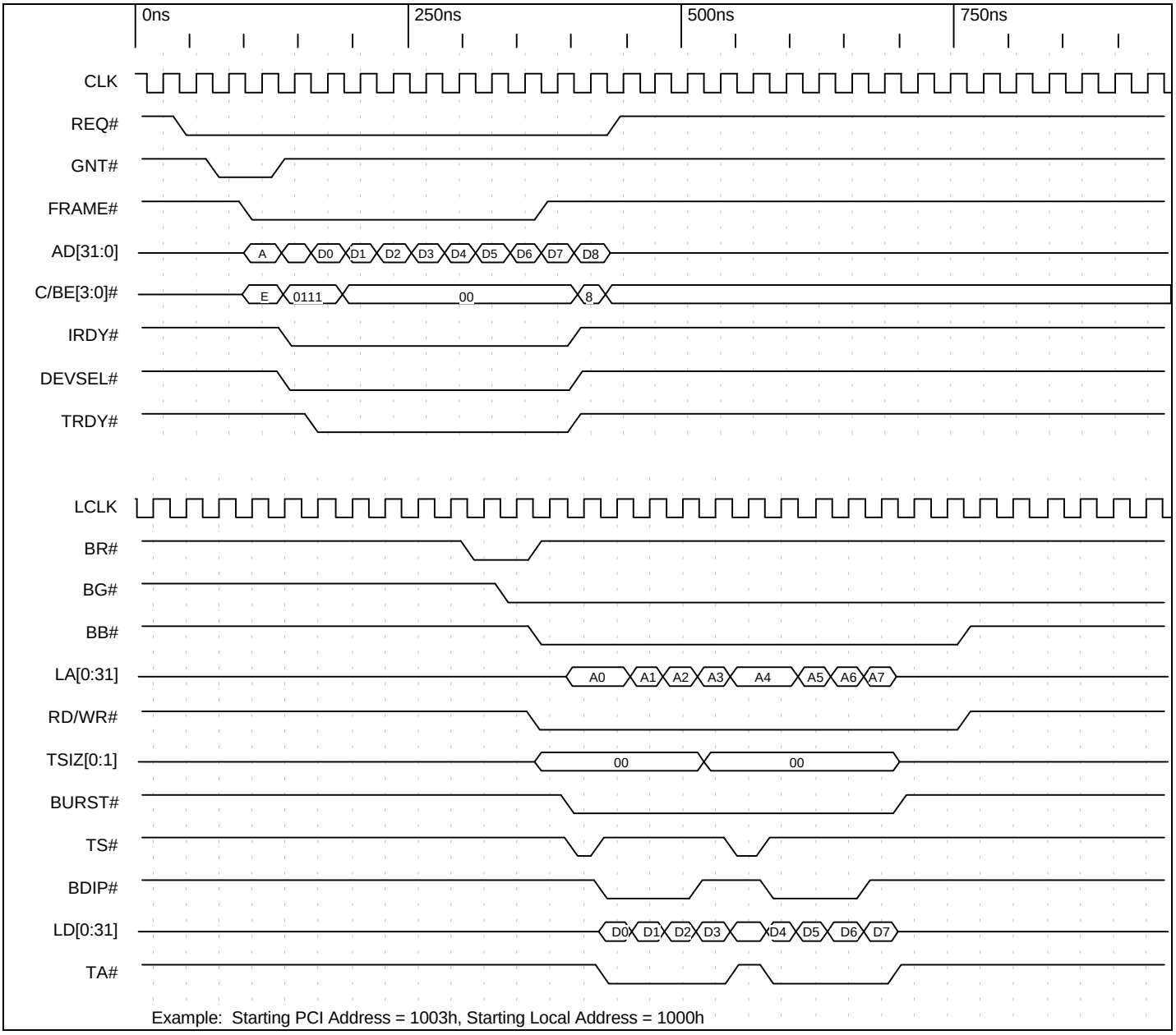
Timing Diagram 3-34. DMA PCI-to-Local, Bterm Disabled, Burst Enabled, Transfer Size = Eight Lwords



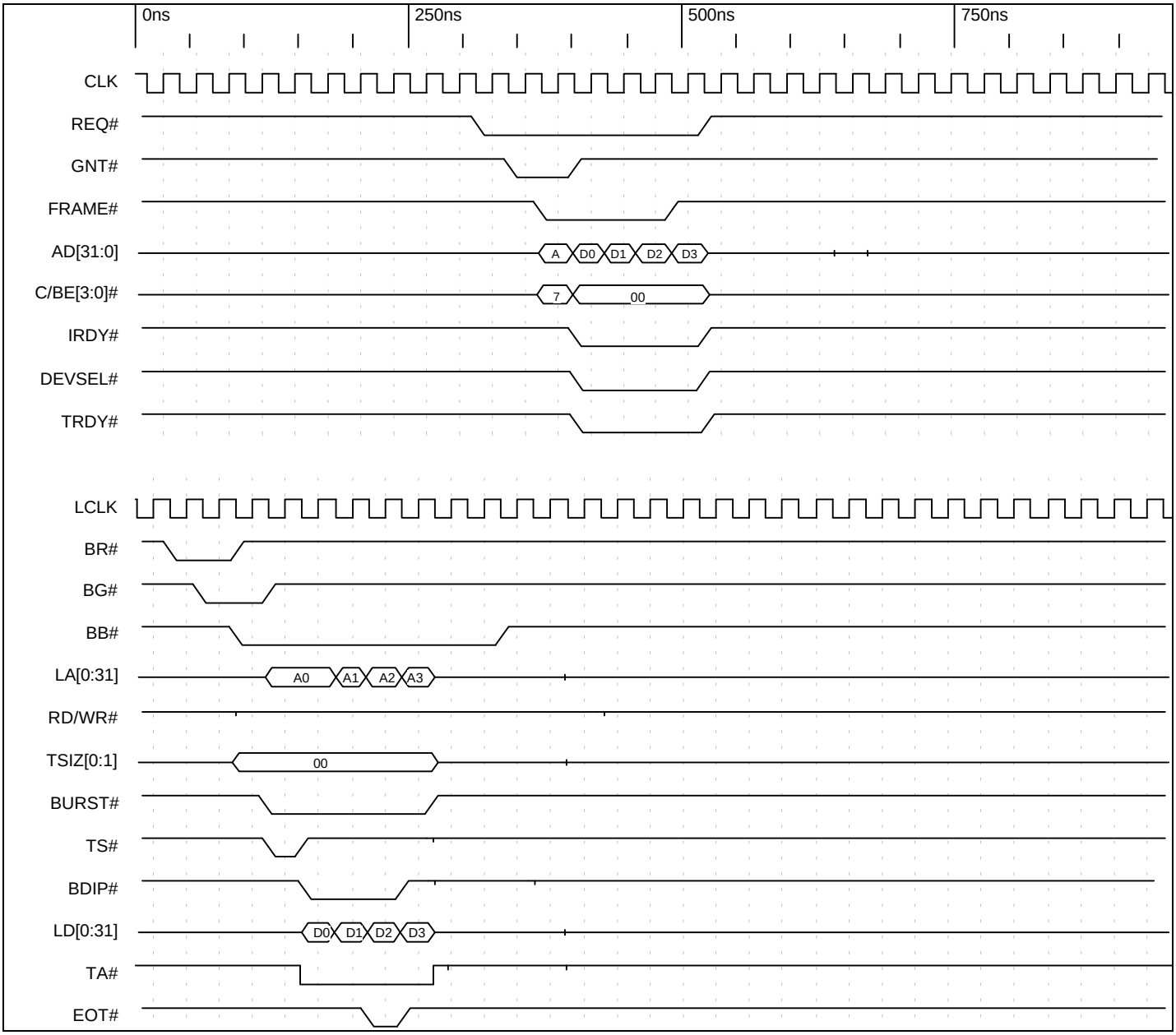
Timing Diagram 3-35. DMA Local-to-PCI, Bterm Disabled, Burst Enabled, Transfer Size = Eight Lwords



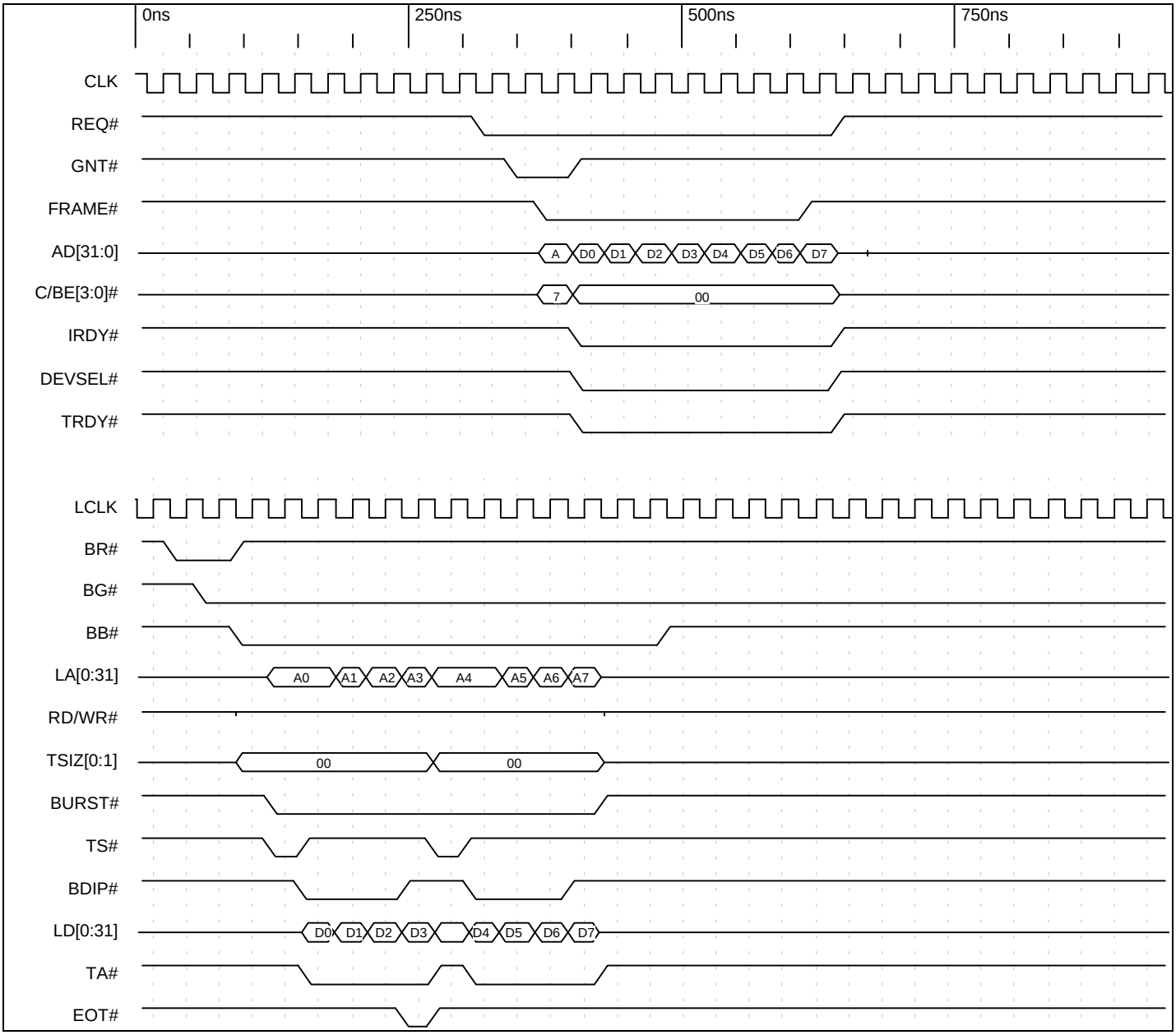
Timing Diagram 3-36. DMA Local-to-PCI, Address Unaligned, Bterm Disabled, Burst Enabled, Transfer Size = Six Lwords



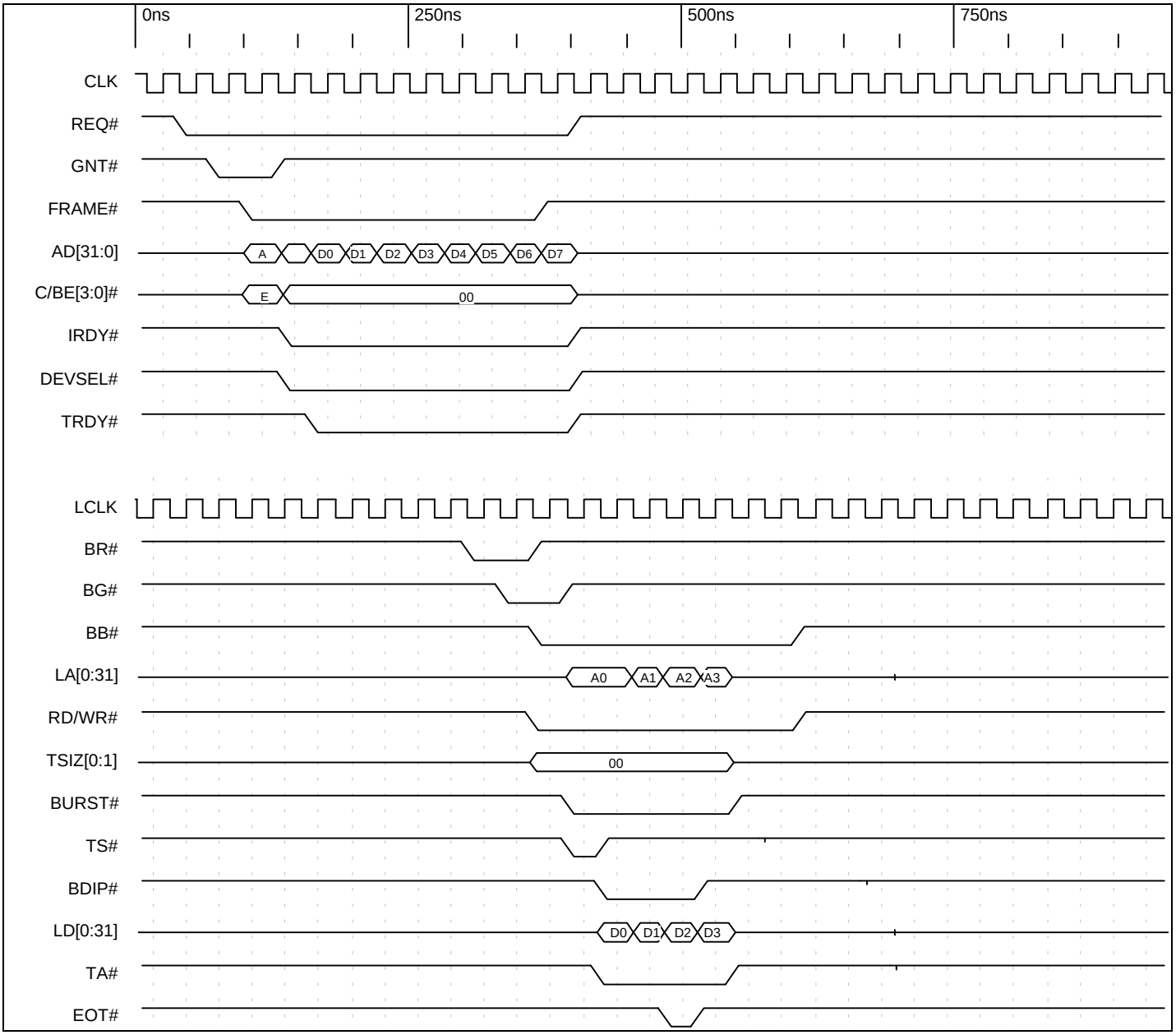
Timing Diagram 3-37. DMA PCI-to-Local, Address Unaligned, Bterm Disabled, Burst Enabled, Transfer Size = Eight Lwords



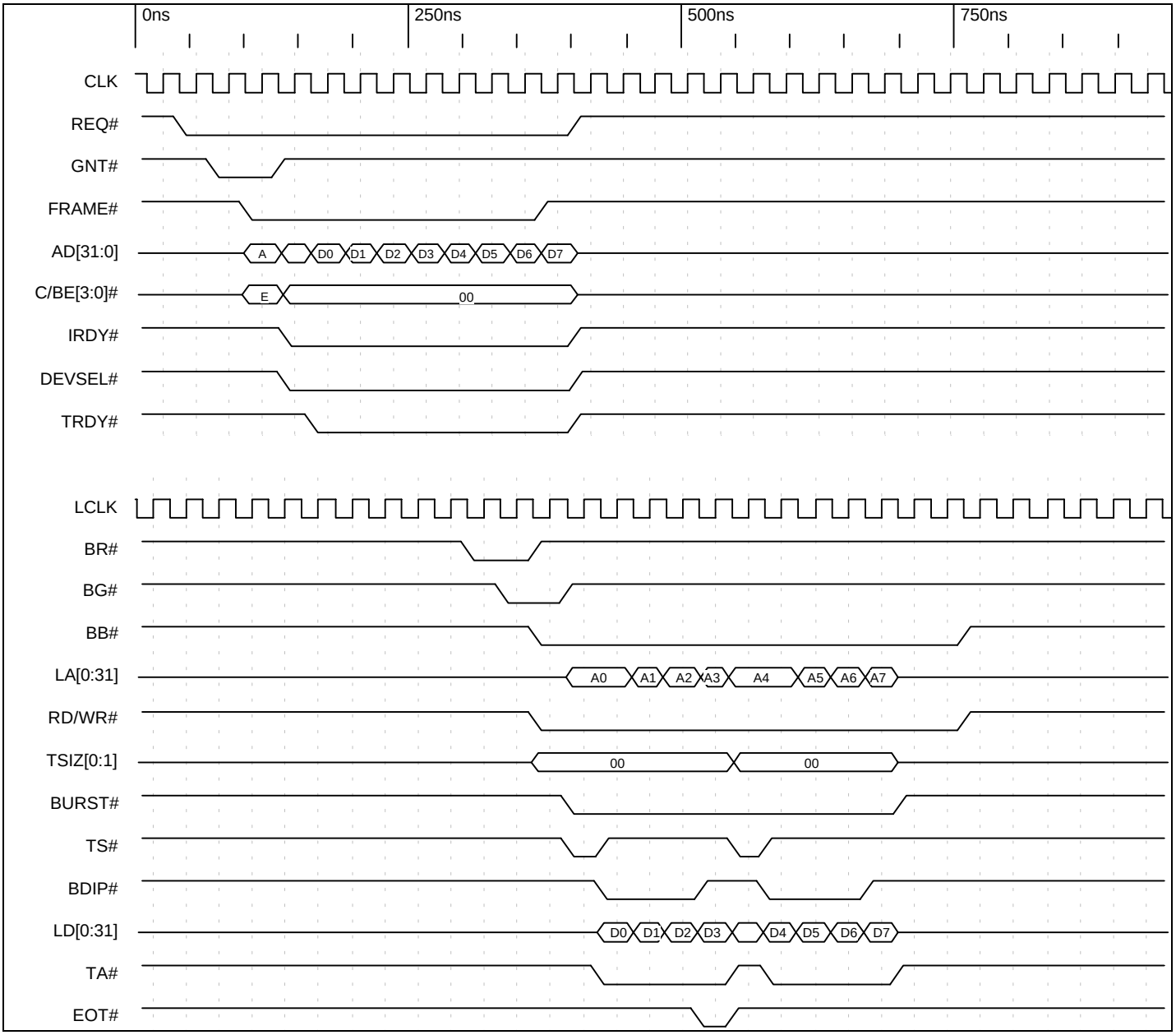
Timing Diagram 3-38. DMA Local-to-PCI, Bterm Disabled, Burst Enabled, Transfer Size = Eight Lwords, EOT# Asserts in the Middle of the Quad-Lword of Data



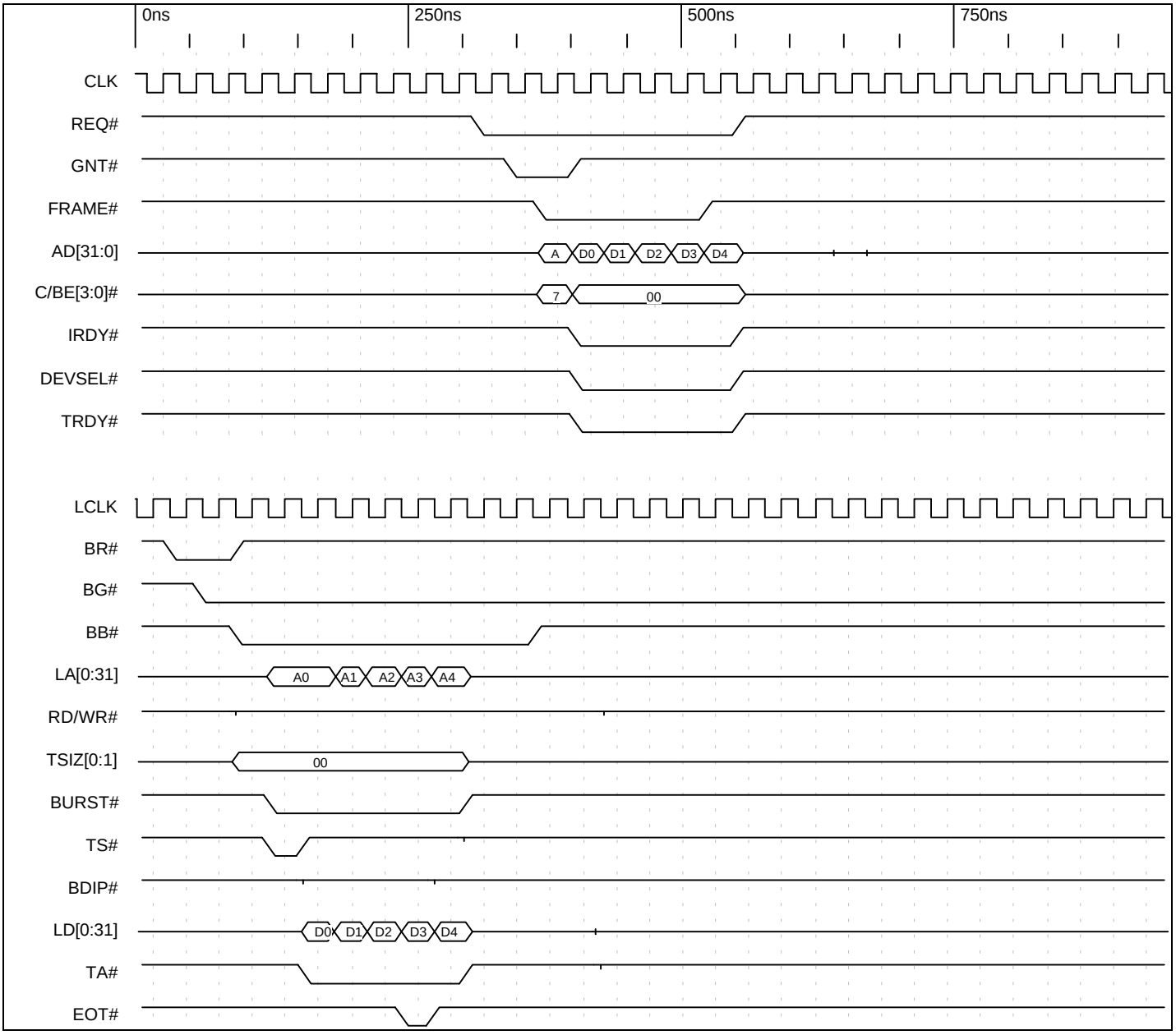
Timing Diagram 3-39. DMA Local-to-PCI, Bterm Disabled, Burst Enabled, Transfer Size = Eight Lwords, EOT# Asserts at the Last Data of the First Quad-Lword



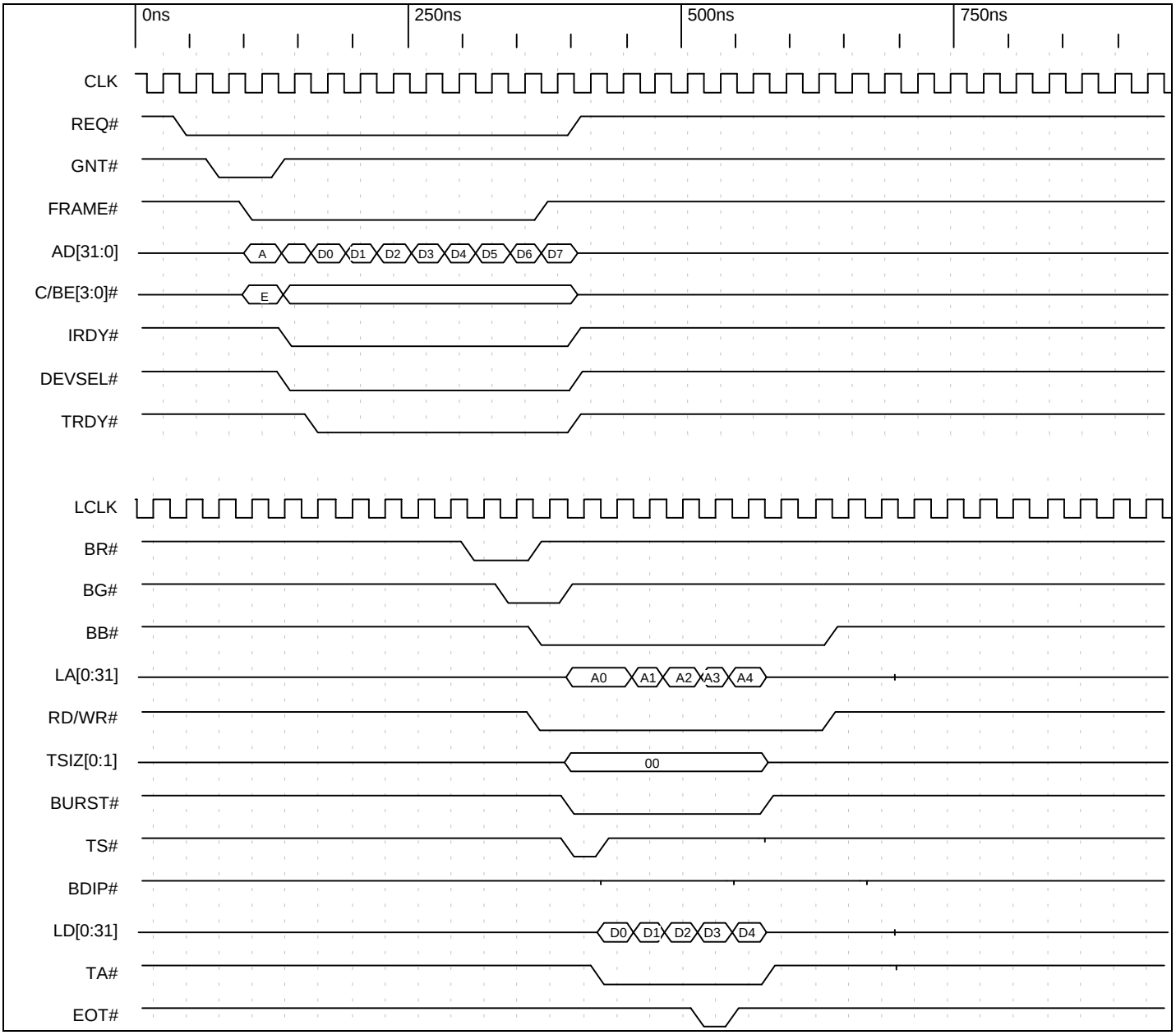
Timing Diagram 3-40. DMA PCI-to-Local, Bterm Disabled, Burst Enabled, Transfer Size = Eight Lwords, EOT# Asserts in the Middle of the First Quad-Lword of Data



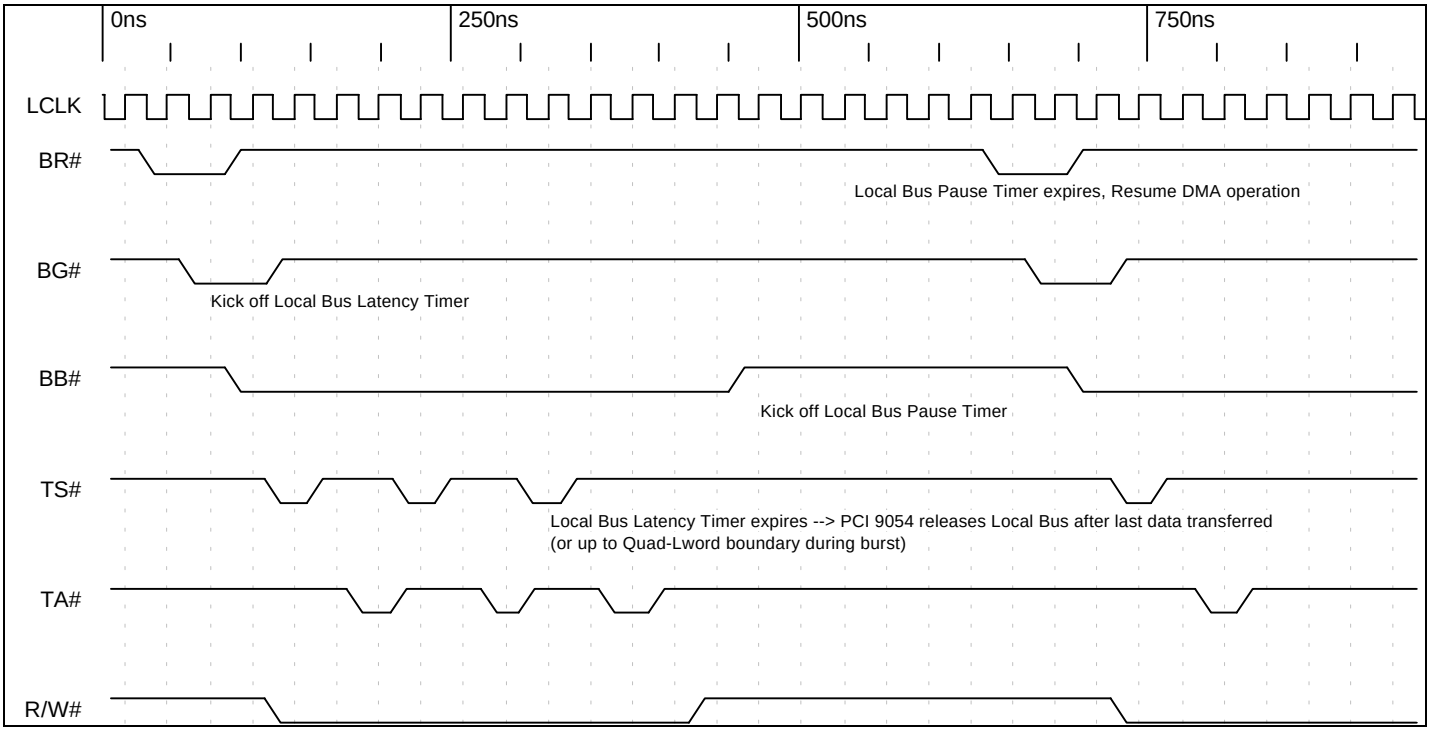
Timing Diagram 3-41. DMA PCI-to-Local, Bterm Disabled, Burst Enabled, Transfer Size = Eight Lwords, EOT# Asserts at the Last Data of the First Quad-Lword



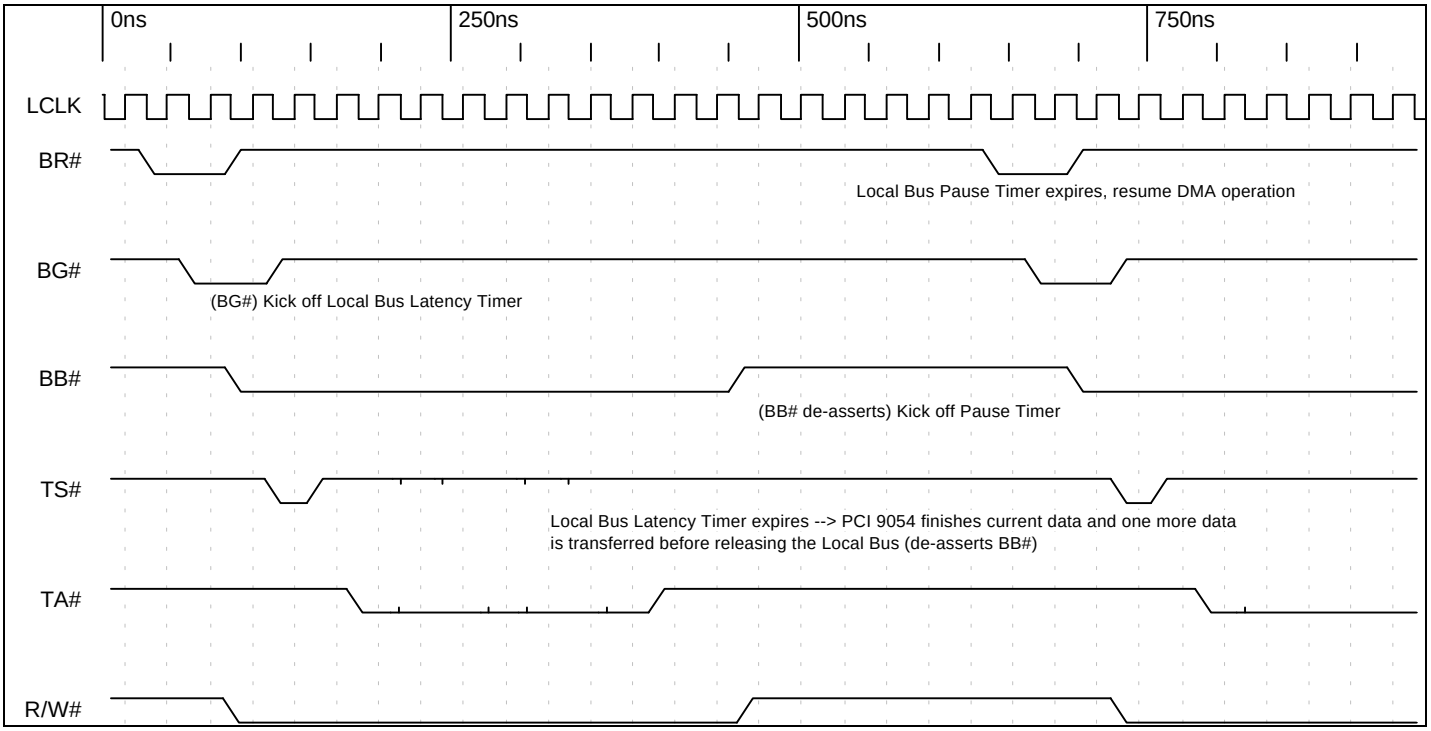
Timing Diagram 3-42. DMA Local-to-PCI, Bterm Enabled, Burst Enabled, Transfer Size = Eight Lwords, EOT# Asserts at the End of the Third Local Data Beyond MPC860 Protocol



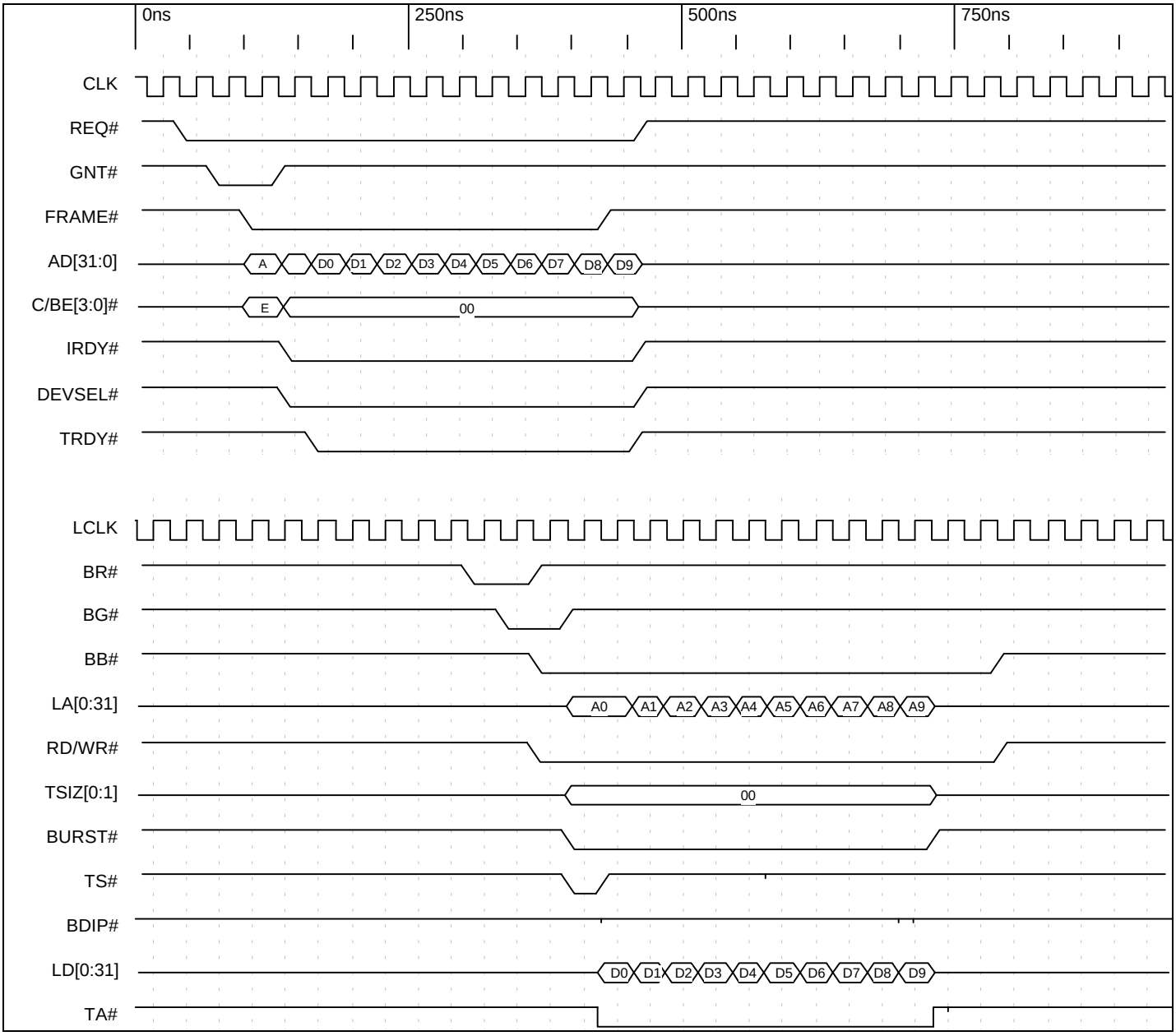
Timing Diagram 3-43. DMA PCI-to-Local, Bterm Enabled, Burst Enabled, Transfer Size = Eight Lwords, EOT# Asserts at the End of the Third Local Data Beyond MPC860 Protocol



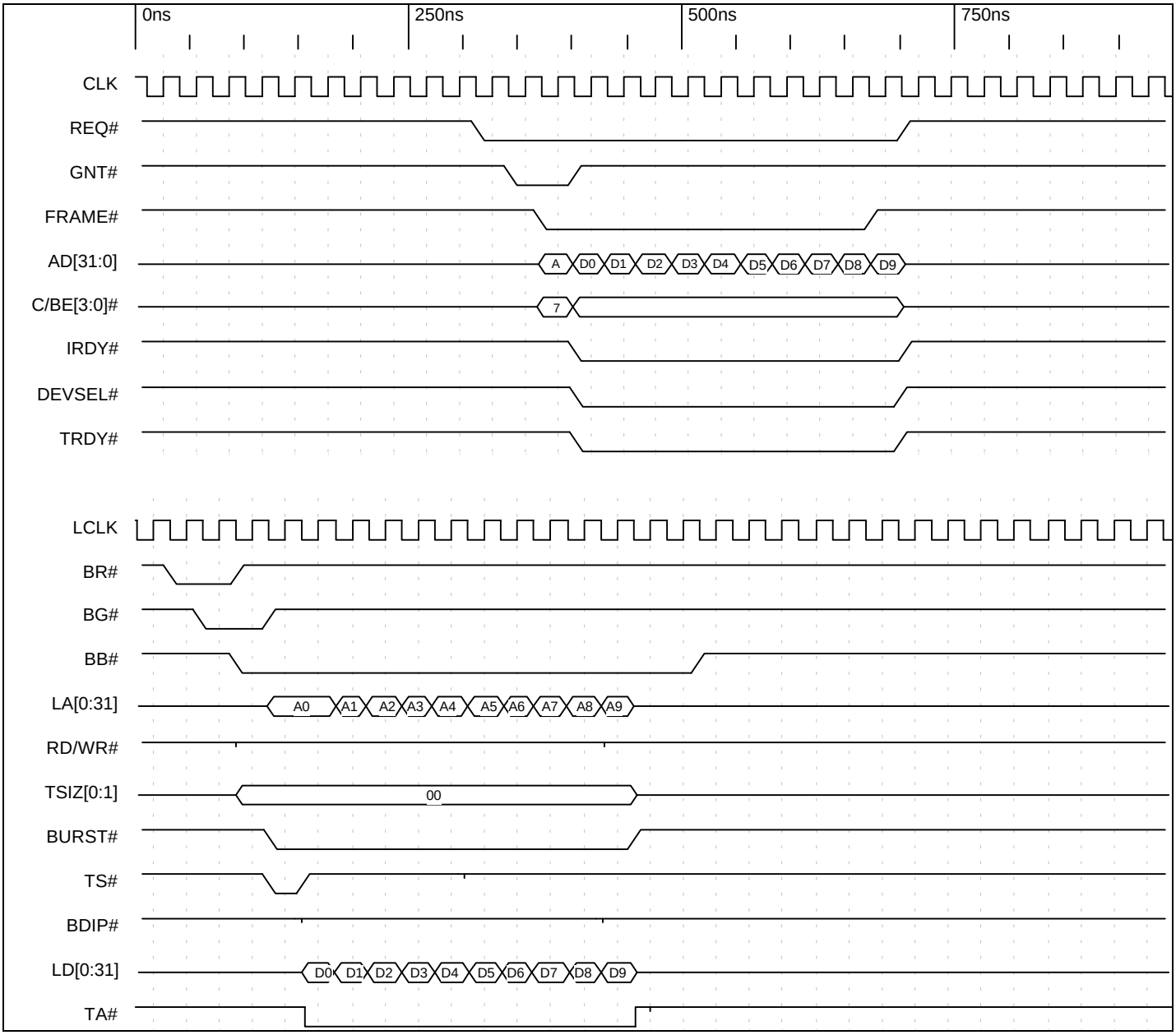
Timing Diagram 3-44. Local Bus Latency Timer (Eight Clocks) and Pause Timer (Four Clocks) in DMA Operation



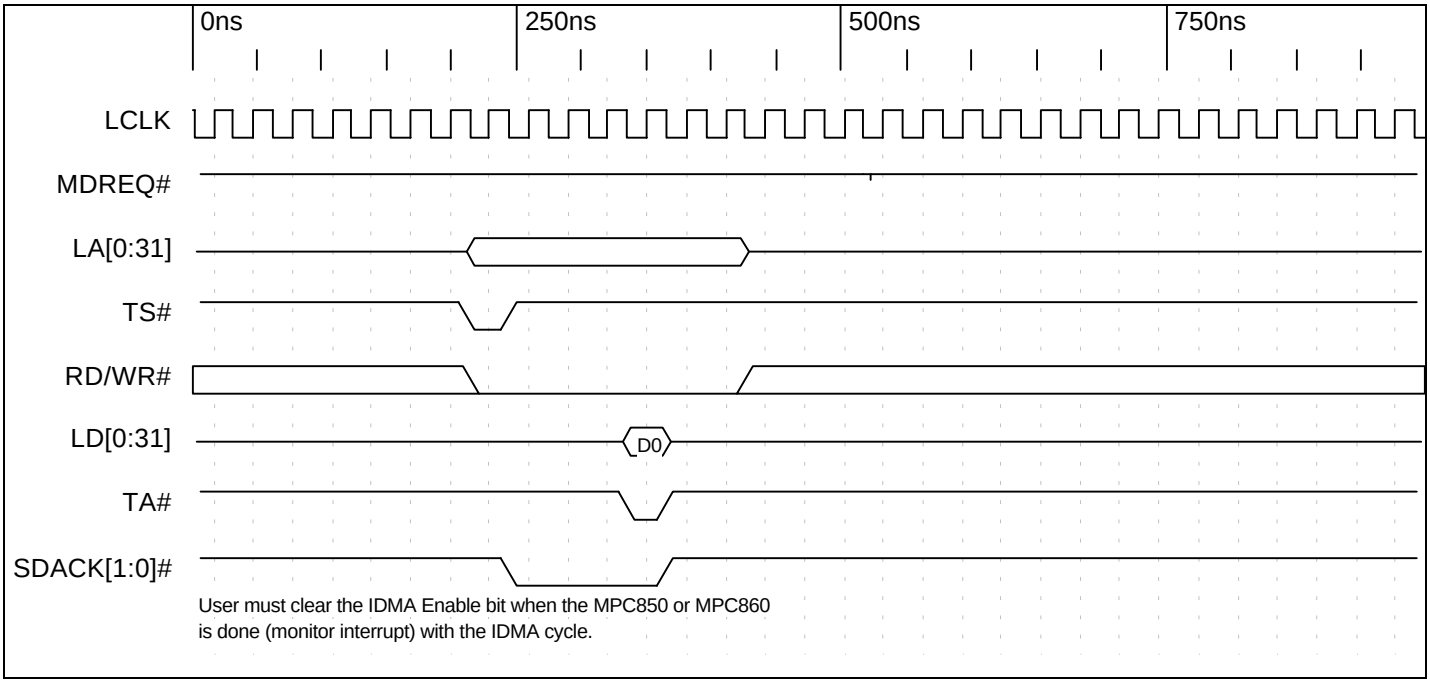
Timing Diagram 3-45. Local Bus Latency Timer (Eight Clocks) and Pause Timer (Four Clocks) in DMA Operation Beyond MPC860 Protocol



Timing Diagram 3-46. DMA PCI-to-Local, Bterm Enabled, Burst Enabled, Transfer Size = 10 Lwords, Beyond MPC860 Protocol



Timing Diagram 3-47. DMA Local-to-PCI, Bterm Enabled, Burst Enabled, Transfer Size = 10 Lwords, Beyond MPC860 Protocol



Timing Diagram 3-48. IDMA Single Write Cycle

Notes: *The PCI 9054 treats the IDMA function from the MPC850 or MPC860 the same as a Direct Master cycle.*

The MPC850 or MPC860 starts IDMA cycle when the IDMA Enable bit is set in the MPC850 or MPC860 respective register.

The PCI 9054 does not look at SDACK[1:0]# because the pins do not exist in the PCI 9054 (not connected).

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4. C AND J MODES BUS OPERATION

4.1 PCI Bus Cycles

The PCI 9054 is compliant with PCI Specification v2.2. Refer to PCI Specification v2.2 for specific PCI Bus functions.

4.1.1 PCI Target Command Codes

As a Target, the PCI 9054 allows access to the PCI 9054 internal registers and the Local Bus, using the commands listed in Table 4-1.

All Read or Write accesses to the PCI 9054 can be Byte, Word, or Lword (longword) accesses, defined as 32 bit. All memory commands are aliased to basic memory commands. All I/O accesses to the PCI 9054 are decoded to an Lword boundary. Byte enables are used to determine which bytes are read or written. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

Table 4-1. PCI Target Command Codes

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)
Memory Read Multiple	1100 (Ch)
PCI Dual Address Cycle	1101 (Dh)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

4.1.2 PCI Master Command Codes

The PCI 9054 can access the PCI Bus to perform DMA or Direct Master Local-to-PCI Bus transfers. During a Direct Master or DMA transfer, the command code assigned to the PCI 9054 internal register location (CNTRL[15:0]) is used as the PCI command code (except for Memory Write and Invalidate mode for DMA cycles where (DMPBAM[9]=1). Table 4-2 through Table 4-5 list various PCI Master Command codes.

Notes: *Programmable internal registers determine PCI command codes when the PCI 9054 is the Master.*

DMA cannot perform I/O or configuration accesses.

4.1.2.1 DMA Master Command Codes

DMA controllers of the PCI 9054 can assert the Memory cycles listed in Table 4-2.

Table 4-2. DMA Master Command Codes

Command Type	Code (C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
PCI Dual Address Cycle	1101 (Dh)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

4.1.2.2 Direct Local-to-PCI Command Codes

For direct Local-to-PCI Bus accesses, the PCI 9054 asserts the cycles listed in Table 4-3 through Table 4-5.

Table 4-3. Local-to-PCI Memory Access

Command Type	Code (C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
PCI Dual Address Cycle	1101 (Dh)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

Table 4-4. Local-to-PCI I/O Access

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)

Table 4-5. Local-to-PCI Configuration Access

Command Type	Code (C/BE[3:0]#)
Configuration Memory Read	1010 (Ah)
Configuration Memory Write	1011 (Bh)

4.1.3 PCI Arbitration

The PCI 9054 asserts REQ# to request the PCI Bus. The PCI 9054 can be programmed using the PCI Request Mode bit (MARBR[23]) to de-assert REQ# when it asserts FRAME# during a Bus Master cycle, or to keep REQ# asserted for the entire Bus Master cycle. The PCI 9054 always de-asserts REQ# for a minimum of two PCI clocks between Bus Master ownership that includes a Target disconnect.

The Direct Master Write Delay bits (DMPBAM[15:14]) can be programmed to delay the PCI 9054 from asserting PCI REQ# during a Direct Master Write cycle. DMPBAM can be programmed to wait 0, 4, 8, or 16 PCI Bus clocks after the PCI 9054 has received its first Write data from the Local Bus Master and is ready to begin the PCI Write transaction. This function is useful in applications where a Local Master is bursting and a Local Bus clock is slower than the PCI Bus clock. This allows Write data to accumulate in the PCI 9054 Direct Master Write FIFO, which provides for better use of the PCI Bus.

4.2 Local Bus Cycles

The PCI 9054 interfaces a PCI Host bus to several Local Bus types, as listed in Table 4-6 and Table 4-7. It operates in one of three modes, selected through MODE[1:0] (PQFP—Pins 157 and 156; PBGA—Pins B7 and E8), corresponding to three bus types—M, J, and C.

Table 4-6. Local Bus Types (176-Pin PQFP)

Pin 157	Pin 156	Mode	Bus Type
1	1	M	32-bit non-multiplexed
1	0	Reserved	—
0	1	J	32-bit multiplexed
0	0	C	32-bit non-multiplexed

Table 4-7. Local Bus Types (225-Pin PBGA)

Pin B7	Pin E8	Bus Mode	Bus Type
1	1	M	32-bit non-multiplexed
1	0	Reserved	—
0	1	J	32-bit multiplexed
0	0	C	32-bit non-multiplexed

4.2.1 Local Bus Arbitration

The PCI 9054 asserts LHOLD to request the Local Bus. It owns the Local Bus when LHOLD is asserted. When the PCI 9054 acknowledges BREQi asserted during DMA or Direct Slave Write transfers, it releases the Local Bus within two Lword transfers by de-asserting LHOLD and floating the Local Bus outputs if either of the following conditions exist:

- BREQi is asserted and enabled
- Gating is enabled and the Local Bus Latency Timer is enabled and expires (MARBR[27, 7:0])

The Local Arbiter can now grant the Local Bus to another Local Master. After the PCI 9054 acknowledges that LHOLDA is de-asserted and the Local Bus Pause Timer is zero, it re-asserts LHOLD to request the Local Bus. When the PCI 9054 receives LHOLDA, it drives the bus and continues the transfer.

Note: *The Local Bus Pause Timer applies only to DMA operation. It does **not** apply to Direct Slave operation.*

4.2.2 Direct Master

Local Bus cycles can be Single or Burst cycles. The BLAST# signal is used to determine if a Single or Burst cycle is to be performed. If BLAST# is asserted at the beginning of the first Data phase, on which the PCI 9054 performs a Single PCI Bus cycle. Otherwise, the PCI 9054 performs a Burst PCI Bus cycle and BLAST# is used to end the cycle. As a Local Bus Target, the PCI 9054 allows access to the PCI 9054 internal registers and the PCI Bus.

Local Bus Direct Master accesses to the PCI 9054 must be for a 32-bit nonpipelined bus.

4.2.3 Direct Slave

The PCI Bus Master reads from and writes to the Local Bus (the PCI 9054 is a PCI Bus Target and a Local Bus Master).

4.2.4 Wait State Control

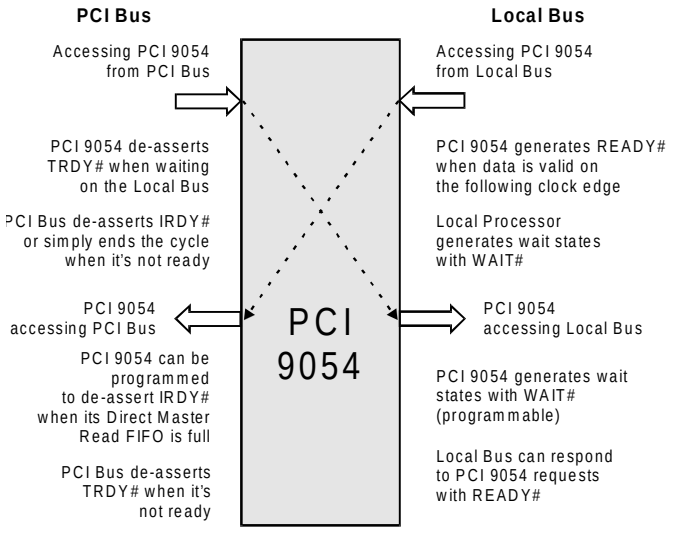


Figure 4-1. Wait States

Note: *The figure represents a sequence of Bus cycles.*

If READY# mode is disabled, the external READY# input signal has no effect on wait states for a Local access. Wait states between Data cycles are asserted internally by a wait state counter. The wait state counter is initialized with its Configuration register value at the start of each data access.

If READY# mode is enabled, it has no effect until the wait state counter reaches 0. READY# then controls the number of additional wait states.

BTERM# input is not sampled until the wait state counter reaches 0. BTERM# overrides READY# when BTERM# is enabled and asserted.

4.2.4.1 Wait States—Local Bus

In Direct Master mode and when accessing the PCI 9054 registers, the PCI 9054 acts as a Local Bus Slave. The PCI 9054 asserts wait states by delaying the READY# signal. The Local processor asserts wait states with the WAIT# signal.

In Direct Slave and DMA modes, the PCI 9054 acts as a Local Bus Master. The PCI 9054 inserts internal wait states with the WAIT# signal. The Local processor asserts external wait states by delaying the READY# signal.

The Internal Wait State bit(s) (LBRD0[21:18, 5:2], (LBRD1[5:2]), DMAMODE0[5:2], and/or DMAMODE1 [5:2]) can be used to program the number of internal wait states between the first address-to-data (and subsequent data-to-data in Burst mode).

During Direct Master accesses, WAIT# signal must be asserted during the ADS phase for the PCI 9054 to sample the wait state phase.

4.2.4.2 Wait States—PCI Bus

The PCI Bus Master throttles IRDY# and the PCI Bus Slave throttles TRDY# to assert PCI Bus wait state(s).

4.2.5 Burst Mode and Continuous Burst Mode (Bterm "Burst Terminate" Mode)

Note: *In the following sections, Bterm refers to the PCI 9054 internal register bit and BTERM# refers to the PCI 9054 external signal.*

4.2.5.1 Burst and Bterm Modes

Table 4-8. Burst and Bterm on the Local Bus

Mode	Burst	Bterm	Result
Single Cycle	0	0	One ADS# per data (default).
Single Cycle	0	1	One ADS# per data.
Burst-4	1	0	One ADS# per four data (recommended for i960 and PPC401 family).
Burst Forever	1	1	One ADS# per BTERM# (refer to Section 4.2.5.2.1).

On the Local Bus, BLAST# and BTERM# perform the following:

- If the Burst Mode bit is enabled, but the Bterm Mode bit is disabled, then the PCI 9054 bursts (up to a quad word boundary) four Lwords. BLAST# is asserted at the beginning of the fourth Lword Data phase (LA[3:2]=11) and a new ADS# is asserted at the first Lword (LA[3:2]=00) of the next burst.
- If BTERM# is enabled and asserted, the PCI 9054 terminates the Burst cycle of the end of the current Data phase without generating BLAST#. The PCI 9054 generates a new burst transfer starting with a new ADS#, terminating it normally using BLAST#.
- BTERM# input is valid only when the PCI 9054 is Master of the Local Bus (Direct Slave or DMA modes).

- As an input, BTERM# is asserted by external logic. It instructs the PCI 9054 to break up a Burst cycle.
- BTERM# is used to indicate a memory access is crossing a page boundary or requires a new Address cycle.

Notes: *If Address Increment is disabled, the DMA transfer bursts beyond four Lwords.*

If the Bterm Mode bit is disabled, the PCI 9054 performs the following:

- ***32-bit Local Bus****—Bursts up to four Lwords*
- ***16-bit Local Bus****—Bursts up to two Lwords*
- ***8-bit Local Bus****—Bursts up to one Lword*

In every case, it performs four transactions.

4.2.5.2 Burst-4 Lword Mode

If the Burst Mode bit is enabled and the Bterm Mode bit is disabled, bursting can start on any Lword boundary and continue up to a 16-byte address boundary. After data up to the boundary is transferred, the PCI 9054 asserts a new Address cycle (ADS#).

Table 4-9. Burst-4 Lword Mode

Bus Width	Burst
32 bit	Four Lwords or up to a quad Lword boundary (LA3, LA2 = 11)
16 bit	Four words or up to a quad word boundary (LA2, LA1 = 11)
8 bit	Four bytes or up to a quad byte boundary (LA1, LA0 = 11)

4.2.5.2.1 Continuous Burst Mode (Bterm "Burst Terminate" Mode)

If both the Burst and Bterm Mode bits are enabled, the PCI 9054 can operate beyond the Burst-4 Lword mode.

Bterm mode enables PCI 9054 to perform long bursts to devices that can accept bursts of longer than four Lwords. The PCI 9054 asserts one Address cycle and continues to burst data. If a device requires a new Address cycle (ADS#), it can assert BTERM# input to cause the PCI 9054 to assert a new Address cycle. BTERM# input acknowledges current Data transfer and requests that a new Address cycle be asserted (ADS#). The new address is for the next Data transfer. If the Bterm Mode bit is enabled and the BTERM# signal is asserted, the PCI 9054 asserts BLAST# only if its Read FIFO is full, its Write FIFO is empty, or if a transfer is complete.

4.2.5.3 Partial Lword Accesses

Lword accesses in which not all byte enables asserted will be broken into Single-Cycle accesses. Burst start addresses can be any Lword boundary. If the Burst Start Address in a Direct Slave or DMA transfer is not aligned to an Lword boundary, the PCI 9054 first performs a Single cycle. It then starts to burst on the Lword boundary if there is remaining data that is not a whole Lword during DMA (*for example*, it will result in a Single cycle at the end).

4.2.6 Recovery States (J Mode Only)

In J mode, the PCI 9054 inserts one recovery state between the last Data transfer and the next Address cycle.

Note: *The PCI 9054 does not support the i960J function that uses READY# input to add recovery states. No additional recovery states are added if READY# input remains asserted during the last Data cycle.*

4.2.7 Local Bus Read Accesses

For all Single-Cycle Local Bus Read accesses, the PCI 9054 reads only bytes corresponding to byte enables requested by the PCI Initiator. For all Burst Read cycles, the PCI 9054 can be programmed to

- Prefetch
- Perform Read Ahead mode
- Generate internal wait states
- Enable external wait control (READY# input)
- Enable type of Burst mode to perform

4.2.8 Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Bus Master or the PCI 9054 DMA controller are written.

4.2.9 Direct Slave Accesses to 8- or 16-Bit Local Bus

Direct PCI access to an 8- or 16-bit Local Bus results in the PCI Bus Lword being broken into multiple Local Bus transfers. For each transfer, byte enables are encoded as in the i960C to provide Local Address bits LA[1:0].

4.2.10 Local Bus Data Parity

Generation or use of Local Bus data parity is optional. Signals on the data parity pins do not affect operation of the PCI 9054. The PCI Bus parity checking and generation is independent of the Local Bus parity checking and generation. PCI Bus parity checking may result in assertion of PERR#, a PCI Bus system error (SERR#), or other means of PCI Bus transfer termination as a result of the parity error on the PCI data address, command code, and byte enables. The Local Bus Parity Check is passive and only provides parity information to the Local processor during Direct Master, Direct Slave, and DMA transfers.

There is one data parity pin for each byte lane of the PCI 9054 data bus (DP[3:0]). “Even data parity” is asserted for each lane during Local Bus reads from the PCI 9054 and during PCI 9054 Master writes to the Local Bus.

Even data parity is checked during Local Bus writes to the PCI 9054 and during PCI 9054 reads from the Local Bus. Parity is checked for each byte lane with an asserted byte enable. If a parity error is detected, LSERR# is asserted in the Clock cycle following the data being checked.

4.3 Big Endian/Little Endian

4.3.1.1 PCI Bus Little Endian Mode

PCI Bus is a Little Endian bus (*that is*, the address is invariant and data is Lword-aligned to the lowermost byte lane).

Table 4-10. PCI Bus Little Endian Byte Lanes

Byte Number	Byte Lane
0	AD[7:0]
1	AD[15:8]
2	AD[23:16]
3	AD[31:24]

4.3.1.2 Local Bus Big/Little Endian Mode

The PCI 9054 Local Bus can be programmed to operate in Big or Little Endian mode**.**

Table 4-11. Byte Number and Lane Cross-Reference

Mode	Byte Number		Byte Lane
	Big Endian	Little Endian	
C	3	0	LD[7:0]
	2	1	LD[15:8]
	1	2	LD[23:16]
	0	3	LD[31:24]
J	3	0	LAD[7:0]
	2	1	LAD[15:8]
	1	2	LAD[23:16]
	0	3	LAD[31:24]

Table 4-12. Big/Little Endian Program Mode

BIGEND# Pin	BIGEND Register (1=Big, 0=Little)	Endian Mode
0	0	Big
0	1	Big
1	0	Little
1	1	Big

Table 4-13 lists registers for information about the following cycles.

Table 4-13. Cycles Reference Tables

Cycles	Register Bits
Local access to the Configuration registers	BIGEND[0]
Direct Master, Memory, and I/O	BIGEND[1]
Direct Slave	BIGEND[2], Space 0, and BIGEND[3], Expansion ROM

In Big Endian mode, the PCI 9054 transposes data byte lanes. Data is transferred as listed in Table 4-14 through Table 4-19.

4.3.1.3 32-Bit Local Bus—Big Endian Mode

Data is Lword aligned to uppermost byte lane (Address Invariance).

Table 4-14. Upper Lword Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

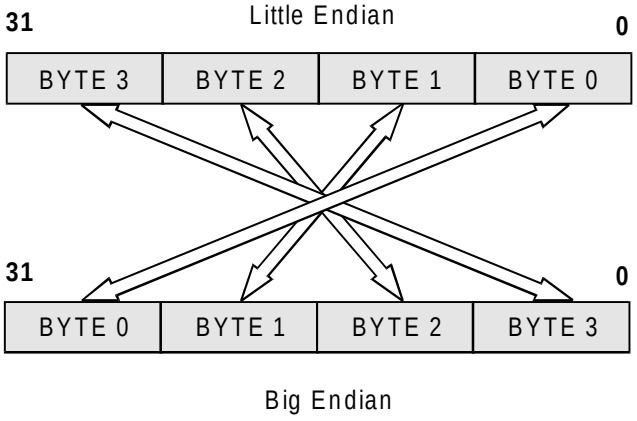


Figure 4-2. Big/Little Endian—32-Bit Local Bus

4.3.1.4 16-Bit Local Bus—Big Endian Mode

For a 16-bit Local Bus, the PCI 9054 can be programmed to use upper or lower word lanes.

Table 4-15. Upper Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
Second Transfer	Byte 2 appears on Local Data [31:24]
	Byte 3 appears on Local Data [23:16]

Table 4-16. Lower Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [15:8]
	Byte 1 appears on Local Data [7:0]
Second Transfer	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

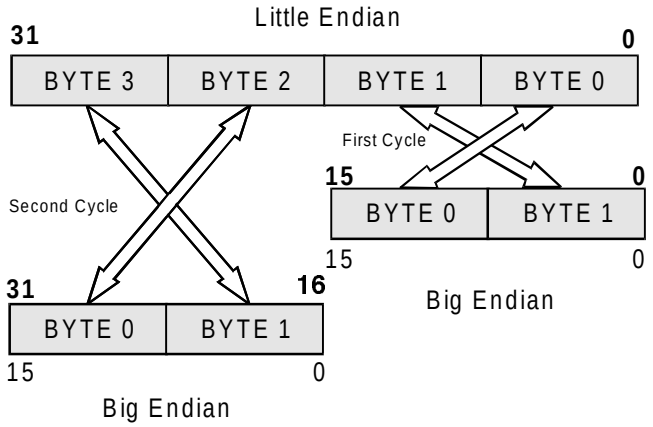


Figure 4-3. Big/Little Endian—16-Bit Local Bus

4.3.1.5 8-Bit Local Bus—Big Endian Mode

For an 8-bit Local Bus, the PCI 9054 can be programmed to use upper or lower byte lanes.

Table 4-17. Upper Byte Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24]
Second transfer	Byte 1 appears on Local Data [31:24]
Third transfer	Byte 2 appears on Local Data [31:24]
Fourth transfer	Byte 3 appears on Local Data [31:24]

Table 4-18. Lower Byte Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [7:0]
Second Transfer	Byte 1 appears on Local Data [7:0]
Third Transfer	Byte 2 appears on Local Data [7:0]
Fourth Transfer	Byte 3 appears on Local Data [7:0]

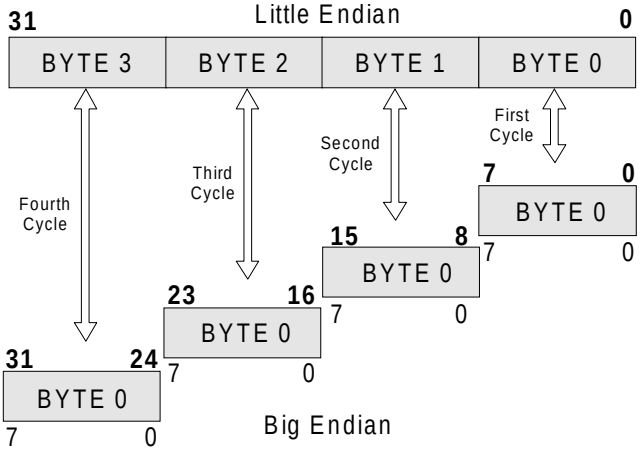


Figure 4-4. Big/Little Endian—8-Bit Local Bus

4.3.1.6 Local Bus Big/Little Endian Mode Accesses

For each of the following transfer types, the PCI 9054 Local Bus can be independently programmed to operate in Little Endian or Big Endian mode:

- Local Bus accesses to the PCI 9054 Configuration registers
- Direct Slave PCI accesses to Local Address Space 0
- Direct Slave PCI accesses to Local Address Space 1
- Direct Slave PCI accesses to Expansion ROM
- DMA Channel 0 accesses to the Local Bus
- DMA Channel 1 accesses to the Local Bus
- Direct Master Accesses to the PCI Bus

For Local Bus accesses to the Internal Configuration registers and Direct Master accesses, use BIGEND# to dynamically change the Endian mode.

Notes: *The PCI Bus is always Little Endian.*

Only byte lanes are swapped, not individual bits.

4.4 Serial EEPROM

Functional operation described can be modified through the PCI 9054 programmable internal registers.

4.4.1 Vendor and Device ID Registers

Three Vendor and Device ID registers are supported:

- **PCIIDR**—Contains the normal Device and Vendor IDs. Can be loaded from the serial EEPROM or Local processor(s).
- **PCISVID**—Contains the Subsystem and Subvendor IDs. Can be loaded from the serial EEPROM or Local processor(s).
- **PCIHIDR**—Contains the (hardcoded) PLX Vendor and Device IDs.

4.4.1.1 Serial EEPROM Initialization

During serial EEPROM initialization, the PCI 9054 responds to PCI Target accesses with a Retry. During serial EEPROM initialization, the PCI 9054 responds to a Local processor access by delaying acknowledgment of the cycle (READY#).

4.4.1.2 Local Initialization

The PCI 9054 issues a Retry to all PCI accesses until the Local Init Status bit (LMISC[2]) is set. This bit can be programmed three different ways:

1. By the Local processor, through the Local Configuration register.
2. By the serial EEPROM, during a serial EEPROM load, if the Local processor does not set this bit or if this bit is missing.
3. If the Local processor and/or the serial EEPROM are missing, the serial EEPROM remains blank and the PCI 9054 reverts to the default values and sets this bit (refer to Table 4-19).

4.4.2 Serial EEPROM Operation

After reset, the PCI 9054 attempts to read the serial EEPROM to determine its presence. An active start bit set to 0 indicates a serial EEPROM is present. The PCI 9054 supports 93CS56L (2 kilobit) or 93CS66L (4 kilobit). (Refer to manufacturer's data sheet for the particular serial EEPROM being used.) The first Lword is then checked to verify that the serial EEPROM is programmed. If the first Lword (32 bits) is all ones, a blank serial EEPROM is present. If the first Lword (32 bits) is all zeros, no serial EEPROM is present. For both conditions, the PCI 9054 reverts to the default

values. (Refer to Table 4-19.) CNTRL[28] is set to 1 if programmed (real or random data if a serial EEPROM is detected).

The 3.3V serial EEPROM clock (EESK) is derived from the PCI clock. The PCI 9054 generates the serial EEPROM clock by internally dividing the PCI clock by 132.

Table 4-19. Serial EEPROM Guidelines

Local Processor	Serial EEPROM	System Boot Condition
None	None	The PCI 9054 uses default values. The EEDI/EEDO pin must be **pulled low**—a 1 K-ohm resistor is required (rather than pulled high, which is typically done for this pin). If the PCI 9054 detects all zeros, it reverts to default values.
None	Programmed	Boot with serial EEPROM values. The Local Init Status bit (LMISC[2]) must be set by the serial EEPROM.
None	Blank	The PCI 9054 detects a blank device and reverts to default values.
Present	None	The Local processor programs the PCI 9054 registers, then sets the Local Init Status bit (LMISC[2]=done). ***Note:*** *Some systems may hang if Direct Slave reads and writes take a long time (during initialization, the PCI Host also performs Direct Slave accesses). The value of the PCI Target Retry Delay Clocks (LBRD0[31:28]) may resolve this problem.*
Present	Programmed	Load serial EEPROM, but the Local processor can reprogram the PCI 9054. Either the Local processor or the serial EEPROM must set the Local Init Status bit (LMISC[2]=done).
Present	Blank	The PCI 9054 detects a blank serial EEPROM and reverts to default values. ***Notes:*** *In some systems, the Local processor may be too late to reconfigure PCI 9054 registers before the BIOS configures the PCI 9054.* *The serial EEPROM can be programmed through the PCI 9054 after the system boots in this condition.*

The serial EEPROM can be read or written from the PCI or Local Buses. The Serial EEPROM Control Register bits (CNTRL[28:24]) control the PCI 9054 pins that enable reading or writing of serial EEPROM data bits. (Refer to manufacturer's data sheet for the particular serial EEPROM being used.)

The serial EEPROM can also be read or written, using the VPD function (refer to Section 10).

The PCI 9054 has two serial EEPROM load options:

- **Long Load Mode**—Default. The PCI 9054 loads 17 Lwords from the Serial EEPROM and the Extra Long Load bit (LBRD0[25])
- **Extra Long Load Mode**—The PCI 9054 loads 22 Lwords if the Serial EEPROM and the Extra Long Load bit (LBRD0[25]) is set to 1 during a Long Load

4.4.2.1 Long Serial EEPROM Load

The registers listed in Table 4-20 are loaded from the serial EEPROM after a reset is de-asserted if the Serial EEPROM Extra Long Load bit is not set (LBRD0[25]=0). The serial EEPROM is organized in words (16 bit). The PCI 9054 first loads the Most Significant Word bits (MSW[31:16]), starting from the most significant bit ([31]). The PCI 9054 then loads the Least Significant Word bits (LSW[15:0]), starting again from the most significant bit ([15]). Therefore, the PCI 9054 loads the Device ID, Vendor ID, class code, and so forth.

The serial EEPROM values can be programmed using a Data I/O programmer. The values can also be programmed using the PCI 9054 VPD function (refer to Section 10) or through the Serial EEPROM Control register (CNTRL).

The CNTRL register allows programming of the serial EEPROM, one bit at a time. To read back the value from the serial EEPROM, the Vital Product Data (VPD) function should be utilized. With full utilization of VPD, the designer can perform reads and writes from/to the serial EEPROM, 32 bits at a time. Values should be programmed in the order listed in Table 4-20. The 34, 16-bit words listed in the table are stored sequentially in the serial EEPROM.

Table 4-20. Long Serial EEPROM Load Registers

Serial EEPROM Offset	Description	Register Bits Affected
0h	Device ID	PCIIDR[31:16]
2h	Vendor ID	PCIIDR[15:0]
4h	Class Code	PCICCR[23:8]
6h	Class Code / Revision	PCICCR[7:0] / PCIREV[7:0]
8h	Maximum Latency / Minimum Grant	PCIMLR[7:0] / PCIMGR[7:0]
Ah	Interrupt Pin / Interrupt Line Routing	PCIIPR[7:0] / PCIILR[7:0]
Ch	MSW of Mailbox 0 (User Defined)	MBOX0[31:16]
Eh	LSW of Mailbox 0 (User Defined)	MBOX0[15:0]
10h	MSW of Mailbox 1 (User Defined)	MBOX1[31:16]
12h	LSW of Mailbox 1 (User Defined)	MBOX1[15:0]
14h	MSW of Range for PCI-to-Local Address Space 0	LAS0RR[31:16]
16h	LSW of Range for PCI-to-Local Address Space 0	LAS0RR[15:0]
18h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[31:16]
1Ah	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[15:0]
1Ch	MSW of Mode/DMA Arbitration Register	MARBR[31:16]
1Eh	LSW of Mode/DMA Arbitration Register	MARBR[15:0]
20h	MSW of Serial EEPROM Write-Protected Address	PROT_AREA[15:0]
22h	LSW of Local Miscellaneous Control Register / LSW of Local Bus Big/Little Endian Descriptor Register	LMISC[7:0] / BIGEND[7:0]
24h	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]
26h	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]
28h	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[31:16]
2Ah	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM	EROMBA[15:0]
2Ch	MSW of Bus Region Descriptors for PCI-to-Local Accesses	LBRD0[31:16]
2Eh	LSW of Bus Region Descriptors for PCI-to-Local Accesses	LBRD0[15:0]
30h	MSW of Range for Direct Master-to-PCI	DMRR[31:16]
32h	LSW of Range for Direct Master-to-PCI	DMRR[15:0]
34h	MSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[31:16]
36h	LSW of Local Base Address for Direct Master-to-PCI Memory	DMLBAM[15:0]
38h	MSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[31:16]
3Ah	LSW of Local Bus Address for Direct Master-to-PCI I/O Configuration	DMLBAI[15:0]
3Ch	MSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[31:16]
3Eh	LSW of PCI Base Address (Remap) for Direct Master-to-PCI	DMPBAM[15:0]
40h	MSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[31:16]
42h	LSW of PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	DMCFGA[15:0]

4.4.2.2 Extra Long Serial EEPROM Load

The registers listed in the Local Address Space 0/Expansion ROM Bus Region Descriptor register (LBRD0) are loaded from serial EEPROM after a reset is de-asserted if the Serial EEPROM Extra Long Load bit is set (LBRD0[25]=1). The serial EEPROM is organized in words (16 bit). The PCI 9054 first loads the Most Significant Word bits ([31:16]), starting from the most significant bit ([31]). It then loads the Least Significant Word bits ([15:0]), restarting from the most significant bit ([15]). Therefore, the PCI 9054 loads Device ID, Vendor ID, class code, and so forth.

The serial EEPROM values can be programmed using a Data I/O programmer. The values can also be programmed using the PCI 9054 VPD function or through the Serial EEPROM Control register (CNTRL). Values should be programmed in the order listed in Table 4-21. The 44 16-bit words listed in Table 4-20 and Table 4-21 should be stored sequentially in the serial EEPROM.

Table 4-21. Extra Long Serial EEPROM Load Registers

Serial EEPROM Offset	Description	Register Bits Affected
44h	Subsystem ID	PCISID[15:0]
46h	Subsystem Vendor ID	PCISVID[15:0]
48h	MSW of Range for PCI-to-Local Address Space 1 (1 MB)	LAS1RR[31:16]
4Ah	LSW of Range for PCI-to-Local Address Space 1 (1 MB)	LAS1RR[15:0]
4Ch	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[31:16]
4Eh	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[15:0]
50h	MSW of Bus Region Descriptors (Space 1) for PCI-to-Local Accesses	LBRD1[31:16]
52h	LSW of Bus Region Descriptors (Space 1) for PCI-to-Local Accesses	LBRD1[15:0]
54h	MSW of Hot Swap Control	Reserved
56h	LSW of Hot Swap Control / Hot Swap Next Capability Pointer	HS_NEXT[7:0] / HS_CNTL[7:0]

4.4.2.3 New Capabilities Function Support

The New Capabilities Function Support includes PCI Power Management, Hot Swap, and VPD features, as listed in Table 4-22.

Table 4-22. New Capabilities Function Support Features

New Capability Function	PCI Register Offset Location
First (Power Management)	40'h, if the New Capabilities Function Support bit (PCISR[4]) is enabled (PCISR[4] is enabled, by default).
Second (Hot Swap)	48'h, which is pointed to from PMNEXT[7:0].
Third (VPD)	4C'h, which is pointed to from HS_NEXT[7:0]. Because PVPD_NEXT[7:0] defaults to zero, this indicates that VPD is the last New Capability Function Support feature of the PCI 9054.

4.4.2.4 Recommended Serial EEPROMs

The PCI 9054 is designed to use either a 2-kilobit (NM93CS56L or compatible) or 4-kilobit (NM93CS66L or compatible) device.

Note: *The PCI 9054 does not support serial EEPROMs that do not support sequential reads and writes (such as the NM93C56L).*

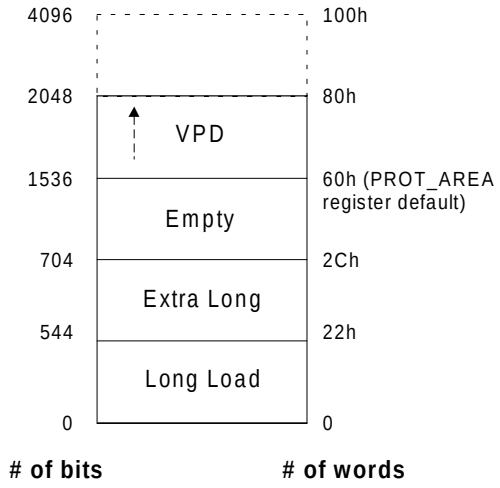


Figure 4-5. Serial EEPROM Memory Map

4.4.2.5 Serial EEPROM Initialization

During serial EEPROM initialization, the PCI 9054 responds to PCI Target accesses with a Retry. During serial EEPROM initialization, the PCI 9054 responds to a Local processor access by delaying acknowledgment of the cycle (READY#).

4.4.3 Internal Register Access

The PCI 9054 provides several internal registers, which allow for maximum flexibility in the bus-interface design and performance. These registers are accessible from the PCI and Local Buses and include the following:

- PCI Configuration registers
- Local Configuration registers
- DMA registers
- Mailbox registers
- PCI-to-Local and Local-to-PCI Doorbell registers
- Messaging Queue registers (I_2O)
- Power Management registers
- Hot Swap registers
- VPD registers

Figure 4-6 illustrates how these registers are accessed.

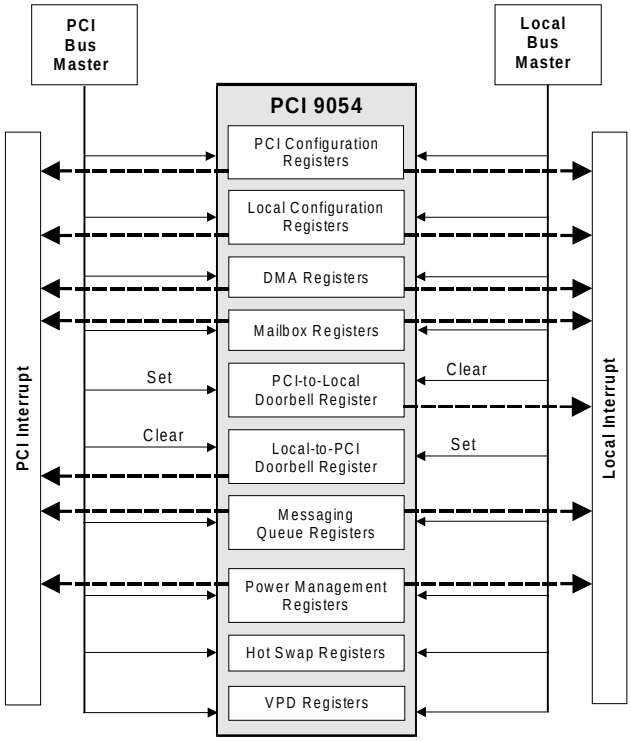


Figure 4-6. PCI 9054 Internal Register Access

4.4.3.1 PCI Bus Access to Internal Registers

The PCI 9054 PCI Configuration registers can be accessed from the PCI Bus with a Configuration Type 0 cycle.

All other PCI 9054 internal registers can be accessed by a Memory cycle, with the PCI Bus address that matches the base address specified in PCI Base Address 0 (PCIBAR0[31:8]) for the PCI 9054 Memory-Mapped Configuration register. These registers can also be accessed by an I/O cycle, with the PCI Bus address matching the base address specified in PCI Base Address 1 for the PCI 9054 I/O-Mapped Configuration register.

All PCI Read or Write accesses to the PCI 9054 registers can be Byte, Word, or Lword accesses. All PCI Memory accesses to the PCI 9054 registers can be Burst or Non-Burst accesses. The PCI 9054 responds with a PCI disconnect for all Burst I/O accesses (PCIBAR1[31:8]) to the PCI 9054 Internal registers.

4.4.3.2 Local Bus Access to Internal Registers

The Local processor can access all PCI 9054 internal registers through an external chip select. The PCI 9054 responds to a Local Bus access when the PCI 9054 Configuration Chip Select input (CCS#) is asserted low. Figure 4-7 illustrates how the Configuration Chip Select logic works.

Note: *CCS# must be decoded while TS# is low.*

Accesses must be for a 32-bit non-pipelined bus.

Local Read or Write accesses to the PCI 9054 internal registers can be Byte, Word, or Lword accesses. Local accesses to the PCI 9054 internal registers can be Burst or Non-Burst accesses.

The PCI 9054 TA# signal indicates that Data transfer is complete.

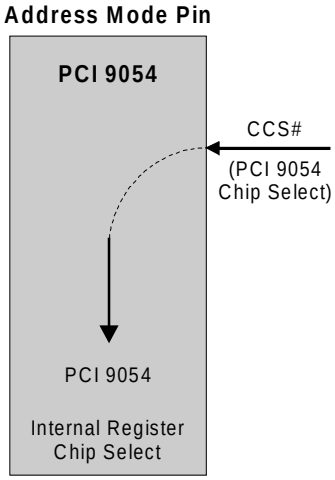
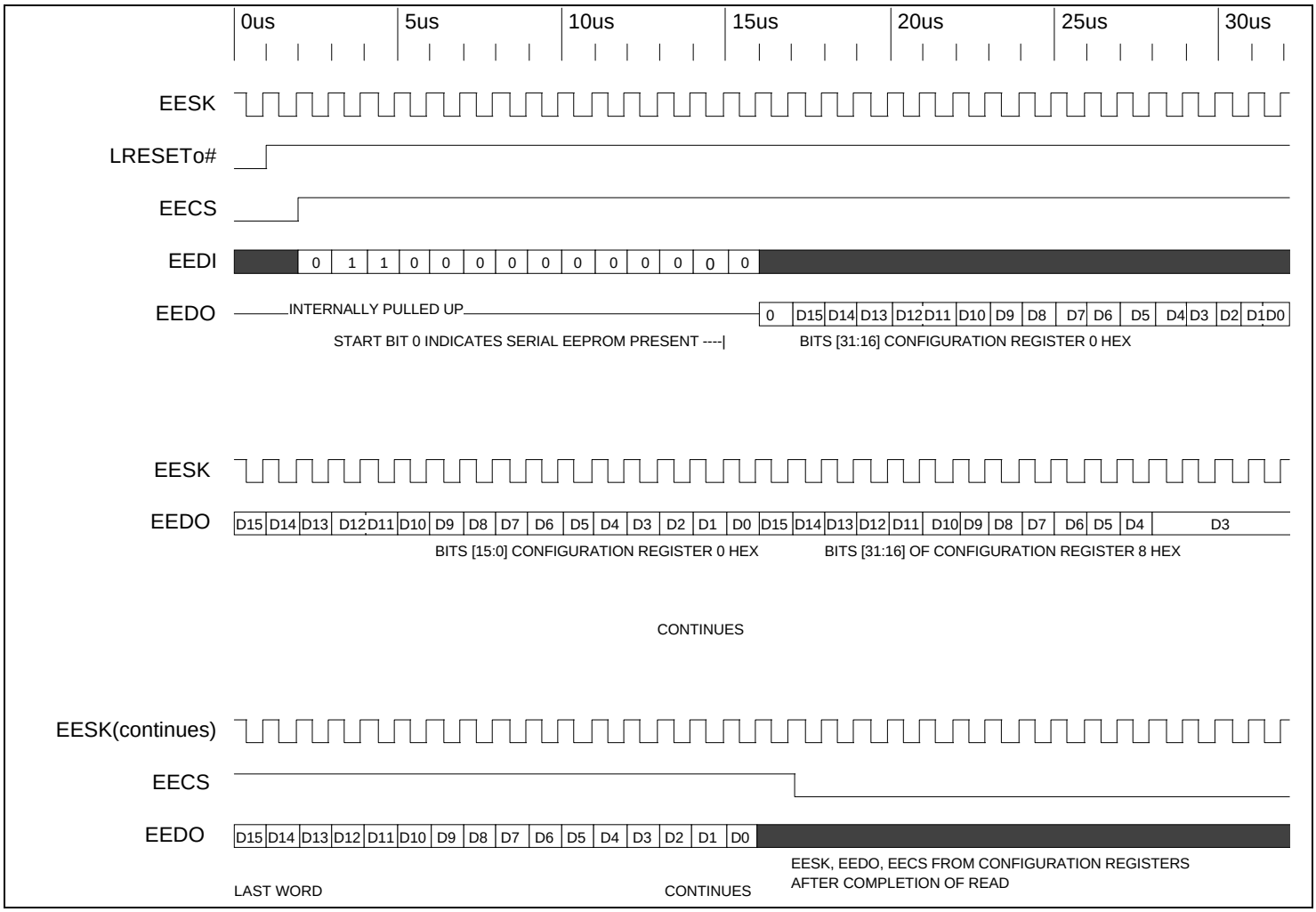


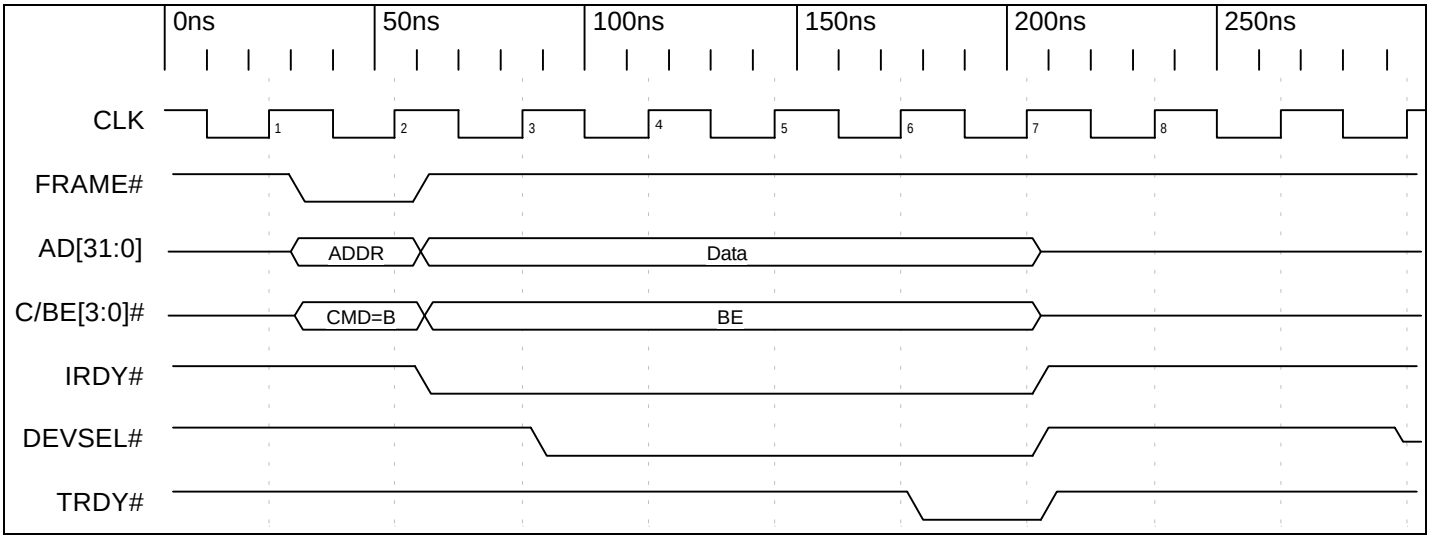
Figure 4-7. Address Decode Mode

4.4.4 Serial EEPROM Timing Diagrams

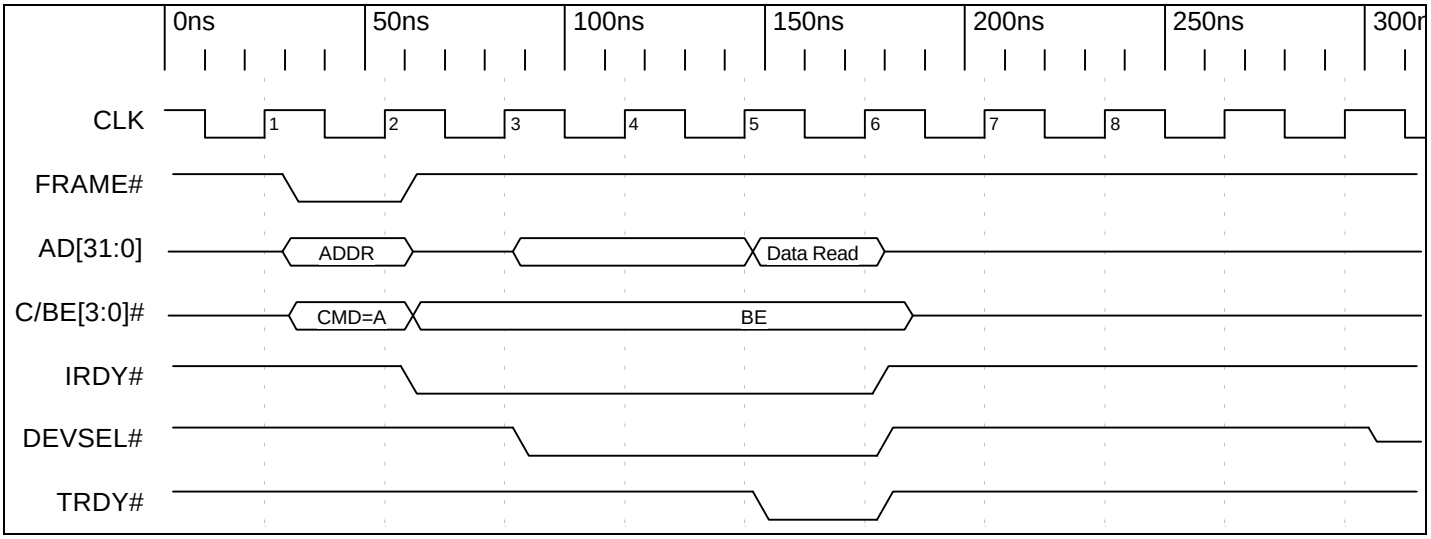
Timing Diagram 4-1. Initialization from Serial EEPROM (2K)



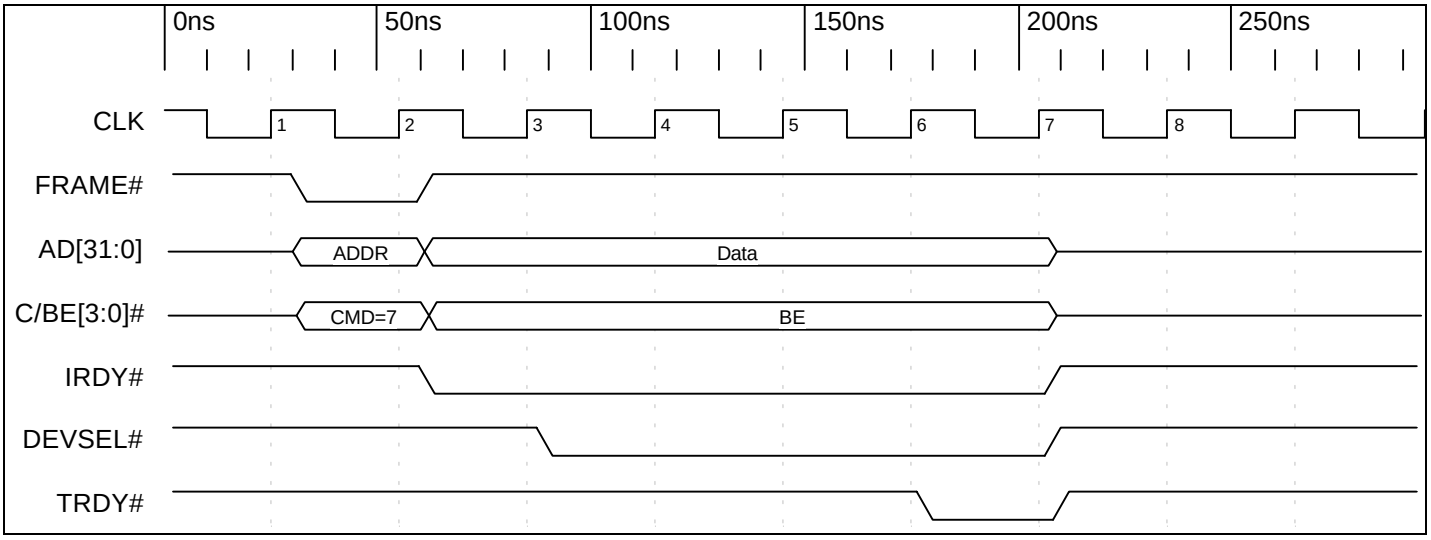
Timing Diagram 4-2. Initialization from Serial EEPROM (4K)



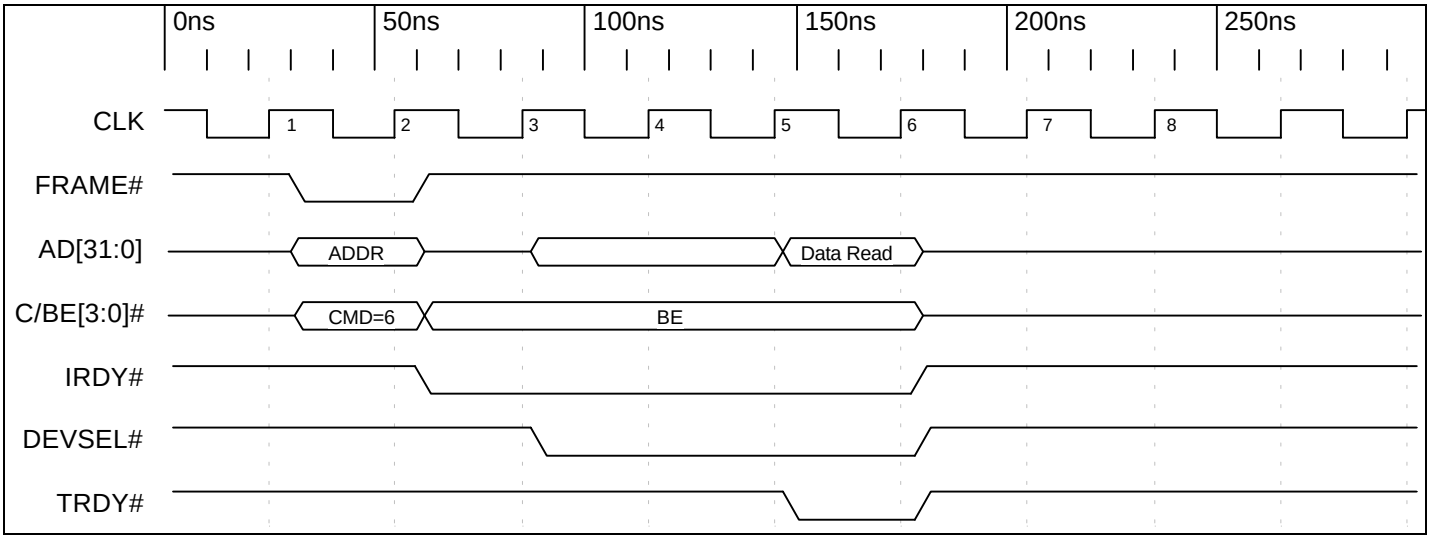
Timing Diagram 4-3. PCI Configuration Write to PCI Configuration Register



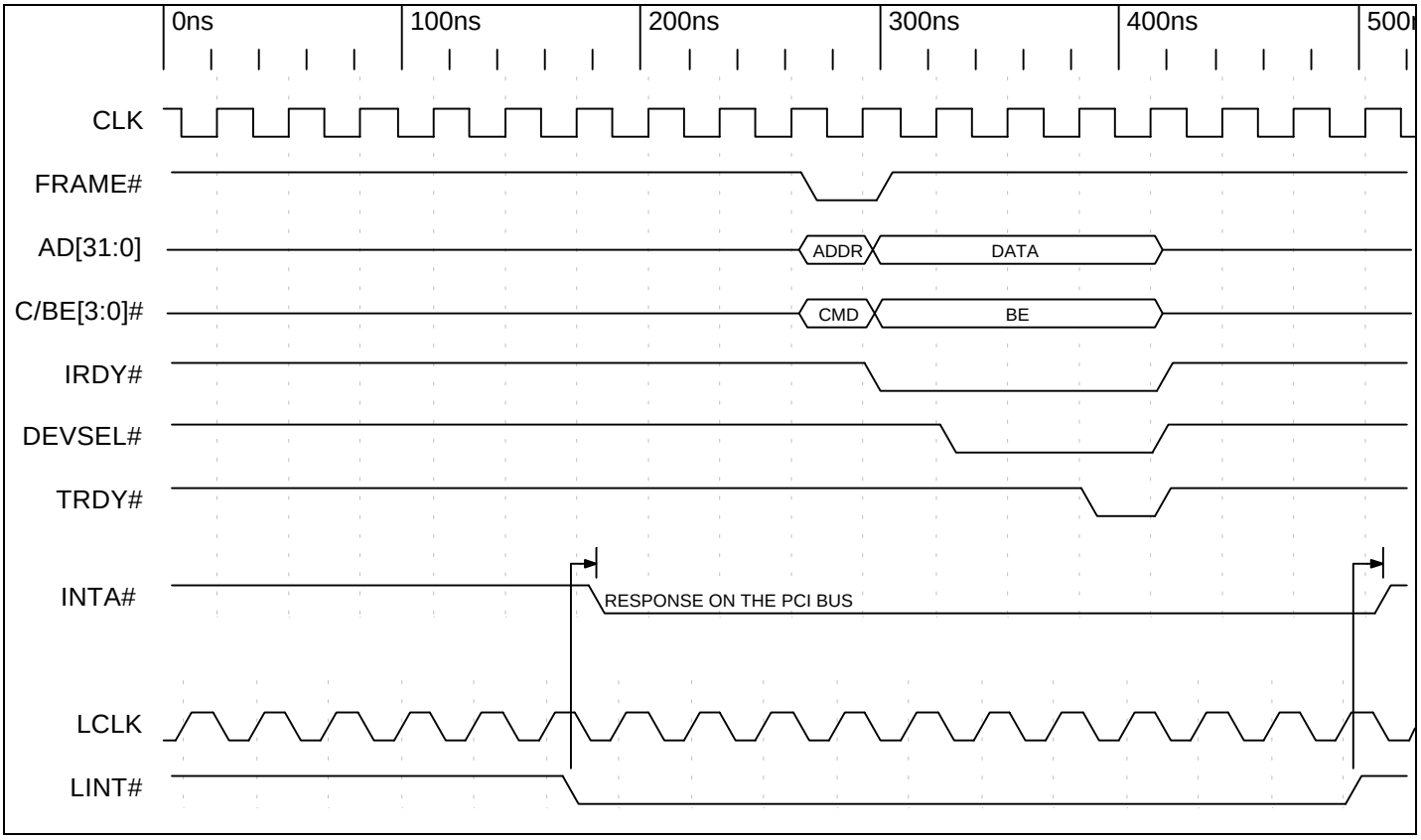
Timing Diagram 4-4. PCI Configuration Read to PCI Configuration Register



Timing Diagram 4-5. PCI Memory Write to Local Configuration Register



Timing Diagram 4-6. PCI Memory Read to Local Configuration Register



Timing Diagram 4-7. Local Interrupt Asserting PCI Interrupt

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5. C AND J MODES FUNCTIONAL DESCRIPTION

Functional operation described can be modified through the PCI 9054 programmable internal registers.

5.1 Reset Operation

5.1.1 PCI Bus Input RST#

PCI Bus RST# input pin is a PCI Host reset. It causes all PCI Bus outputs to float, resets the entire PCI 9054 and causes the Local reset LRESETo# signal to be asserted.

5.1.2 Software Reset

A Host on the PCI Bus can set the PCI Adapter Software Reset bit (CNTRL[30]=1) to reset the PCI 9054 and assert LRESETo# output. All Local Configuration registers are reset; however, the PCI Configuration DMA and Shared Runtime registers and the Local Init Status bit (LMISC[2]) are not reset. When the Software Reset bit (CNTRL[30]) is set, the PCI 9054 responds to PCI accesses, but not to Local Bus accesses. The PCI 9054 remains in this reset condition until the PCI Host clears the bit. The serial EEPROM is reloaded if the Reload Configuration Registers bit is set (CNTRL[29]=1).

Note: *The Local Bus cannot clear this reset bit because the Local Bus is in a reset state, even if the Local processor does not use LRESETo# to reset.*

5.2 PCI 9054 Initialization

The PCI 9054 Configuration registers can be programmed by an optional serial EEPROM and/or by a Local processor, as listed in Table 4-19. The serial EEPROM can be reloaded by setting the Reload Configuration Registers bit (CNTRL[29]).

The PCI 9054 retries all PCI cycles until the Local Init Status bit is set to “done” (LMISC[2]=1).

Note: *The PCI Host processor can also access Internal Configuration registers after the Local Init Status bit is set.*

If a PCI Host is present, the Master Enable, Memory Space, and I/O Space bits (PCICR[2:0]) are programmed by that Host after initialization completes (LMISC[2]=1).

5.3 Response to FIFO Full or Empty

Table 5-1 lists the response of the PCI 9054 to full and empty FIFOs.

5.4 Direct Data Transfer Modes

The PCI 9054 supports three direct transfer modes:

- **Direct Master**—Local CPU accesses PCI memory or I/O
- **Direct Slave**—PCI Master accesses Local memory or I/O
- **DMA**—PCI 9054 DMA controller reads/writes PCI memory to/from Local memory

5.4.1 Direct Master Operation (Local Master-to-PCI Target)

The PCI 9054 supports a direct access of the PCI Bus by the Local processor or an intelligent controller. Master mode must be enabled in the PCI Command register. The following registers define Local-to-PCI accesses:

- Direct Master Memory and I/O Range (DMRR)
- Local Base Address for Direct Master to PCI Memory (DMLBAM)
- Local Base Address for Direct Master to PCI I/O and Configuration (DMLBAI)
- PCI Base Address (DMPBAM)
- Direct Master Configuration (DMCFGA)
- Direct Master PCI Dual Address Cycles (DMDAC)
- Master Enable (PCICR)
- PCI Command Code (CNTRL)

Table 5-1. Response to FIFO Full or Empty

Mode	Direction	FIFO	PCI Bus	Local Bus
Direct Master Write	Local-to-PCI	Full	Normal	De-assert READY#
		Empty	De-assert REQ# (off PCI Bus)	Normal
Direct Master Read	PCI-to-Local	Full	De-assert REQ# or throttle IRDY#[2]	Normal
		Empty	Normal	De-assert READY#
Direct Slave Write	PCI-to-Local	Full	Disconnect or throttle TRDY#[3]	Normal
		Empty	Normal	De-assert LHOLD, assert BLAST#[1]
Direct Slave Read	Local-to-PCI	Full	Normal	De-assert LHOLD, assert BLAST#[1]
		Empty	Throttle TRDY#[3]	Normal
DMA	Local-to-PCI	Full	Normal	De-assert LHOLD, assert BLAST#[1]
		Empty	De-assert REQ#	Normal
	PCI-to-Local	Full	De-assert REQ#	Normal
		Empty	Normal	De-assert LHOLD, assert BLAST#[1]

Notes:

1 LHOLD de-assert depends upon the Local Bus Direct Slave Release Bus Mode bit (MARBR[21]).

2 Throttle IRDY# depends on the Direct Master PCI Read Mode bit (DMPBAM[4]).

3 Throttle TRDY# depends on the Direct Slave Write Mode bit (LBRD0[27]).

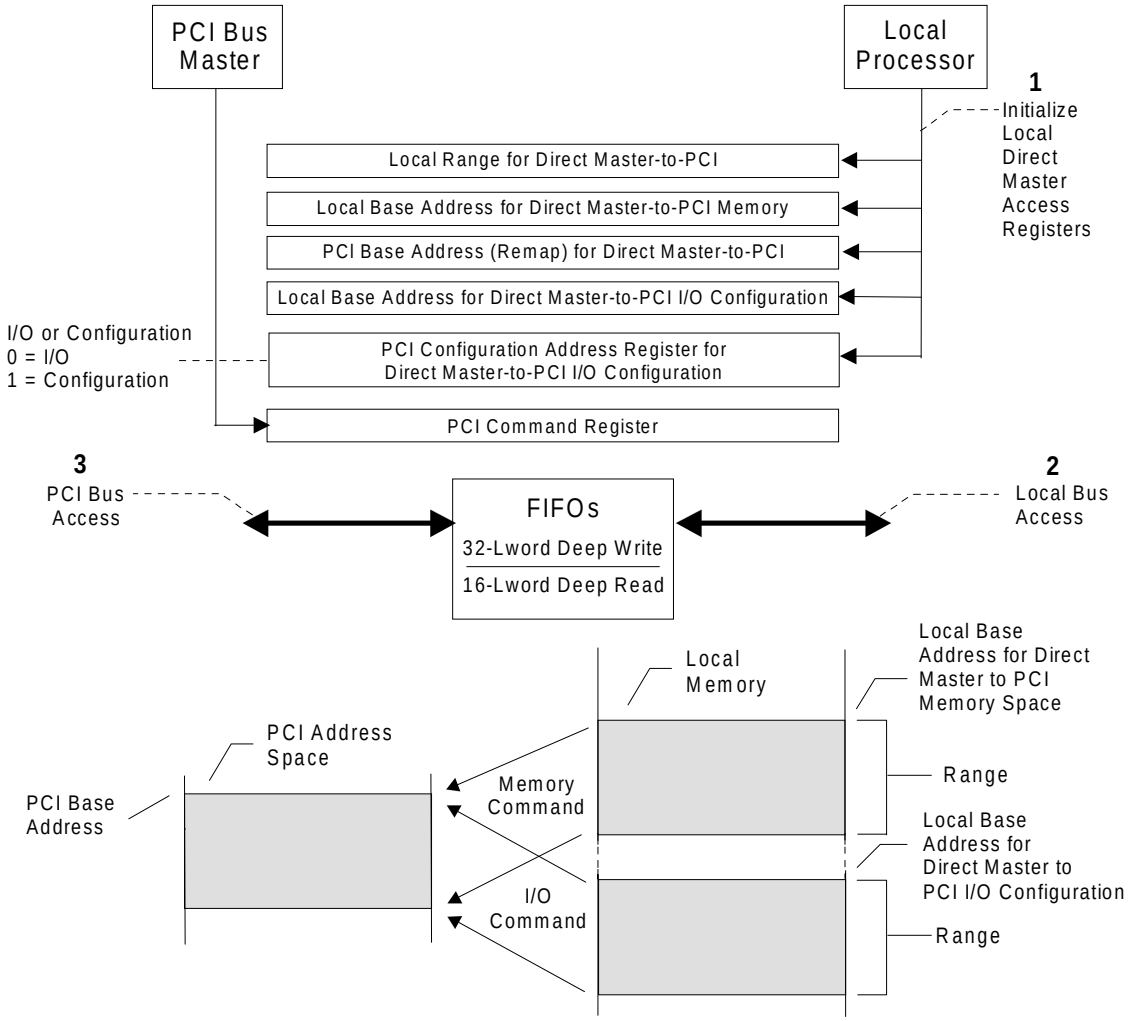


Figure 5-1. Direct Master Access of the PCI Bus

5.4.1.1 Direct Master Memory and I/O Decode

The Range register and the Local Base Address specifies the Local Address bits to use for decoding a Local-to-PCI access (Direct Master). The range of memory or I/O space must be a power of 2 and the Range register value must be the inverse of the Range value. In addition, the Local Base Address must be a multiple of the range value.

Any Local Master Address starting from the Direct Master Local Base Address (Memory or I/O) to the range value is recognized as a Direct Master access by the PCI 9054. All Direct Master cycles are then decoded as PCI Memory, I/O, or Configuration Type 0 or 1. Moreover, a Direct Master memory or I/O cycle is remapped according to the Remap register value. The Remap Register value must be a multiple of the Direct Master Range value (not the Range register value).

The PCI 9054 can only accept Memory cycles from the Local processor. The Local Base Address and/or the range determine whether PCI Memory or PCI I/O transactions occur.

5.4.1.2 Direct Master FIFOs

For Direct Master Memory access to the PCI Bus, the PCI 9054 has a 32-Lword (128-byte) Write FIFO and a 16-Lword (64-byte) Read FIFO. The FIFOs enable the Local Bus to operate independent of the PCI Bus and allows high-performance bursting on the PCI and Local Buses. In a Direct Master write, the Local processor (Master) writes data to the PCI Bus (Slave). In a Direct Master read, the Local processor (Master) reads data from the PCI Bus (Slave). The FIFOs that function during a Direct Master write and read are illustrated in Figure 5-2 and Figure 5-3.

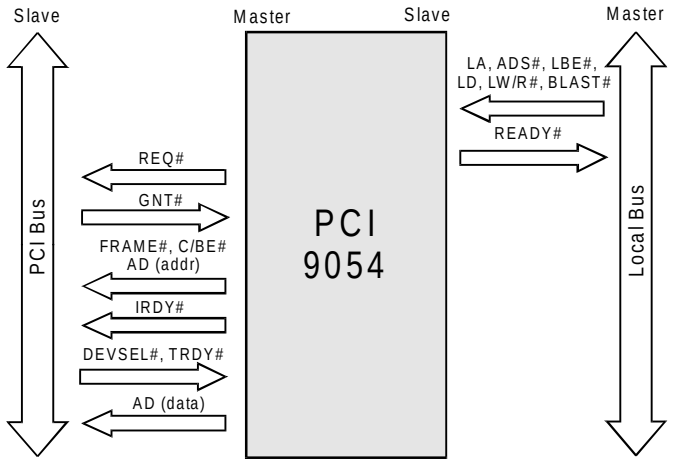


Figure 5-2. Direct Master Write

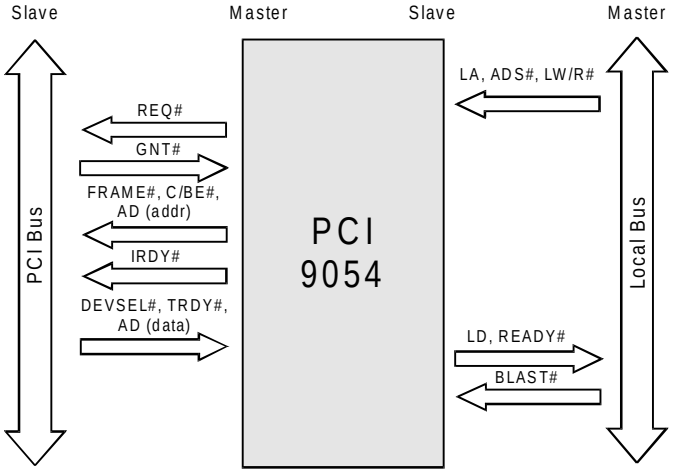


Figure 5-3. Direct Master Read

Note: *The figures represent a sequence of Bus cycles.*

5.4.1.3 Direct Master Memory Access

The Local processor can read or write to the PCI memory. The PCI 9054 converts the Local Read/Write access. The Local Address space starts from the Direct Master Local Base Address up to the range. Remap (PCI Base Address) defines the PCI starting address.

Writes—PCI 9054 continues to accept writes and returns READY# until the Write FIFO is full. It then holds off READY# until space becomes available in the Write FIFO. A programmable Direct Master FIFO "almost full" status output is provided (DMPAF).

Reads—PCI 9054 holds off READY# while gathering an Lword from the PCI Bus. Programmable prefetch modes are available if prefetch is enabled: prefetch, 4, 8, 16, or continuous until the Direct Master cycle ends. The Read cycle is terminated when the Local BLAST# input is asserted. Unused Read data is flushed from the FIFO.

The PCI 9054 does not prefetch Read data for Single-Cycle Direct Master reads (Local BLAST# input asserted during the first Data phase). In this case, the PCI 9054 reads a single PCI Lword unless Direct Master Read Ahead mode is enabled.

For Direct Master Single-Cycle reads, the PCI 9054 sets the same PCI Bus byte enables as set on the Local Bus.

For Burst-Cycle reads, the PCI 9054 reads entire Lwords (all PCI Bus byte enables are asserted).

If the Direct Master Prefetch Limit bit is enabled (DMPBAM[11]=1), the PCI 9054 does not prefetch past a 4-kilobit boundary. Also, the Local Bus must not cross a 4-kilobit boundary during a Burst read.

The PCI 9054 never prefetches beyond the region specified for Direct Master accesses.

5.4.1.4 Direct Master I/O Configuration Access

When a Local Direct Master I/O access to the PCI Bus occurs, the PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration Enable bit (DMCFGA[31]) determines whether an I/O or Configuration access is to be made to the PCI Bus.

Local Burst accesses are broken into single PCI I/O address/Data cycles. The PCI 9054 does not prefetch Read data for I/O and configuration reads.

For Direct Master I/O or Configuration cycles, the PCI 9054 asserts the same PCI Bus byte enables as set on the Local Bus.

5.4.1.5 Direct Master I/O

If the Configuration Enable bit is cleared (DMCFGA[31]=0), a Single I/O access is made to the PCI Bus. The Local Address, Remapped Decode Address bits, and Local byte enables are encoded to provide the address and are output with an I/O Read or Write command during a PCI Address cycle.

When the I/O Remap Select bit is set (DMPBAM[13]=1), the PCI Address bits [31:16] are forced to 0 for the 64-kilobit I/O address limit.

For writes, data is loaded into the Write FIFO and READY# is returned to the Local Bus. For reads, the PCI 9054 holds off READY# while receiving an Lword from the PCI Bus.

5.4.1.6 Direct Master Configuration (PCI Configuration Type 0 or Type 1 Cycles)

If the Configuration Enable bit (DMCFGA[31]) is set, a Configuration access is made to the PCI Bus. In addition to enabling configuration of this bit, the user must provide all register information. The Register Number and Device Number bits (DMCFGA[7:2] and DMCFGA[15:11], respectively) must be modified and a new Configuration Read/Write cycle must be performed before accessing other registers or devices.

If the PCI Configuration Address register selects a Type 0 command, bits [10:0] of the register are copied to address bits [10:0]. Bits [15:11] (device number) are translated into a single bit being set in the PCI Address bits [31:11]. The PCI Address bits [31:11] can be used as a device select. For a Type 1 command, bits [23:0] are copied from the register to bits [23:0] of the PCI address. The PCI Address bits [31:24] are set to 0. A Configuration Read or Write command code is output with the address during the PCI Address cycle (refer to the DMCFGA register).

For writes, Local data is loaded into the Write FIFO and READY# is returned. For reads, the PCI 9054 holds off READY# while gathering an Lword from the PCI Bus.

5.4.1.6.1 Direct Master Configuration Cycle Example

To perform a Type 0 Configuration cycle to PCI device on AD[21]:

1. The PCI 9054 must be configured to allow Direct Master access to the PCI Bus. The PCI 9054 must also be set to respond to I/O space accesses. These bits must be set (PCICR[2:0]=111b).

   In addition, Direct Master memory and I/O access must be enabled (DMPBAM[1:0]=11).

2. The Local memory map selects the Direct Master range. For this example, use a range of 1 MB:

   1 MB = 2^{20} = 000FFFFFh

   The value to program into the Range register is the inverse of 000FFFFFh (FFF00000h):

   DMRR = FFF00000h

3. The Local memory map determines the Local Base Address for the Direct Master-to-PCI I/O Configuration register. For this example, use 40000000h:

   DMLBAI = 40000000h

4. The PCI Address (Remap) for Direct Master-to-PCI Memory register must enable the Direct Master I/O access. The Direct Master I/O Access Enable bit must be set (DMPBAM[1]=1).

5. The user must know which PCI device and PCI Configuration register the PCI Configuration cycle is accessing. This example assumes the IDSEL signal of the Target PCI device is connected to AD[21] (logical device #10=0Ah). Also access PCIBAR0 (the fourth register, counting from 0; use Table 11-2 for reference). Set DMCFGA[31, 23:0] as follows:

Bit	Description	Value
1:0	Configuration Type 0.	00b
7:2	Register Number. Fourth register. Must program a "4" into this value, beginning with bit 2.	000100b
10:8	Function Number.	000b
15:11	Device Number n-11, where n is the value in AD[n]=21-11 = 10.	01010b
23:16	Bus Number.	00000000b
31	Configuration Enable.	1

After these registers are configured, a simple Local Master Memory cycle to the I/O base address is necessary to generate a PCI Configuration Read or Write cycle. Offset to the base address is not necessary because the register offset for the read or write is specified in the Configuration register. The PCI 9054 takes the Local Bus Master Memory cycle and checks for the Configuration Enable bit (DMCFGA[31]). If set, the PCI 9054 converts the current cycle to a PCI Configuration cycle, using the DMCFGA register and the Write/Read signal (LW/R#).

The Register Number and Device Number bits (DMCFGA[7:2] and DMCFGA[15:11], respectively) must be modified and a new Configuration Read/Write cycle must be performed before accessing other registers or devices.

5.4.1.7 Direct Master PCI Dual Address Cycle

The PCI 9054 supports PCI Dual Address Cycle (DAC) when it is a PCI Bus Master, using the DMADAC0 and DMADAC1 registers for Block DMA transactions. Scatter/Gather DMA can utilize the DAC function via the DMADAC0 and DMADAC1 registers or DMAMODE0[18] AND DMAMODE1[18]. The DAC command is used to transfer a 64-bit address to devices that support 64-bit addressing when the address is above the 4-GB Address space. The PCI 9054 performs a DAC within two PCI clock periods, where the first PCI address is a Lo-Addr, with the command (C/BE[3:0]#) "D", and the second PCI address is a Hi-Addr, with the command (C/BE[3:0]#) "6" or "7", depending upon whether it is a PCI Read or PCI Write cycle.

5.4.1.8 Direct Master/Target Abort

The PCI 9054 Direct Master/Target Abort logic enables a Local Bus Master to perform a Direct Master Bus poll of devices to determine whether devices exist (typically when the Local Bus performs Configuration cycles to the PCI Bus). When a PCI Master device attempts to access and does not receive DEVSEL# within six PCI clocks, it results in a Master Abort. The Local Bus Master must clear the Received Master Abort bit or Target Abort bit (PCISR[13 or 11]=0, respectively) and continue by processing the next task.

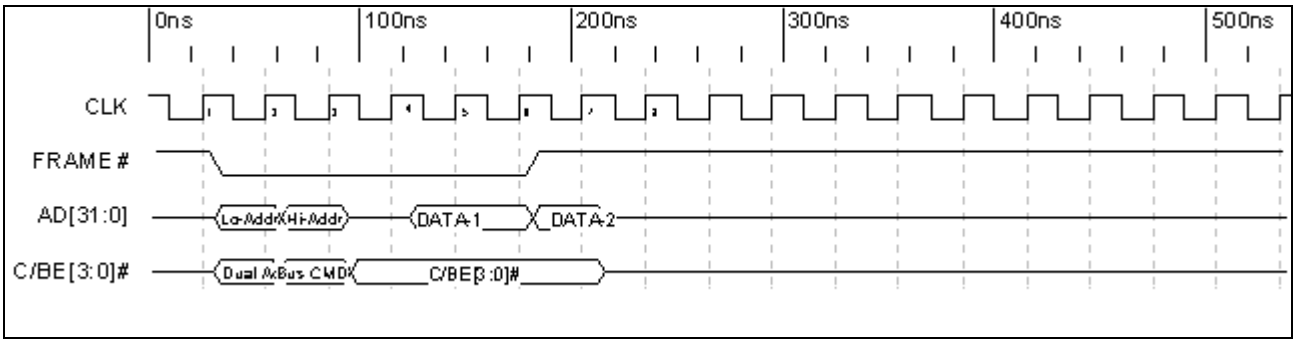


Figure 5-4. Dual Address Timing

If a PCI Master/Target Abort, or Retry Time-Out is encountered during a transfer, the PCI 9054 asserts LSERR# if enabled [(INTCSR[1:0]=1), which can be used as an NMI]. If a Local Bus Master is waiting for READY#, it is asserted along with BTERM#. The Local Master's interrupt handler can take the appropriate application-specific action It can then clear the Target Abort bit (PCISR[11]) to de-assert the LSERR# interrupt and re-enable Direct Master transfers.

If a Local Bus Master is attempting a Burst read from a nonresponding PCI device (Master/Target Abort), it receives READY# and BTERM# for the first cycle only. In addition, the PCI 9054 asserts LSERR# if the Enable Local Bus LSERR# bits are enabled (INTCSR[1:0], which can be used as an NMI). If the Local processor cannot terminate its Burst cycle, it may cause the Local processor to hang. The Local Bus must then be reset from the PCI Bus. If a Local Bus Master cannot terminate its cycle with BTERM# output, it should not perform Burst cycles when attempting to determine whether a PCI device exists.

5.4.1.9 Direct Master Memory Write and Invalidate

The PCI 9054 can be programmed to perform Memory Write and Invalidate cycles to the PCI Bus for Direct Master transfers, as well as DMA transfers (refer to Section 5.5.4). The PCI 9054 supports Memory Write and Invalidate transfers for cache line sizes of 8 or 16 Lwords. Size is specified in the System Cache Line Size bits (PCICLSR[7:0]). If a size other than 8 or 16 is specified, the PCI 9054 performs Write transfers rather than Memory Write and Invalidate transfers.

Direct Master Memory Write and Invalidate transfers are enabled when the Invalidate Enable bit (DMPBAM[9]) and the Memory Write and Invalidate Enable bit (PCICR[4]) are set.

In Memory Write and Invalidate mode, if the start address of the Direct Master transfer is on a cache line boundary, the PCI 9054 waits until the number of Lwords required for the specified cache line size are written from the Local Bus before starting a PCI Memory Write and Invalidate access. This ensures a complete cache line write can complete in one PCI Bus ownership.

If the start address is not on a cache line boundary, the PCI 9054 starts a normal PCI Write access (PCI command code = 7h). The PCI 9054 terminates a cycle at a cache line boundary if it is performing a normal write or if it is performing a Memory Write and Invalidate cycle and another cache line of data is not available. If an entire cache line is available by the time PCI 9054 regains use of the PCI Bus, the PCI 9054 resumes Memory Write and Invalidate cycles. Otherwise, it continues with a normal write. If a Target disconnects before a cache line is completed, the PCI 9054 completes the remainder of that cache line, using normal writes.

5.4.2 Direct Slave Operation (PCI Master-to-Local Bus Access)

The PCI 9054 supports both Burst Memory-Mapped Transfer accesses and I/O-Mapped, Single-Transfer accesses to the Local Bus from the PCI Bus through a 16-Lword (64-byte) Direct Slave Read FIFO and a 32-Lword (128-byte) Direct Slave Write FIFO. The PCI Base Address registers are provided to set up the location of the adapter in the PCI memory and the I/O space. In addition, Local mapping registers allow address translation from the PCI Address Space to the Local Address Space. Three spaces are available:

- Space 0
- Space 1
- Expansion ROM space

Expansion ROM space is intended to support a bootable ROM device for the Host.

For Single Cycle Direct Slave reads, the PCI 9054 reads a single Local Bus Lword or partial Lword. The PCI 9054 disconnects after one transfer for all Direct Slave I/O accesses.

For the highest data-transfer rate, the PCI 9054 supports posted writes and can be programmed to prefetch data during a PCI Burst Read. The Prefetch size, when enabled, can be from one to 16 Lwords or until the PCI Bus stops requesting. When the PCI 9054 prefetches, if enabled, it drops the Local Bus after reaching the prefetch counter. In Continuous Prefetch mode, the PCI 9054 prefetches as long as FIFO space is available and stops prefetching when the PCI Bus terminates the request. If Read prefetching is disabled, the PCI 9054 disconnects after one Read transfer.

In addition to Prefetch mode, the PCI 9054 supports Read Ahead mode (refer to Section 5.4.2.3).

Each Local space can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width. The PCI 9054 has an internal wait state generator and external wait state input, READY#. READY# can be disabled or enabled with the Internal Configuration registers.

With or without wait state(s), the Local Bus, independent of the PCI Bus, can

- Burst as long as data is available (Continuous Burst mode)
- Burst four Lwords at a time (recommended)
- Perform a continuous Single cycle

5.4.2.1 Direct Slave Lock

The PCI 9054 supports direct PCI-to-Local-Bus Exclusive accesses (locked atomic operations). A PCI-locked operation to the Local Bus results in the entire address Space 0, Space 1, and Expansion ROM space being locked until they are released by the PCI Bus Master. Locked operations are enabled or disabled with the Direct Slave LOCK# Enable bit (MARBR[22]) for PCI-to-Local accesses.

5.4.2.2 Direct Slave PCI v2.1 Delayed Read Mode

The PCI 9054 can be programmed through the PCI Specification v2.1 Mode bit (MARBR[24]=1) to perform delayed reads, as specified in PCI Specification v2.1.

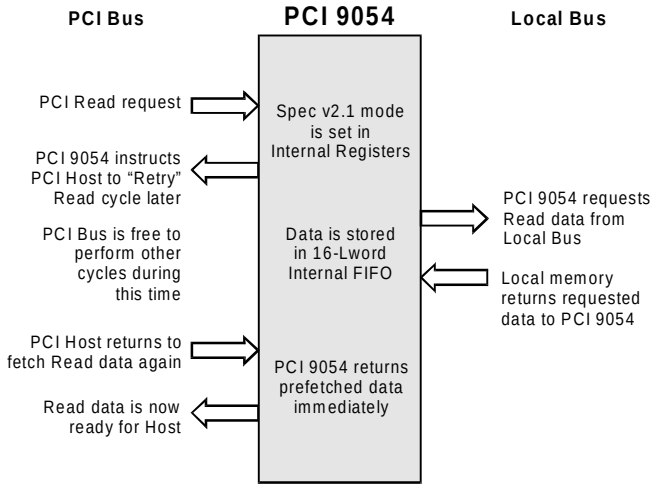


Figure 5-5. Direct Slave PCI v2.1 Delayed Reads

Note: *The figure represents a sequence of Bus cycles.*

In addition to delayed reads, the PCI 9054 supports the following PCI Specification v2.1 functions:

- No write while a read is pending (PCI Retry for reads)
- Write and flush pending read

5.4.2.3 Direct Slave PCI Read Ahead Mode

The PCI 9054 also supports Read Ahead mode, where prefetched data can be read from the internal FIFO of the PCI 9054 instead of from the Local Bus. The address must be subsequent to the previous address and 32-bit aligned (next address = current address + 4). Read Ahead mode functions with or without PCI Delayed Read mode.

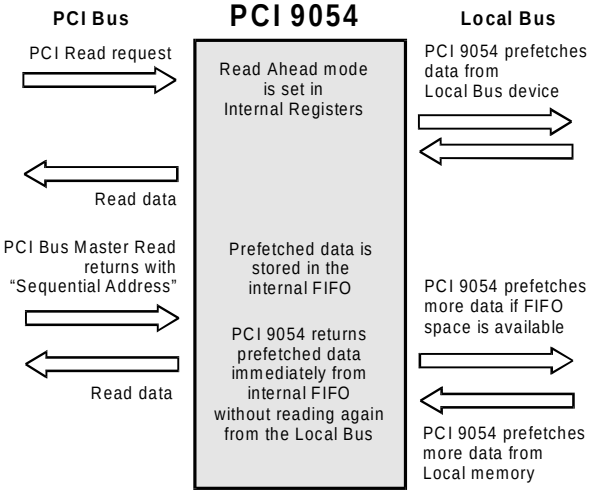


Figure 5-6. Direct Slave PCI 9054 Read Ahead Mode

Note: *The figure represents a sequence of Bus cycles.*

5.4.2.4 Direct Slave Transfer

Transactions are initiated by a PCI Bus Master addressing the Memory space decoded for the Local Bus. Upon a PCI Read/Write, the PCI 9054 becomes a Local Bus Master and arbitrates for the Local Bus.

The PCI 9054 then reads data into the Direct Slave Read FIFO or writes data to the Local Bus.

The Direct Slave or Direct Master pre-empts DMA; however, the Direct Slave does not pre-empt the Direct Master (refer to Section 5.4.3.1).

The PCI 9054 can be programmed to "keep" the PCI Bus by generating a wait state(s) and de-asserting TRDY# if the Write FIFO becomes full. The PCI 9054 can also be programmed to "keep" the Local Bus and continue asserting LHOLD if the Direct Slave Write FIFO becomes empty or the Direct Slave Read FIFO becomes full. In either case, the Local Bus is dropped when the Local Bus Latency Timer is enabled and expires (MARBR[7:0]).

For Direct Slave writes, the PCI Bus writes data to the Local Bus. The Direct Slave is the "Command from the PCI Host," which has highest priority.

For Direct Slave reads, the PCI Bus Master reads data from the Local Bus Slave.

The PCI 9054 supports on-the-fly Endian conversion for Space 0, Space 1, and Expansion ROM space. The Local Bus can be Big/Little Endian by using the programmable internal register configuration.

Note: *The PCI Bus is always Little Endian.*

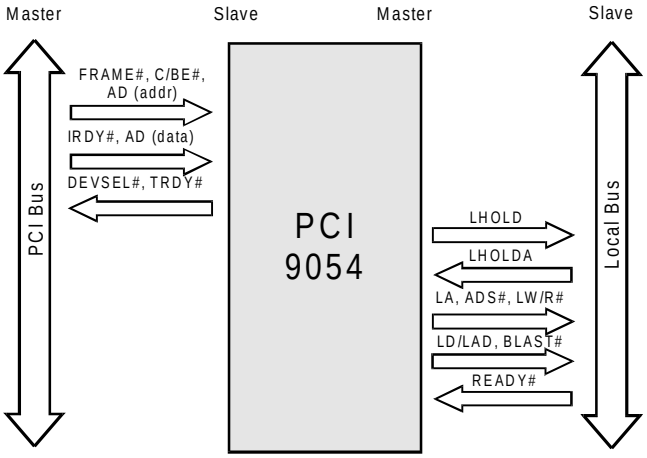


Figure 5-7. Direct Slave Write

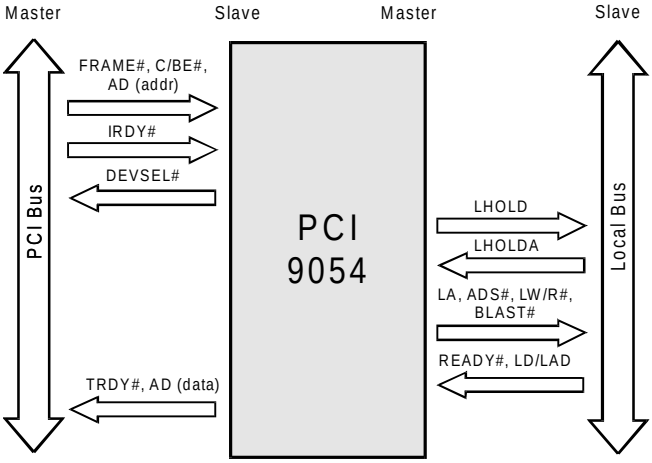


Figure 5-8. Direct Slave Read

Note: *The figures represent a sequence of Bus cycles.*

5.4.2.5 Direct Slave PCI-to-Local Address Mapping

***Note**: Not applicable in I_2O mode.*

Three Local Address spaces—Space 0, Space 1, and Expansion ROM—are accessible from the PCI Bus. Each is defined by a set of three registers:

- Local Address Range (LAS0RR, LAS1RR, and/or EROMRR)
- Local Base Address (LAS0BA, LAS1BA, and/or EROMBA)
- PCI Base Address (PCIBAR2, PCIBAR3, and/or PCIERBAR)

A fourth register, the Bus Region Descriptor register for PCI-to-Local Accesses (LBRD0 and/or LBRD1), defines the Local Bus characteristics for the Direct Slave regions (refer to Figure 5-9).

Each PCI-to-Local Address space is defined as part of reset initialization, as described in Section 5.4.2.5.1. These Local Bus characteristics can be modified at any time before actual data transactions.

5.4.2.5.1 Direct Slave Local Bus Initialization

Range—Specifies which PCI Address bits to use for decoding a PCI access to Local Bus space. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits that must be included in decode and 0 to all others.

Remap PCI-to-Local Addresses into a Local Address Space—Bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor—Specifies the Local Bus characteristics.

5.4.2.5.2 Direct Slave PCI Initialization

After a PCI reset, the software determines how much address space is required by writing all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9054 returns zeroes (0) in the Don't Care Address bits, effectively specifying the address space required. The PCI software then maps the Local Address space into the PCI Address space by programming the PCI Base Address register. (Refer to Figure 5-9.)

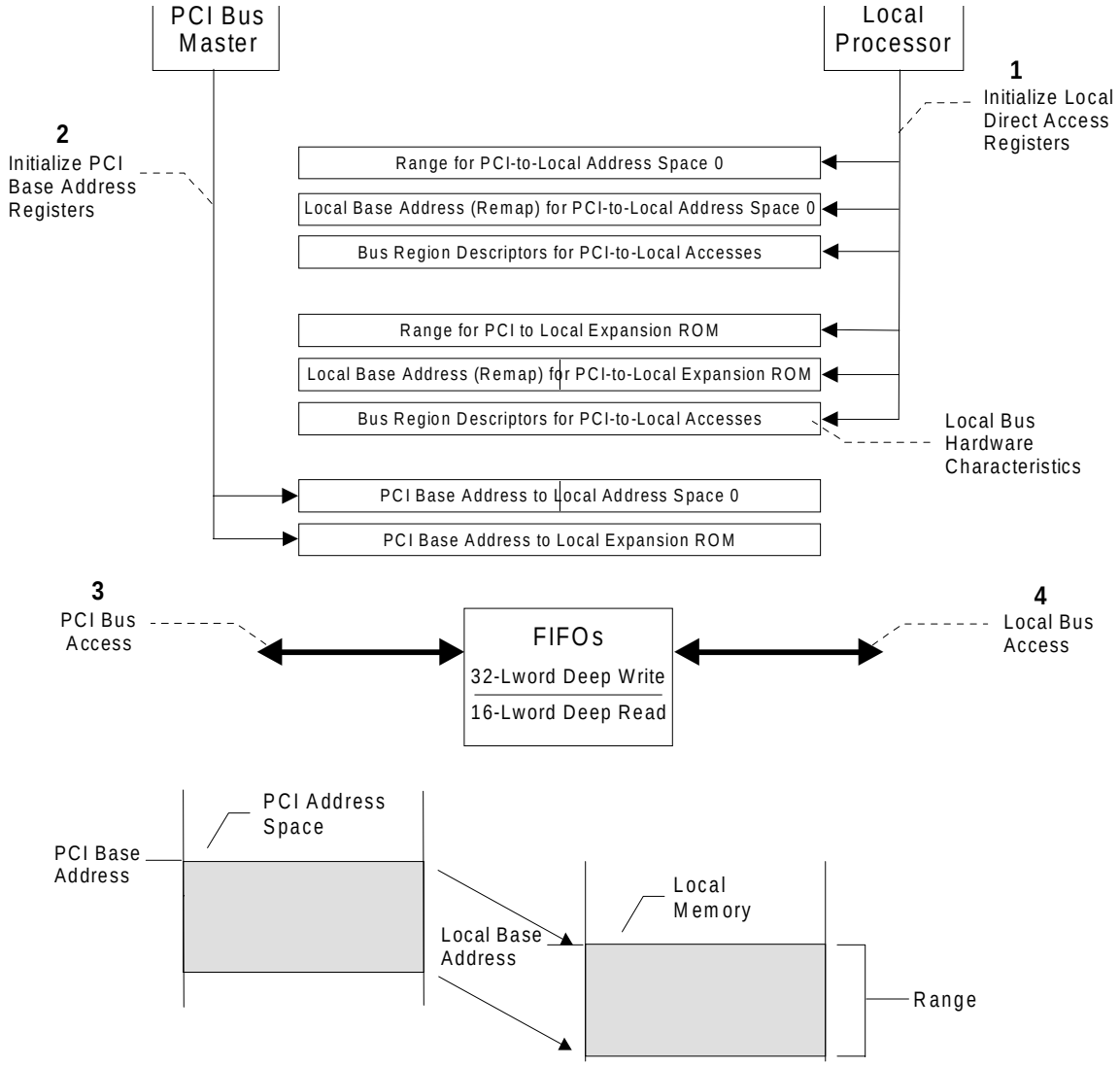


Figure 5-9. Direct Slave Access of the Local Bus

5.4.2.5.3 Direct Slave Byte Enables (C Mode)

During a Direct Slave transfer, each of three spaces (Space 0, Space 1, and Expansion ROM spaces) can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local Byte Enables (LBE[3:0]#).

LBE[3:0]# (PQFP—Pins 91-94; PBGA—Pins P15, N14, L11, and M13) are encoded, based on the configured bus width, as follows:

32-Bit Bus—The four-byte enables indicate which of the four bytes are active during a Data cycle.

- BE3# Byte Enable 3—LD[31:24]
- BE2# Byte Enable 2—LD[23:16]
- BE1# Byte Enable 1—LD[15:8]
- BE0# Byte Enable 0—LD[7:0]

16-Bit Bus—BE3#, BE1# and BE0# are encoded to provide BHE#, LA1, and BLE#, respectively.

- BE3# Byte High Enable (BHE#)—LD[15:8]
- BE2# not used
- BE1# Address bit 1 (LA1)
- BE0# Byte Low Enable (BLE#)—LD[7:0]

8-Bit Bus—BE1# and BE0# are encoded to provide LA1 and LA0, respectively.

- BE3# not used
- BE2# not used
- BE1# Address bit 1 (LA1)
- BE0# Address bit 0 (LA0)

5.4.2.5.4 Direct Slave Byte Enables (J Mode)

During a Direct Slave transfer, each of three spaces (Space 0, Space 1, and Expansion ROM spaces) can be programmed to operate in an 8-, 16-, or 32-bit Local Bus width by encoding the Local Byte Enables (LBE[3:0]#).

LBE[3:0]# (PQFP—Pins 91-94; PBGA—Pins P15, N14, L11, and M13) are encoded, based on the configured bus width, as follows:

32-Bit Bus—The four-byte enables indicate which of the four bytes are active during a Data cycle.

- BE3# Byte Enable 3—LAD[31:24]
- BE2# Byte Enable 2—LAD[23:16]
- BE1# Byte Enable 1—LAD[15:8]
- BE0# Byte Enable 0—LAD[7:0]

16-Bit Bus—BE3#, BE1# and BE0# are encoded to provide BHE#, LAD1, and BLE#, respectively.

- BE3# Byte High Enable (BHE#)—LAD[15:8]
- BE2# not used
- BE1# Address bit 1 (LAD1)
- BE0# Byte Low Enable (BLE#)—LAD[7:0]

8-Bit Bus—BE1# and BE0# are encoded to provide LAD1 and LAD0, respectively.

- BE3# not used
- BE2# not used
- BE1# Address bit 1 (LAD1)
- BE0# Address bit 0 (LAD0)

5.4.2.5.4.1 Direct Slave Example

A 1 MB Local Address Space, 12300000h through 123FFFFFh, is accessible from the PCI Bus at PCI addresses 78900000h through 789FFFFFh.

a. Local initialization software sets the Range and Local Base Address registers as follows:
   - **Range**—FFF00000h (1 MB, decode the upper 12 PCI Address bits)
   - **Local Base Address (remap)**—123XXXXXh, (Local Base Address for PCI-to-Local accesses) [Space Enable bit(s) must be set to be recognized by the PCI Host (LAS0BA[0]=1, LAS1BA[0]=1)]

b. PCI Initialization software writes all ones to the PCI Base Address, then reads it back again.
   - The PCI 9054 returns a value of FFF00000h. The PCI software then writes to the PCI Base Address register(s).
   - **PCI Base Address**—789XXXXXh (PCI Base Address for Access to the Local Address Space registers, PCIBAR2 and PCIBAR3).

For a PCI Direct access to the Local Bus, the PCI 9054 has a 32-Lword (128-byte) Write FIFO and a 16-Lword (64-byte) Read FIFO. The FIFOs enable the Local Bus to operate independent of the PCI Bus. The PCI 9054 can be programmed to return a Retry response or to throttle TRDY# for any PCI Bus transaction attempting to write to the PCI 9054 Local Bus when the FIFO is full.

For PCI Read transactions from the Local Bus, the PCI 9054 holds off TRDY# while gathering data from the Local Bus. For Read accesses mapped to PCI Memory space, the PCI 9054 prefetches up to 16 Lwords (has Continuous Prefetch mode) from the Local Bus. Unused Read data is flushed from the FIFO. For Read accesses mapped to PCI I/O space, the PCI 9054 does not prefetch Read data. Rather, it breaks each read of a Burst cycle into a Single Address/Data cycle on the Local Bus.

The PCI Target Retry Delay Clocks bits (LBRD0[31:28]) can be used to program the period of time in which the PCI 9054 holds off TRDY#. The PCI 9054 issues a Retry to the PCI Bus Transaction Master when the programmed time period expires. This occurs when the PCI 9054 cannot gain control of the Local Bus and return TRDY# within the programmed time period.

5.4.2.6 Direct Slave Priority

Direct Slave accesses have a higher priority than DMA accesses, thereby preempting DMA transfers. During a DMA transfer, if the PCI 9054 detects a pending Direct Slave access, it releases the Local Bus within two Data transfers. The PCI 9054 resumes operation after the Direct Slave access completes.

When the PCI 9054 DMA controller owns the Local Bus, its LHOLD output and LHOLDA input are asserted. When a Direct Slave access occurs, the PCI 9054 releases the Local Bus within two Lword transfers by de-asserting LHOLD and floating the Local Bus outputs. After the PCI 9054 acknowledges that LHOLDA is de-asserted, it requests the Local Bus for a Direct Slave transfer by asserting LHOLD. When the PCI 9054 receives LHOLDA, it drives the bus and performs the Direct Slave transfer. Upon completing a Direct Slave transfer, the PCI 9054 releases the Local Bus by de-asserting LHOLD and floating the Local Bus outputs. After the PCI 9054 samples LHOLDA is de-asserted and the Local Bus Pause Timer is set to zero, it requests a DMA transfer from the Local Bus by re-asserting LHOLD. When it receives LHOLDA, it drives the bus and continues the DMA transfer.

5.4.3 Deadlock Conditions

Deadlock can occur when a PCI Bus Master must access the PCI 9054 Local Bus at the same time a Master on the PCI 9054 Local Bus must access the PCI Bus.

There are two types of deadlock:

- **Partial Deadlock**—A Local Bus Master is performing a Direct Bus Master access to a PCI Bus device other than the PCI Bus device concurrently trying to access the Local Bus
- **Full Deadlock**—A Local Bus Master is performing a Direct Bus Master access to the same PCI Bus device concurrently trying to access the Local Bus

This applies only to Direct Master and Direct Slave accesses through the PCI 9054. Deadlock does not occur in transfers through the PCI 9054 DMA channels or the PCI 9054 internal registers (such as mailboxes).

For partial deadlock, the PCI access to the Local Bus times out (the PCI Target Retry Delay Clock (LBRD0[31:28]), which is programmable through the Local Bus Region Descriptor register) and the PCI 9054 responds with a PCI Retry. The PCI Specification requires that a PCI Master release its request for the PCI Bus (de-assert REQ#) for a minimum of two PCI clocks after receiving a Retry. This allows the PCI Bus arbiter to grant the PCI Bus to the PCI 9054 so that it can complete its Direct Master access and free up the Local Bus. Possible solutions are described in the following sections for cases in which the PCI Bus arbiter does not function as described (PCI Bus architecture dependent), waiting for a time out is undesirable, or a full deadlock condition exists.

For full deadlock, the only solution is to back off the Local Bus Master.

5.4.3.1 Backoff

The PCI 9054 BREQo signal indicates whether a possible deadlock condition exists. The PCI 9054 starts the Backoff Timer (programmable through registers) when it detects the following conditions:

- A PCI Bus Master is attempting to access memory or an I/O device on the Local Bus and is not gaining access (*for example*, LHOLDA is not received).
- A Local Bus Master is performing a Direct Bus Master Read access to the PCI Bus. Or, a Local Bus Master is performing a Direct Bus Master Write access to the PCI Bus and the PCI 9054 Direct Master Write FIFO cannot accept another Write cycle.

If the Local Bus Backoff Enable bit is enabled (EROMBA[4]=1) and expires and the PCI 9054 has not received BG#, the PCI 9054 asserts BREQo. External bus logic can use this signal to perform backoff.

The Backoff cycle is device/bus architecture dependent. External logic (an arbiter) can assert the necessary signals necessary to cause a Local Bus Master to release a Local Bus (backoff). After the Local Bus Master backs off, it can grant the bus to the PCI 9054 by asserting LHOLDA.

Once BREQo is asserted, READY# for the current Data cycle is never asserted (the Local Bus Master must perform backoff). When the PCI 9054 detects LHOLDA, it proceeds with the PCI Master-to-Local-Bus access. When this access completes and the PCI 9054 releases the Local Bus, external logic can release the backoff and the Local Bus Master can resume the cycle interrupted by the Backoff cycle. The PCI 9054 Write FIFO retains all data it acknowledged (*that is*, the last data for which READY# was asserted).

After the backoff condition ends, the Local Bus Master restarts the last cycle with ADS#. For writes, data following ADS# should be the data the PCI 9054 did not acknowledge prior to the Backoff cycle (*for example*, the last data for which READY# is not asserted).

If a PCI Read cycle completes when the Local Bus is backed off, the Local Bus Master receives that data if the Local Master restarts the same last cycle (data is not read twice). A new read is performed if the resumed Local Bus cycle is not the same as the Backed Off cycle.

5.4.3.1.1 Software/Hardware Solution for Systems without Backoff Capability

For adapters that do not support backoff, a possible deadlock solution is as follows.

PCI Host software, external Local Bus hardware, general purpose output USERo and general purpose input USERi can be used by the PCI Host software to prevent deadlock. USERo can be asserted to request that the external arbiter not grant the bus to any Local Bus Master except the PCI 9054. Status output from the Local arbiter can be connected to the general purpose input USERi to indicate that no Local Bus Master owns the Local Bus, or the PCI Host to determine that no Local Bus Master that currently owns the Local Bus can read input. The PCI Host can then perform Direct Slave access. When the Host finishes, it de-asserts USERo.

5.4.3.1.1.1 Preempt Solution

For devices that support preempt, USERo can be used to preempt the current Bus Master device. When USERo is asserted, the current Local Bus Master device completes its current cycle and releases the Local Bus, de-asserting LHOLD.

5.4.3.1.2 Software Solutions to Deadlock

Both PCI Host and Local Bus software can use a combination of mailbox registers, doorbell registers, interrupts, direct Local-to-PCI accesses and direct PCI-to-Local accesses to avoid deadlock.

5.5 C and J Modes DMA Operation

The PCI 9054 supports two independent DMA channels capable of transferring data from the:

- Local-to-PCI Bus
- PCI-to-Local Bus

Each channel consists of a DMA controller and a dedicated bidirectional FIFO. Both channels support Block transfers, Scatter/Gather transfers, with or without End of Transfer (EOT#). Only DMA Channel 0 supports Demand mode DMA transfers. Master mode must be enabled with the Master Enable bit (PCICR[2]) before the PCI 9054 can become a PCI Bus Master. In addition, both DMA channels can be programmed to

- Operate in 8-, 16-, or 32-bit Local Bus width
- Use zero to 15 internal wait states (Local Bus)
- Enable/disable internal wait states (Local Bus)
- Enable/disable Local Bus Burst capability
- Limit Local Bus bursts to four (BTERM# enable/disable)
- Hold Local address constant (Local Target is FIFO) or increment
- Perform PCI Memory Write and Invalidate (command code = Fh) or normal PCI Memory Write (command code = 7h)
- Pause Local transfer with/without BLAST# (DMA Fast/Slow termination)
- Assert PCI interrupt (INTA#) or Local interrupt (LINT#) when DMA transfer is complete or Terminal Count is reached during Scatter/Gather DMA mode transfers
- Operate in DMA Clear Count mode (only if the descriptor is in Local memory)

The PCI 9054 also supports PCI Dual Address with the upper 32-bit registers (DMADAC0 and DMADAC1). The Local Bus Latency Timer determines the number of Local clocks the PCI 9054 can burst data before relinquishing the Local Bus. The Local Pause Timer sets how soon the DMA channel can request the Local Bus.

5.5.1 DMA PCI Dual Address Cycle

The PCI 9054 supports PCI Dual Address Cycle (DAC) when it is a PCI Bus Master using the DMDAC register for Direct Master transactions. The DAC command is used to transfer a 64-bit address to devices that support 64-bit addressing when the address is not in the low 4-GB Address space. The PCI 9054 performs a DAC within two PCI clock periods, where the first PCI address is a Lo-Addr with the command (C/BE[3:0]#) “D” and the second PCI address will be a Hi-Addr with the command (C/BE[3:0]#) “6” or “7”, depending upon it being a PCI Read or a PCI Write cycle. Whenever the DMDAC register contains a value of 0x00000000, the PCI 9054 performs a Single Address Cycle (SAC) on the PCI Bus. (Refer to Figure 5-10.)

5.5.2 Block DMA Mode

The Host processor or the Local processor sets the Local and PCI starting addresses, transfer byte count, and transfer direction. The Host or Local processor then sets the DMA Start bit to initiate a transfer. The PCI 9054 arbitrates the PCI and Local Buses and transfers data. Once the transfer completes, the PCI 9054 sets the Channel Done bit(s) (DMACSR0[4]=1 and/or DMACSR1[4]=1) and, if enabled, asserts an interrupt(s) (DMAMODE0[10] and/or DMAMODE1[10]) to the Local processor or the PCI Host (programmable). The Channel Done bit(s) can be polled, instead of interrupt generation, to indicate the DMA transfer status.

DMA registers are accessible from the PCI and Local Buses (refer to Figure 5-10).

During DMA transfers, the PCI 9054 is a Master on both the PCI and Local Buses. For simultaneous access, Direct Slave or Direct Master has a higher priority than DMA.

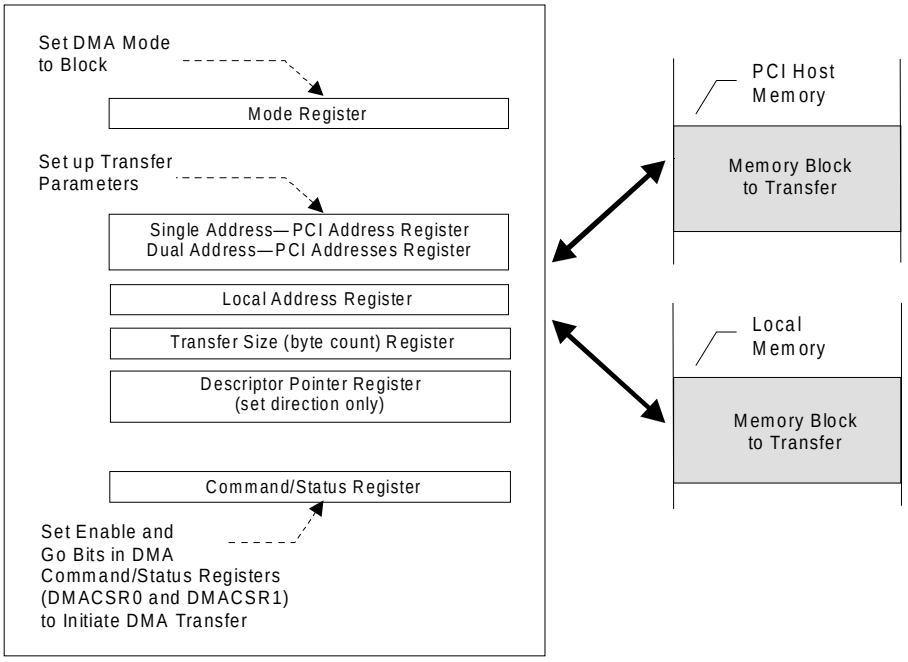


Figure 5-10. Block DMA Mode Initialization (Single Address or Dual Address PCI)

The PCI 9054 releases the PCI Bus if one of the following conditions occur (refer to Figure 5-11 and Figure 5-12):

- FIFO is full (PCI-to-Local Bus)
- FIFO is empty (Local-to-PCI Bus)
- Terminal count is reached
- PCI Bus Latency Timer expires (PCILTR[7:0])—normally programmed by the Host PCI BIOS—and PCI GNT# de-asserts
- PCI Host asserts STOP#

The PCI 9054 releases the Local Bus if one of the following conditions occurs:

- FIFO is empty (PCI-to-Local Bus)
- FIFO is full (Local-to-PCI Bus)
- Terminal count is reached
- Local Bus Latency Timer is enabled and expires (MARBR[7:0])
- Special cycle BREQi# is asserted
- Direct Slave request is pending

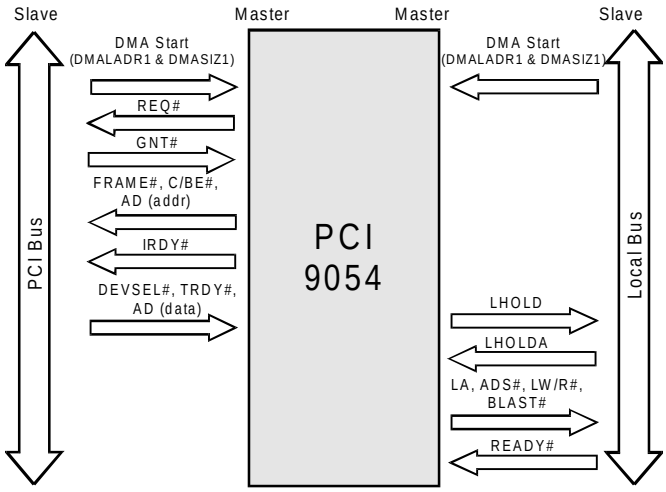


Figure 5-11. DMA, PCI-to-Local Bus

Note: *The figure represents a sequence of Bus cycles.*

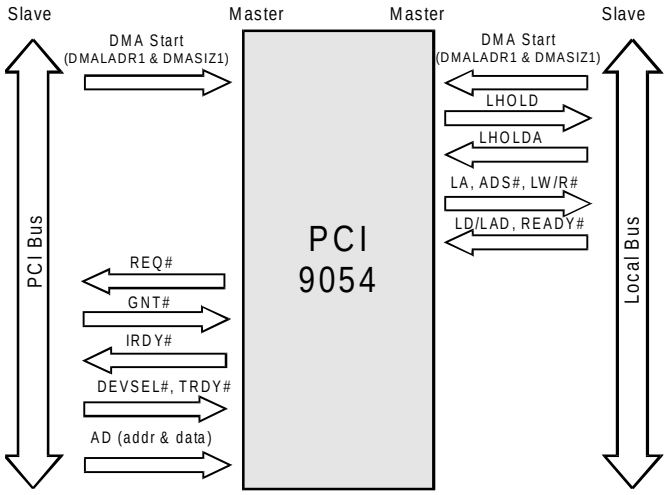


Figure 5-12. DMA, Local-to-PCI Bus

Note: *The figure represents a sequence of Bus cycles.*

Table 5-2. DMA Local Burst Mode

Burst Enable Bit	BTERM# Enable Bit	Result
0	X	Single cycle
1	0	Burst up to four Data cycles
1	1	Burst forever (terminate when BTERM# is asserted or transfer is completed)

Note: *"X" is "Don't Care."*

5.5.2.1 Block DMA PCI Dual Address Cycle

The PCI 9054 supports the DAC feature in Block DMA mode. Whenever the DMADAC0 or DMADAC1 registers contain a value of 0x00000000, the PCI 9054 performs a Single Address Cycle (SAC) on the PCI Bus. Any other value causes a Dual Address to appear on the PCI Bus. (Refer to Figure 5-13.)

5.5.3 Scatter/Gather DMA Mode

In Scatter/Gather DMA mode, the Host processor or Local processor sets up descriptor blocks in Local or Host memory composed of PCI and Local addresses, transfer count, transfer direction, and address of next descriptor block (refer to Figure 5-14 and Figure 5-15). The Host or Local processor then

- Enables the Scatter/Gather mode bit(s) (DMAMODE0[9]=1 and/or DMAMODE1[9]=1)
- Sets up the address of initial descriptor block in the PCI 9054 Descriptor Pointer register(s) (DMADPR0 and/or DMADPR1)
- Initiates the transfer by setting a control bit(s) (DMACSR0[1:0] and/or DMACSR1[1:0])

The PCI 9054 loads the first descriptor block and initiates the Data transfer. The PCI 9054 continues to load descriptor blocks and transfer data until it detects the End of Chain bit(s) (DMADPR0[1] and/or DMADPR1[1]) is set (these bits are part of each descriptor). When the End of Chain bit(s) is detected, the PCI 9054 completes the current descriptor block and sets the DMA Done bit(s) (DMACSR0[4] and/or DMACSR1[4]). If the End of Chain bit(s) are detected, the PCI 9054 asserts a PCI interrupt (INTA#) and/or Local interrupt (LINT#).

The PCI 9054 can also be programmed to assert PCI or Local interrupts after each descriptor is loaded, then finish transferring.

If Scatter/Gather descriptors are in Local memory, the DMA controller can be programmed to clear the transfer size at completion of each DMA, using the DMA Clear Count Mode bit(s) (DMAMODE0[16] and/or DMAMODE1[16]).

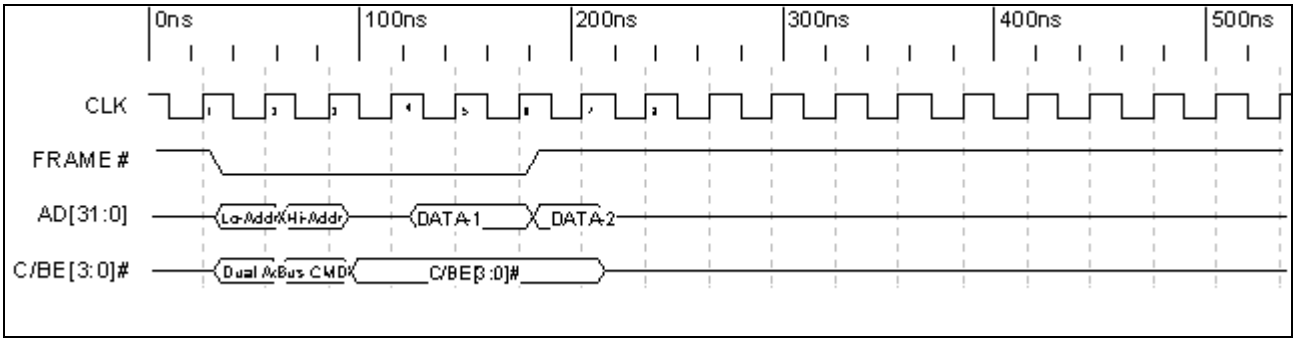


Figure 5-13. Dual Address Timing

Notes: *In Scatter/Gather DMA mode, the descriptor includes the PCI and Local Address Space, transfer size, and next descriptor pointer. It also includes a DAC value if DMADPR0[18] and/or DMAMODE1[I8] is enabled. Otherwise, the register value is used. The Descriptor Pointer register(s) (DMADPR0 and/or DMADPR1) contains end of chain (bit 1), direction of transfer (bit 3), next descriptor address (bits [31:4]), interrupt after terminal count (bit 2), and next descriptor location (bit 0) bits.*

The Local Bus width must be the same as Local memory bus width.

A DMA descriptor can be on the Local memory or the PCI memory, or both (for example, one descriptor on Local memory, another descriptor on PCI memory and vice-versa).

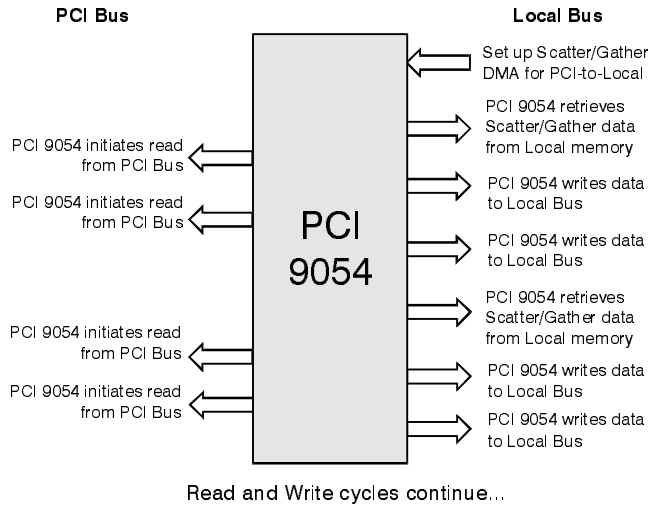


Figure 5-14. Scatter/Gather DMA Mode from PCI-to-Local Bus (Control Access from the Local Bus)

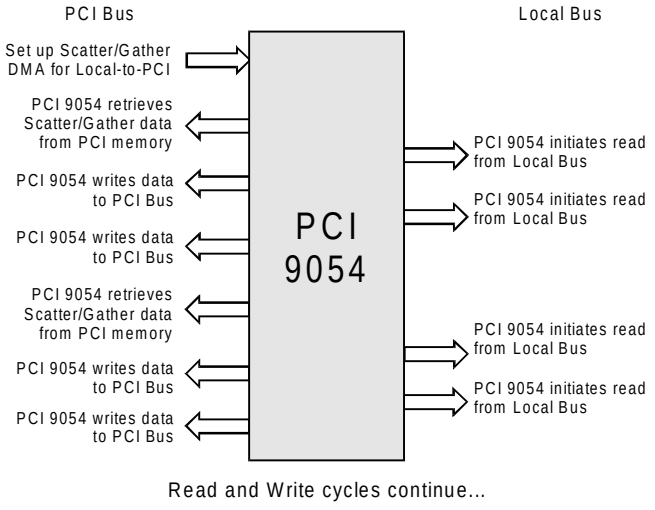


Figure 5-15. Scatter/Gather DMA Mode from Local-to-PCI Bus (Control Access from the PCI Bus)

Note: *The figures represent a sequence of Bus cycles.*

5.5.3.1 Scatter/Gather DMA PCI Dual Address Cycle

The PCI 9054 supports the PCI DAC feature in Scatter/Gather DMA mode for Data transfers only. The descriptor blocks should reside below the 4-GB Address space. The PCI 9054 offers three different options of how PCI DAC Scatter/Gather DMA is utilized. Assuming the descriptor blocks are located on the PCI Bus:

- DMADAC0 and/or DMADAC1 contain(s) a non-zero value. DMAMODE0[18] and/or DMAMODE1[18] is set to 0. The PCI 9054 performs a Single Address Cycle (SAC) four-Lword descriptor block load from PCI memory and DMA transfer with DAC on the PCI Bus. (Refer to Figure 5-16.)
- DMADAC0 and/or DMADAC1 contain(s) an 0x00000000 value. DMAMODE0[18] and/or DMAMODE1[18] is set to 1. The PCI 9054 performs a SAC five-Lword descriptor block load from PCI memory and DMA transfer with PCI DAC on the PCI Bus. (Refer to Figure 5-17.)
- DMADAC0 and/or DMADAC1 contain(s) a non-zero value. DMAMODE0[18] and/or DMAMODE1[18] is set to 1. The PCI 9054 performs a SAC five-Lword descriptor block load from PCI memory and DMA transfer with DAC on the PCI Bus. The fifth descriptor overwrites the value of the DMADAC0 and/or DMADAC1 register. (Refer to Figure 5-17.)

5.5.3.2 DMA Clear Count Mode

The PCI 9054 supports DMA Clear Count mode (Write-Back feature, DMAMODE0[16] and DMAMODE1[16]). This feature allows users to control the data transfer blocks during Scatter/Gather DMA operations. The PCI 9054 clears the Transfer Size descriptor to zero by writing to a descriptor-memory location at the end of each transfer chain. This feature works only if DMA descriptors are on the Local Bus.

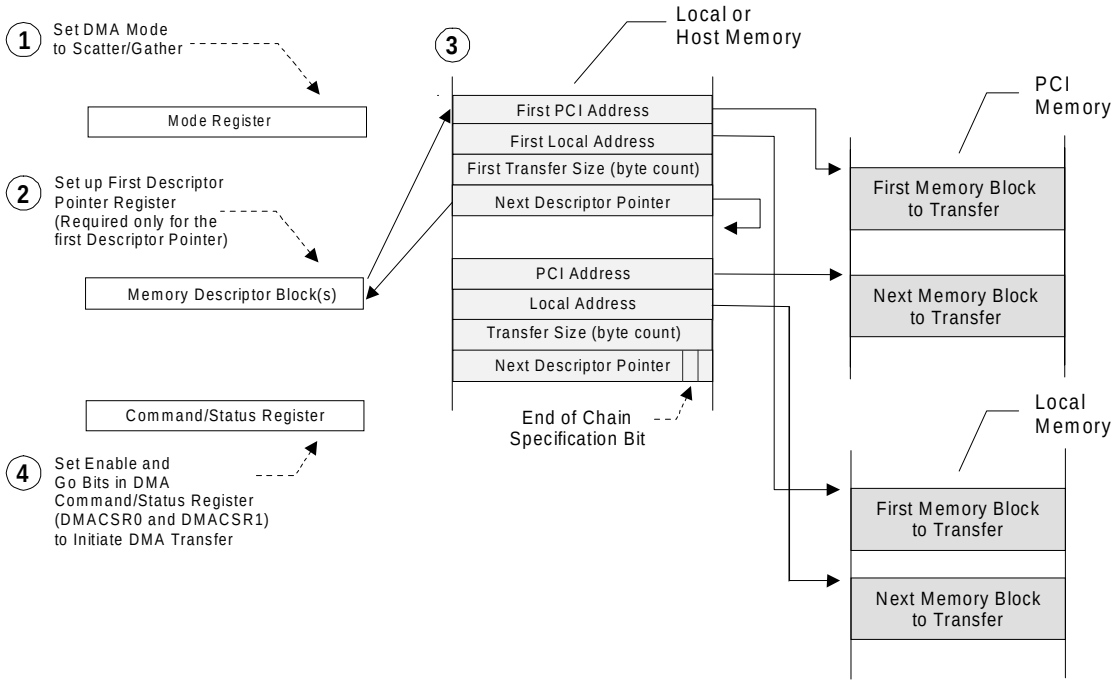


Figure 5-16. Scatter/Gather DMA Mode Descriptor Initialization [PCI SAC/DAC PCI Address (DMADAC0, DMADAC1) Register Dependent]

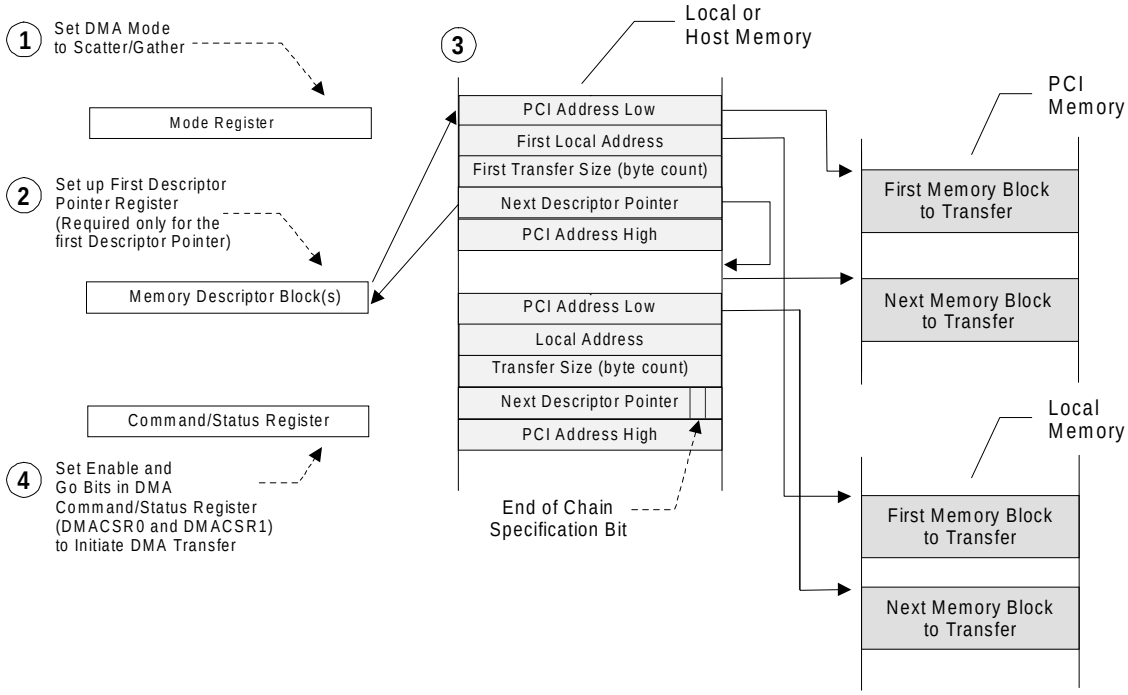


Figure 5-17. Scatter/Gather DMA Mode Descriptor Initialization [DAC PCI Address (DMAMODE0[18], DMAMODE1[18]) Descriptor Dependent]

5.5.4 DMA Memory Write and Invalidate

The PCI 9054 can be programmed to perform Memory Write and Invalidate cycles to the PCI Bus for DMA transfers, as well as Direct Master transfers (refer to Section 5.4.1.9). The PCI 9054 supports Memory Write and Invalidate transfers for cache line sizes of 8 or 16 Lwords. Size is specified in the System Cache Line Size bits (PCICLSR[7:0]). If a size other than 8 or 16 is specified, the PCI 9054 performs Write transfers rather than Memory Write and Invalidate transfers.

DMA Memory Write and Invalidate transfers are enabled when the DMA controller Memory Write and Invalidate Enable bit(s) (DMAMODE0[13] and/or DMAMODE1[13]) and the Memory Write and Invalidate Enable bit (PCICR[4]) are set.

In Memory Write and Invalidate mode, the PCI 9054 waits until the number of Lwords required for specified cache line size are read from the Local Bus before starting the PCI access. This ensures a complete cache line write can complete in one PCI Bus ownership. If a Target disconnects before a cache line completes, the PCI 9054 completes the remainder of that cache line, using normal writes before resuming Memory Write and Invalidate transfers. If a Memory Write and Invalidate cycle is in progress, the PCI 9054 continues to burst if another cache line is read from the Local Bus before the cycle completes. Otherwise, the PCI 9054 terminates the burst and waits for the next cache line to be read from the Local Bus. If the final transfer is not a complete cache line, the PCI 9054 completes the DMA transfer, using normal writes.

5.5.4.1 DMA Abort

DMA transfers can be aborted, in addition to the EOT# signal, as follows:

1. Set the Channel Enable bit(s) (DMACSR0[0]=1 and/or DMACSR1[0]=1).
2. Set the Channel Start bit(s) (DMACSR0[1]=1 and/or DMACSR1[1]=1).
3. Clear the DMA Channel Enable bit(s) (DMACSR0[0]=0 and/or DMACSR1[0]=0).
4. Abort DMA by setting the Channel Abort bit(s) (DMACSR0[2]=1 and/or DMACSR1[2]=1).
5. Wait until the Channel Done bit(s) is set (DMACSR0[4]=1 and/or DMACSR1[4]=1).

Note: *One to two Data transfers occur after the Abort bit is set. Aborting when no DMA cycles are in progress causes the next DMA to abort.*

5.5.5 DMA Priority

The DMA Channel Priority bit (MARBR[20:19]) can be used to specify the following priorities:

- Rotating (MARBR[20:19]=00)
- DMA Channel 0 (MARBR[20:19]=01)
- DMA Channel 1 (MARBR[20:19]=10)

5.5.6 DMA Channel 0/1 Interrupts

A DMA channel can assert a PCI Bus or Local Bus interrupt when done (transfer complete) or after a transfer is complete for the current descriptor in Scatter/Gather DMA mode. The DMA Channel Interrupt Select bit(s) determine whether to assert a PCI (DMAMODE0[17]=1 and/or DMAMODE1[17]=1) or Local (DMAMODE0[17]=0 and/or DMAMODE1[17]=0) interrupt. The Local or PCI processor can read the DMA Channel 0 Interrupt Active bits to determine whether a DMA Channel 0 (INTCSR[21]) or DMA Channel 1 (INTCSR[22]) interrupt is pending.

The Channel Done bit(s) (DMACSR0[4] and/or DMACSR1[4]) can be used to determine whether an interrupt is:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt

The Done Interrupt Enable bit(s) (DMAMODE0[10] and/or DMAMODE1[10]) enable a Done interrupt. In Scatter/Gather DMA mode, a bit in the Next Descriptor Pointer register of the channel (loaded from Local memory) specifies whether to assert an interrupt at the end of the transfer for the current descriptor.

A DMA Channel interrupt is cleared by the Channel Clear Interrupt bit(s) (DMACSR0[3]=1 and/or DMACSR1[3]=1).

5.5.7 DMA Data Transfers

The PCI 9054 DMA controller can be programmed to transfer data from the Local Bus to the PCI Bus or from the PCI Bus to the Local Bus.

5.5.7.1 Local-to-PCI Bus DMA Transfer

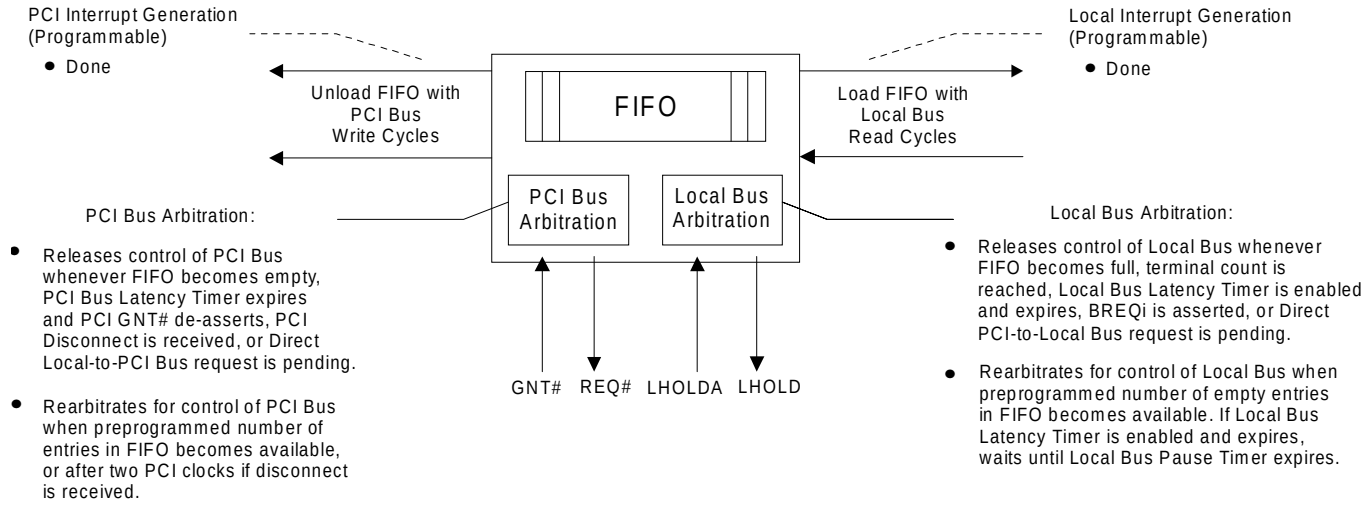


Figure 5-18. Local-to-PCI Bus DMA Data Transfer Operation

5.5.7.2 PCI-to-Local Bus DMA Transfer

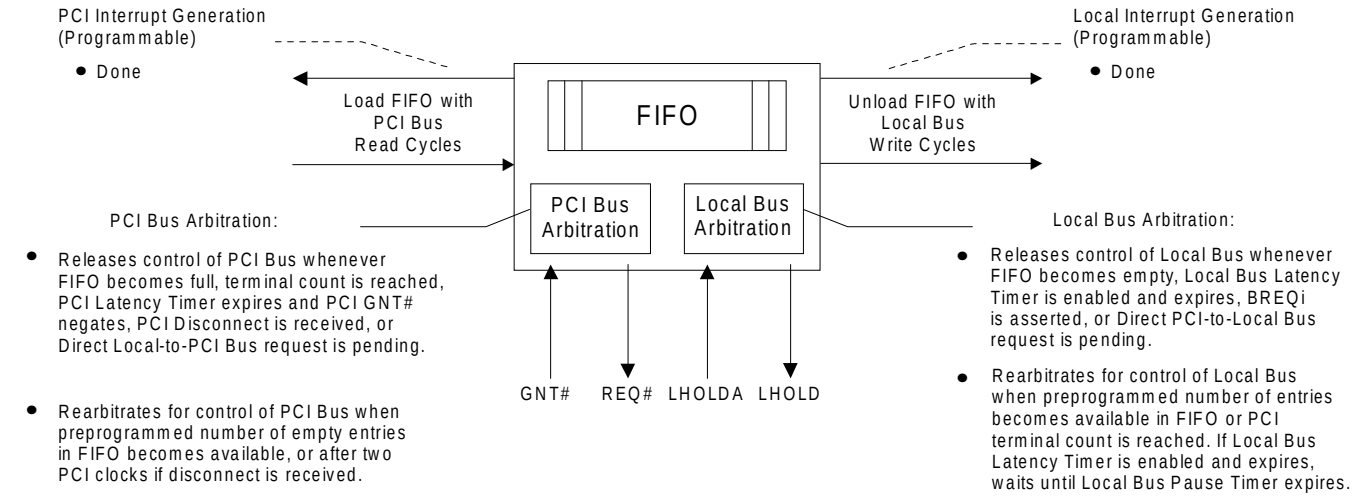


Figure 5-19. PCI-to-Local Bus DMA Data Transfer Operation

5.5.7.3 DMA Unaligned Transfers

For unaligned Local-to-PCI transfers, the PCI 9054 reads a partial Lword from the Local Bus. It continues to read Lwords from the Local Bus. Lwords are assembled, aligned to the PCI Bus address, and loaded into the FIFO.

For PCI-to-Local transfers, Lwords are read from the PCI Bus and loaded into the FIFO. On the Local Bus, Lwords are assembled from the FIFO, aligned to the Local Bus address and written to the Local Bus.

On both the PCI and Local Buses, the byte enables for writes determine LA[1:0] for the start of a transfer. For the last transfer, byte enables specify the bytes to be written. All reads are Lwords.

5.5.8 Demand Mode DMA, Channel 0

The Fast/Slow Terminate Mode Select bit(s) (DMAMODE0[15] and/or DMAMODE1[15]) determines the number of Lwords to transfer after the DMA controller DREQ0# input is de-asserted.

If BLAST# output is not required for the last Lword of a DMA transfer (bit [15]=1), the DMA controller releases the data bus after it receives an external READY# or the internal wait state counter decrements to 0 for the current Lword. If the DMA controller is currently bursting data, which is not the last Data phase for the Burst, BLAST# is not asserted.

If BLAST# output is required for the last Lword of the DMA transfer (bit [15]=0), the DMA controller transfers one or two Lwords. If DREQ0# is de-asserted during the Address phase of the first transfer in the PCI 9054 Local Bus ownership (ADS#, LHOLDA asserted), the DMA controller completes current Lword. If DREQ0# is de-asserted during any phase other than the Address phase of the first transfer in the PCI 9054 Local Bus ownership, the DMA controller completes the current Lword, and one additional Lword (this allows BLAST# output to be asserted during the final Lword). If the DMA FIFO is full or empty after the Data phase in which DREQ0# is de-asserted, the second Lword is not transferred.

DREQ0# controls only the number of Lword transfers. For an 8-bit bus, the PCI 9054 releases the bus after transferring the last byte for the Lword. For a 16-bit bus, the PCI 9054 releases the bus after transferring the last word for the Lword. (Refer to the timing diagrams in Section 5.6 for C mode and in Section 5.7 for J mode.)

5.5.9 End of Transfer (EOT#) Input

The DMA EOT# Enable bit(s) (DMAMODE0[14] and/or DMAMODE1[14]) determines the number of Lwords to transfer after a DMA controller asserts EOT# input. EOT# input should be asserted only when the PCI 9054 owns a bus.

If BLAST# output is not required for the last Lword of the DMA transfer (DMAMODE0[14]=1 and/or DMAMODE1[14]=1), the DMA controller releases the data bus and terminates DMA after it receives an external READY#. Or, the internal wait state counter decrements to 0 for the current Lword. If the DMA controller is currently bursting data that is not the last Data phase for the burst, BLAST# output is not asserted.

If BLAST# output is required for last Lword of the DMA transfer (DMAMODE0[14]=0 and/or DMAMODE1[14]=0), the DMA controller transfers one or two Lwords. If EOT# is asserted, the DMA controller completes the current Lword and one additional Lword (this allows BLAST# output to be asserted during the final Lword). If the DMA FIFO is full or empty after the Data phase in which EOT# is asserted, the second Lword is not transferred.

The DMA controller terminates a transfer on an Lword boundary after EOT# is asserted. For an 8-bit bus, the PCI 9054 terminates after transferring the last byte for the Lword. For a 16-bit bus, the PCI 9054 terminates after transferring the last word for the Lword.

During the descriptor loading on the Local Bus, assertion of EOT# causes a complete descriptor load and no subsequent Data transfer; however, this is not recommended. This has no effect when the descriptor is loaded from the PCI Bus.

5.5.10 DMA Arbitration

The PCI 9054 DMA controller releases control of the Local Bus (de-asserts LHOLD) when one of the following conditions occur:

- Local Bus Latency Timer is enabled and expires (MARBR[7:0])
- BREQi is asserted (BREQi can be enabled or disabled, or gated with a Local Bus Latency Timer before the PCI 9054 releases the Local Bus)
- Direct Slave access is pending
- EOT# input is received (if enabled)

The DMA controller releases control of the PCI Bus when one of the following conditions occurs:

- FIFOs are full or empty
- PCI Bus Latency Timer expires (PCILTR [7:0])—and loses the PCI GNT# signal
- Target disconnect response is received

The DMA controller de-asserts its PCI Bus request (REQ#) for a minimum of two PCI clocks.

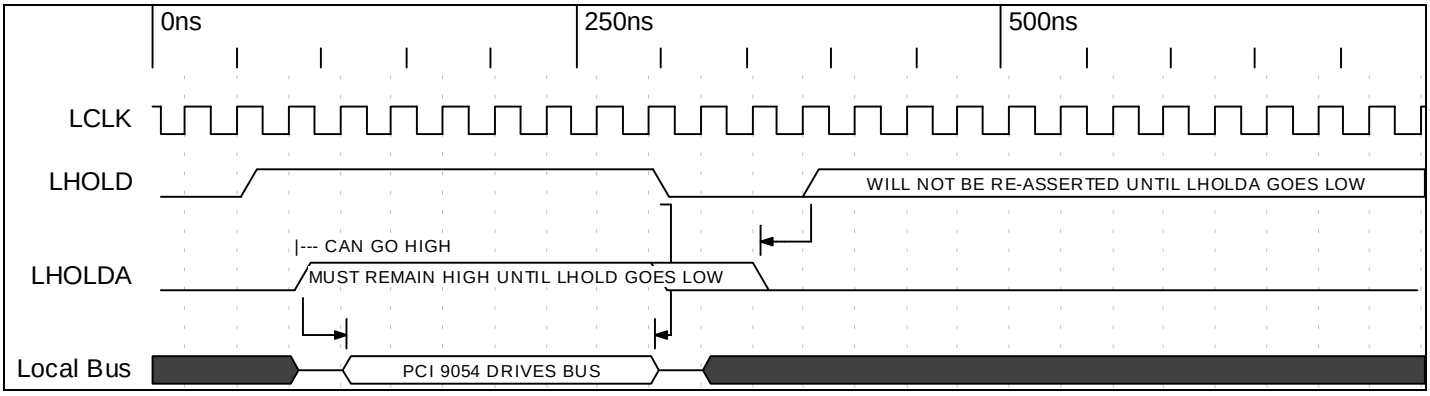
5.5.11 Local Bus Latency and Pause Timers

The Local Bus Latency and Pause Timers are programmable with the Mode/DMA Arbitration register (MARBR[7:0, 15:8]). If the Local Bus Latency Timer is enabled and expires (MARBR[7:0]), the PCI 9054 completes the current Lword transfer and releases LHOLD. After its programmable Pause Timer expires (MARBR[7:0]), it reasserts LHOLD. It continues to transfer when it receives LHOLDA. The PCI Bus transfer continues until the FIFO is empty for a Local-to-PCI transfer or full for a PCI-to-Local transfer.

The DMA transfer could be paused by writing a 0 to the Channel Enable bit. To acknowledge the disable, the PCI 9054 gets at least one data from the bus before it stops. However, this is not recommended during a burst.

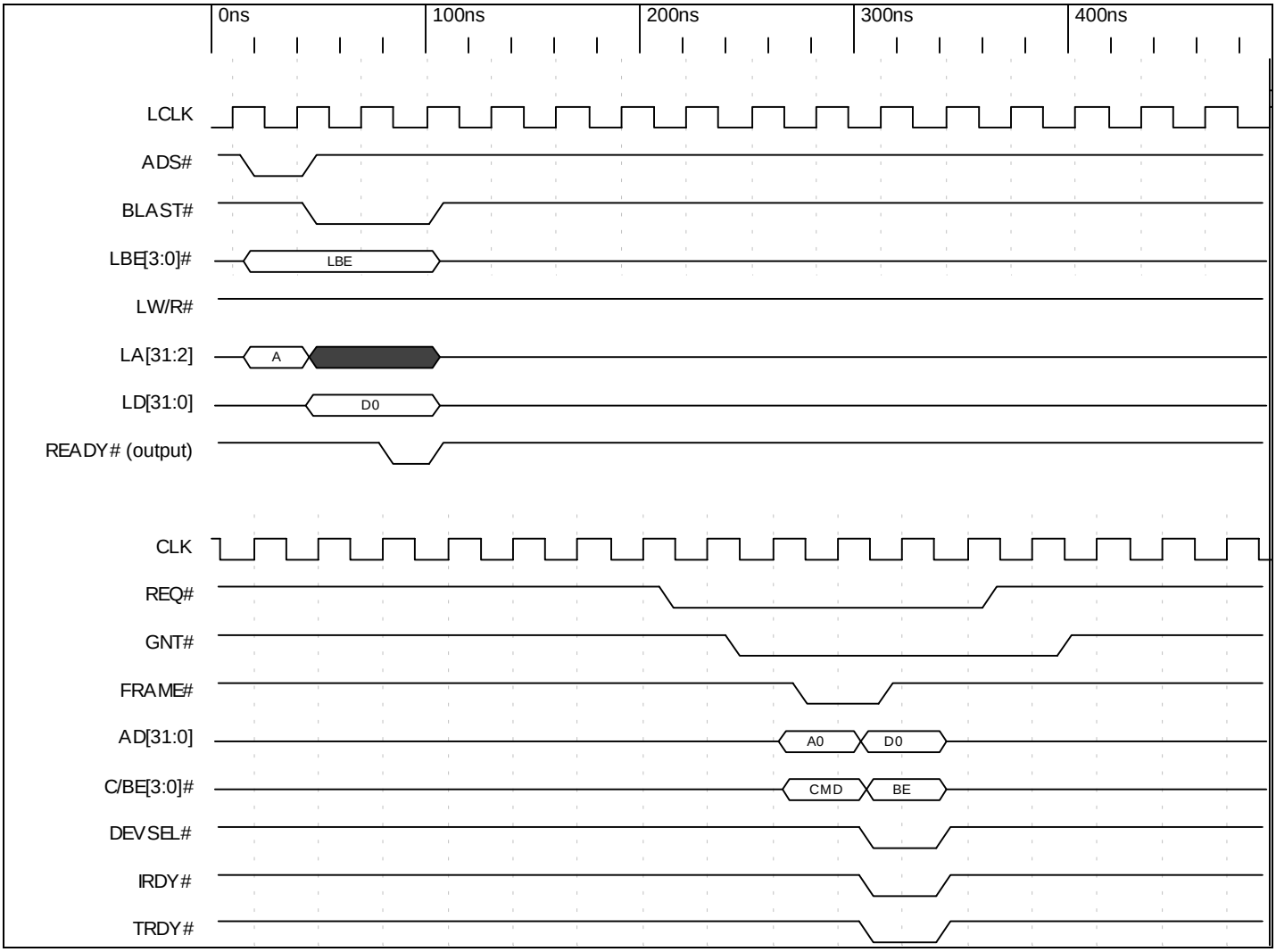
The DMA Local Bus Timer starts after the Local Bus is granted to the PCI 9054 and the Local Pause Timer starts after LHOLDA is de-asserted.

5.6 C Mode Timing Diagrams

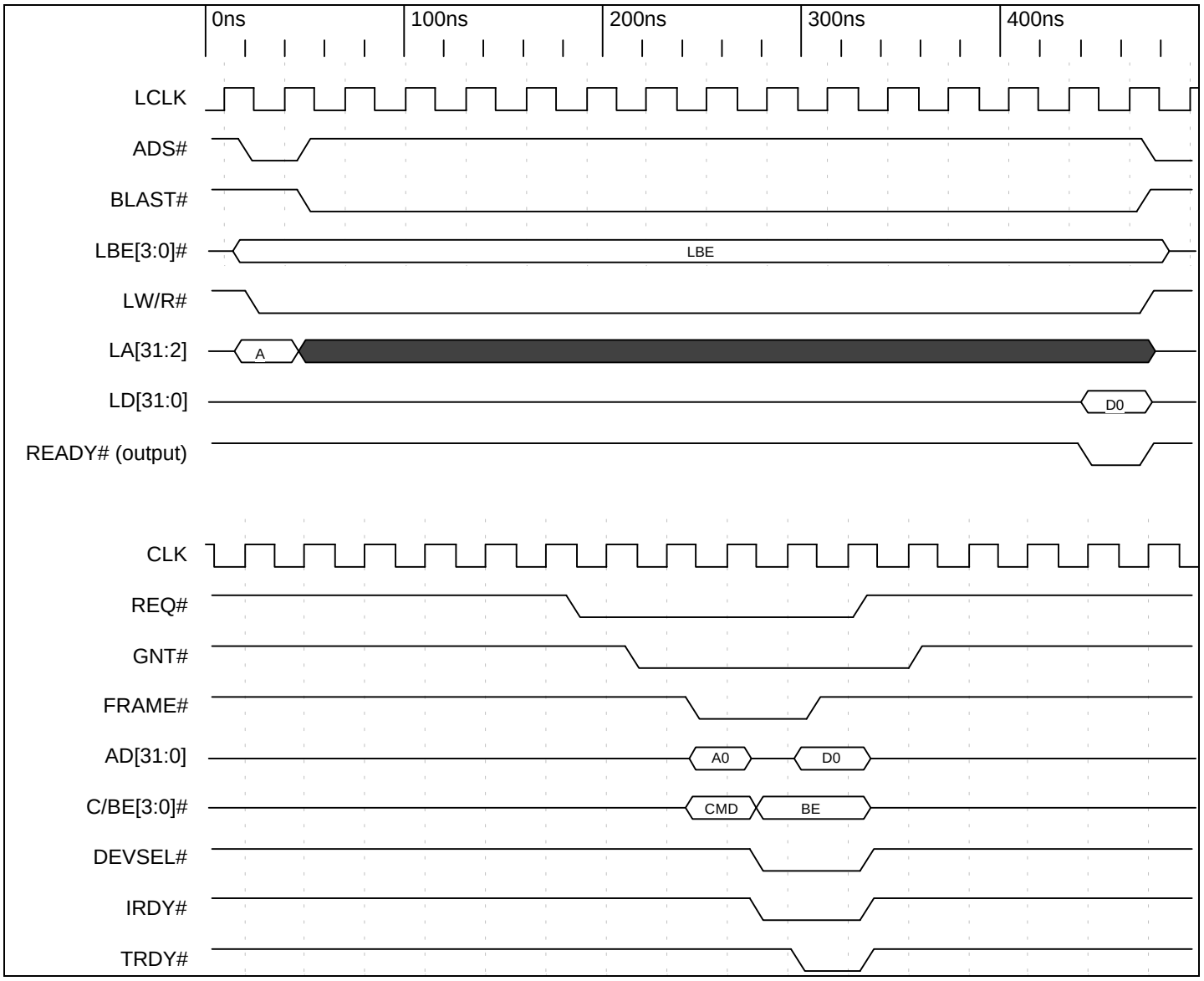


Timing Diagram 5-1. Local Bus Arbitration (LHOLD and LHOLDA)

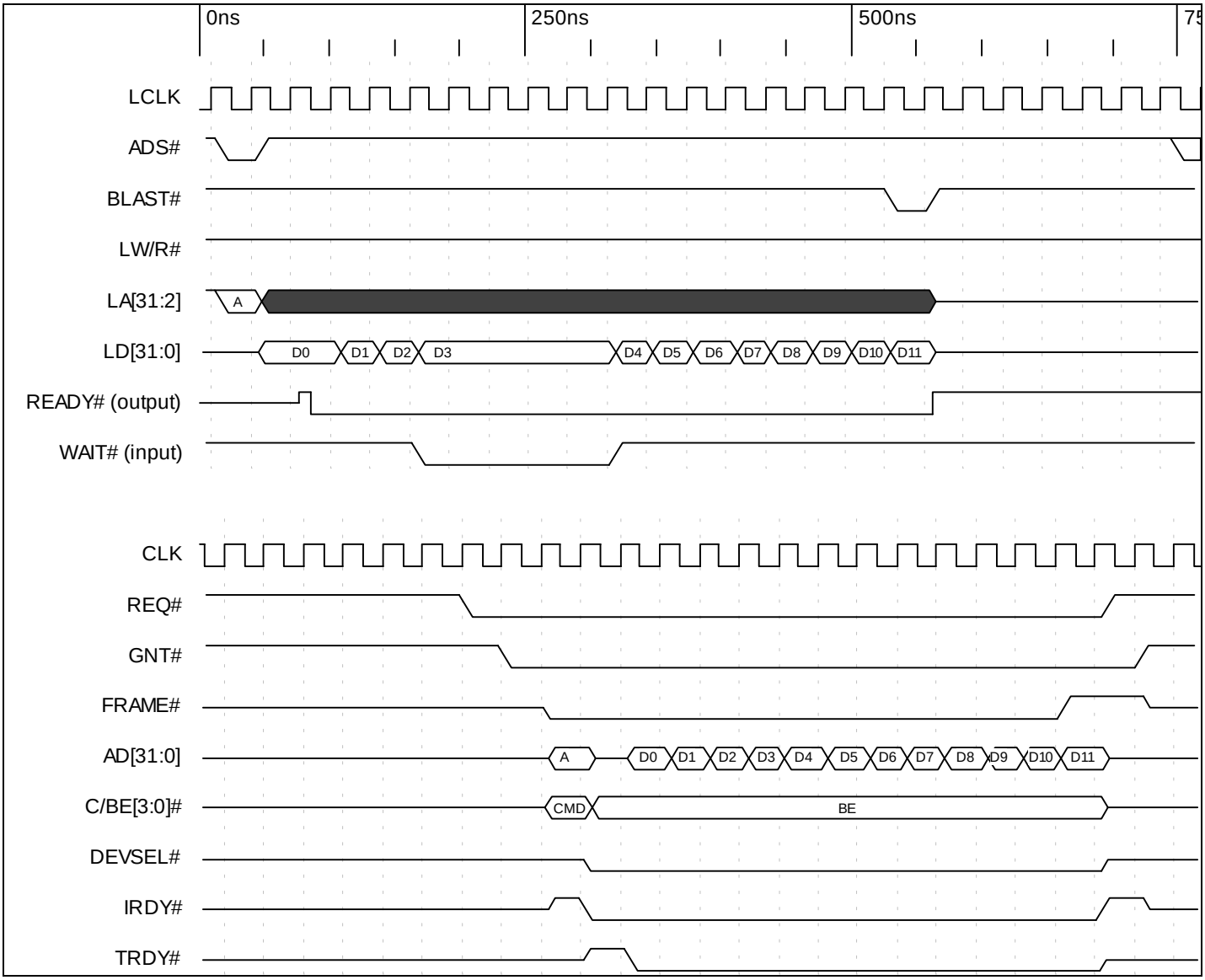
5.6.1 C Mode Direct Master



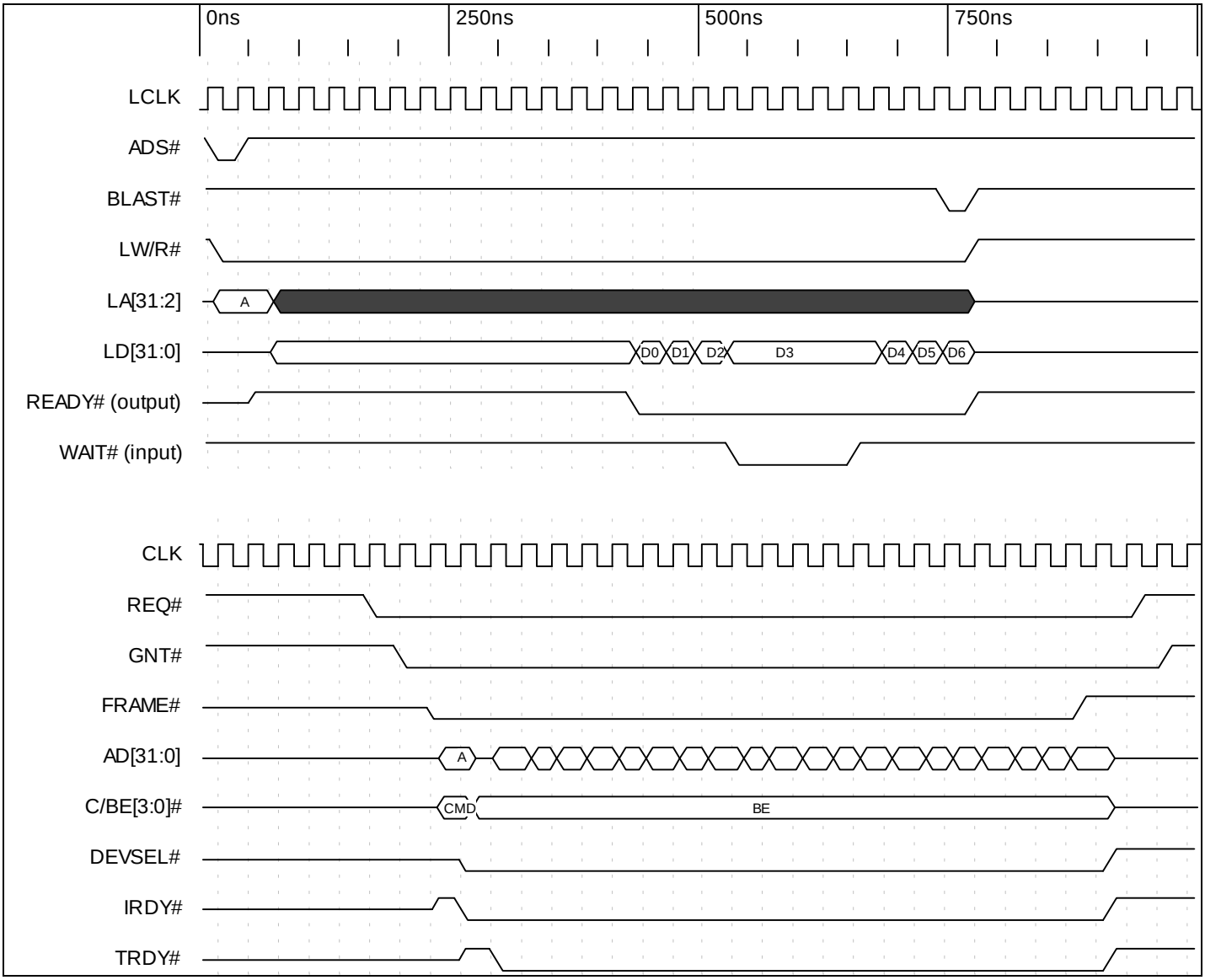
Timing Diagram 5-2. Direct Master Single Write



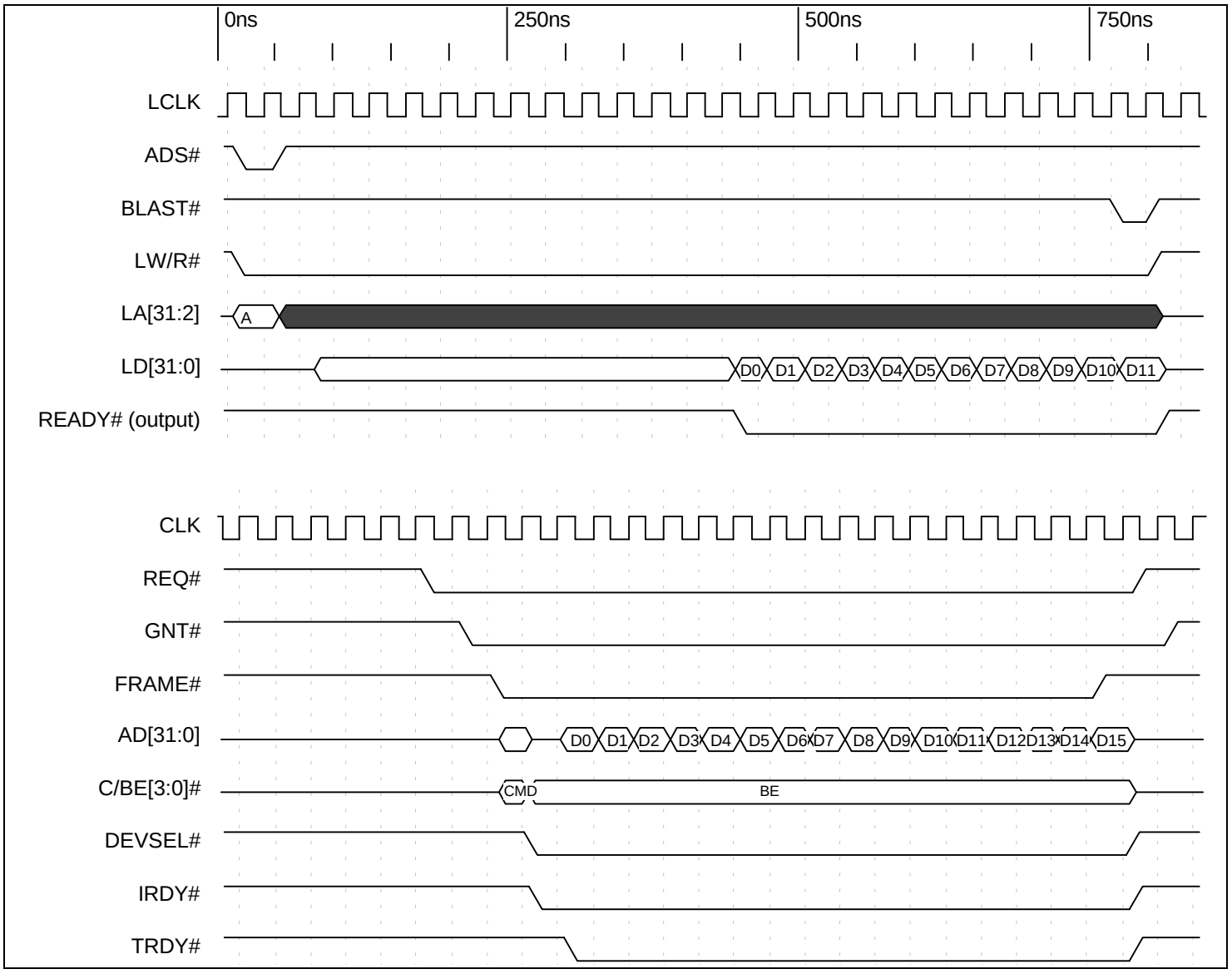
Timing Diagram 5-3. Direct Master Single Read



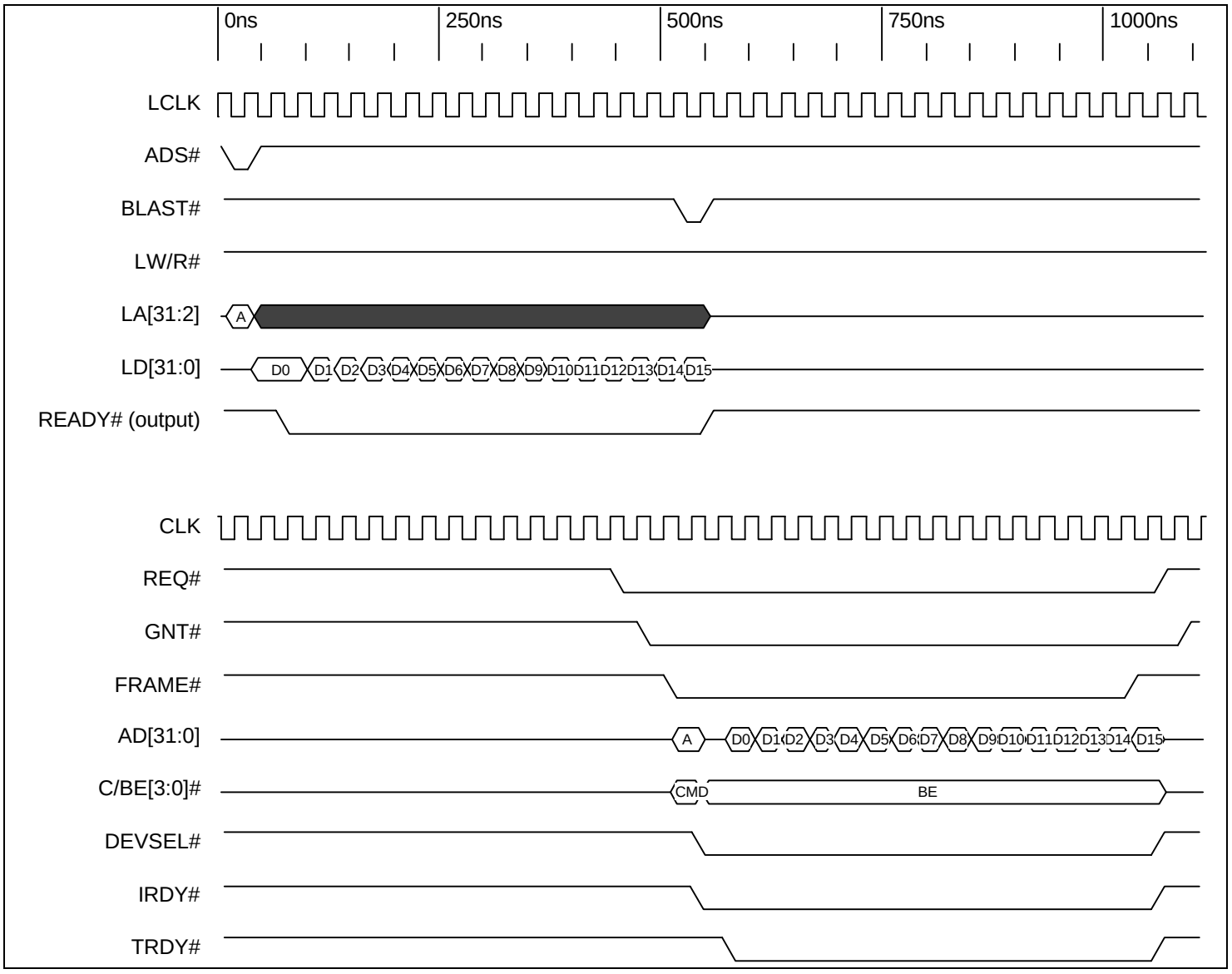
Timing Diagram 5-4. Direct Master Memory Write of 12 Lwords with WAIT# Input



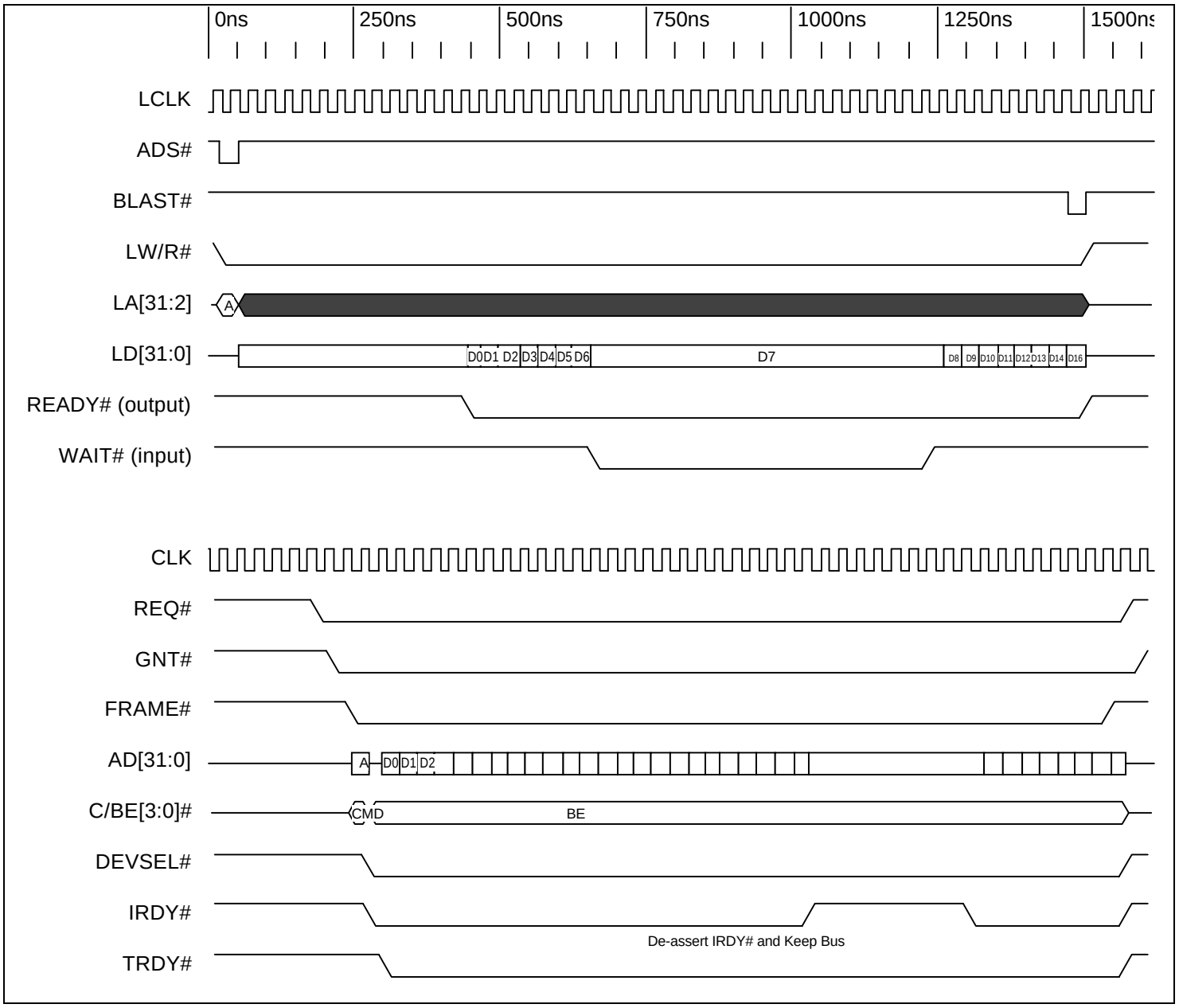
Timing Diagram 5-5. Direct Master Burst Read of Seven Lwords with WAIT# Input



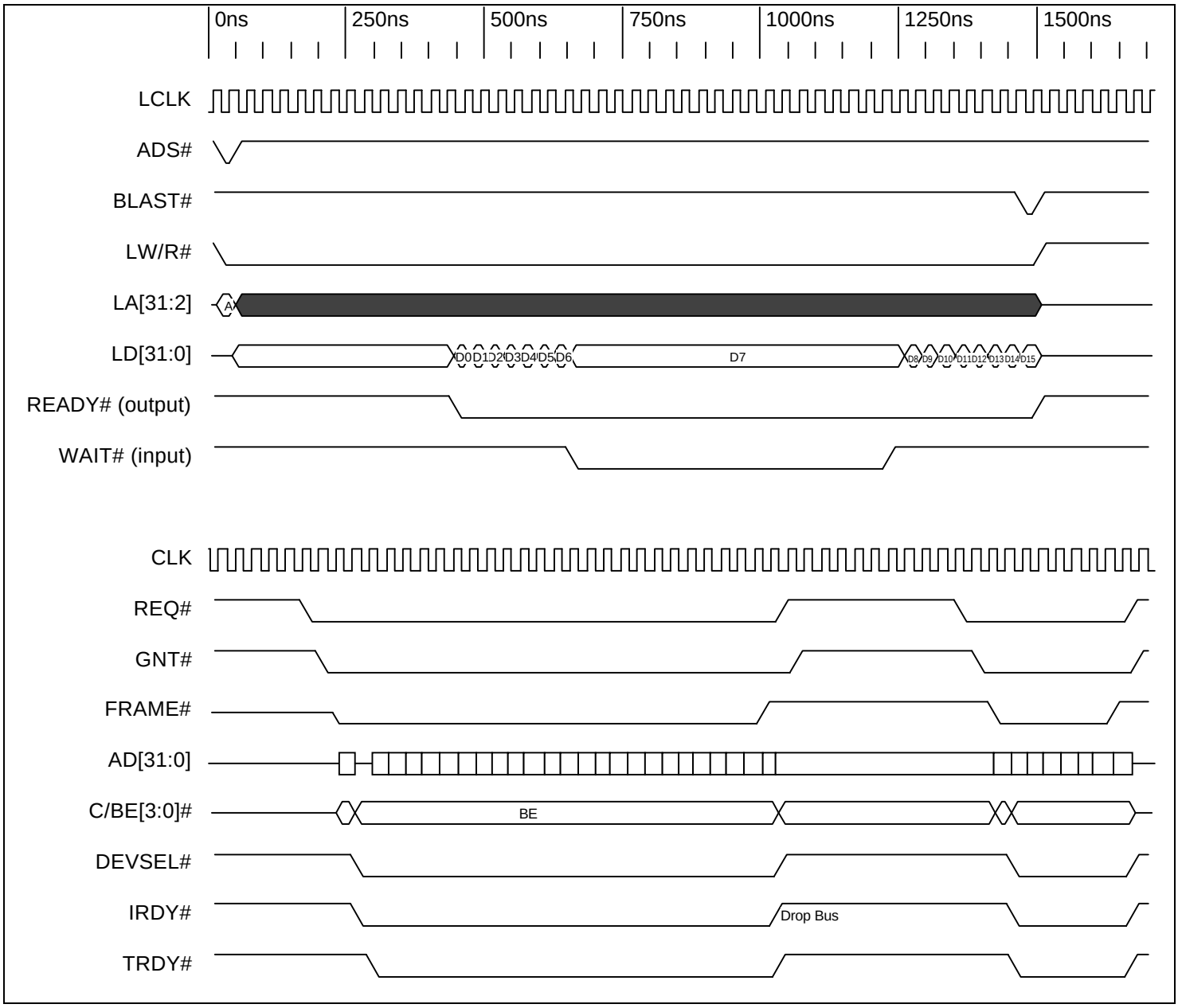
Timing Diagram 5-6. Direct Master Memory Read of 12 Lwords with Prefetch Counter Set to 16



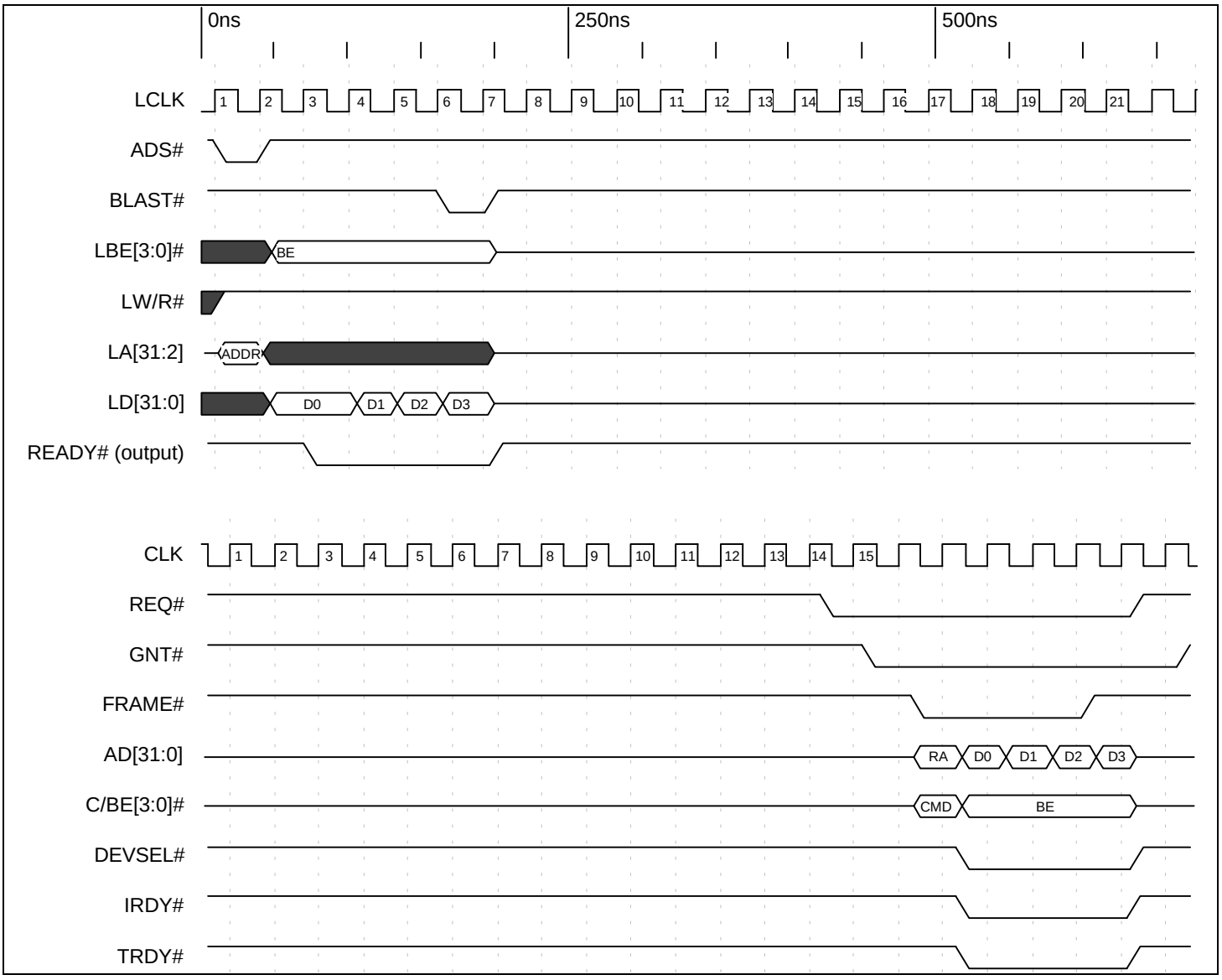
Timing Diagram 5-7. Memory Write and Invalidate with Cache Line Size of Eight



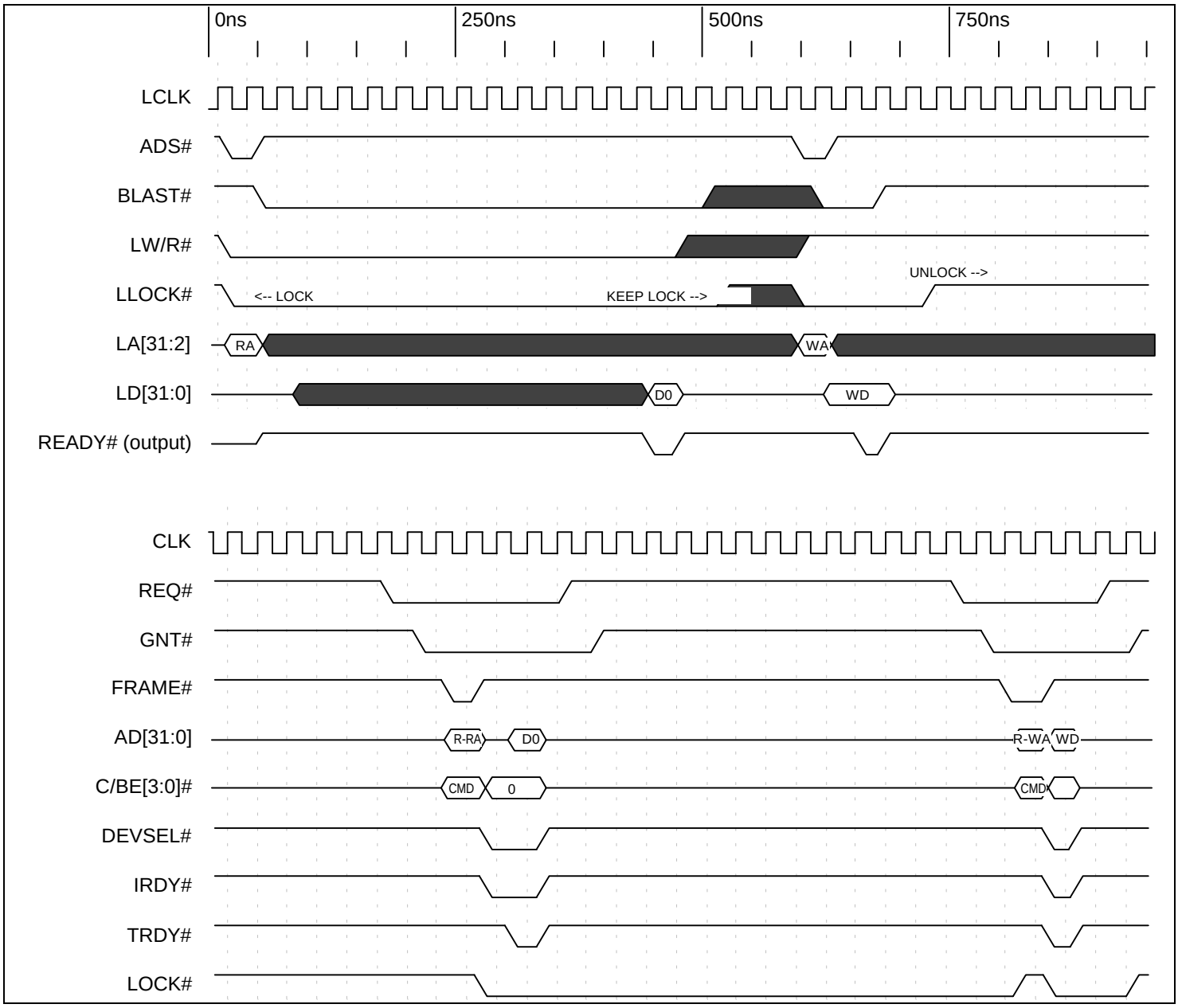
Timing Diagram 5-8. Direct Master Memory Read with Keep Bus Mode



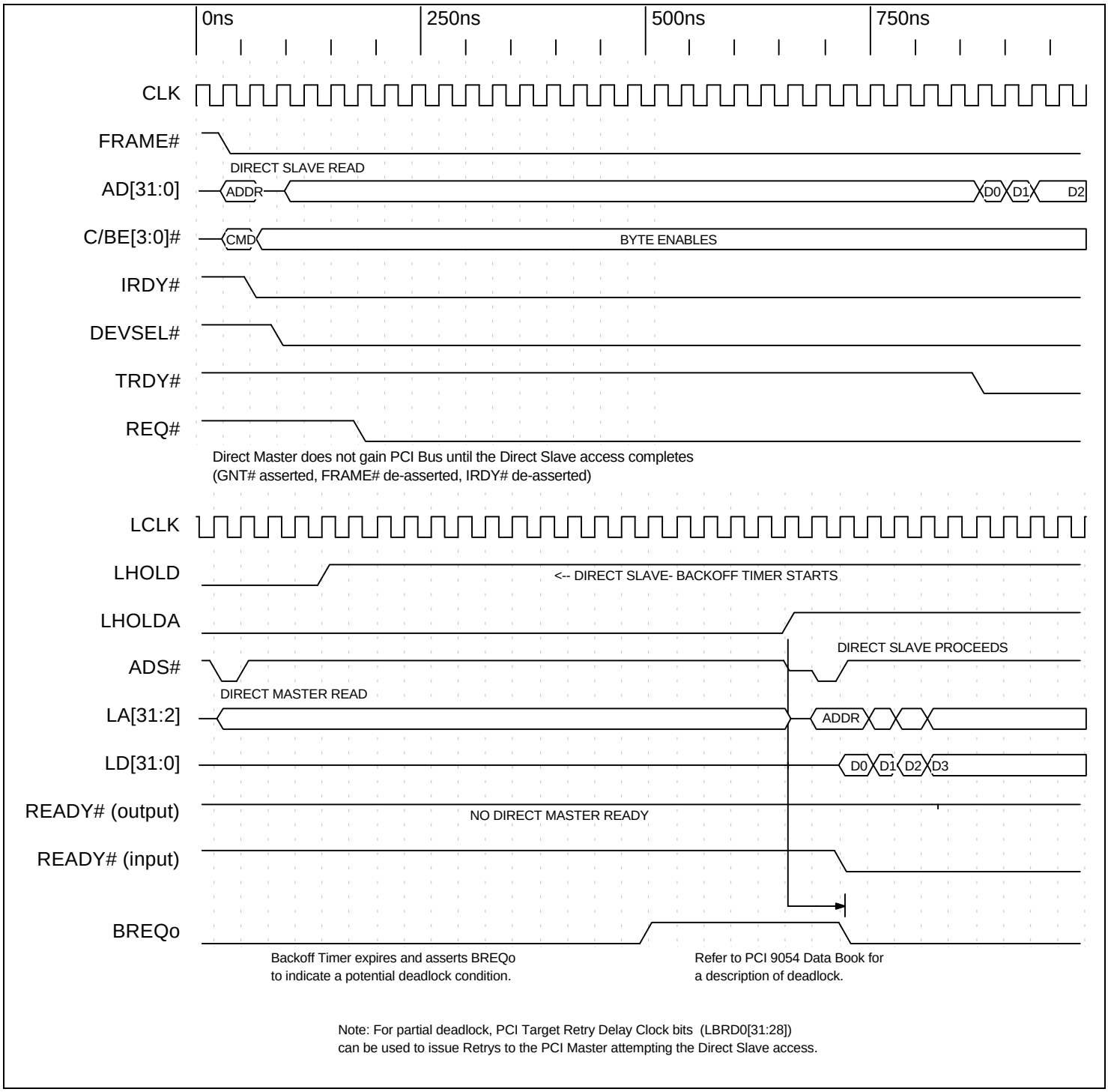
Timing Diagram 5-9. Direct Master Memory Read with Drop Bus Mode



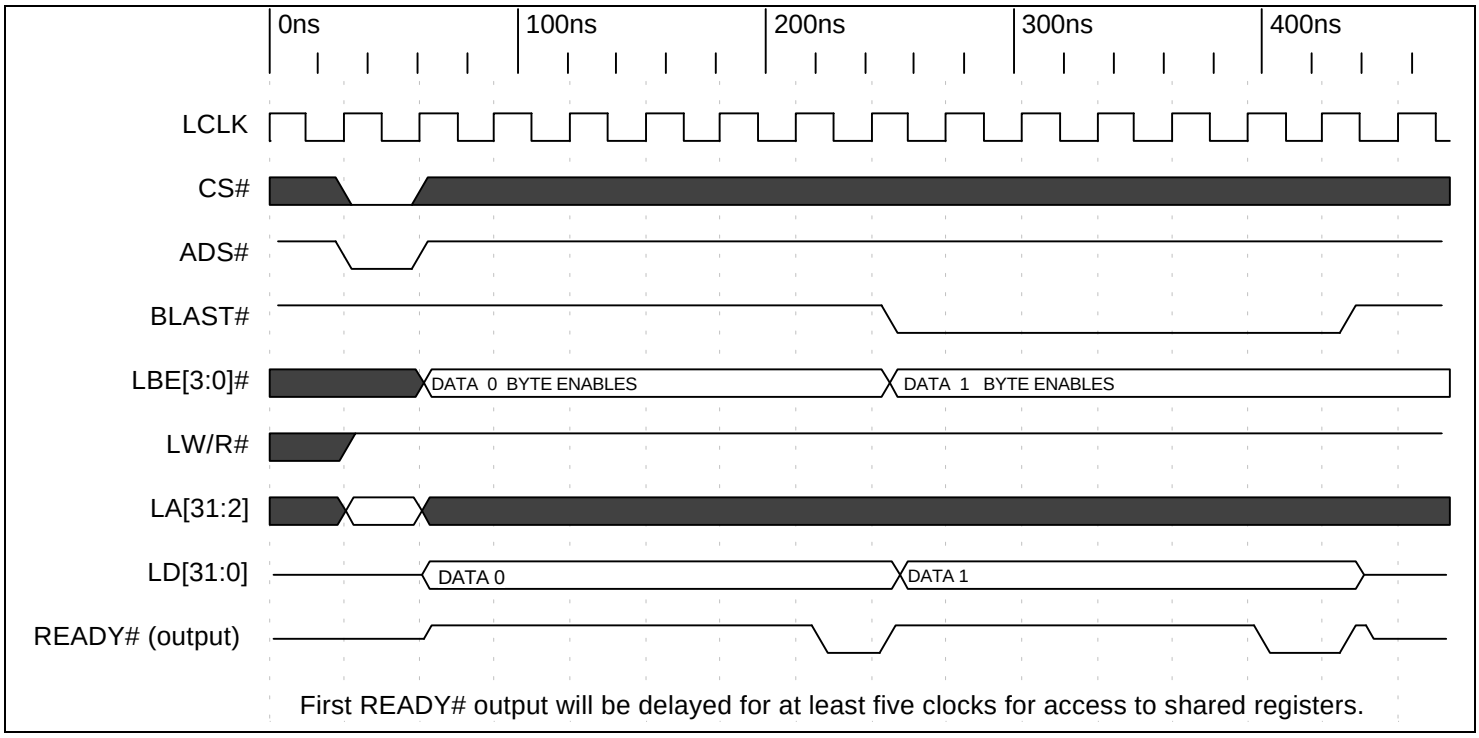
Timing Diagram 5-10. PCI Bus Request (REQ#) Delay During Direct Mater Write (Eight-PCI Clock Delay)



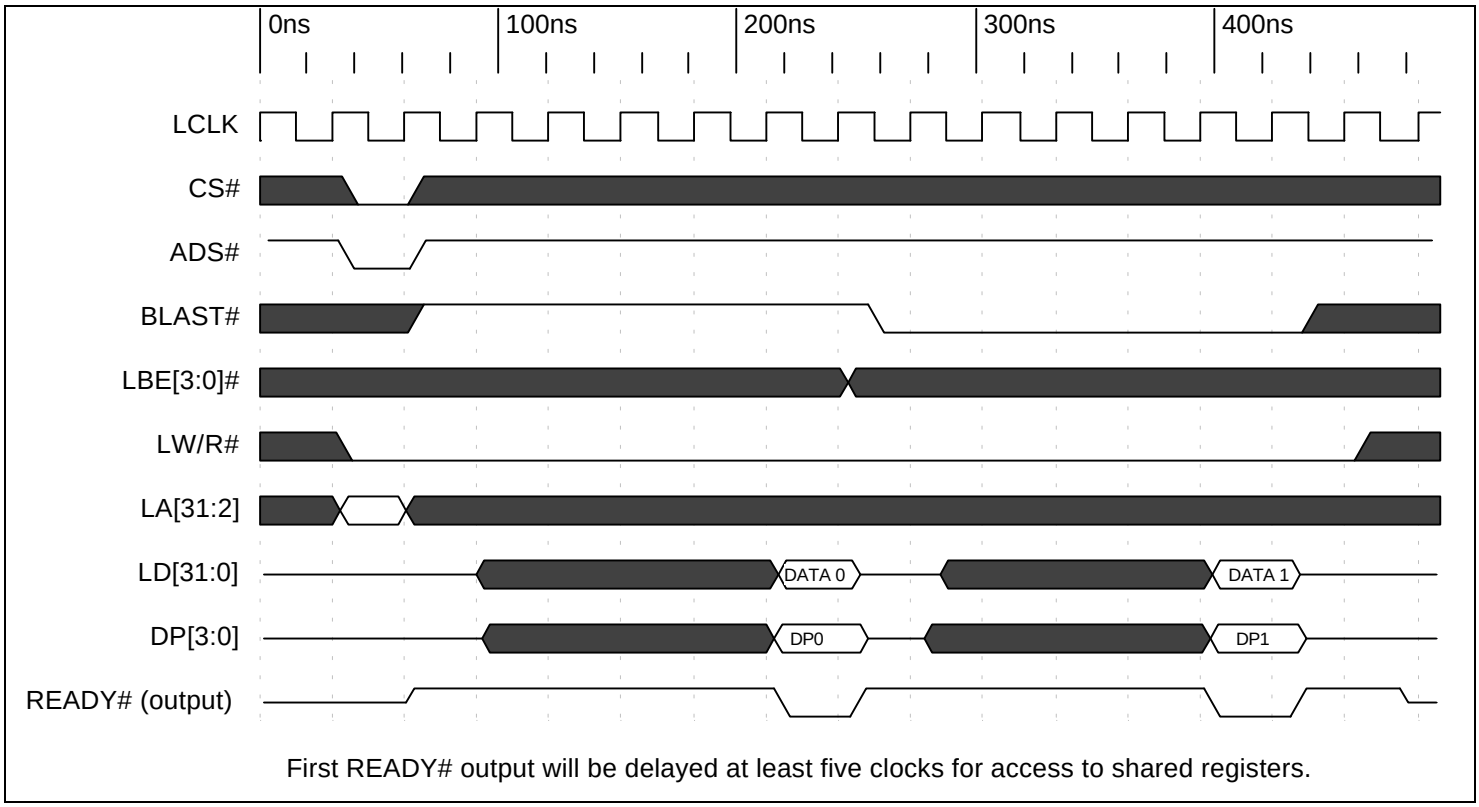
Timing Diagram 5-11. Direct Master Locked Read Followed by Write and Release (LLOCK# and LOCK#)



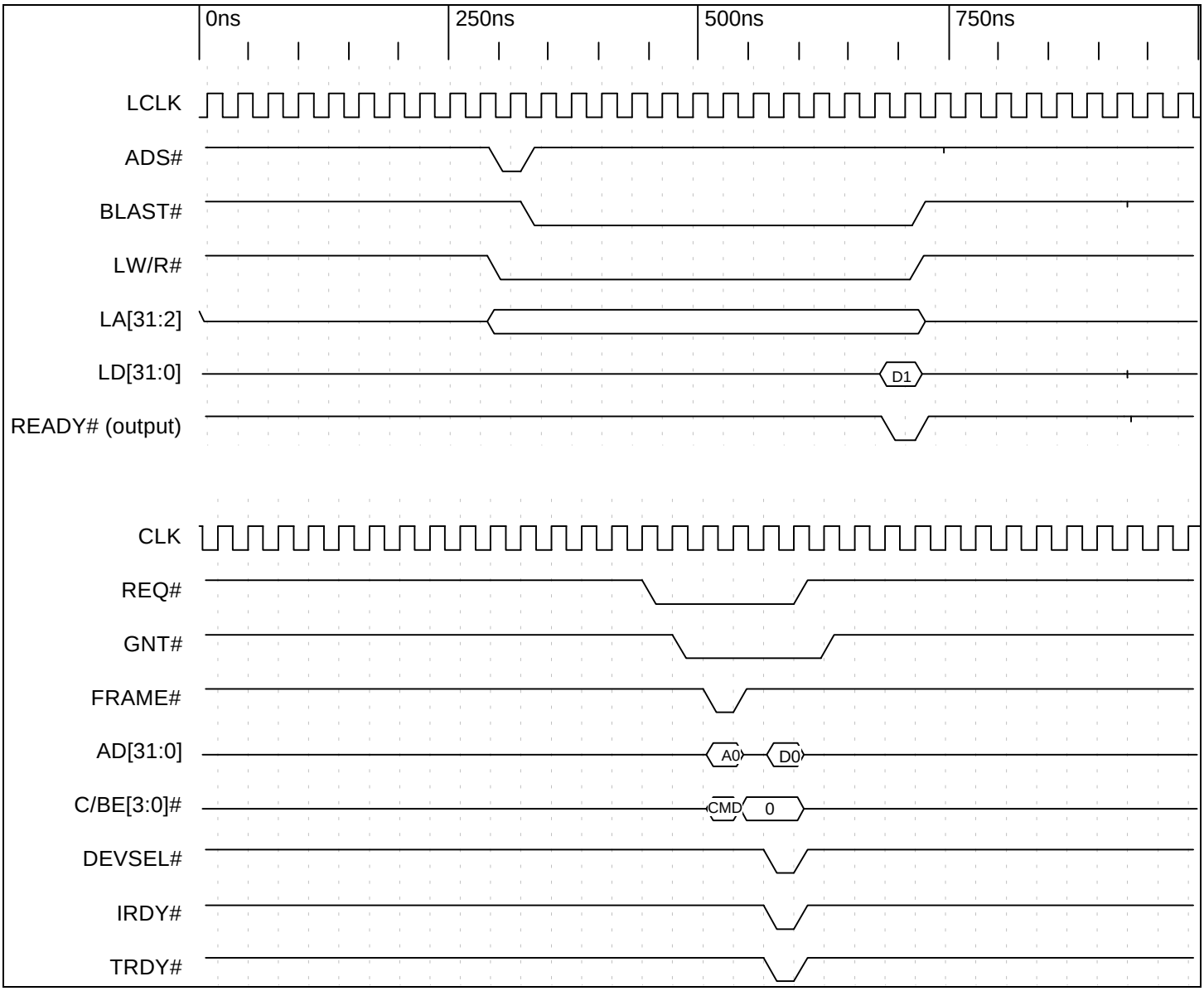
Timing Diagram 5-12. BREQo and Deadlock



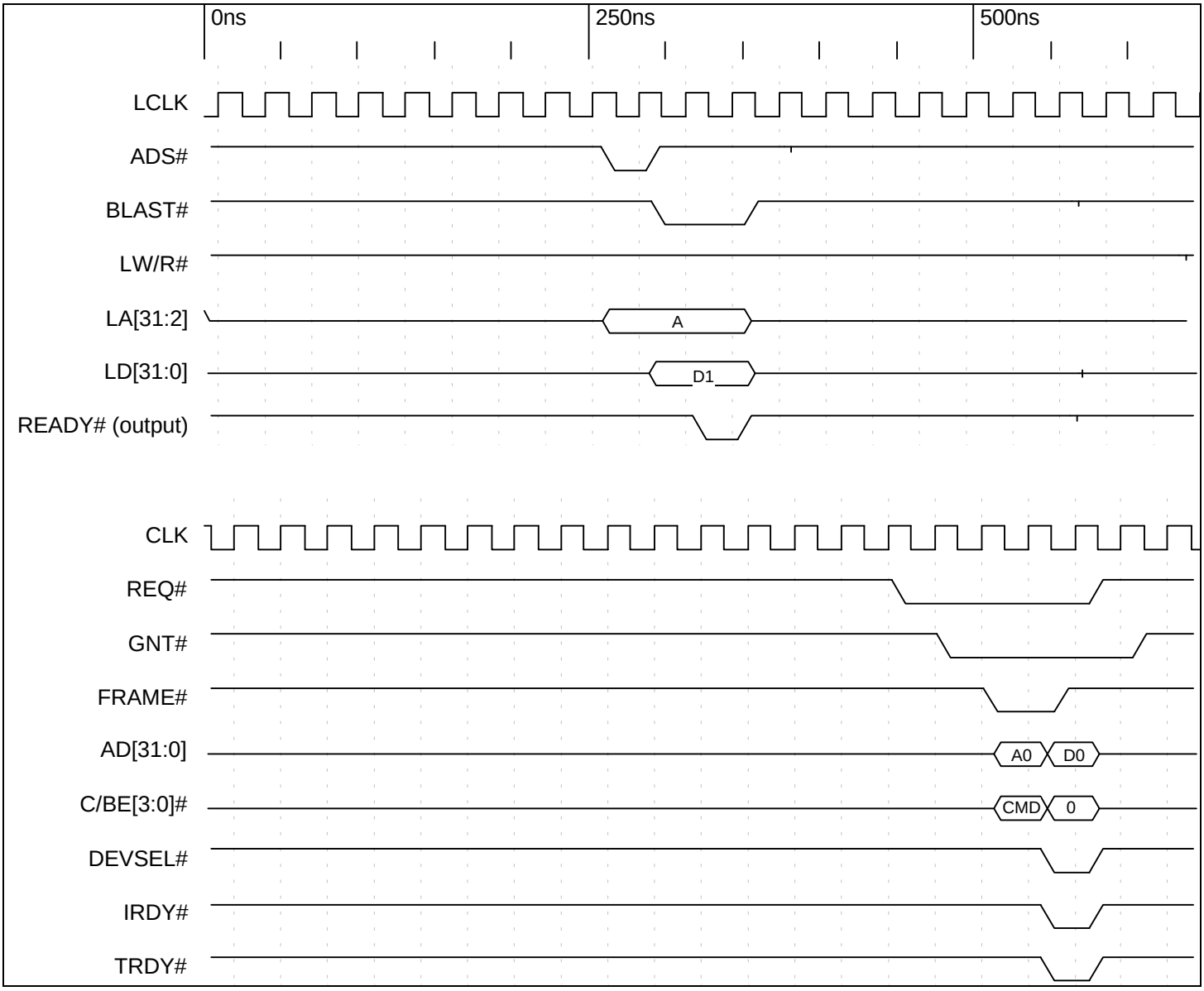
Timing Diagram 5-13. Local Bus Write to Configuration Register



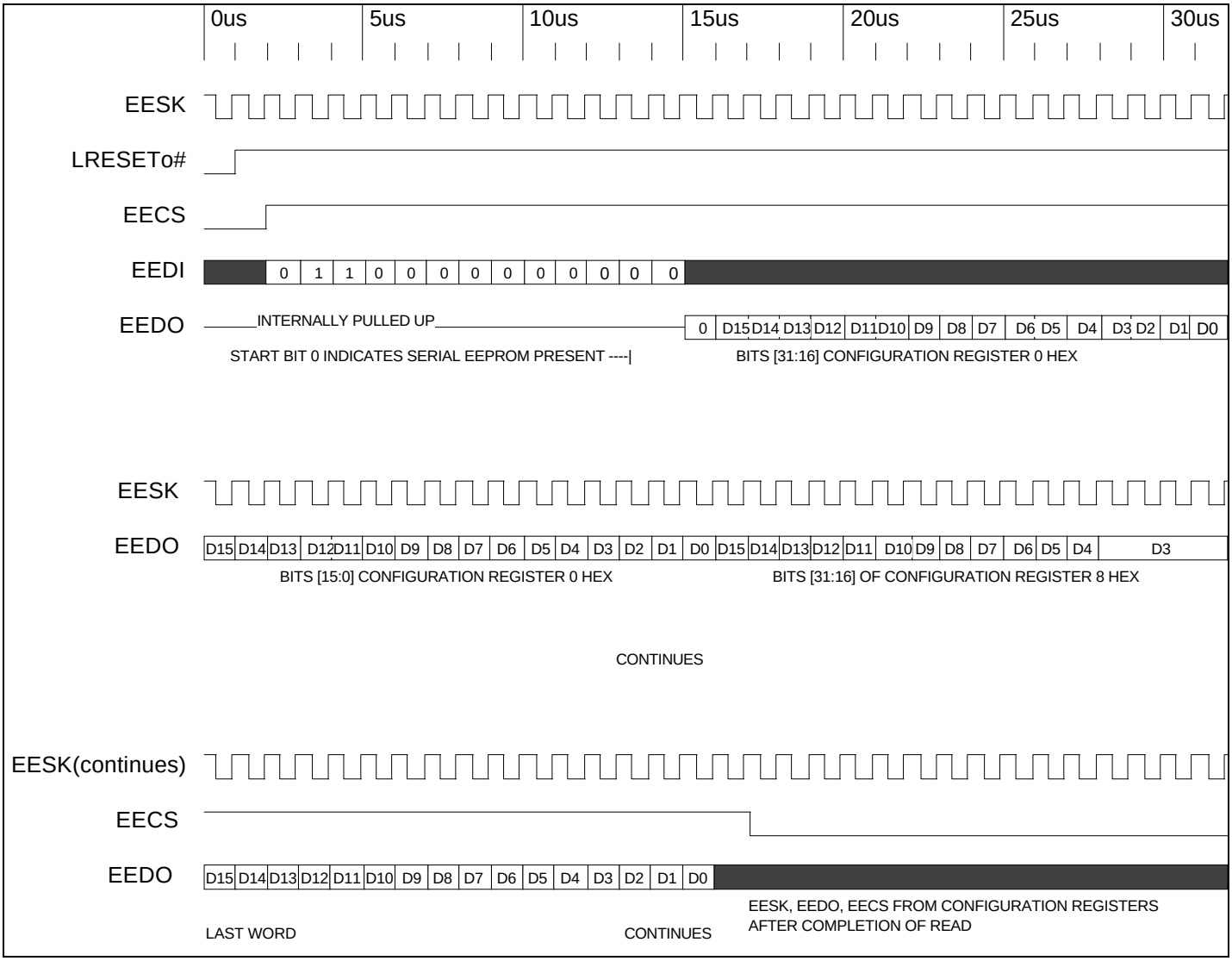
Timing Diagram 5-14. Local Bus Read to Configuration Register



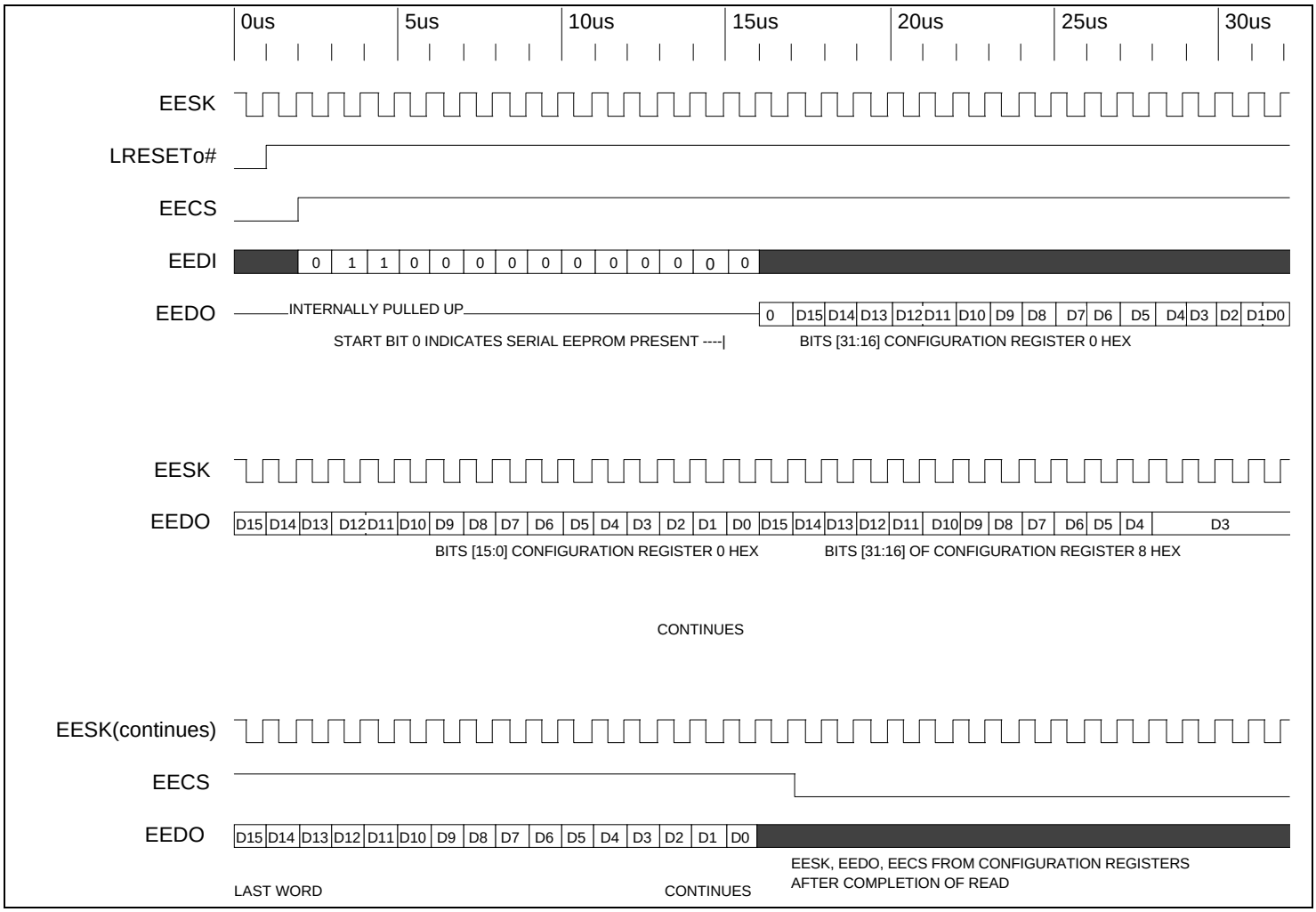
Timing Diagram 5-15. Direct Master Configuration Read—Type 1 or Type 0



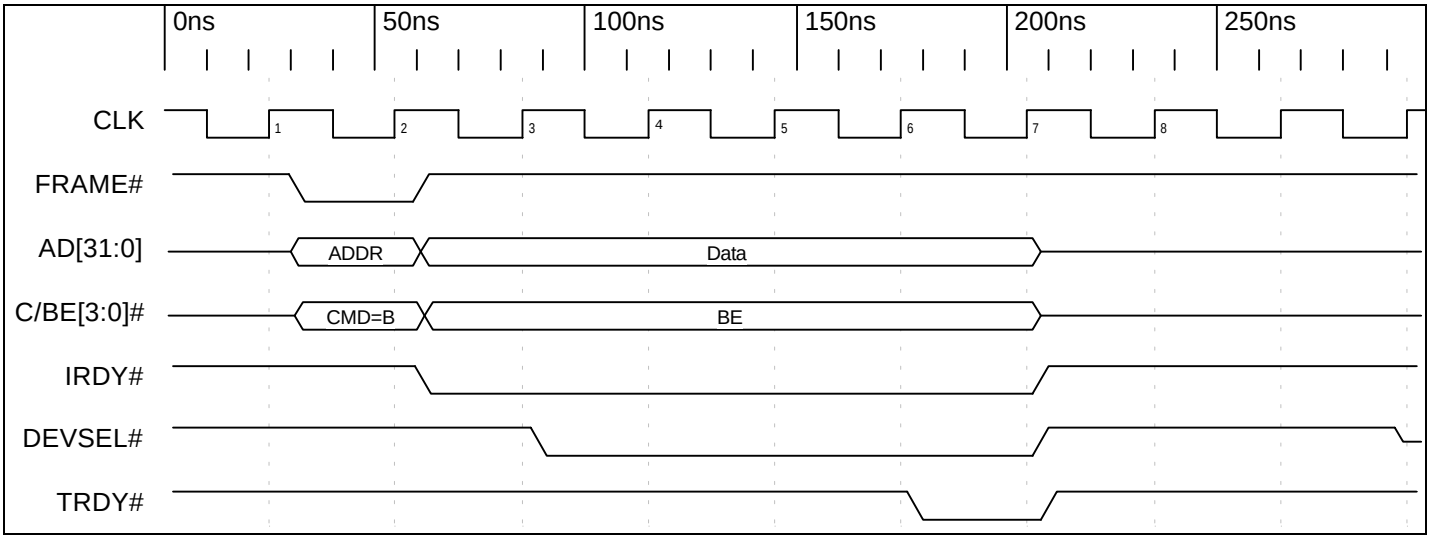
Timing Diagram 5-16. Direct Master Configuration Write—Type 1 or Type 0



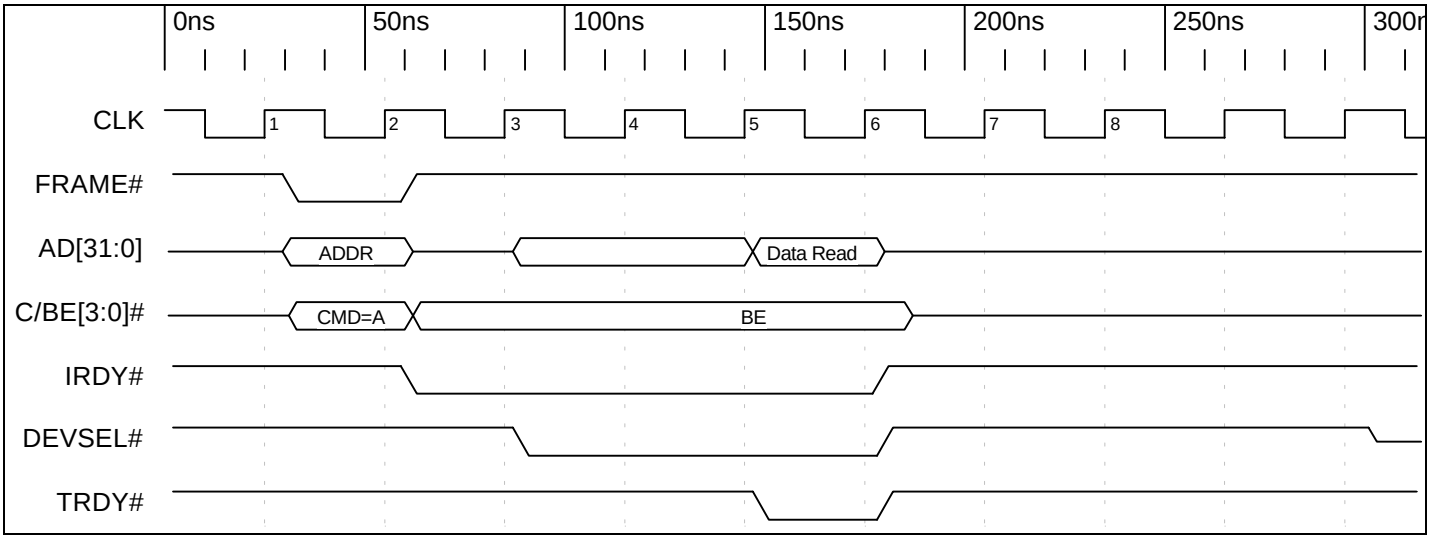
Timing Diagram 5-17. Initialization from Serial EEPROM (2K)



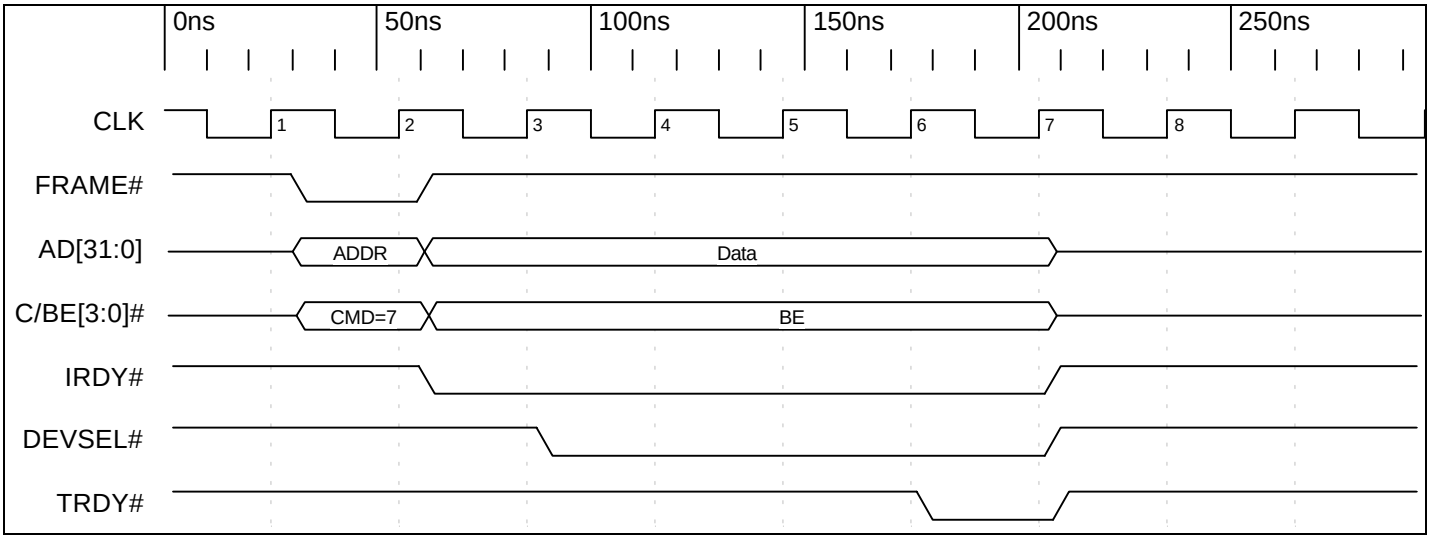
Timing Diagram 5-18. Initialization from Serial EEPROM (4K)



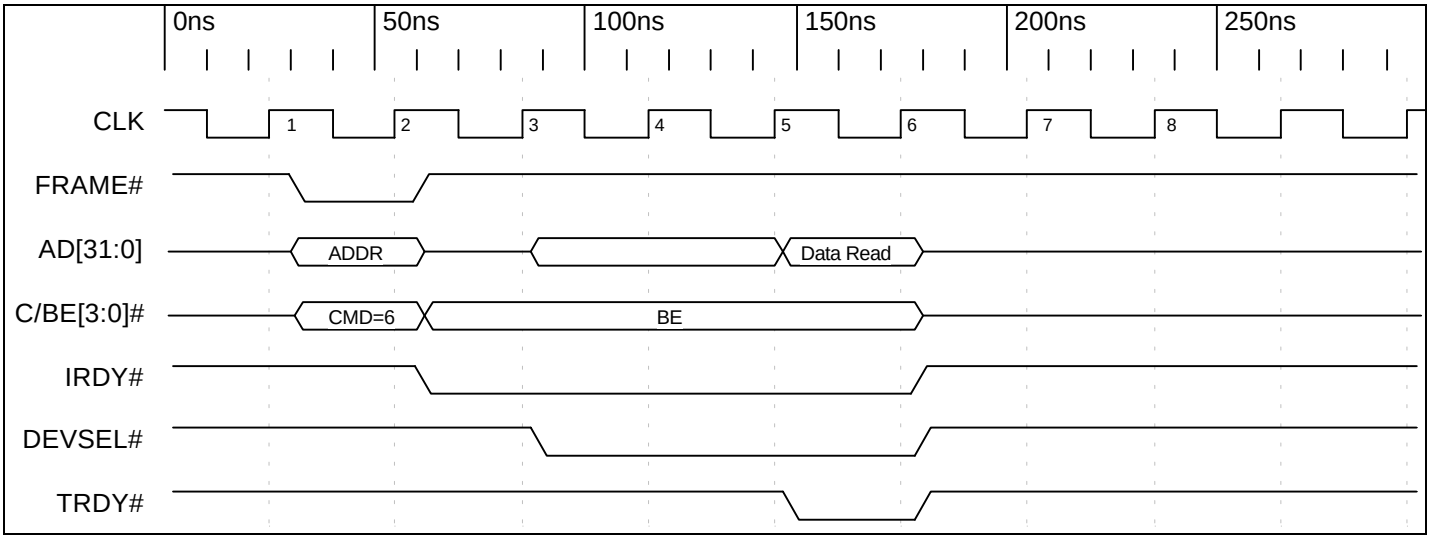
Timing Diagram 5-19. PCI Configuration Write to PCI Configuration Register



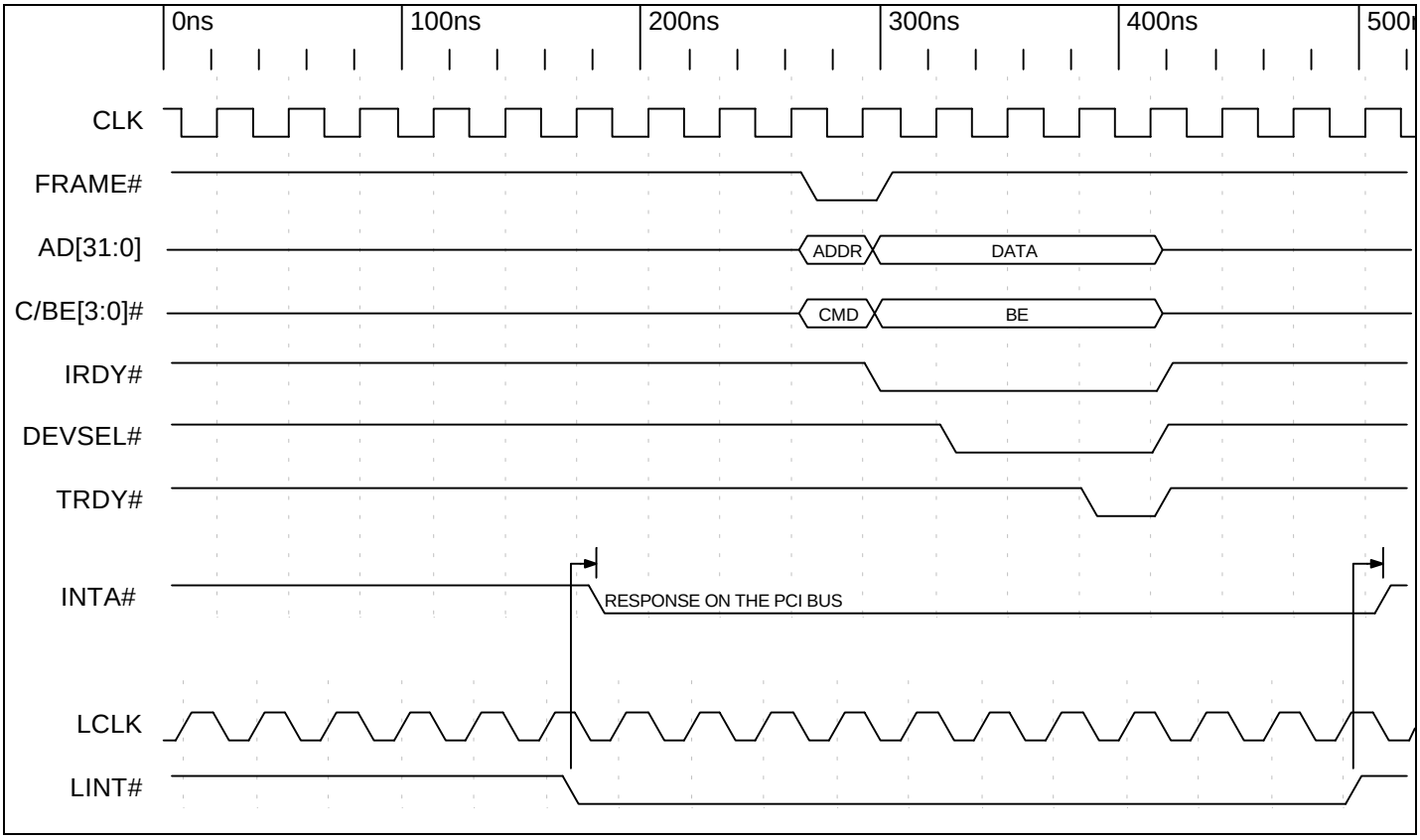
Timing Diagram 5-20. PCI Configuration Read to PCI Configuration Register



Timing Diagram 5-21. PCI Memory Write to Local Configuration Register

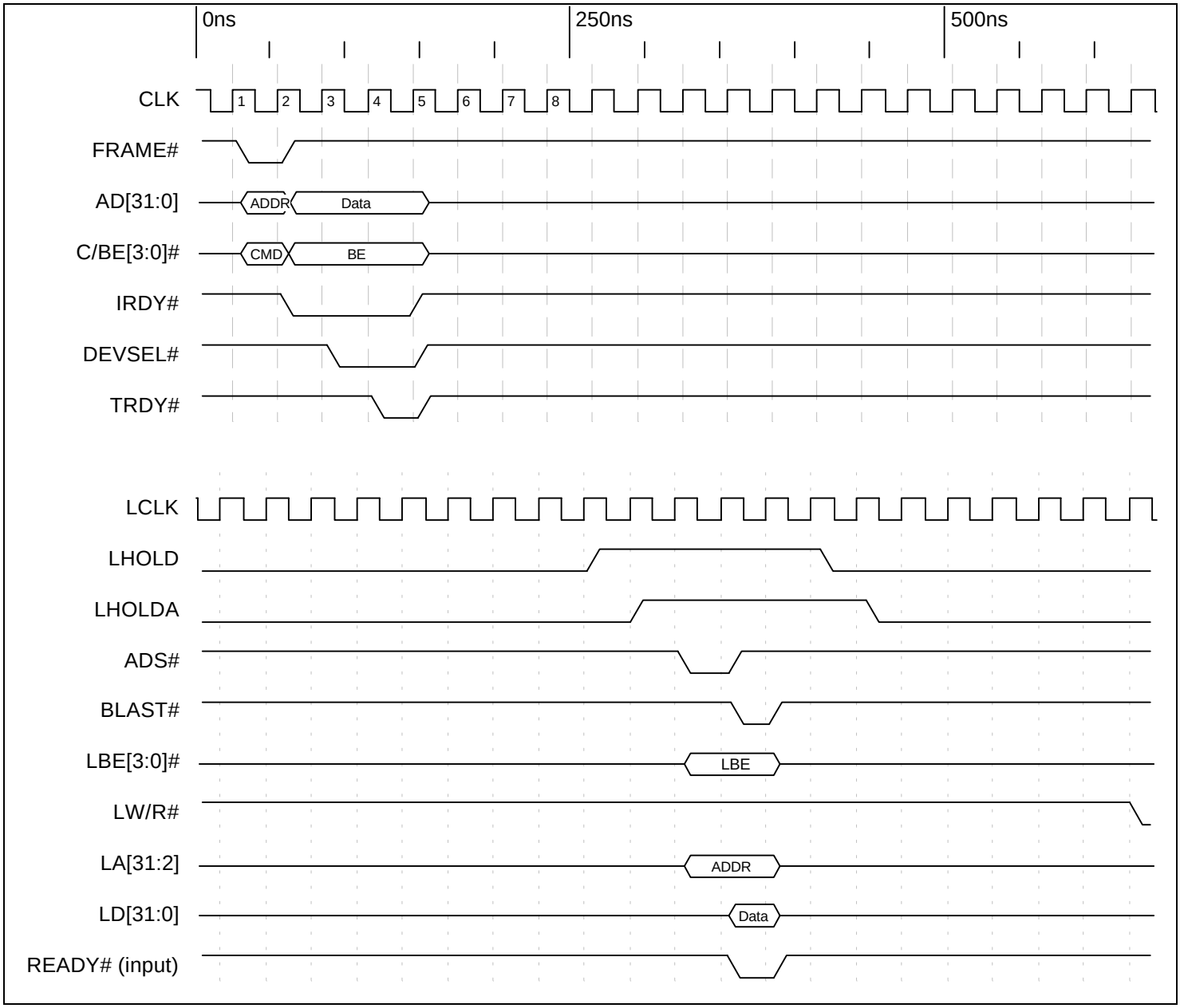


Timing Diagram 5-22. PCI Memory Read to Local Configuration Register

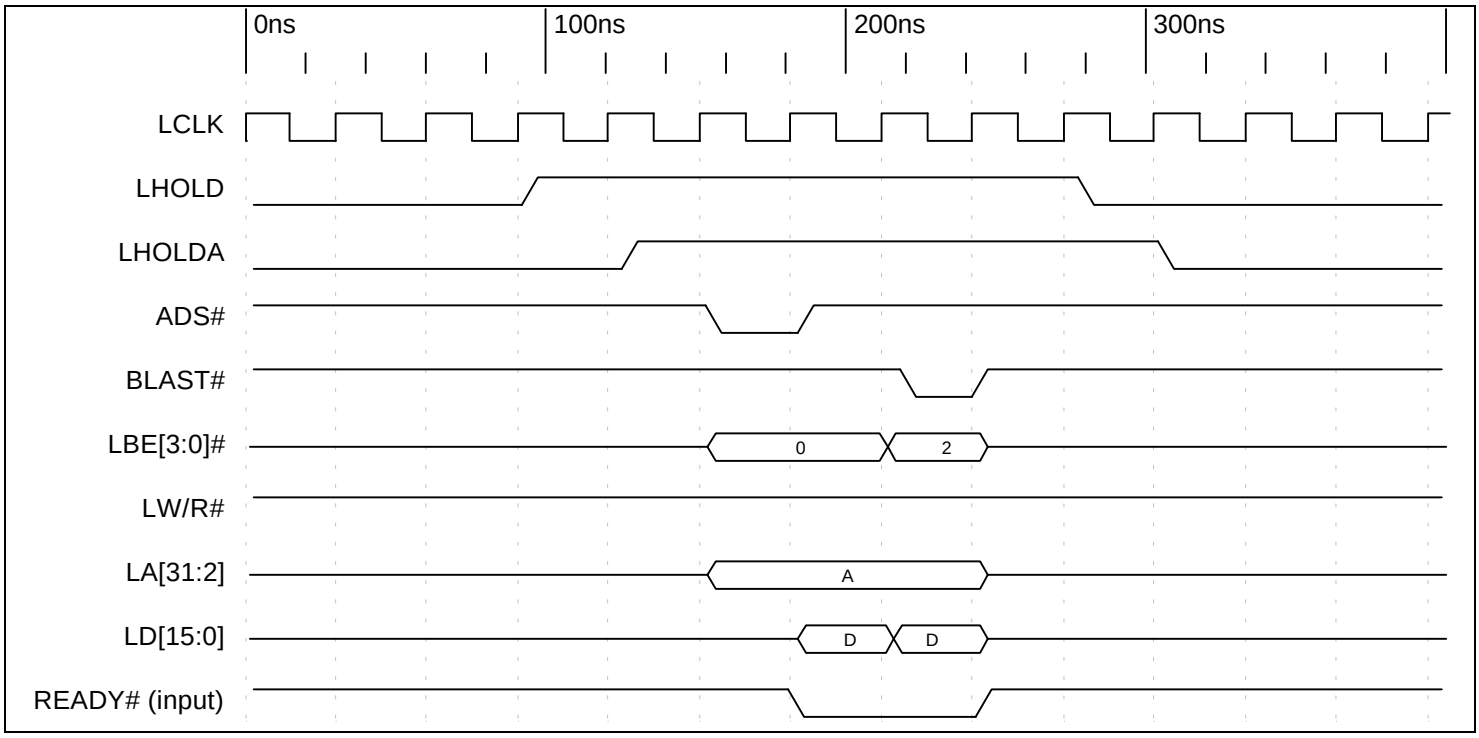


Timing Diagram 5-23. Local Interrupt Asserting PCI Interrupt

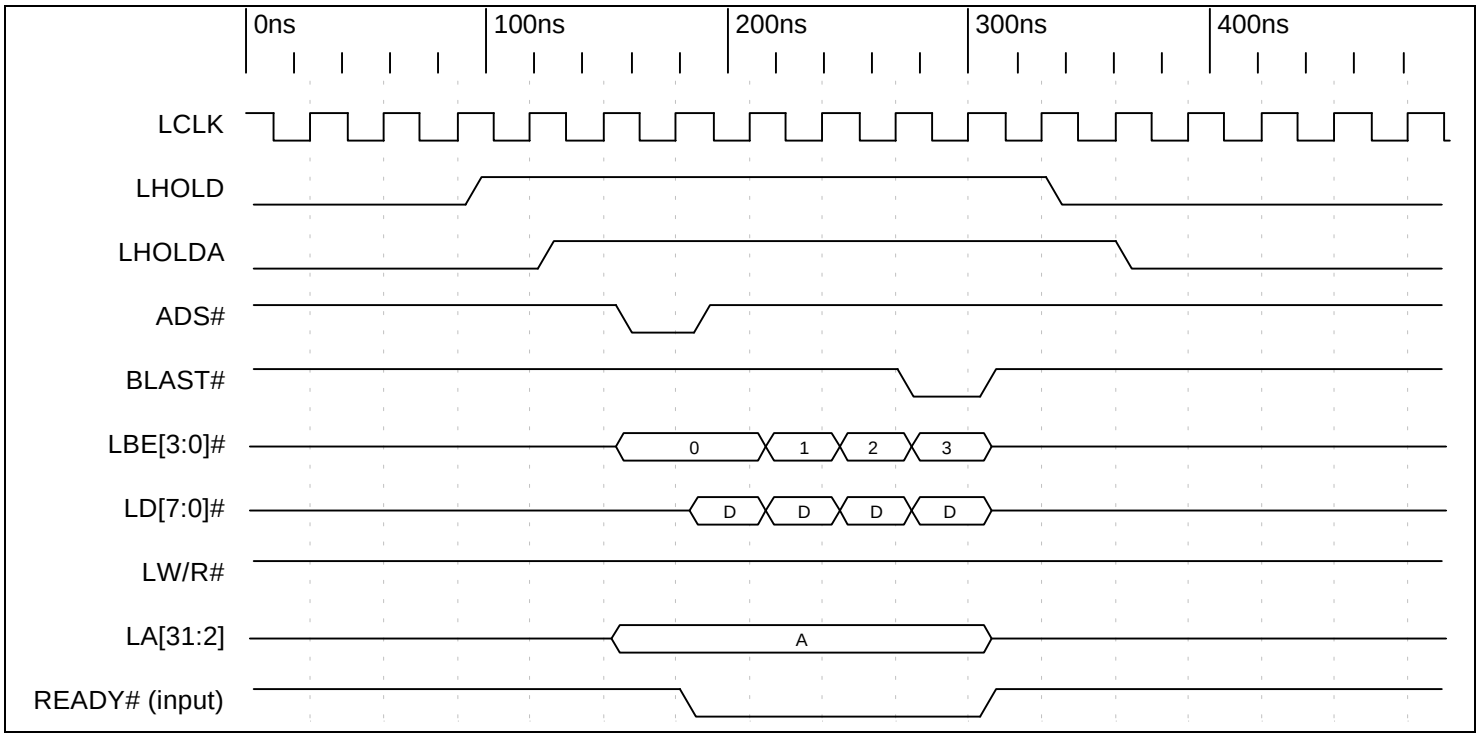
5.6.2 C Mode Direct Slave



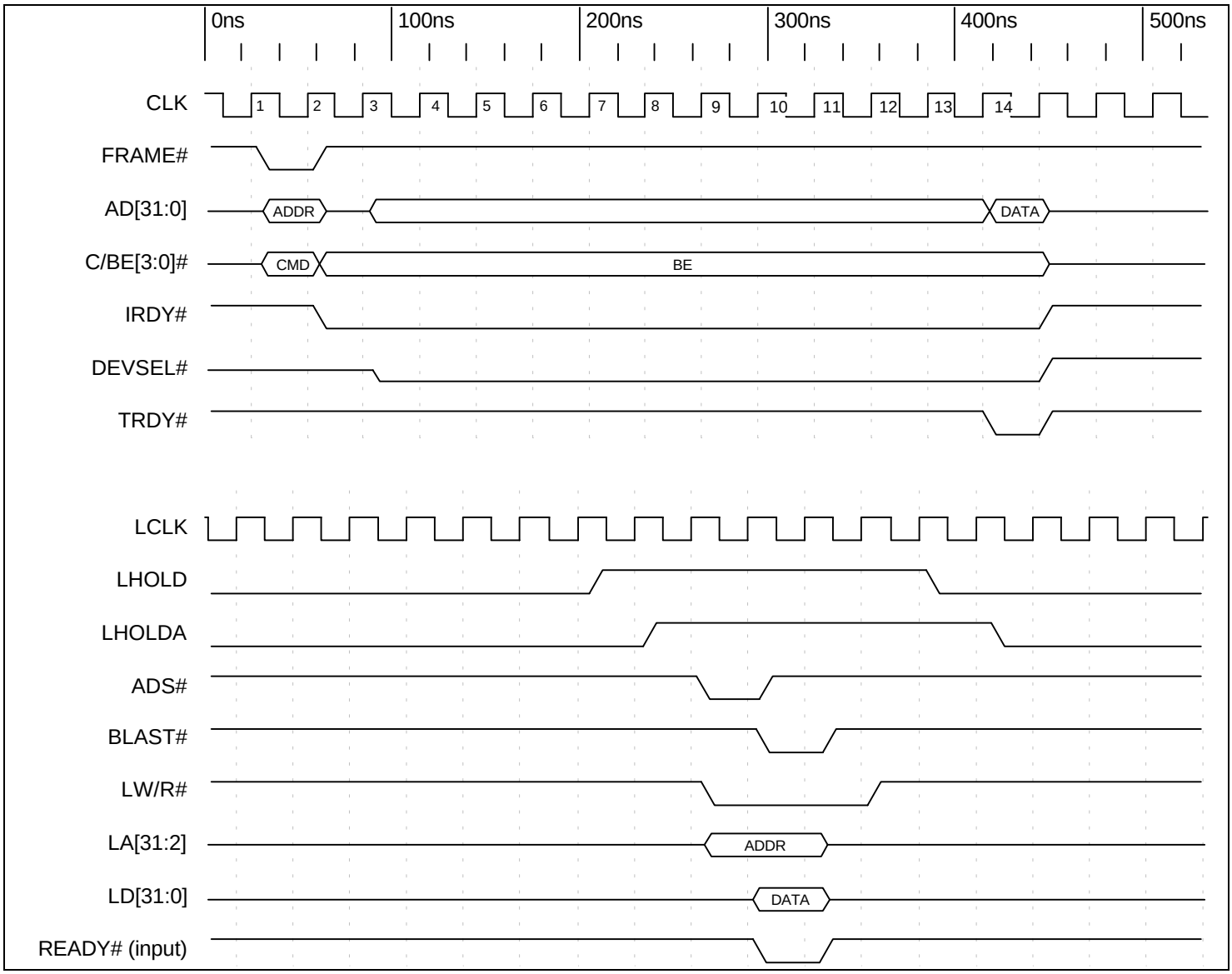
Timing Diagram 5-24. Direct Slave Single Write (32-Bit Local Bus)



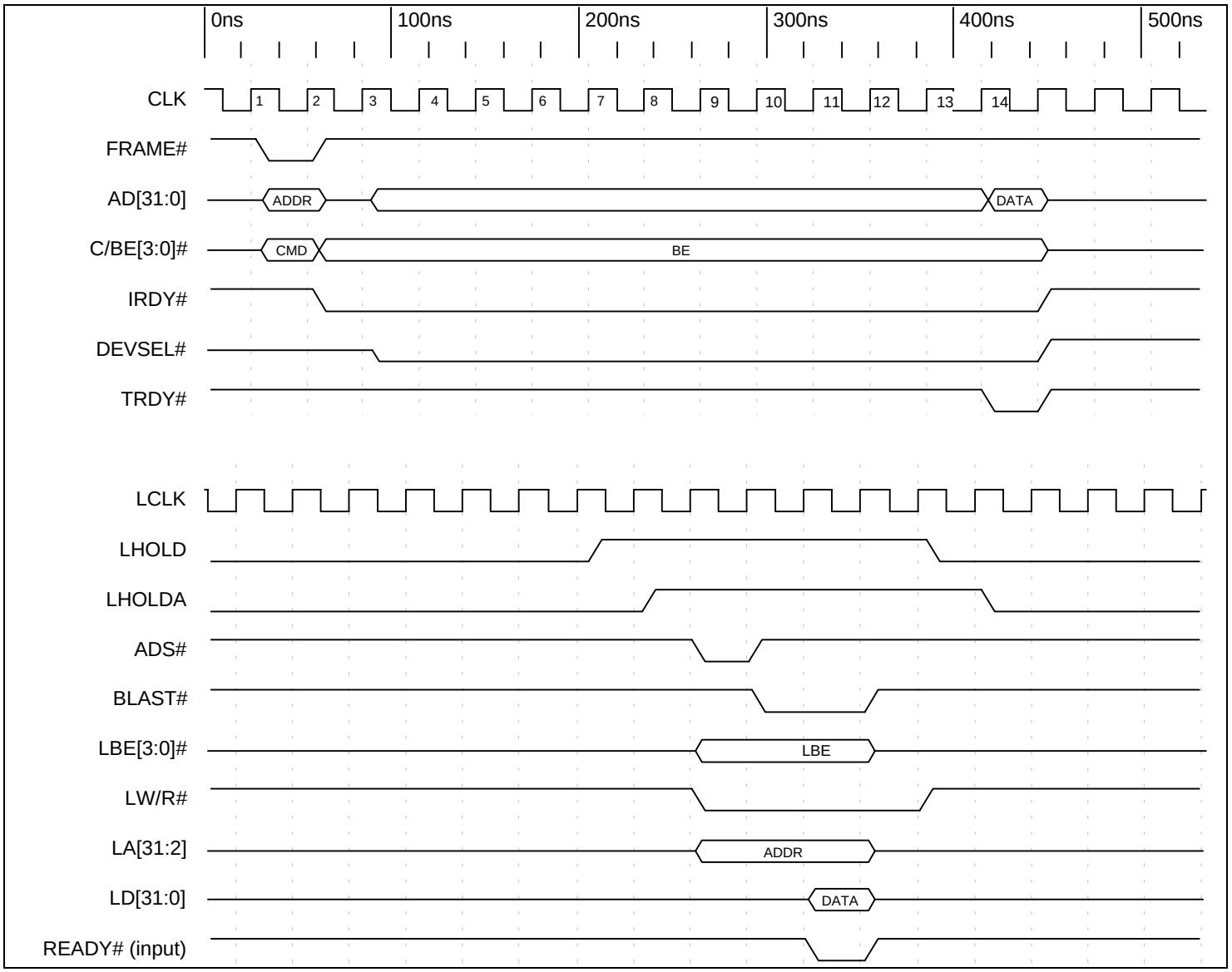
Timing Diagram 5-25. Direct Slave Single-Cycle Write (16-Bit Local Bus)



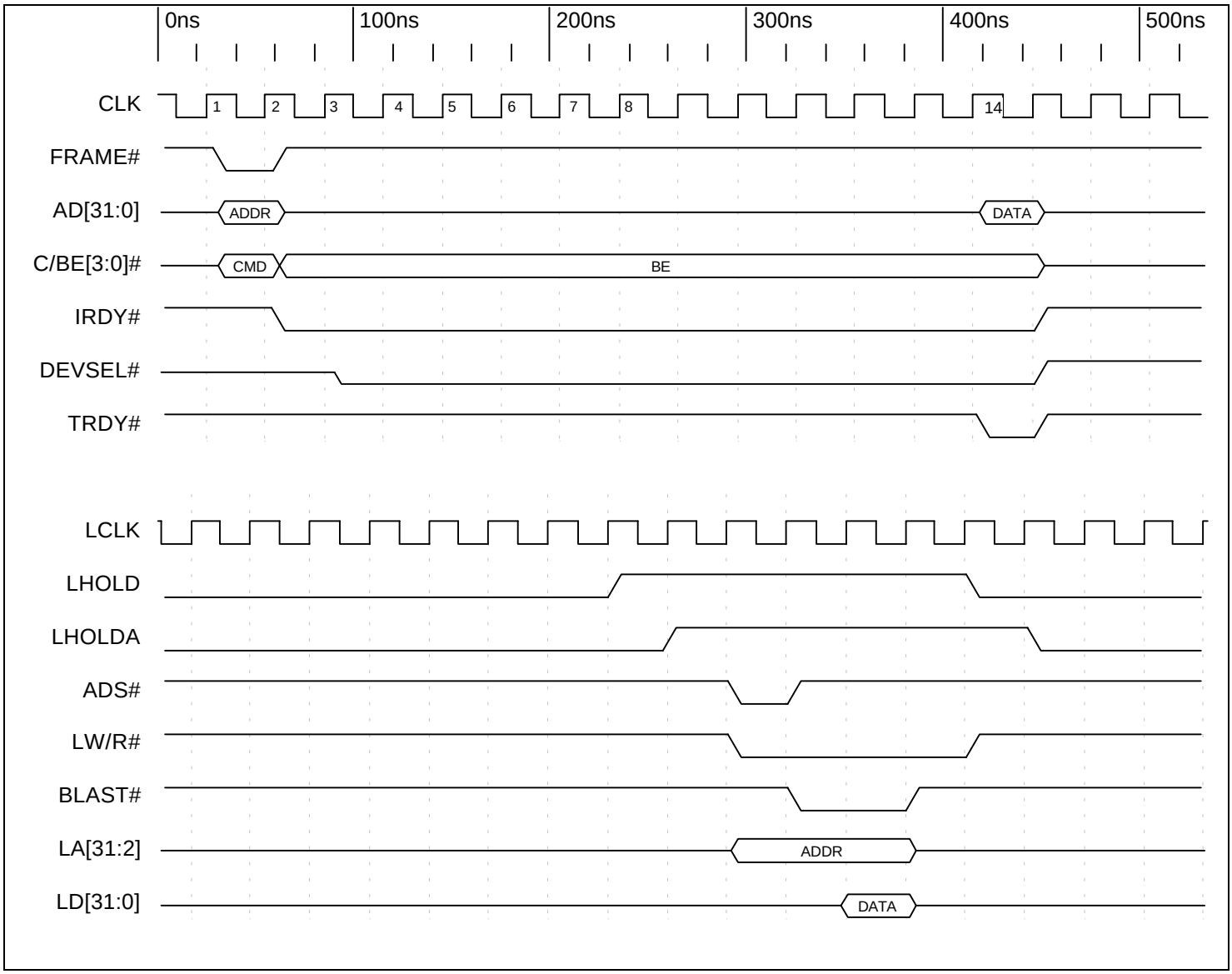
Timing Diagram 5-26. Direct Slave Single-Cycle Write (8-Bit Local Bus)



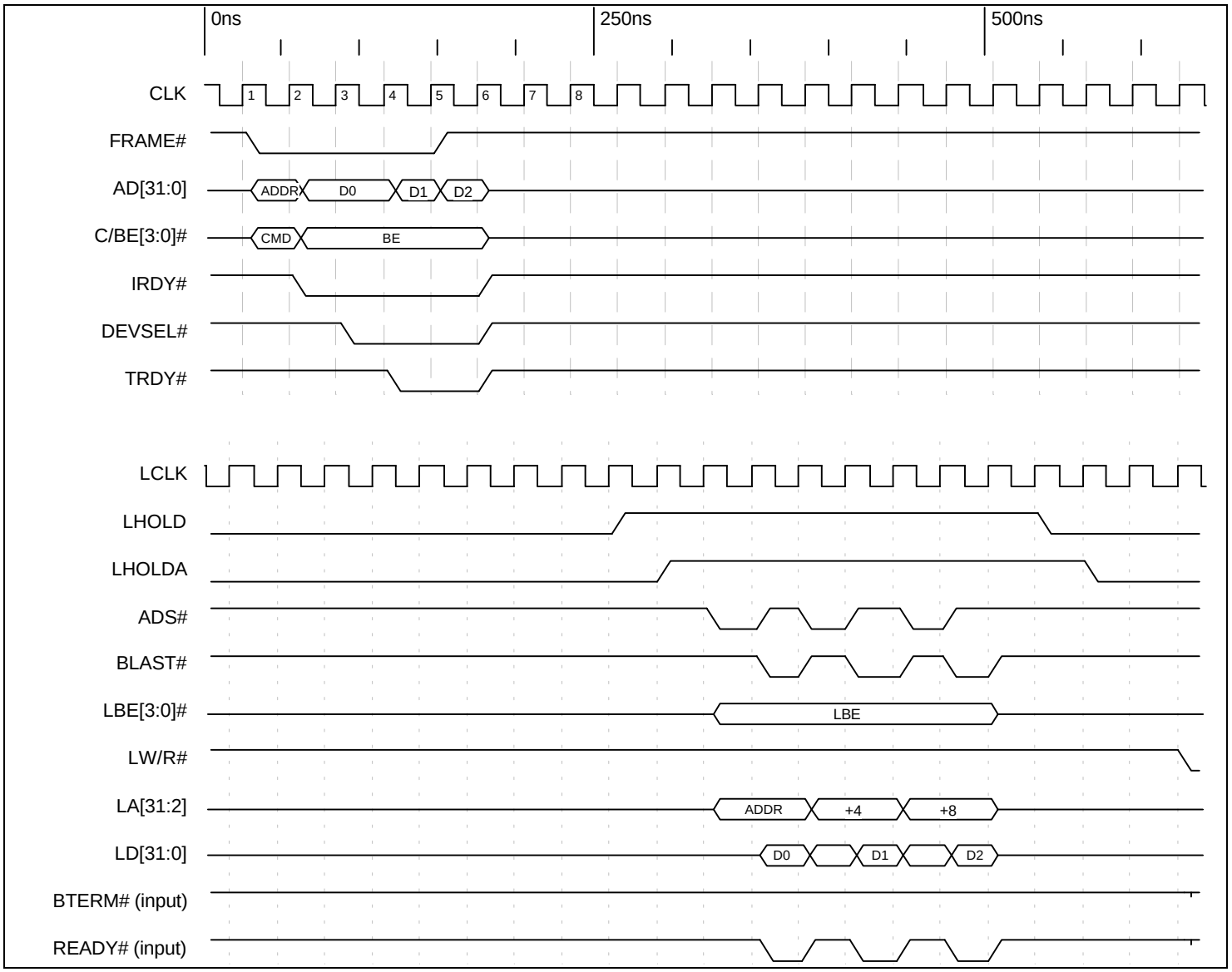
Timing Diagram 5-27. Direct Slave Single-Cycle Read (32-Bit Local Bus)



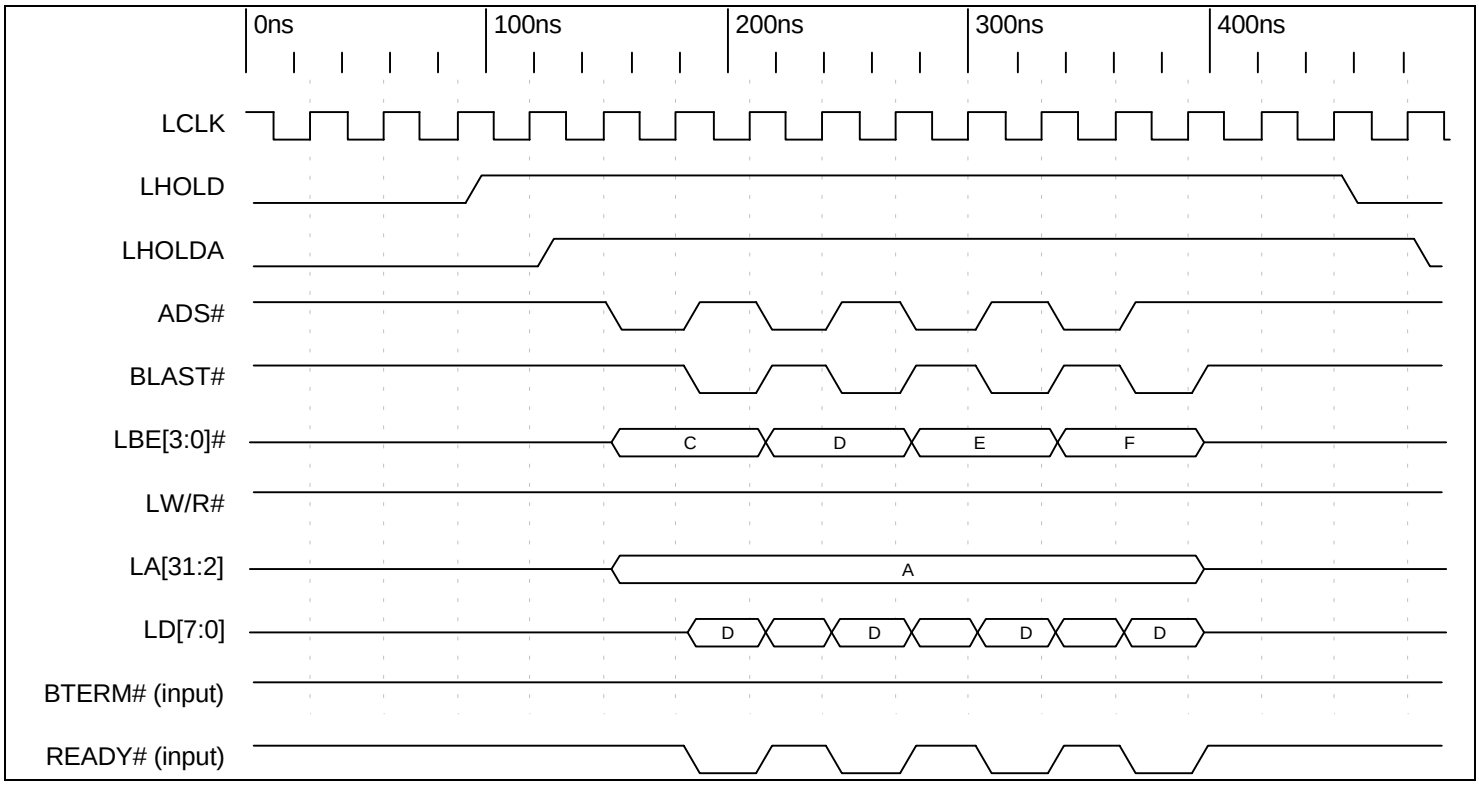
Timing Diagram 5-28. Direct Slave Single Read with One Wait State Using READY# Input (32-Bit Local Bus)



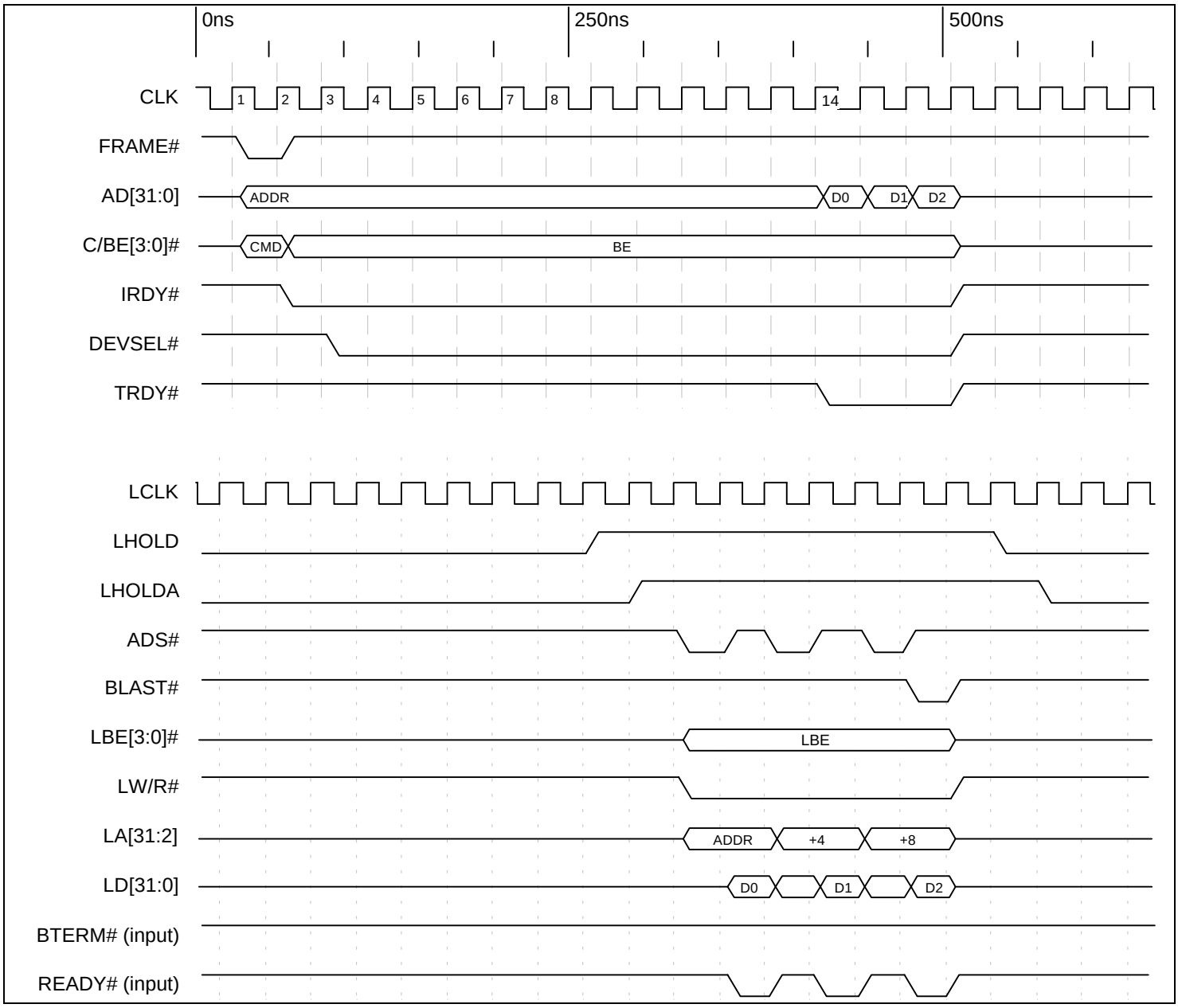
Timing Diagram 5-29. Direct Slave Single Read with One Wait State Using Internal Wait State (32-Bit Local Bus)



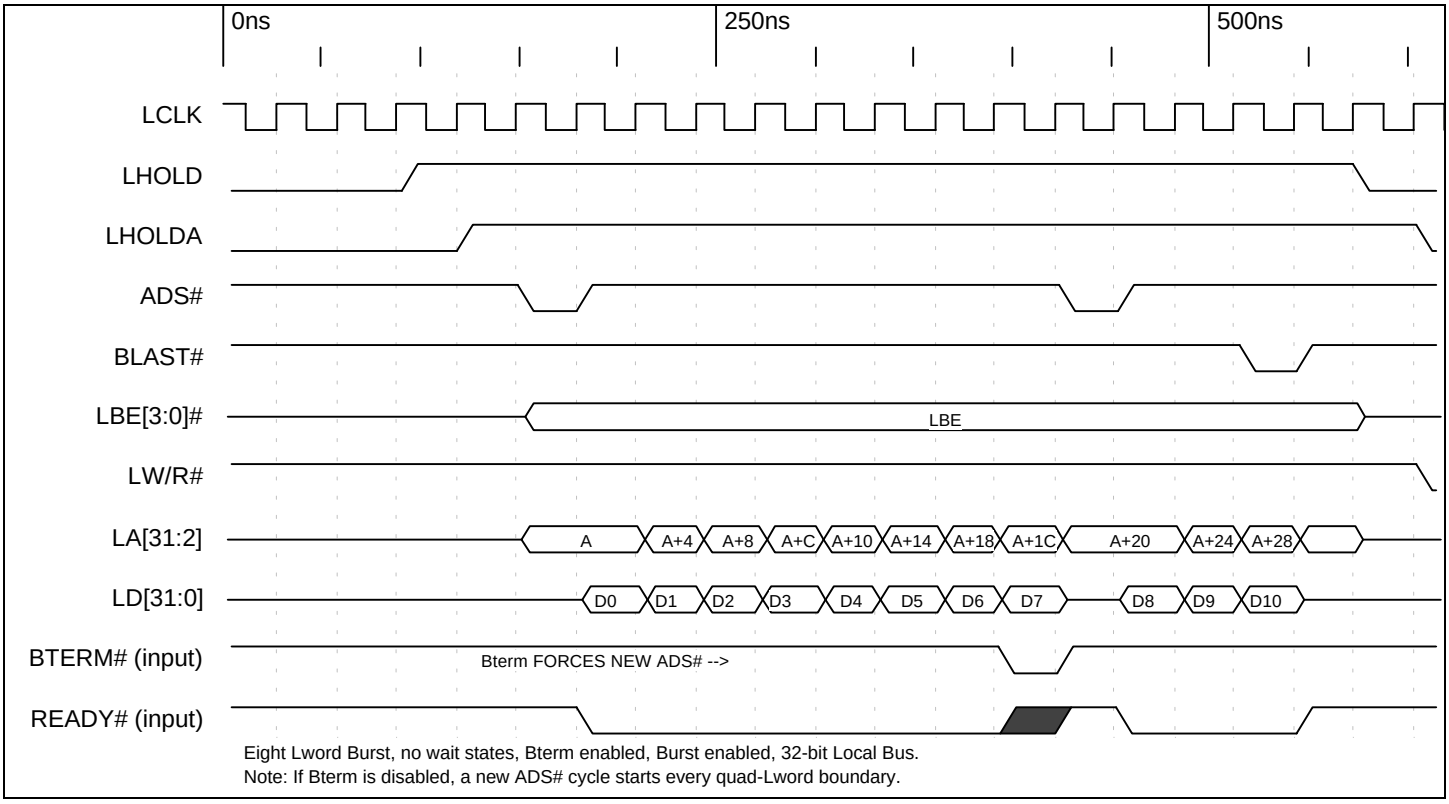
Timing Diagram 5-30. Direct Slave Non-Burst Write (32-Bit Local Bus)



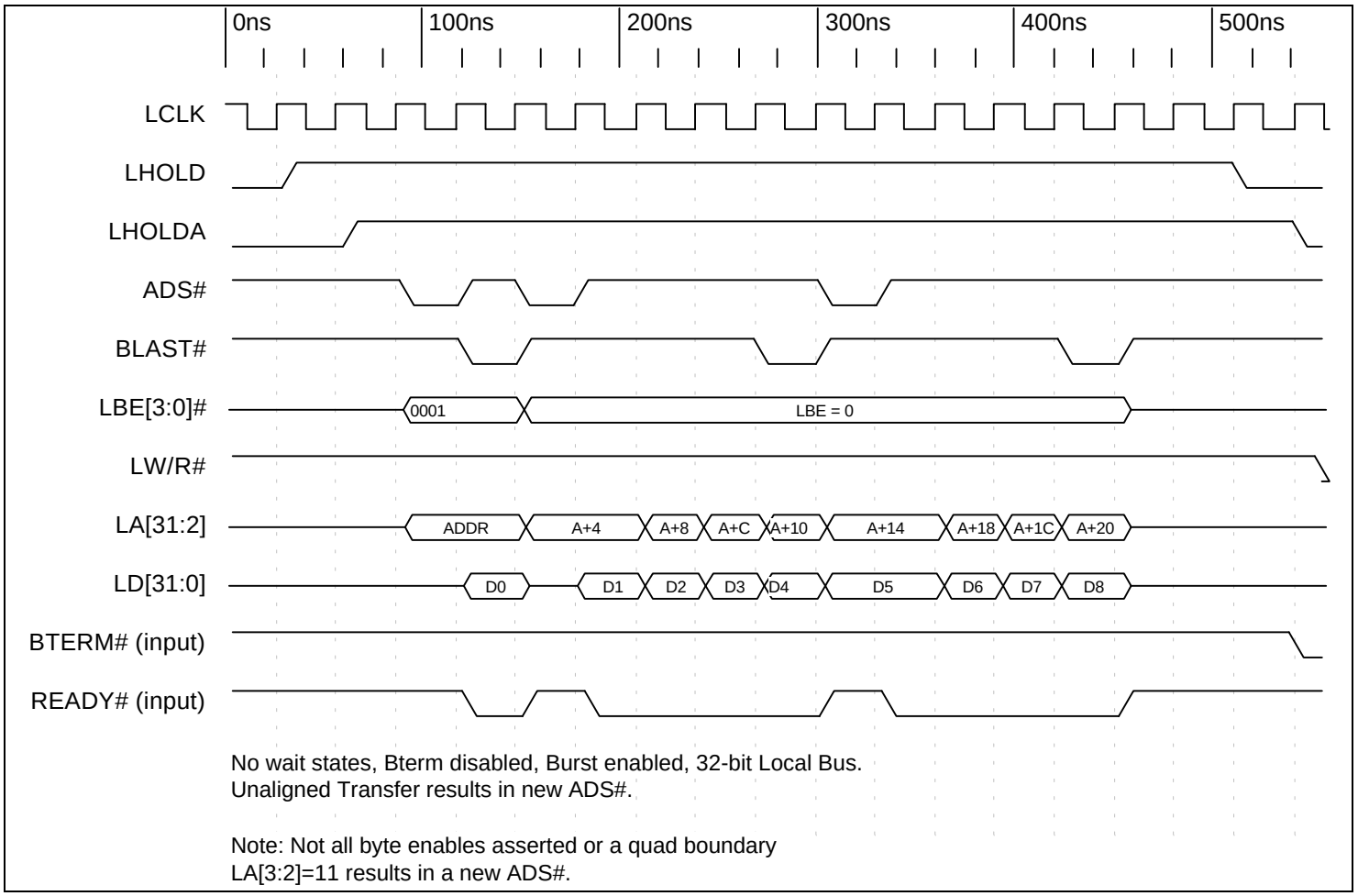
Timing Diagram 5-31. Direct Slave Non-Burst Write (8-Bit Local Bus)



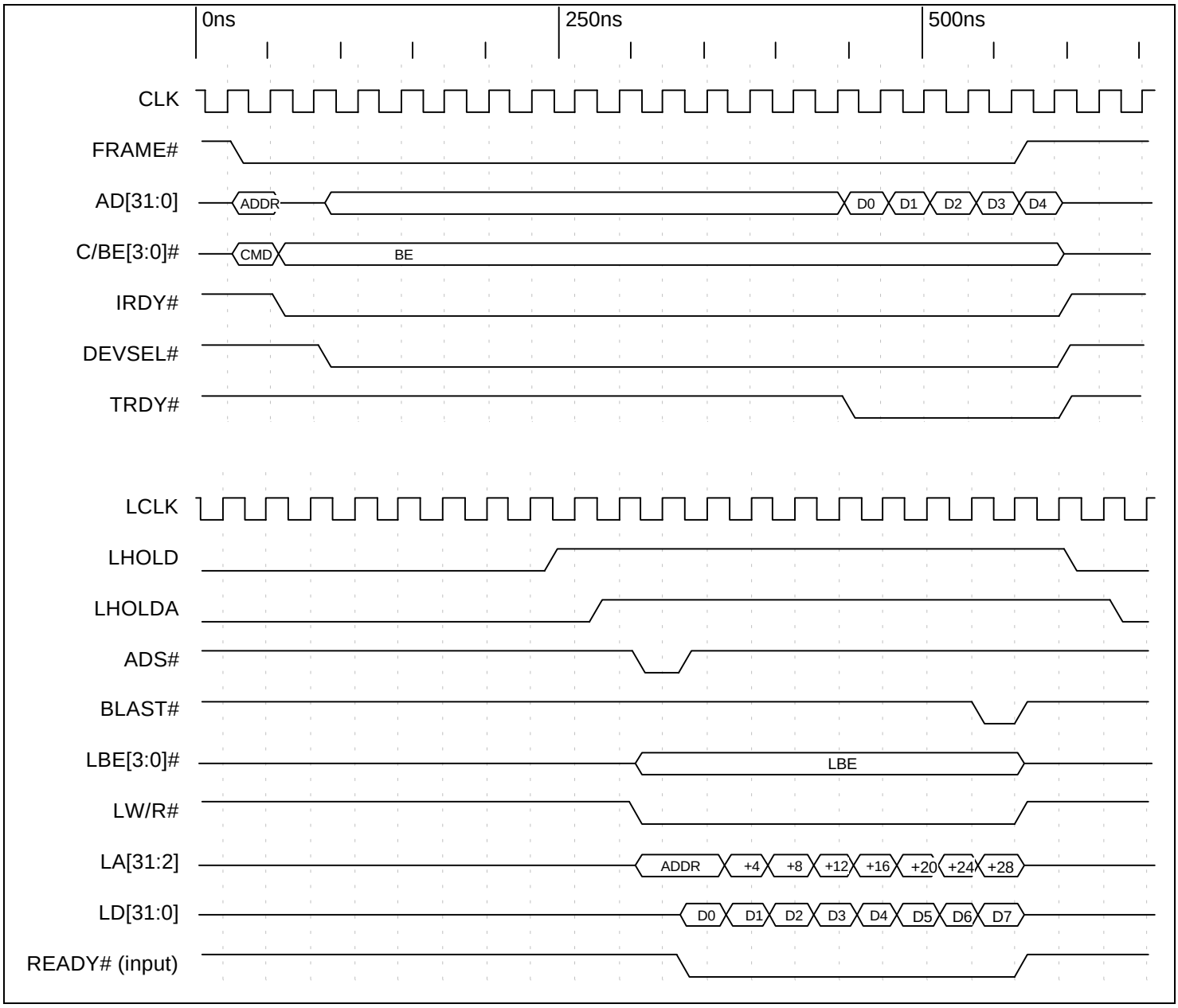
Timing Diagram 5-32. Direct Slave Non-Burst Read



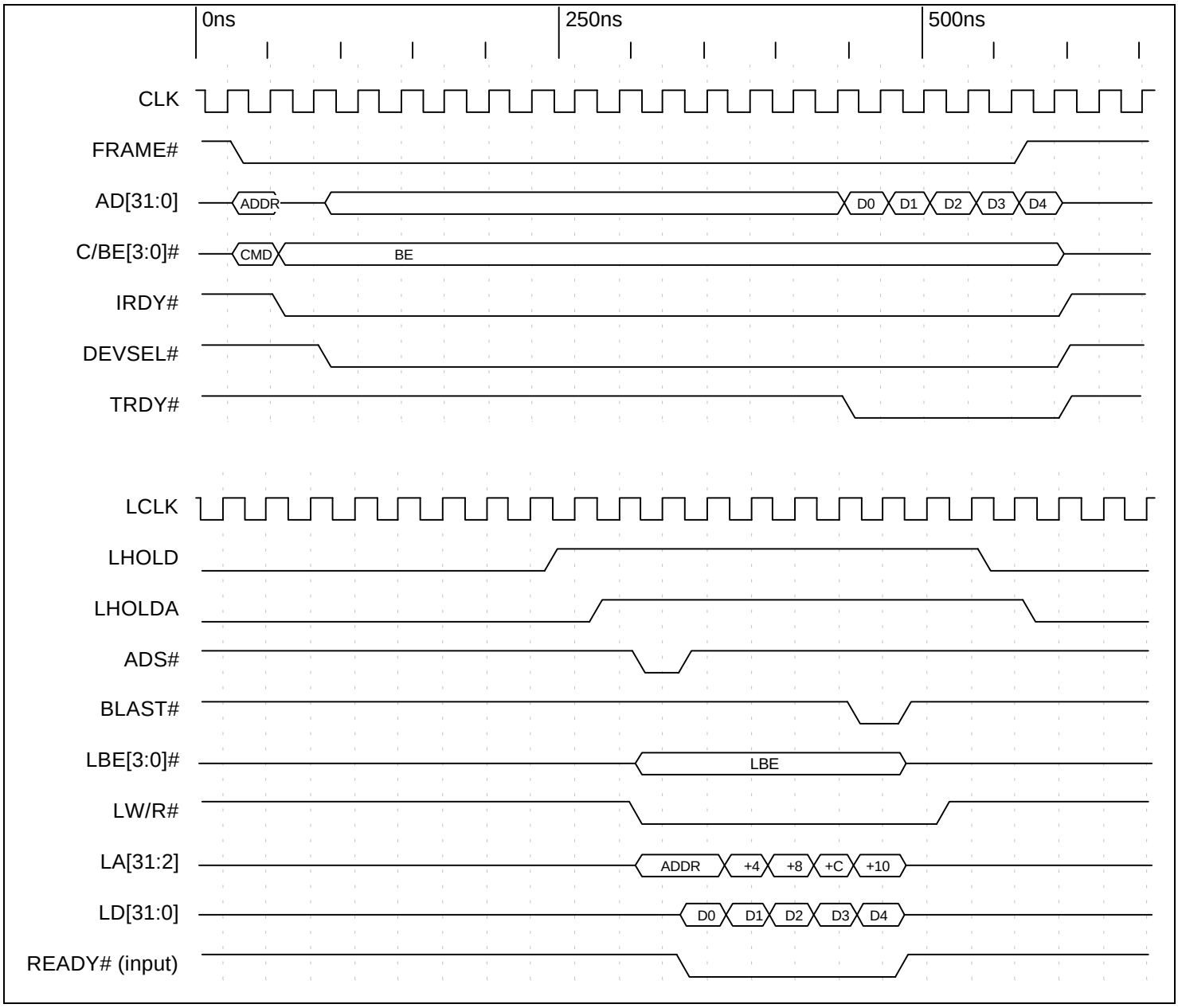
Timing Diagram 5-33. Direct Slave Burst Write with Bterm Enabled (32-Bit Local Bus)



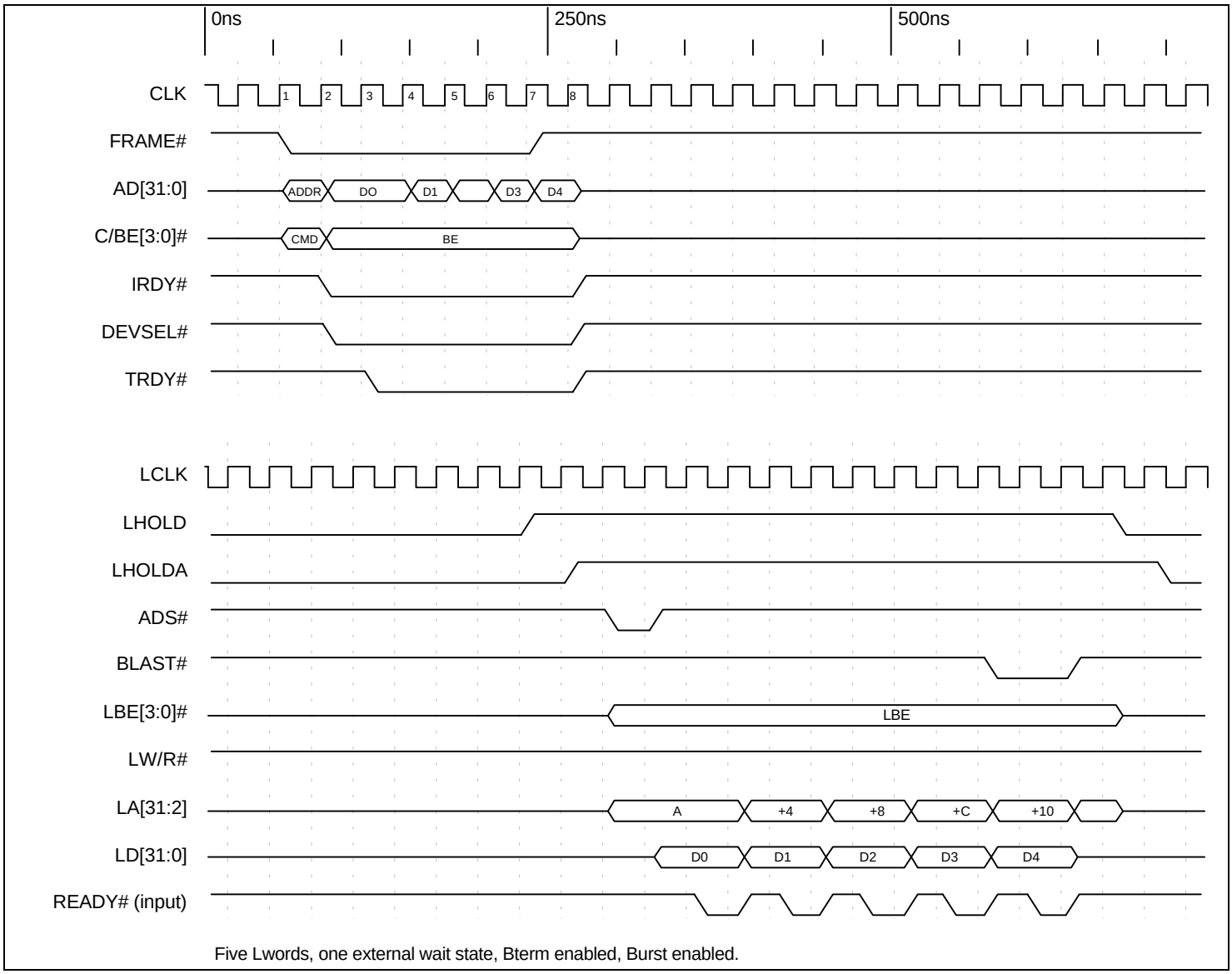
Timing Diagram 5-34. Direct Slave Burst Write with Bterm Disabled (32-Bit Local Bus)



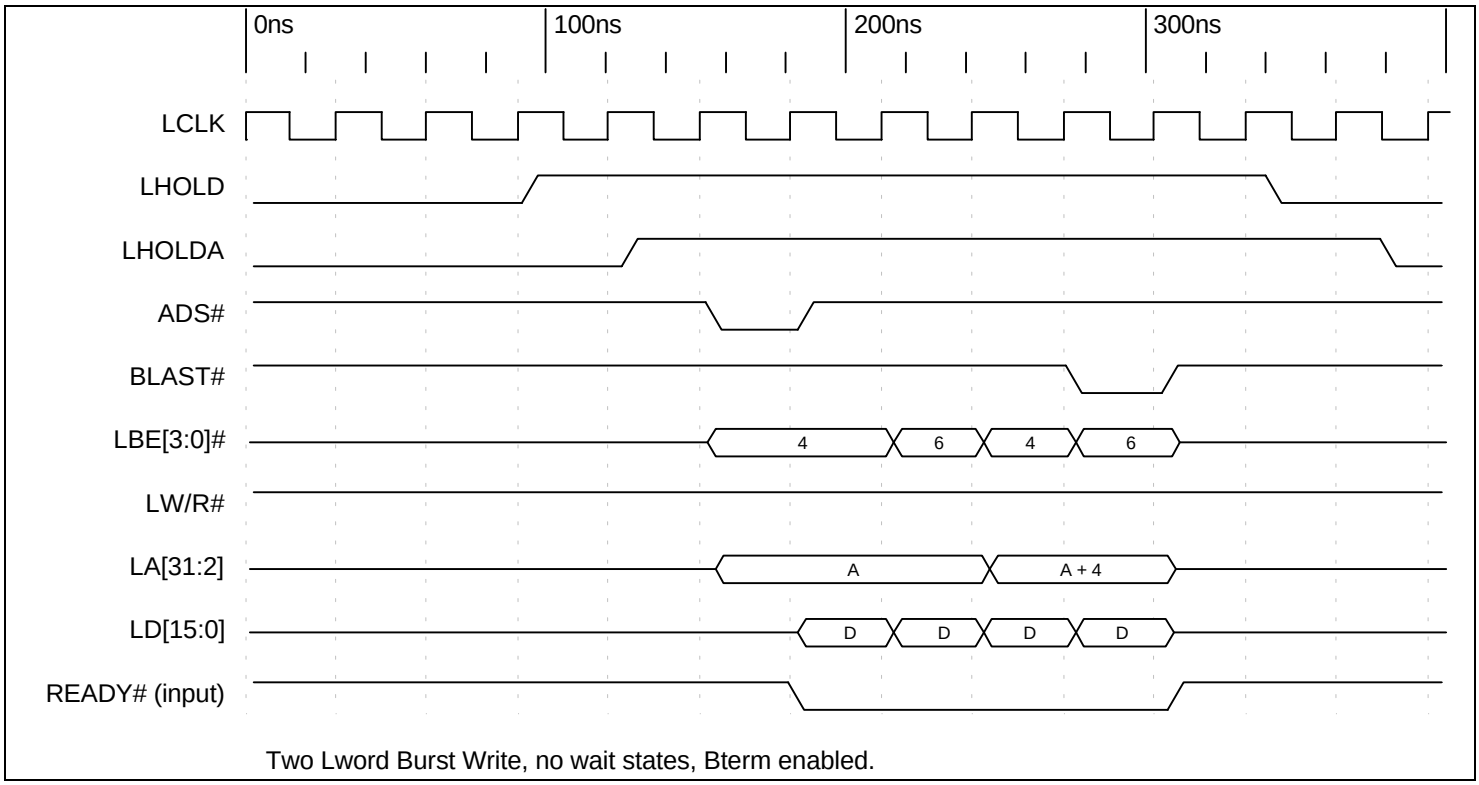
Timing Diagram 5-35. Direct Slave Burst Read with Prefetch Counter Set to 8 (32-Bit Local Bus)



Timing Diagram 5-36. Direct Slave Burst Read with Prefetch Counter Set to 5 (32-Bit Local Bus)

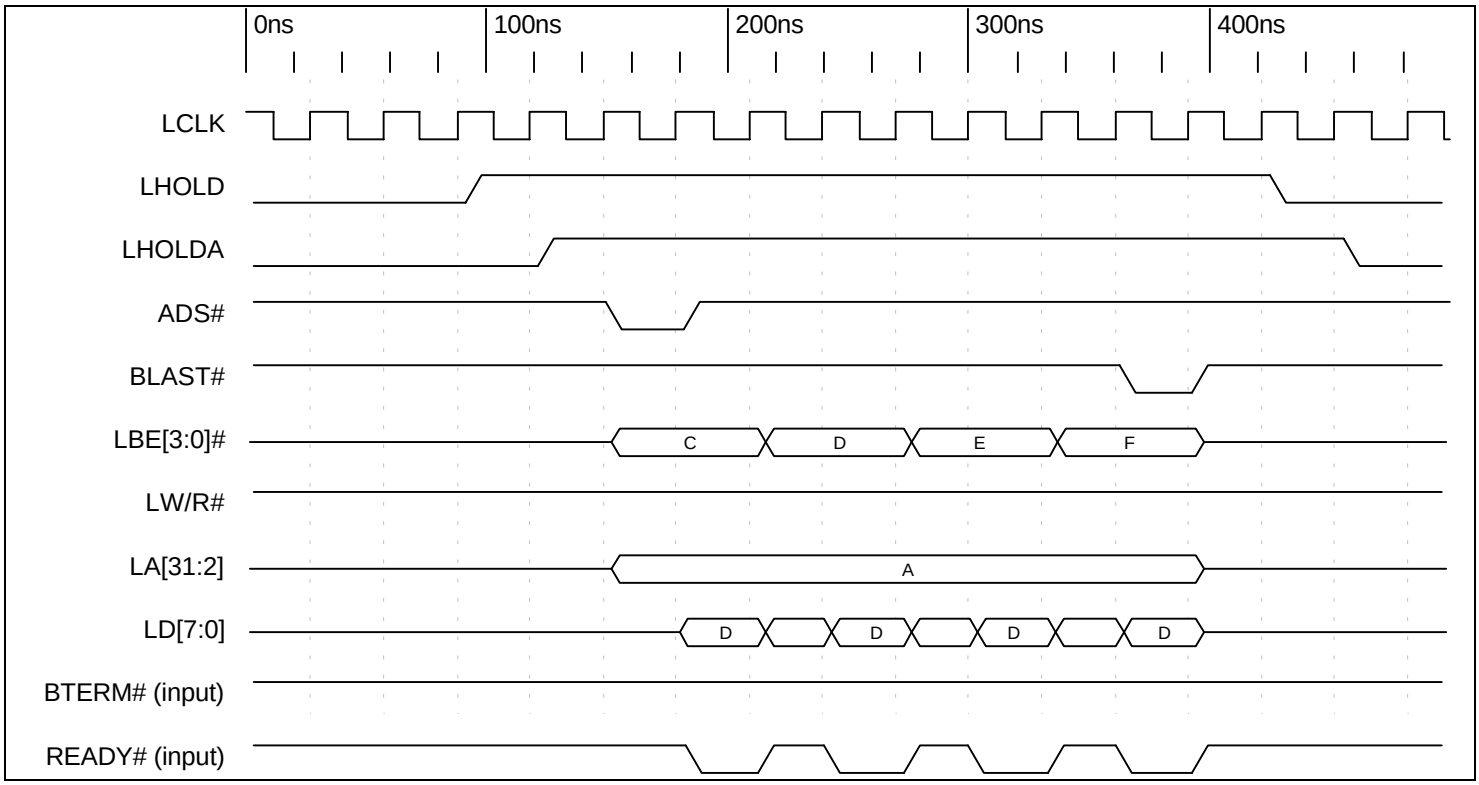


Timing Diagram 5-37. Direct Slave Burst Write (32-Bit Local Bus)

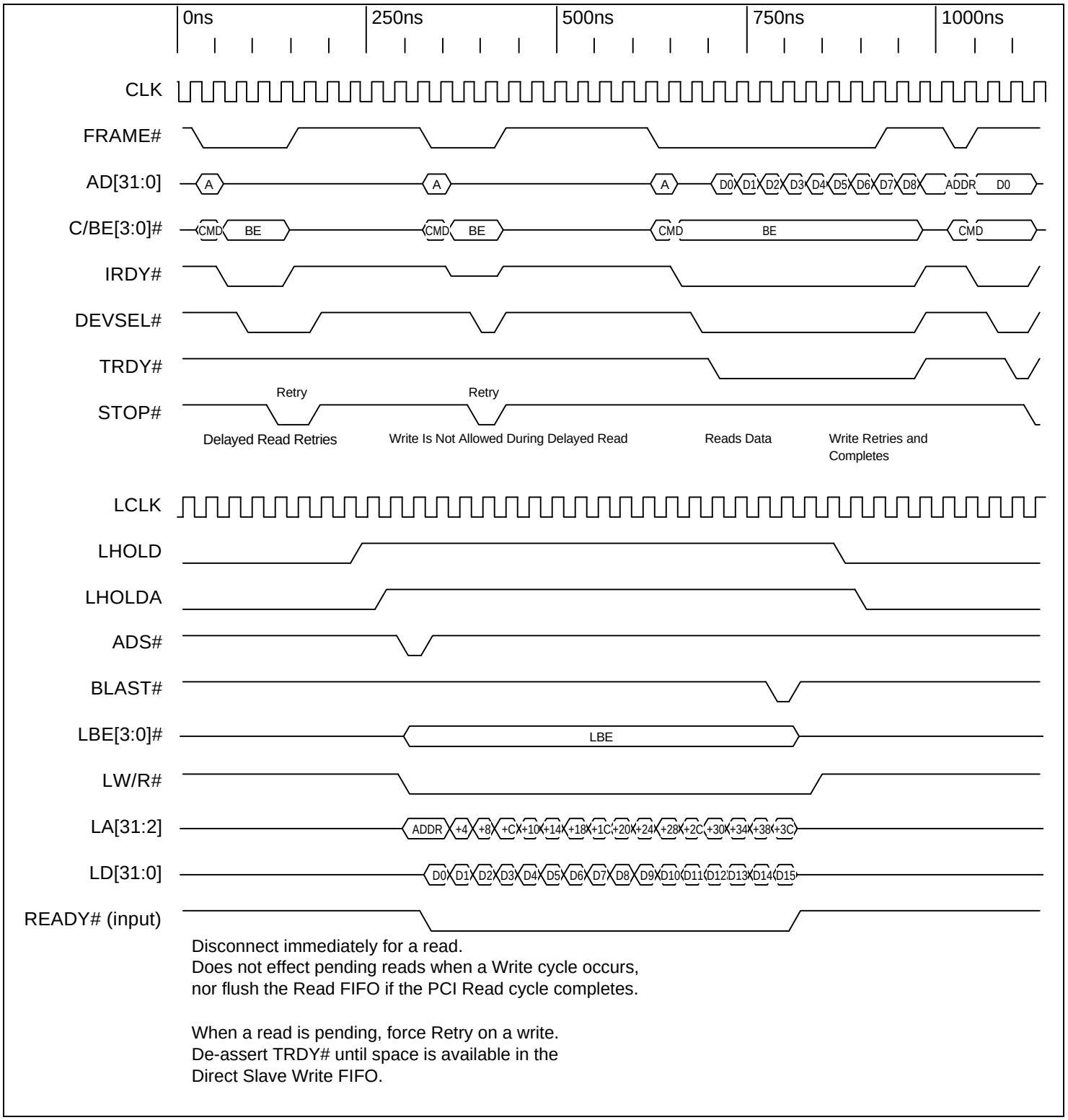


Two Lword Burst Write, no wait states, Bterm enabled.

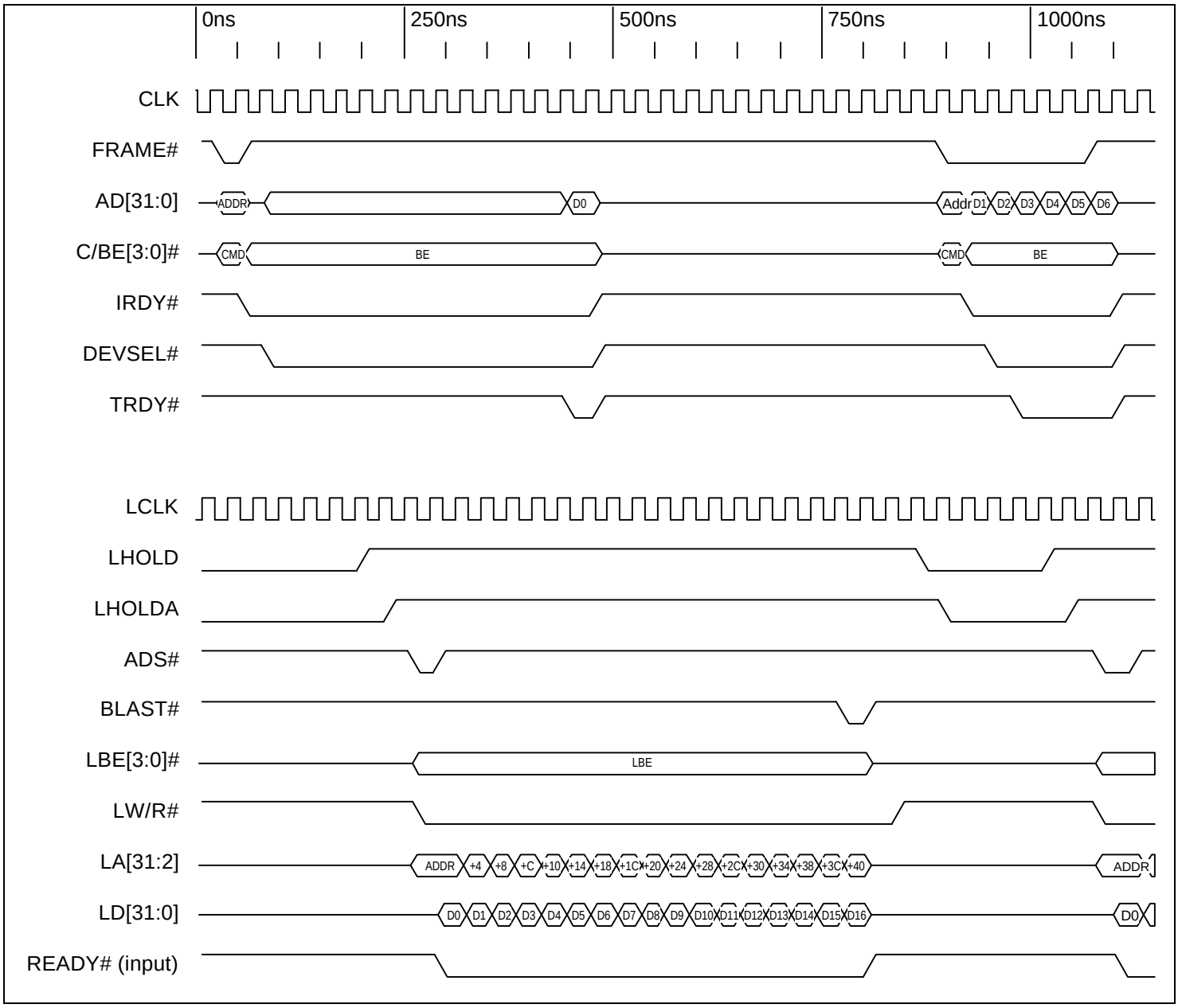
Timing Diagram 5-38. Direct Slave Burst Write (16-Bit Local Bus)



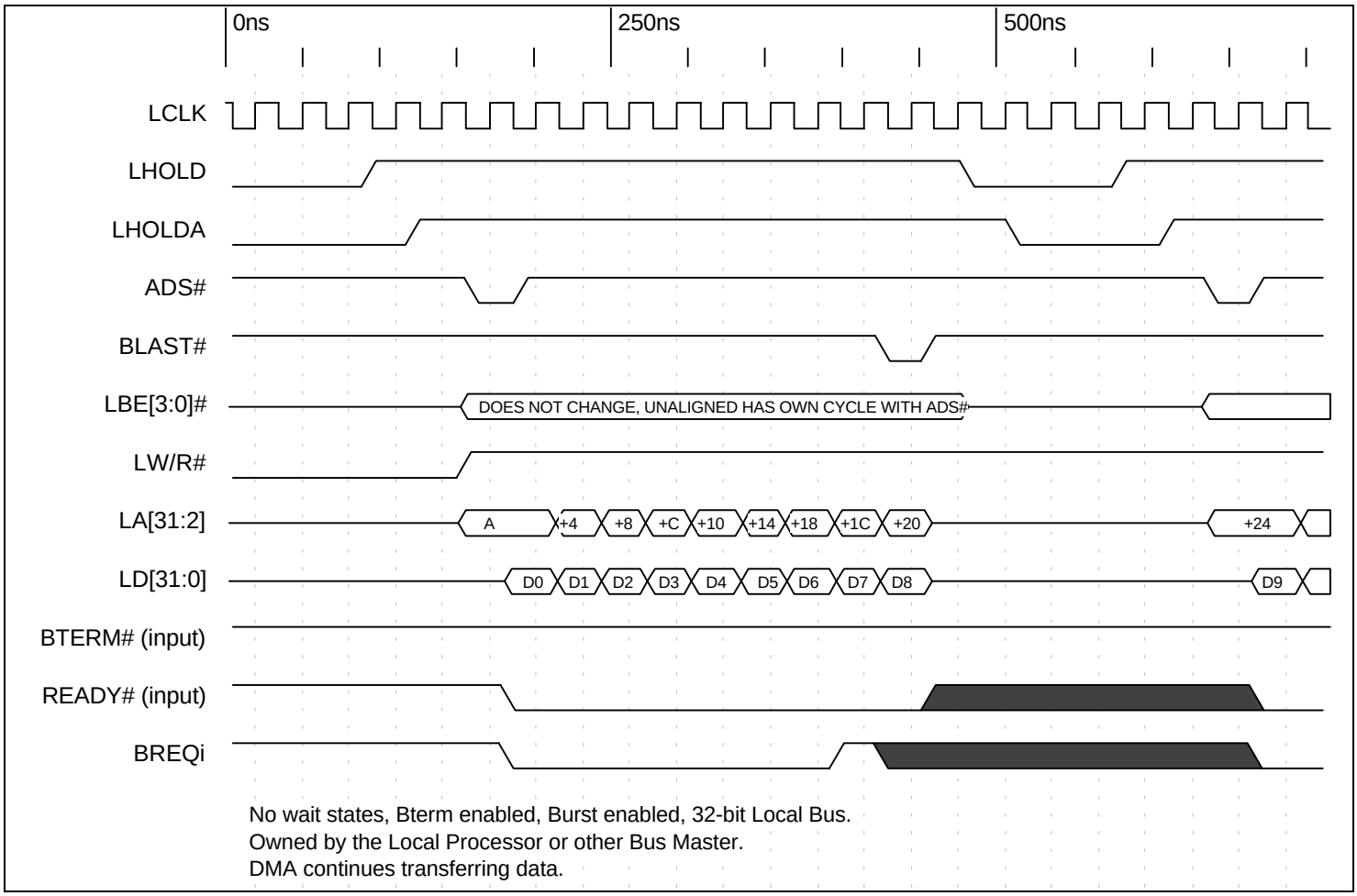
Timing Diagram 5-39. Direct Slave Burst Write with External Wait States (8-Bit Local Bus)



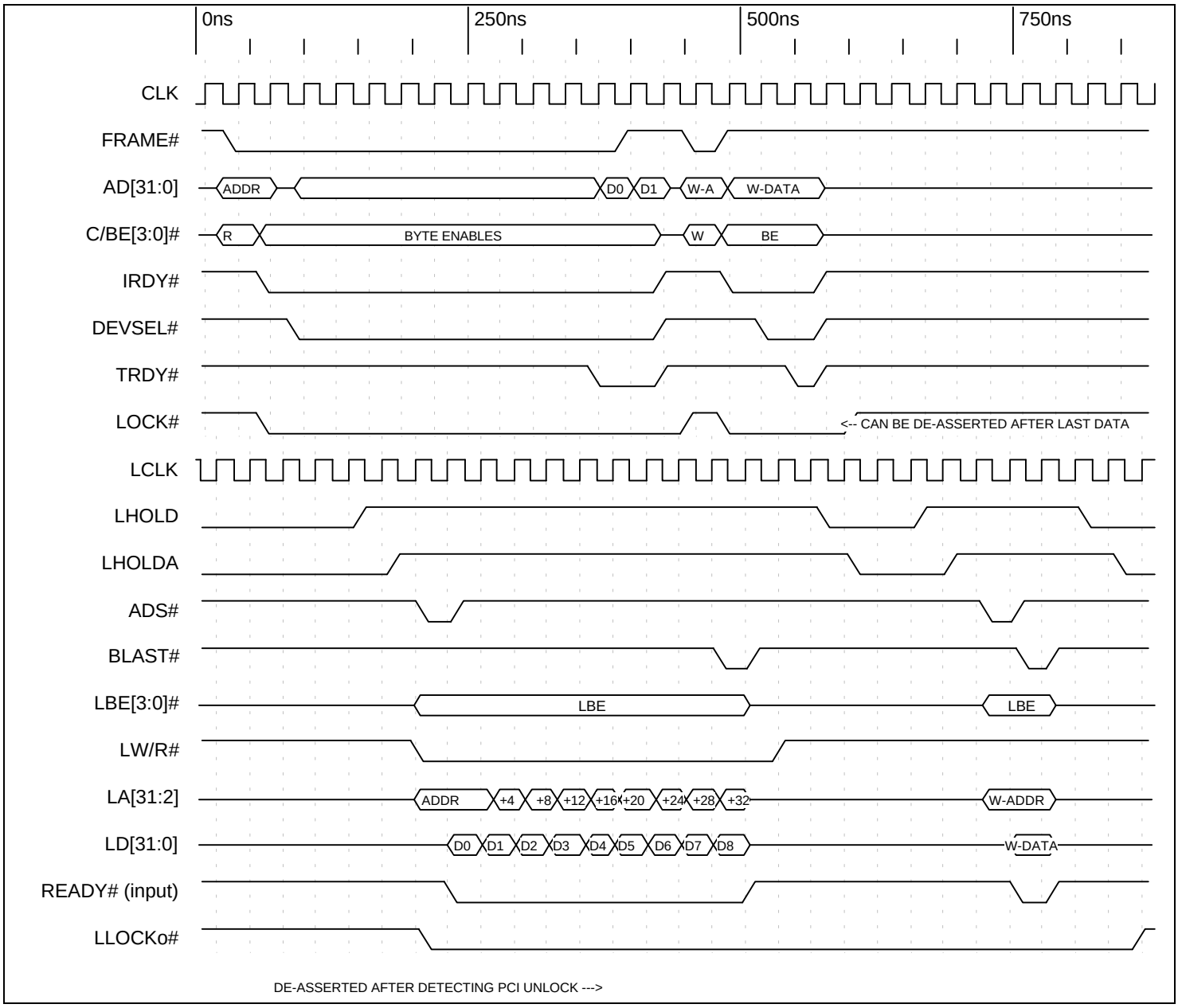
Timing Diagram 5-40. Delayed Read Transaction PCI Specification v2.1



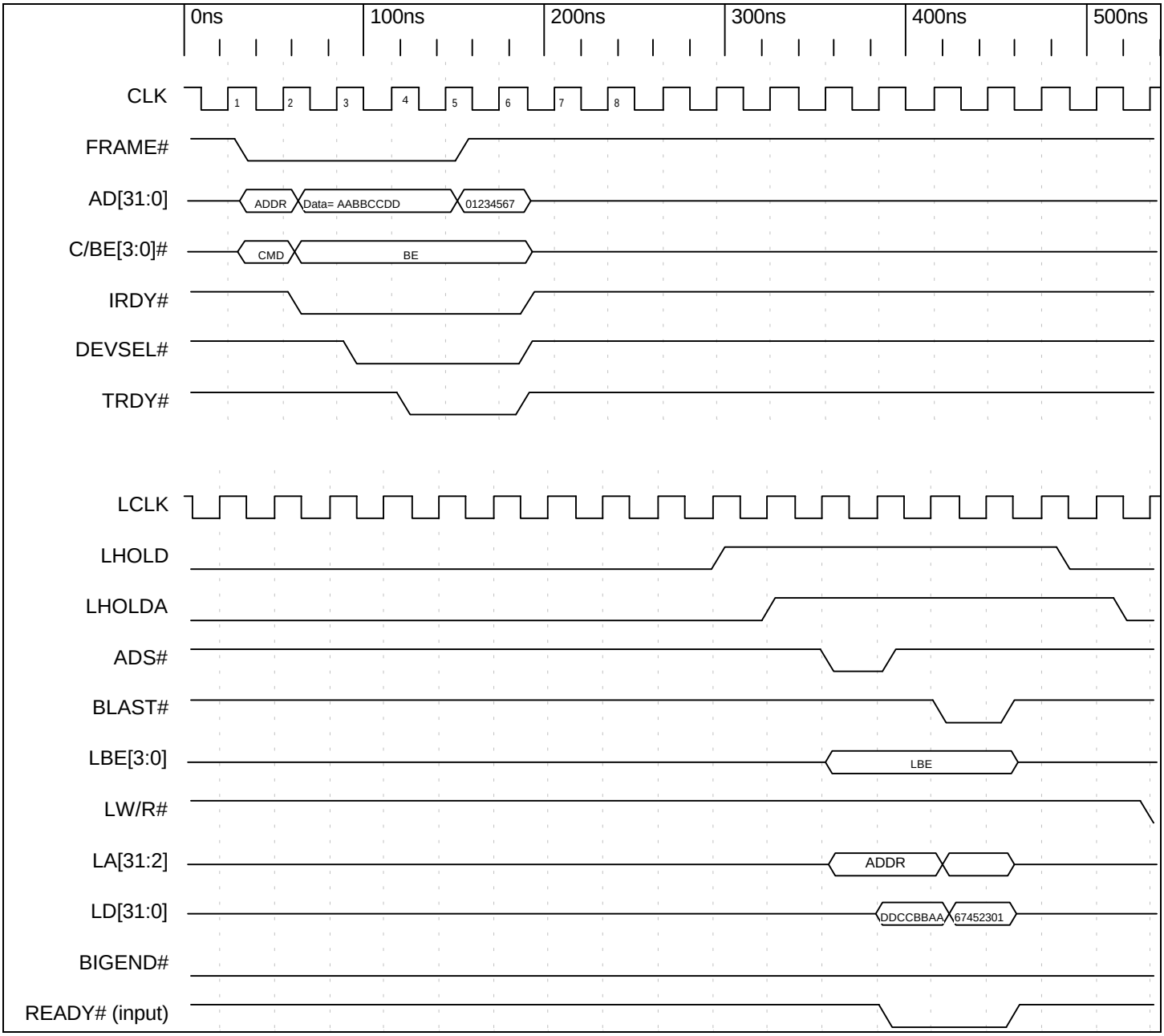
Timing Diagram 5-41. Direct Slave Read No Flush Mode (Read Ahead Mode), Prefetch Enabled, Prefetch Count Disabled



Timing Diagram 5-42. Direct Slave Burst Write Suspended by BREQi

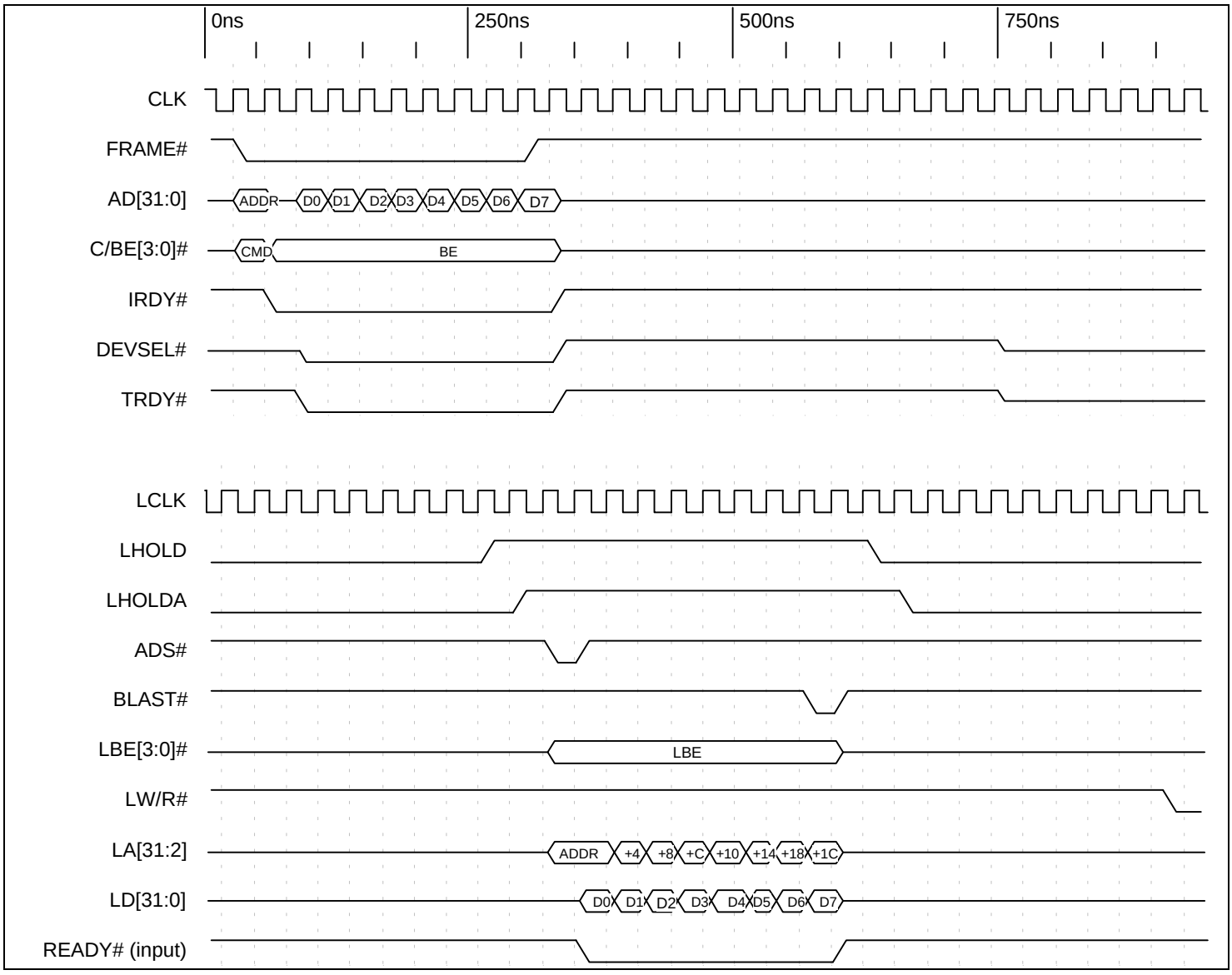


Timing Diagram 5-43. Locked Direct Slave Read Followed by Write and Release (LLOCKo#)

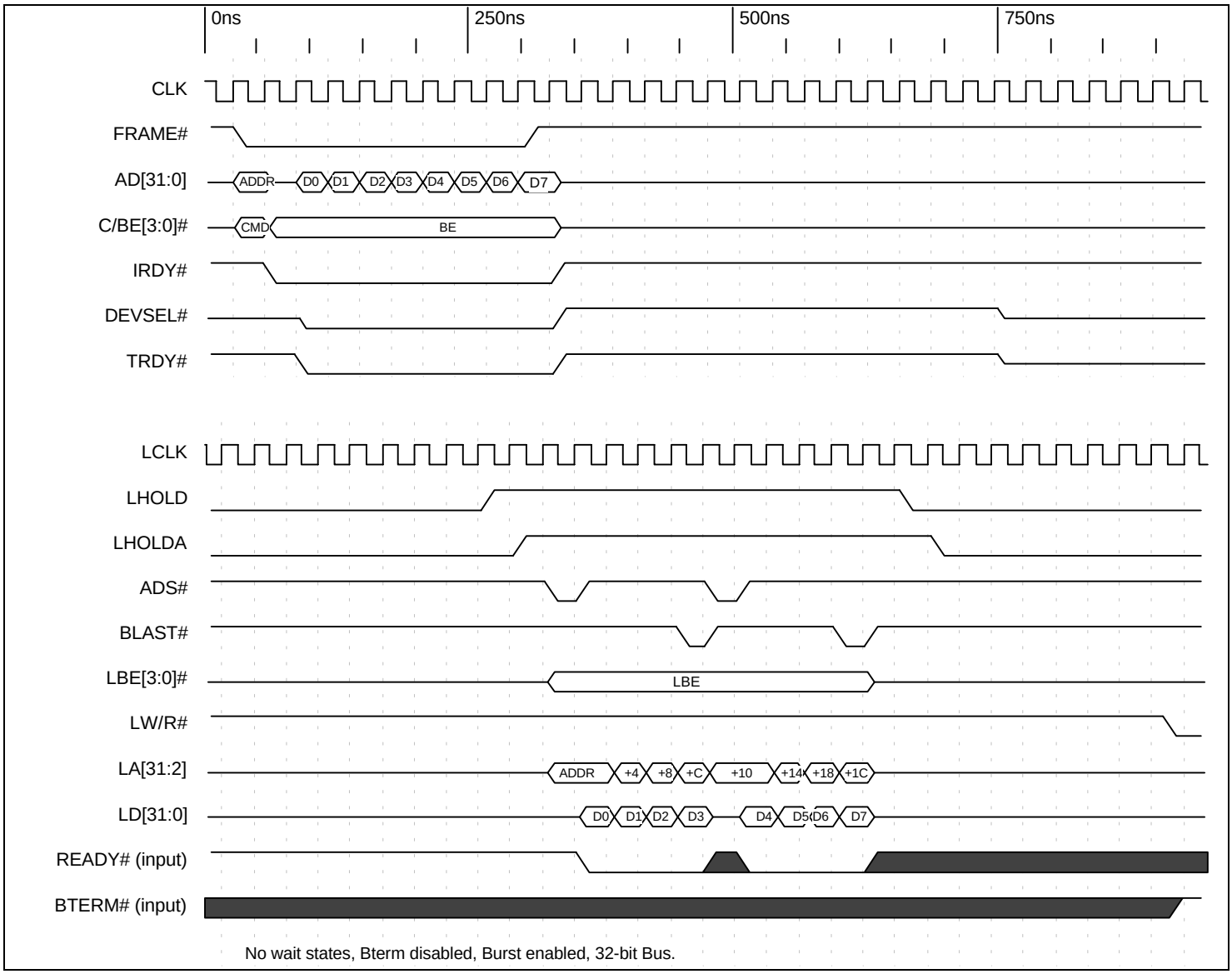


Timing Diagram 5-44. Direct Slave in BIGEND Local Bus with BIGEND# Input

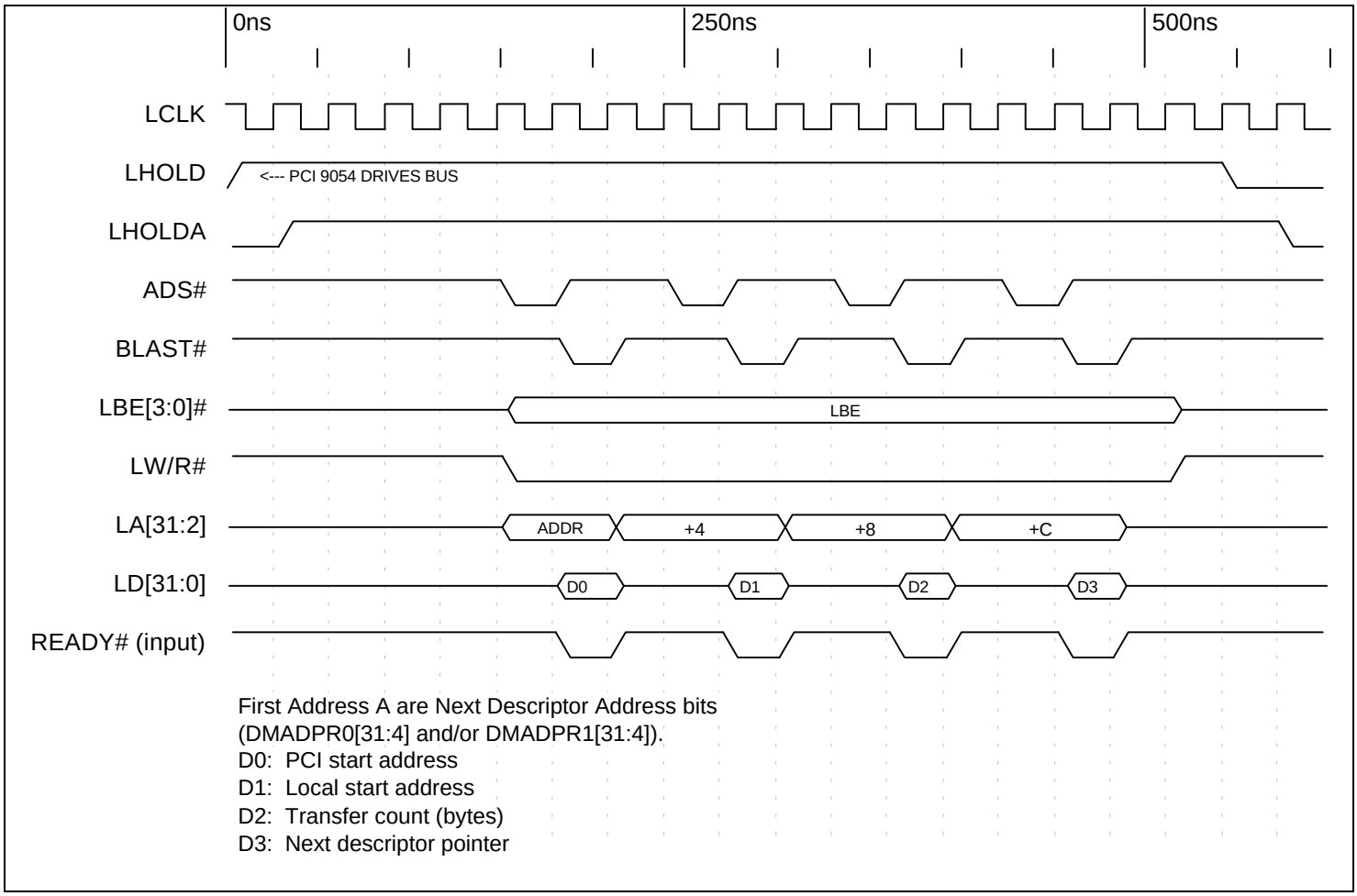
5.6.3 C Mode DMA



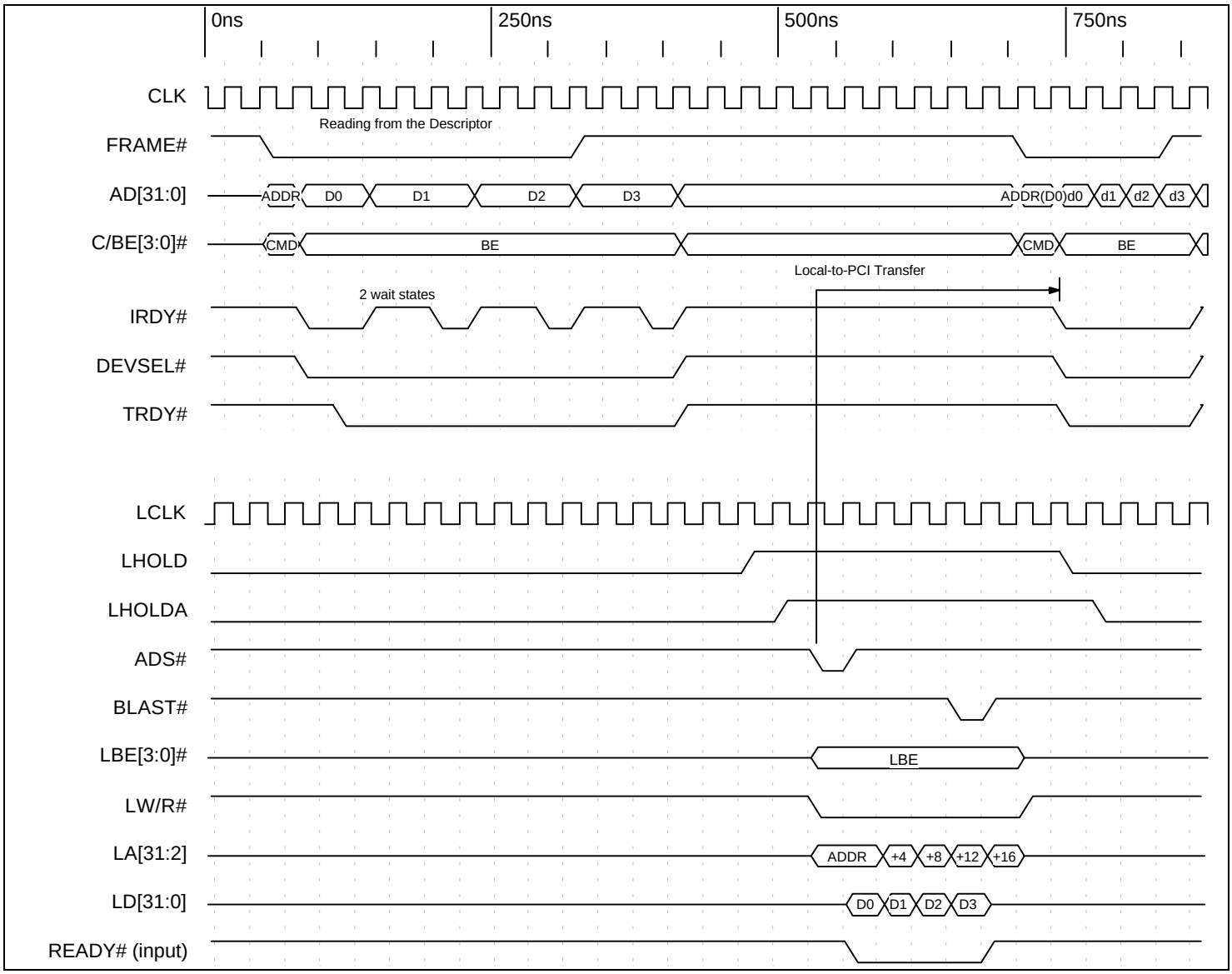
Timing Diagram 5-45. DMA Aligned PCI Address to Aligned Local Address, Bterm Enabled, Burst Enabled



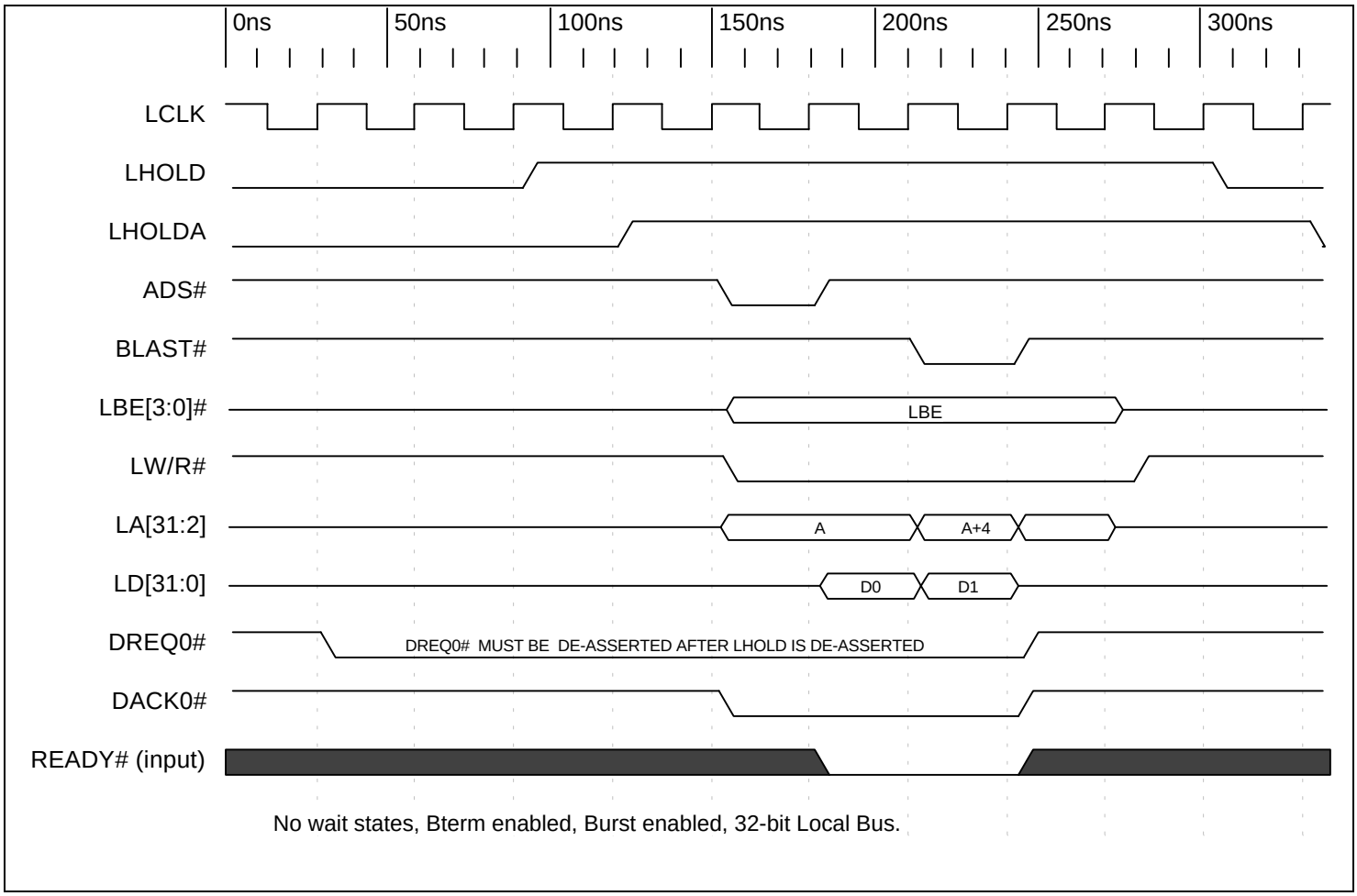
Timing Diagram 5-46. DMA Aligned PCI Address to Aligned Local Address, Bterm Disabled, Burst Enabled



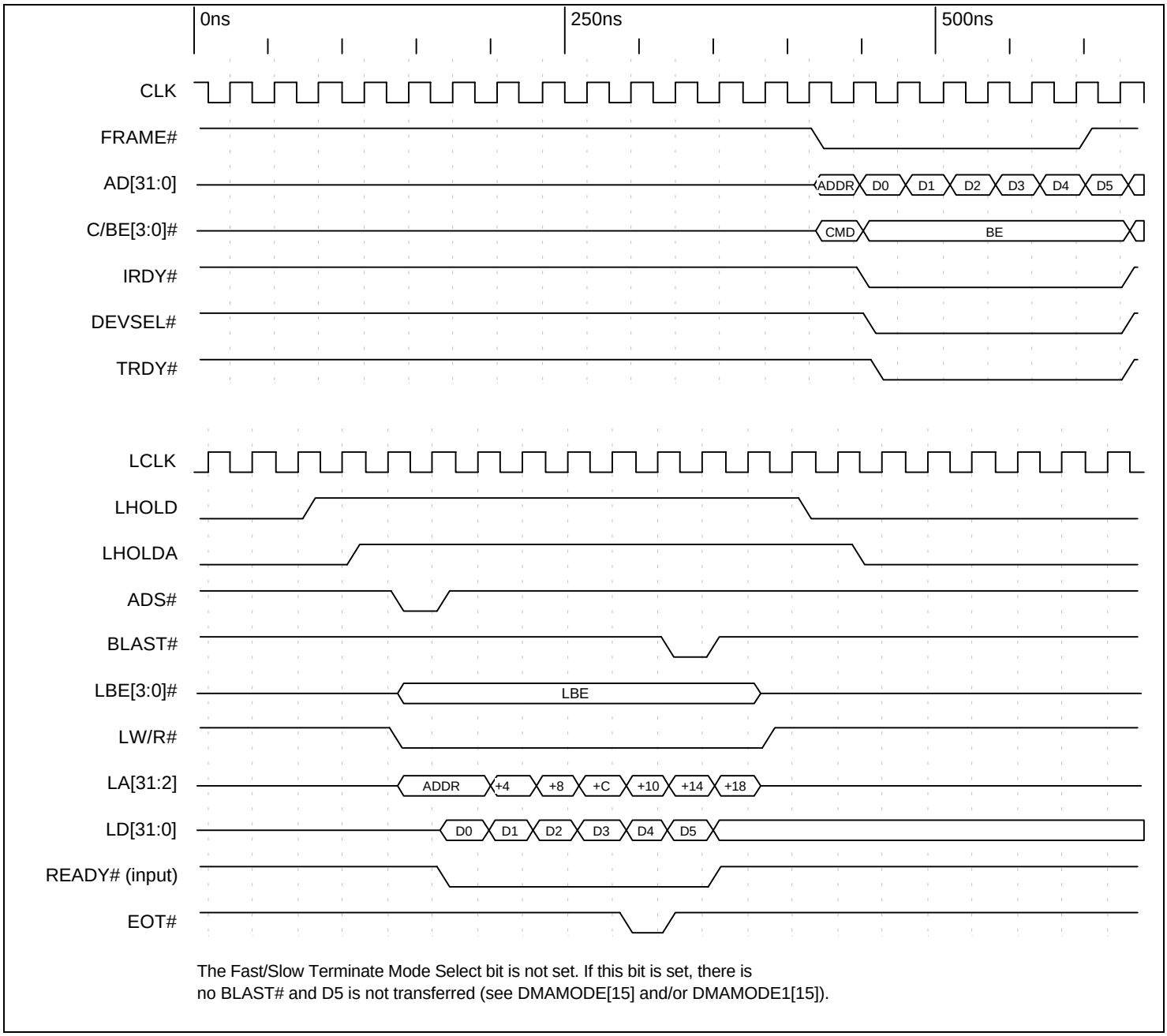
Timing Diagram 5-47. Scatter/Gather DMA with Descriptor on Local Bus



Timing Diagram 5-48. Scatter/Gather DMA from Local-to-PCI with Descriptor on PCI Bus

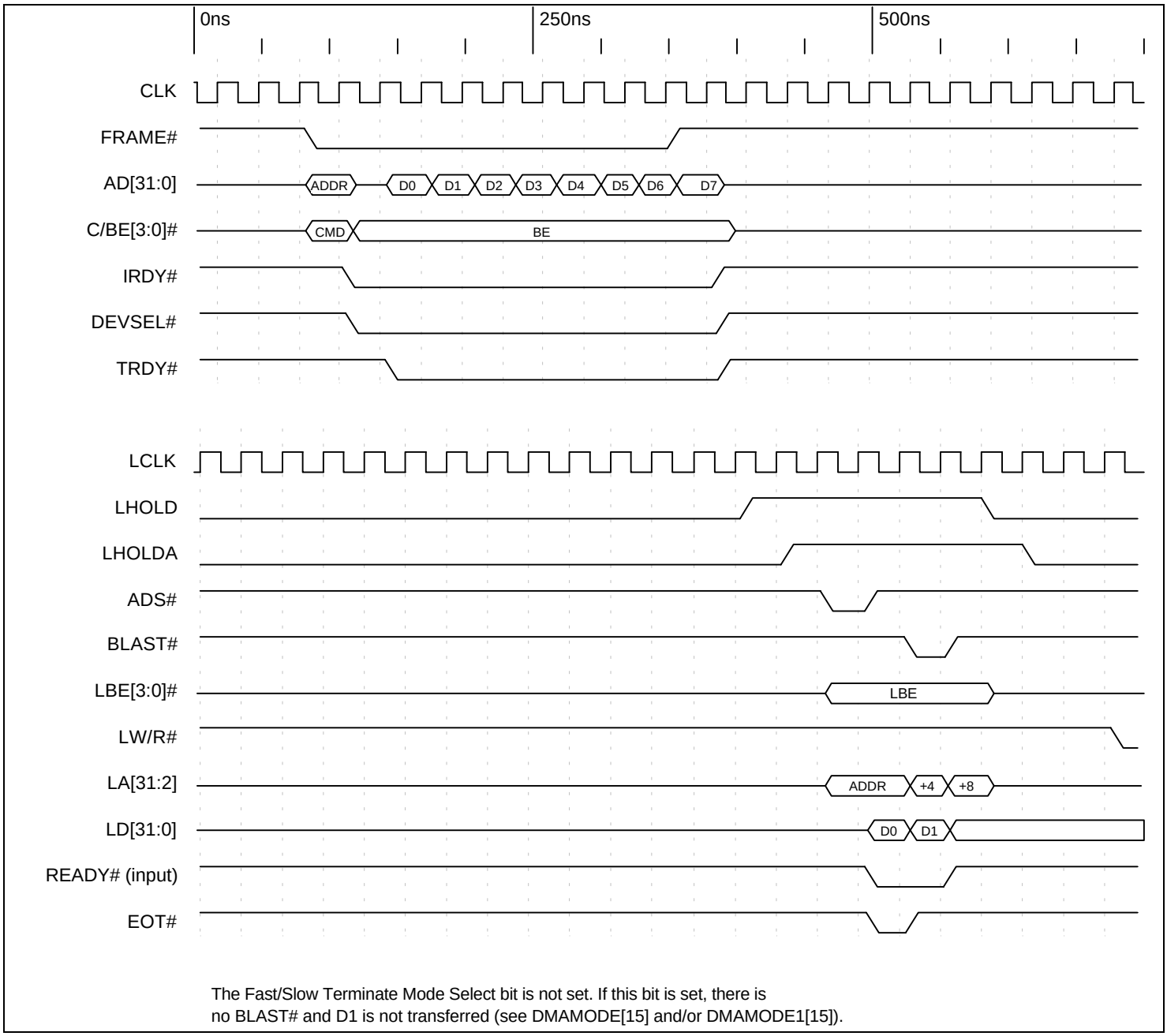


Timing Diagram 5-49. Demand DMA, Terminate with BLAST# (Local-to-PCI)



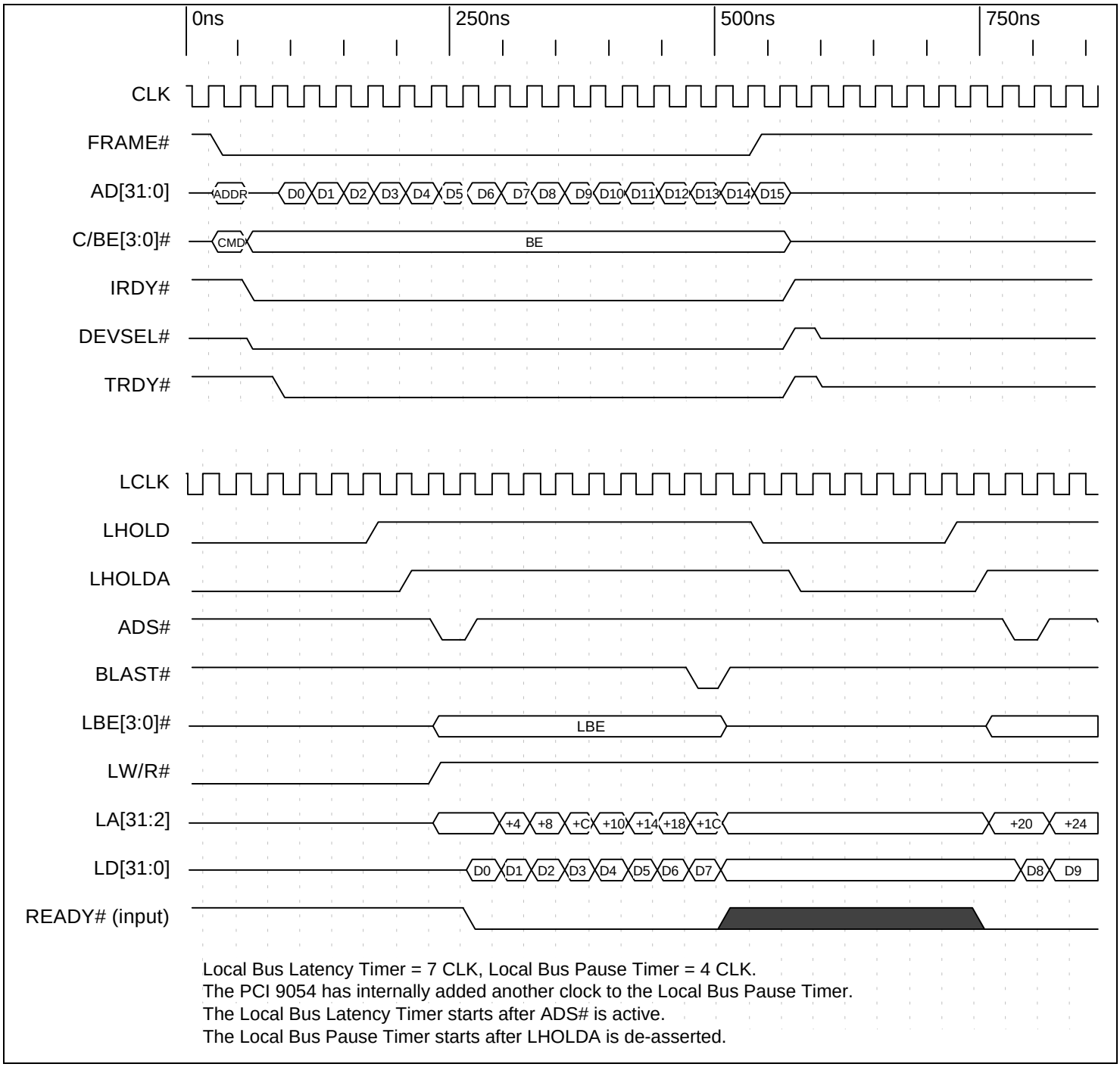
The Fast/Slow Terminate Mode Select bit is not set. If this bit is set, there is no BLAST# and D5 is not transferred (see DMAMODE[15] and/or DMAMODE1[15]).

Timing Diagram 5-50. DMA Local-to-PCI, Terminate with EOT#

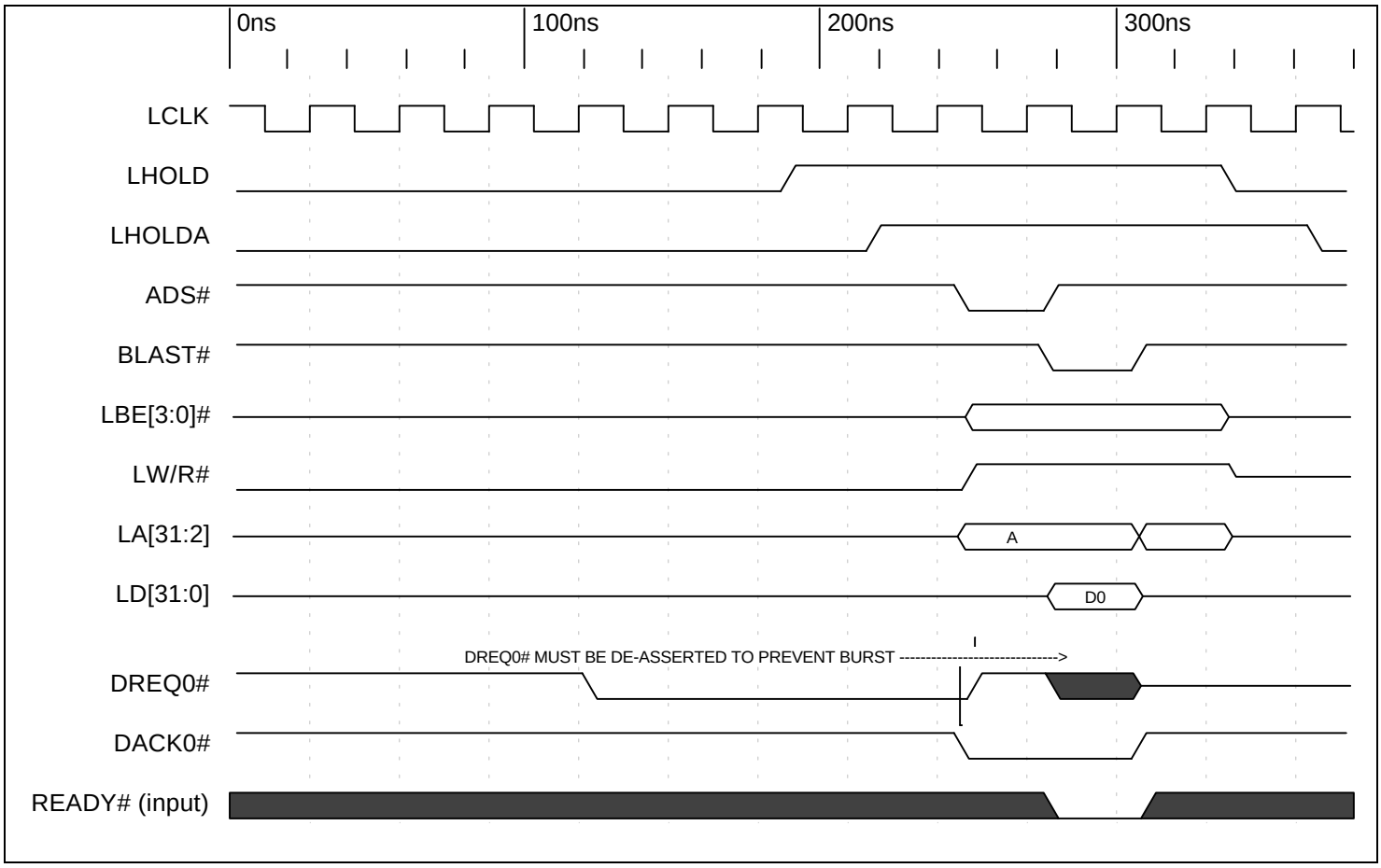


The Fast/Slow Terminate Mode Select bit is not set. If this bit is set, there is no BLAST# and D1 is not transferred (see DMAMODE[15] and/or DMAMODE1[15]).

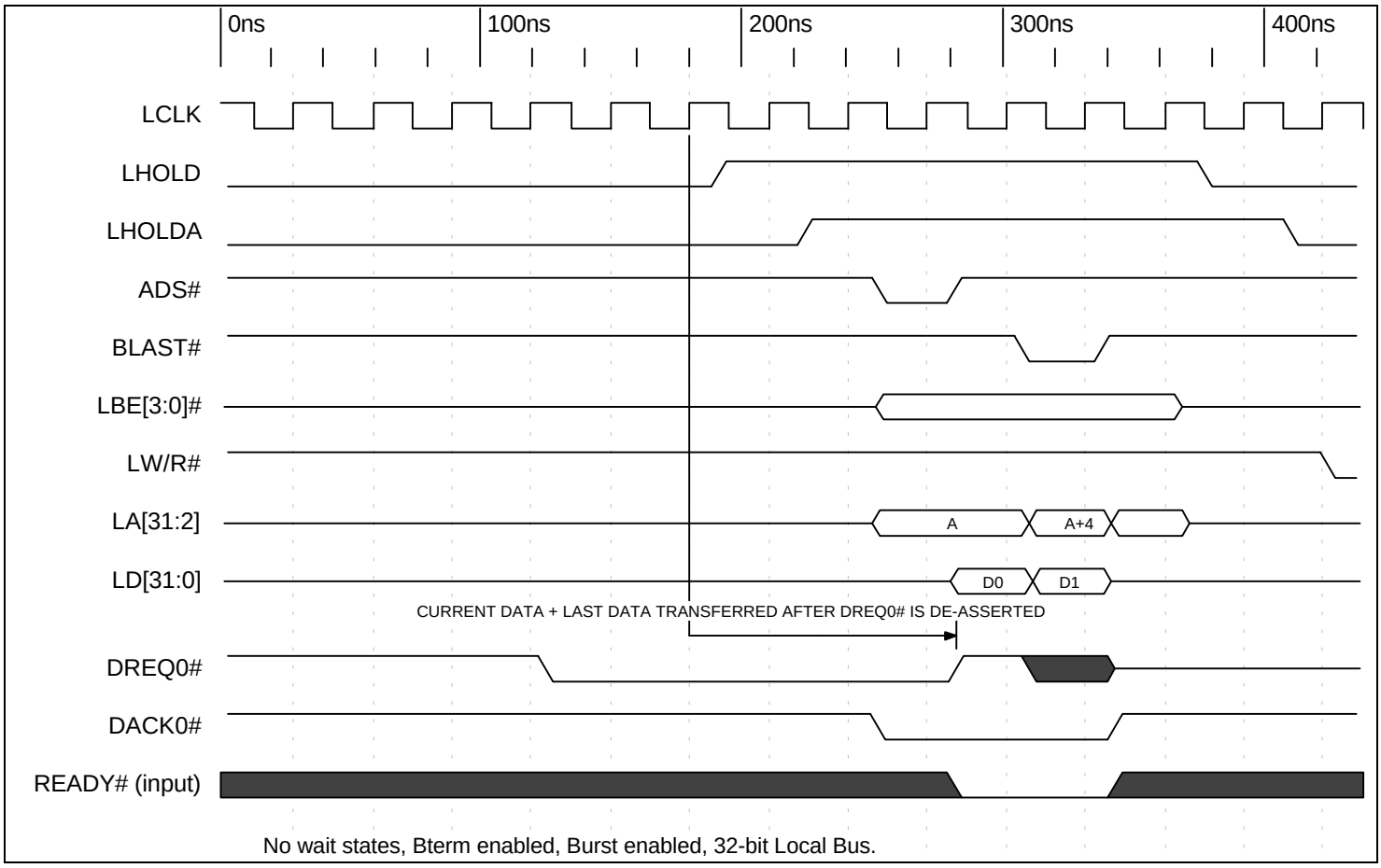
Timing Diagram 5-51. DMA PCI-to-Local, Terminate with EOT#



Timing Diagram 5-52. DMA PCI-to-Local with Local Bus Pause and Latency Timers



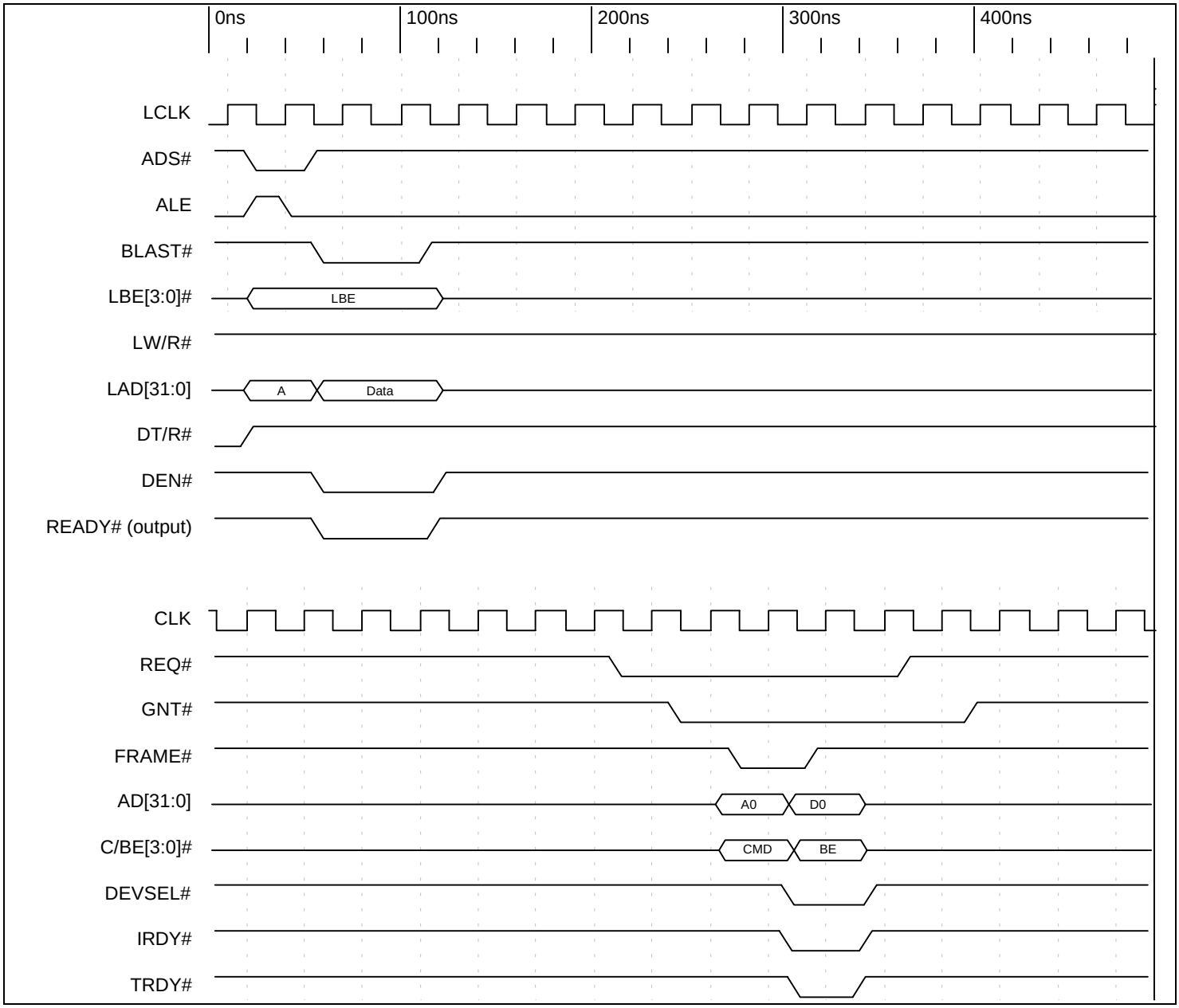
Timing Diagram 5-53. Single-Cycle Demand DMA Mode (PCI-to-Local)



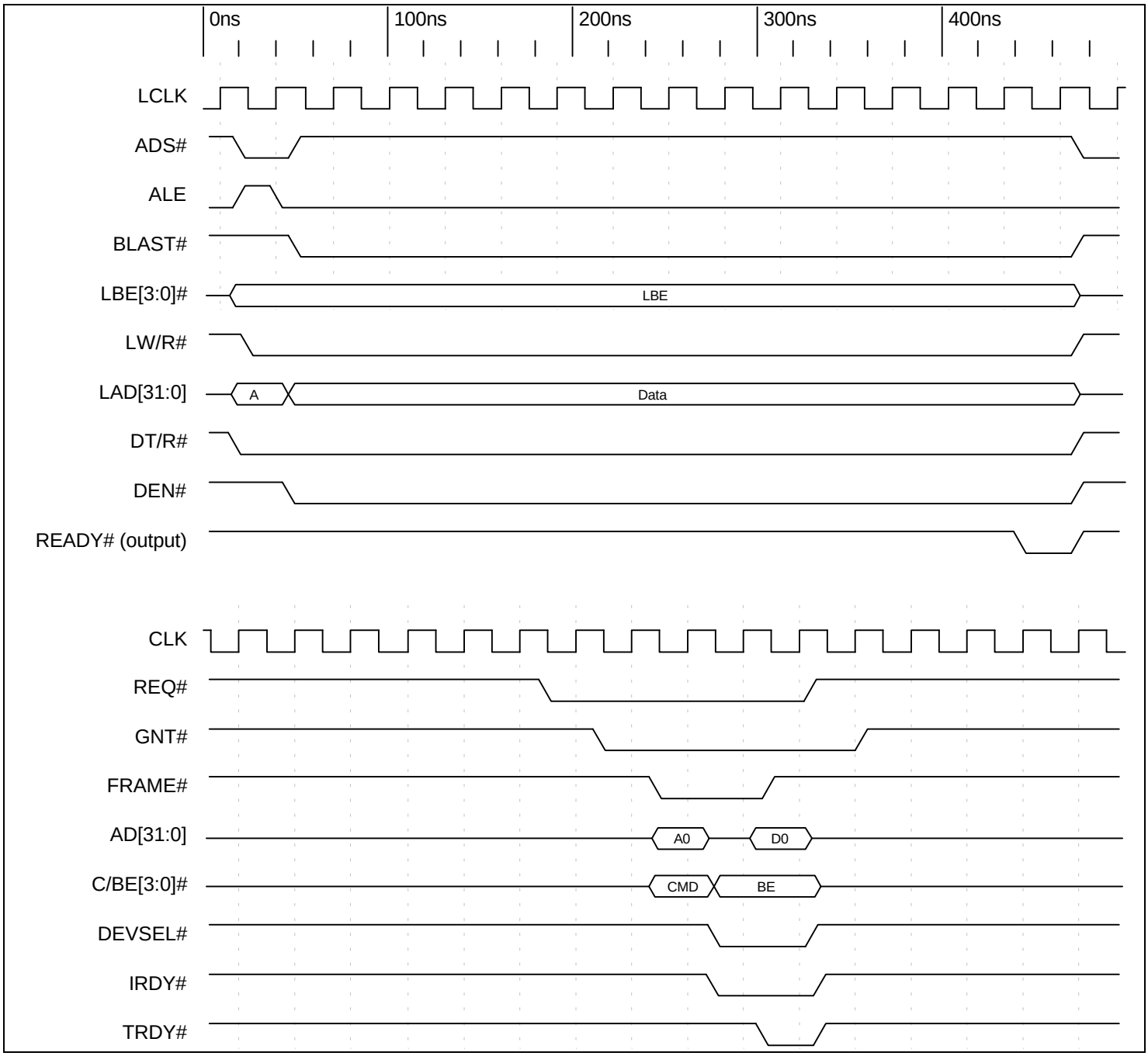
Timing Diagram 5-54. Multiple-Cycle Demand DMA Mode (PCI-to-Local)

5.7 J Mode Timing Diagrams

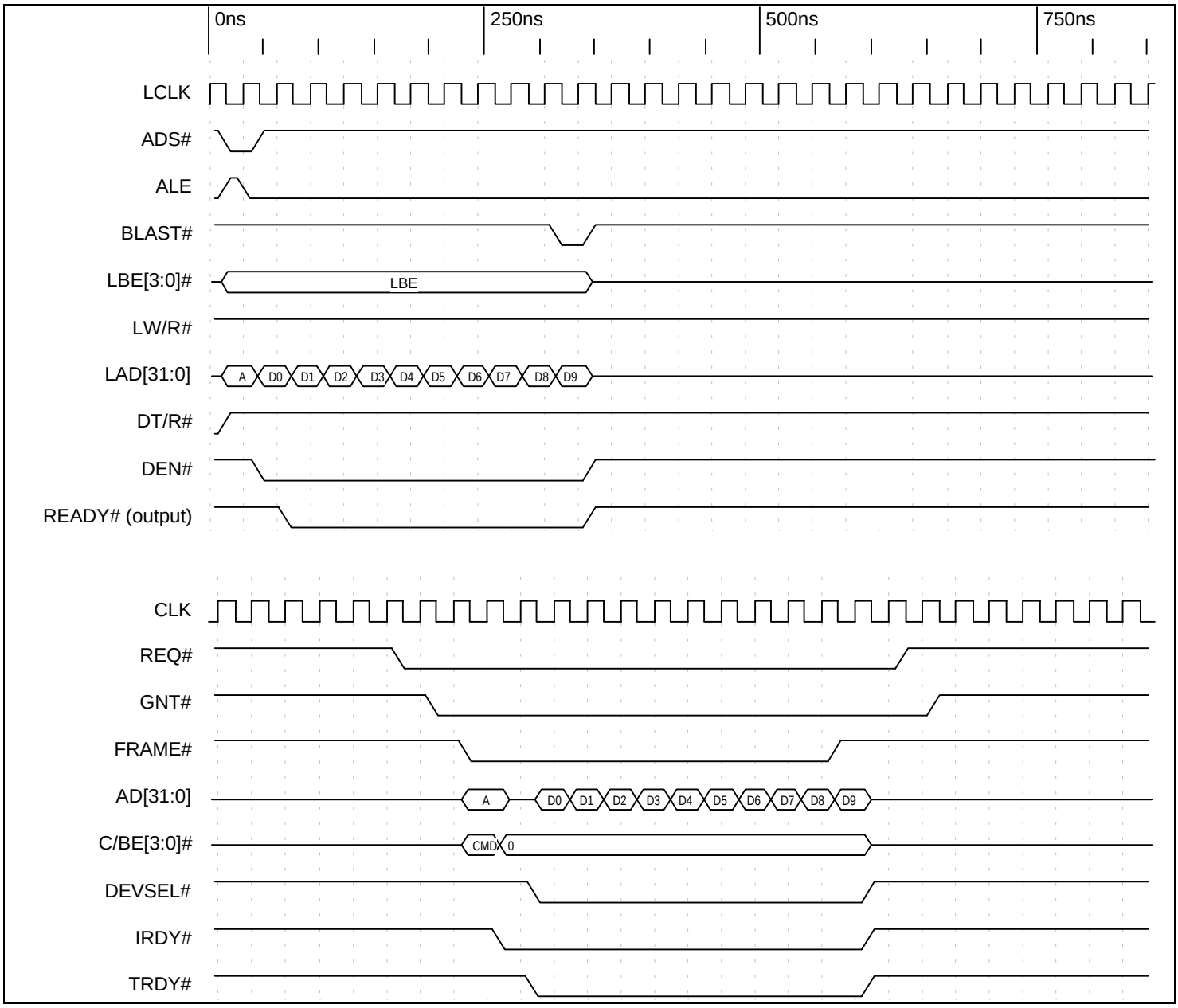
5.7.1 J Mode Direct Master



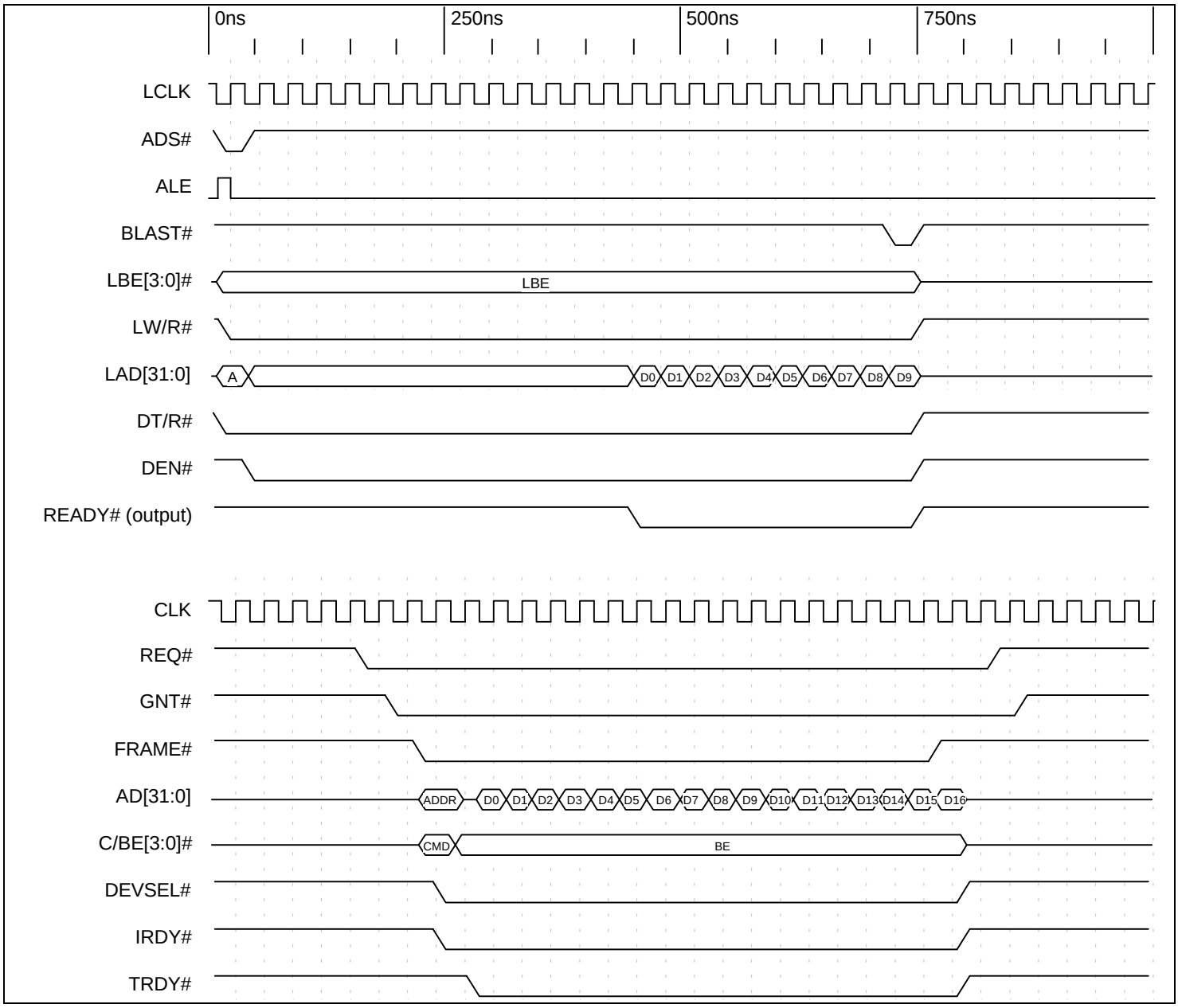
Timing Diagram 5-55. Direct Master Single Write



Timing Diagram 5-56. Direct Master Single Read

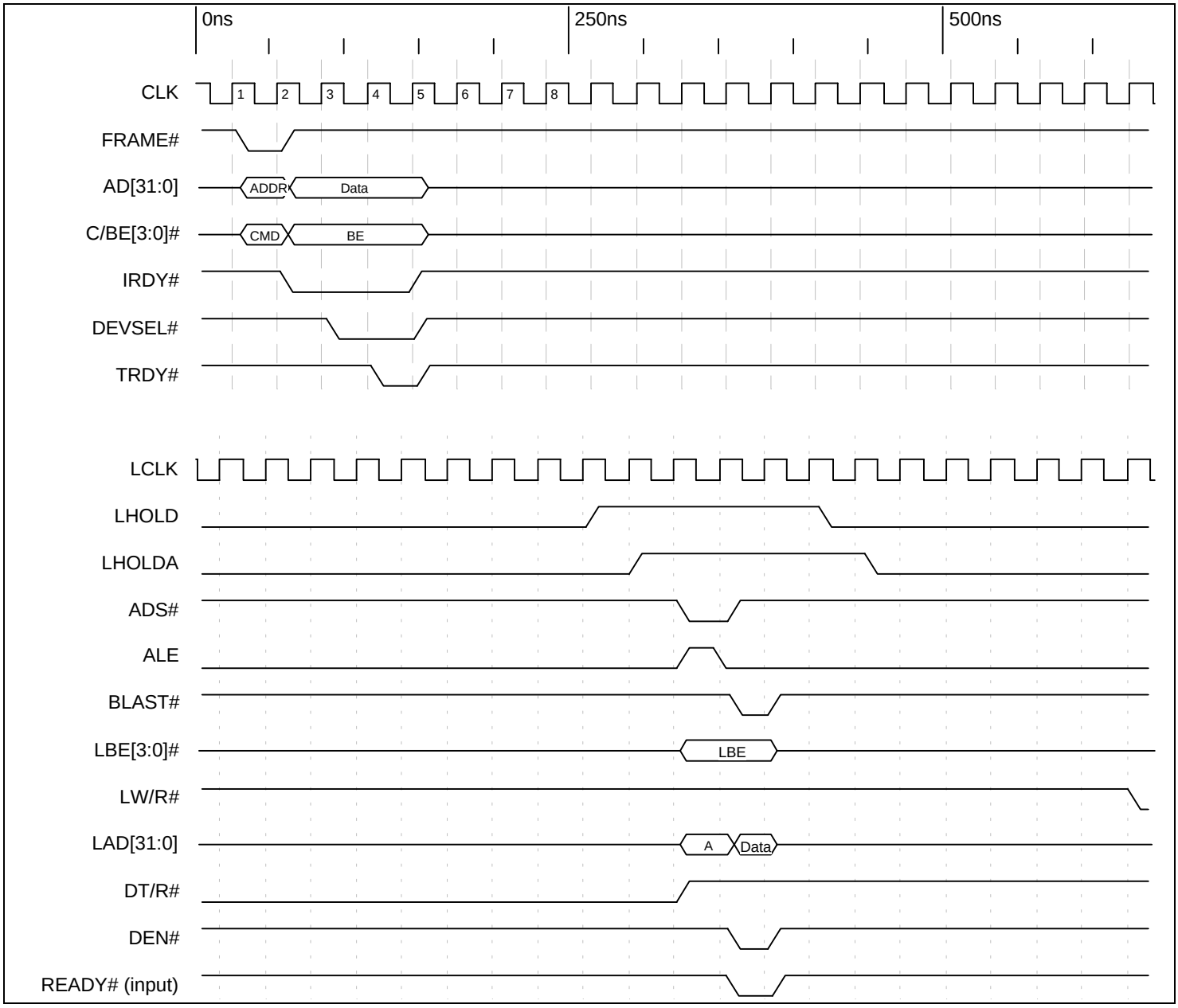


Timing Diagram 5-57. Direct Master Burst Write of 10 Lwords, Zero Wait States

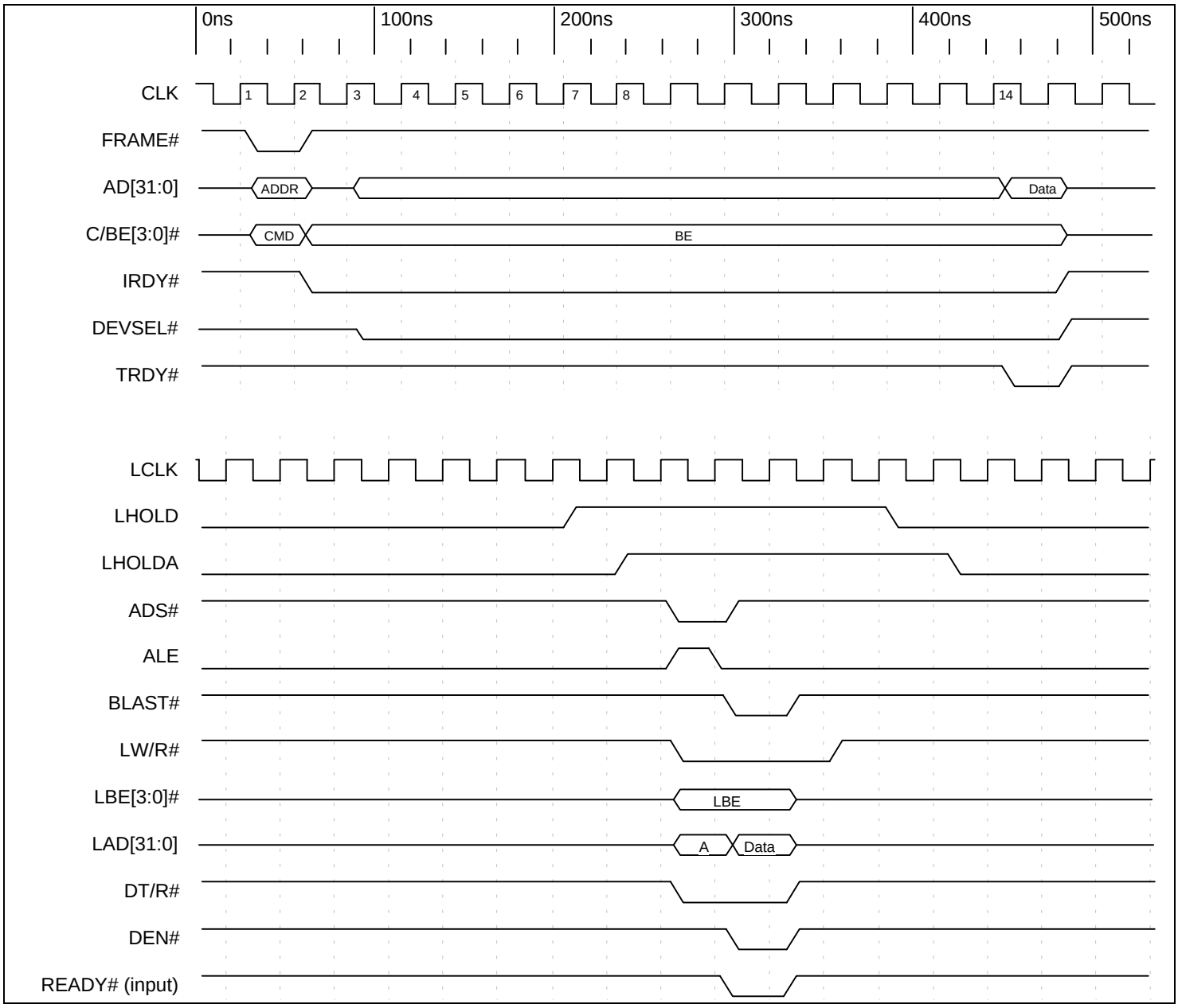


Timing Diagram 5-58. Direct Master Burst Read of 10 Lwords, Zero Wait States

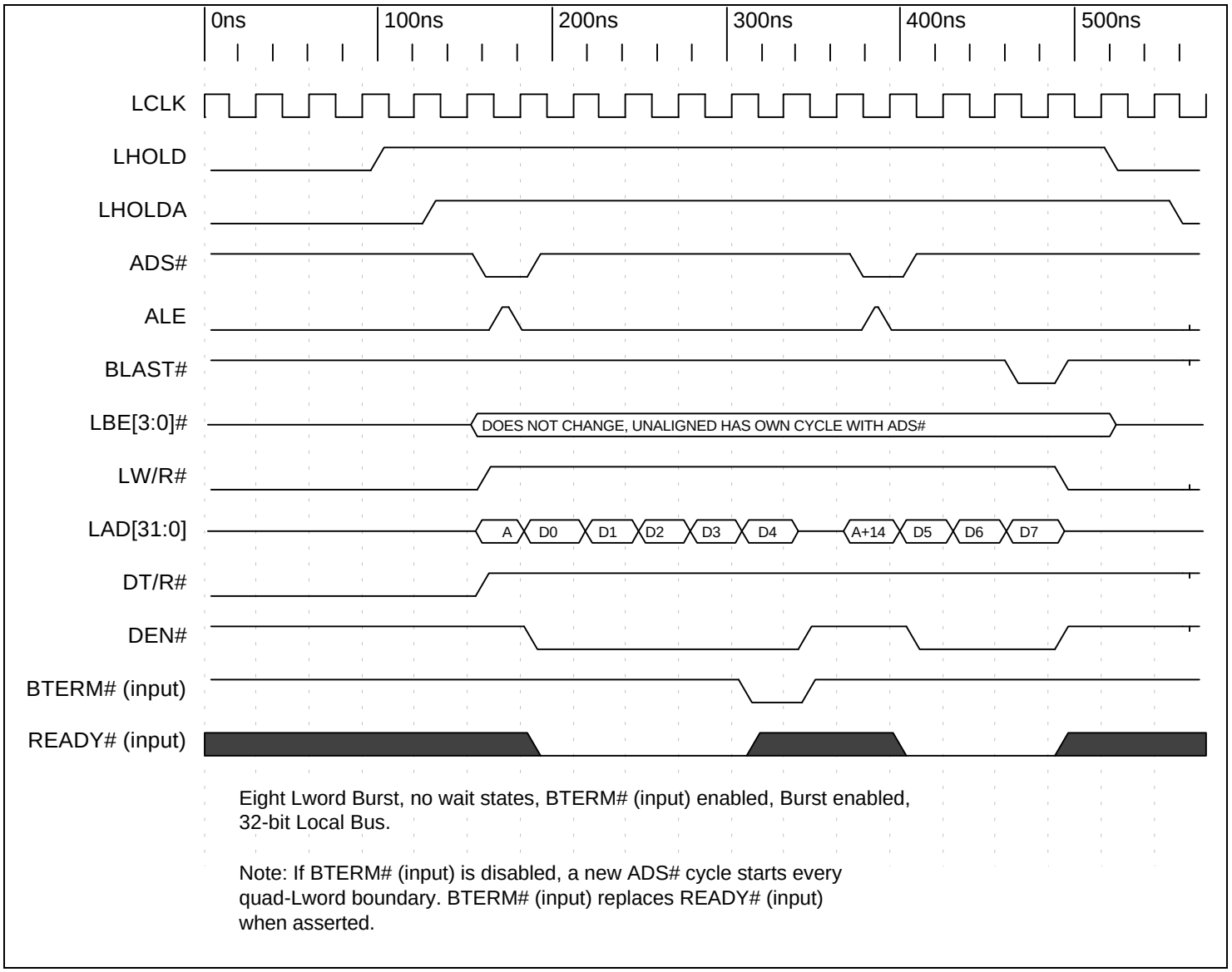
5.7.2 J Mode Direct Slave



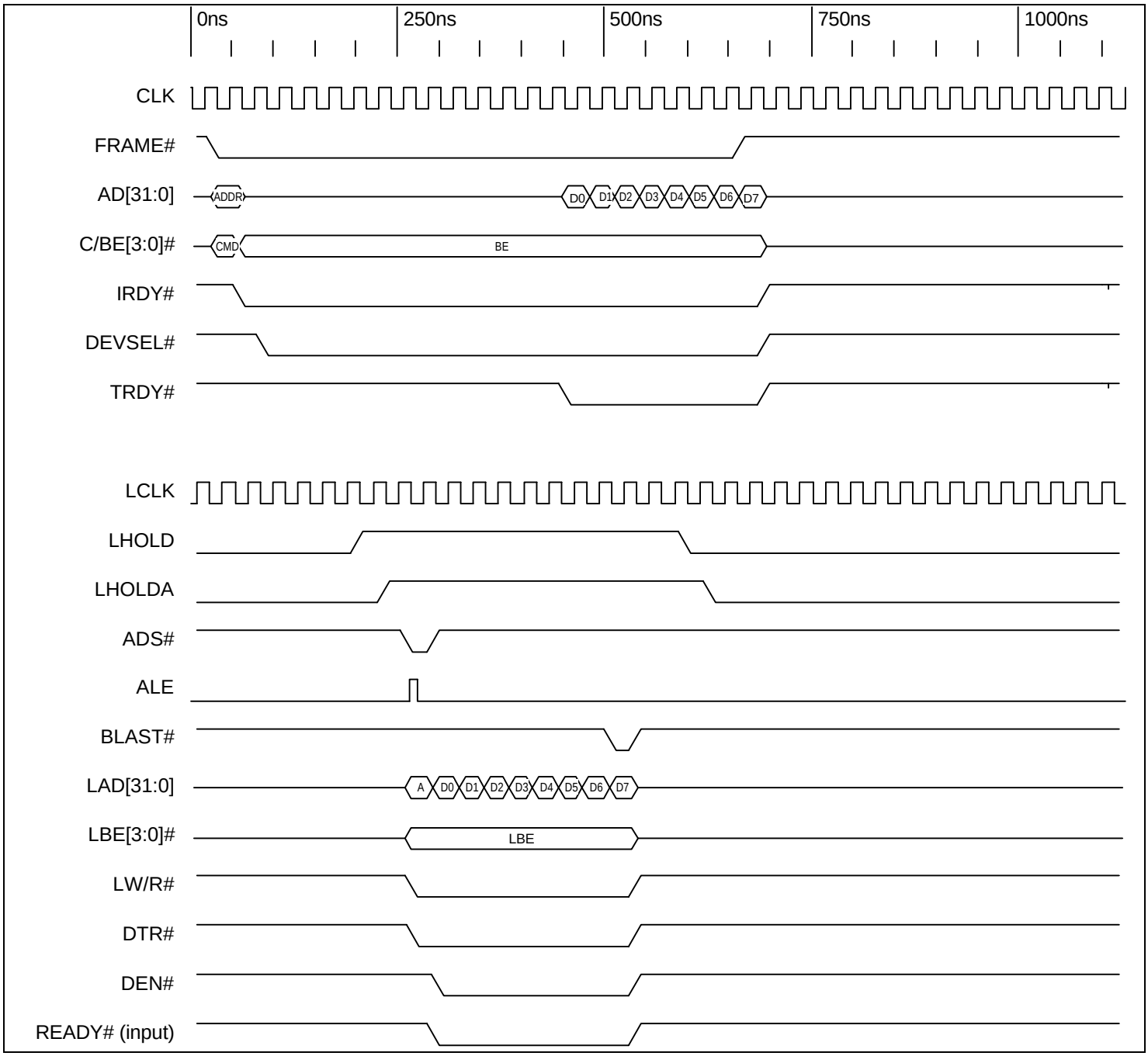
Timing Diagram 5-59. Direct Slave Single Write (32-Bit Local Bus)



Timing Diagram 5-60. Direct Slave Single Read (32-Bit Local Bus)

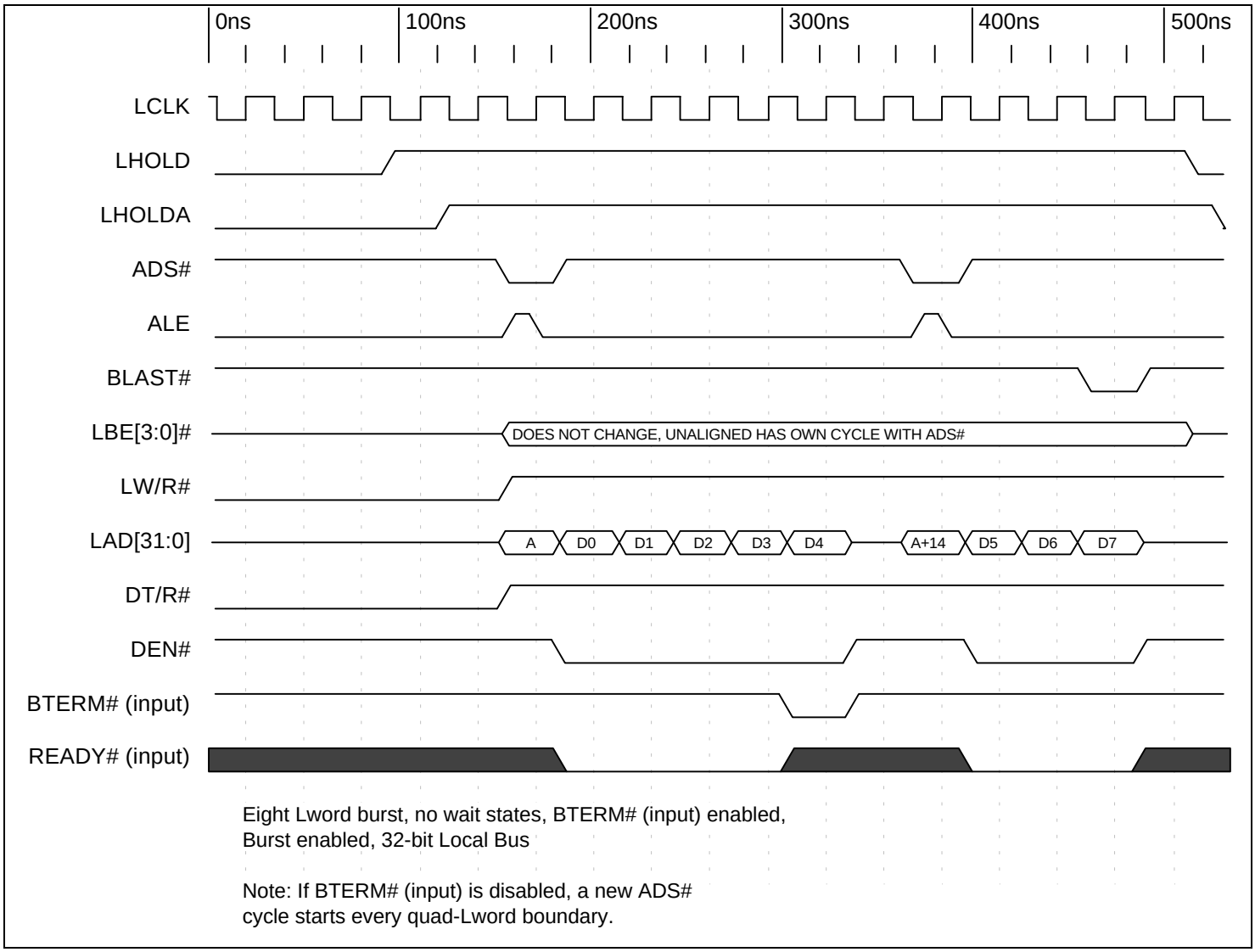


Timing Diagram 5-61. Direct Slave Burst Write with Bterm Enabled (32-Bit Local Bus)

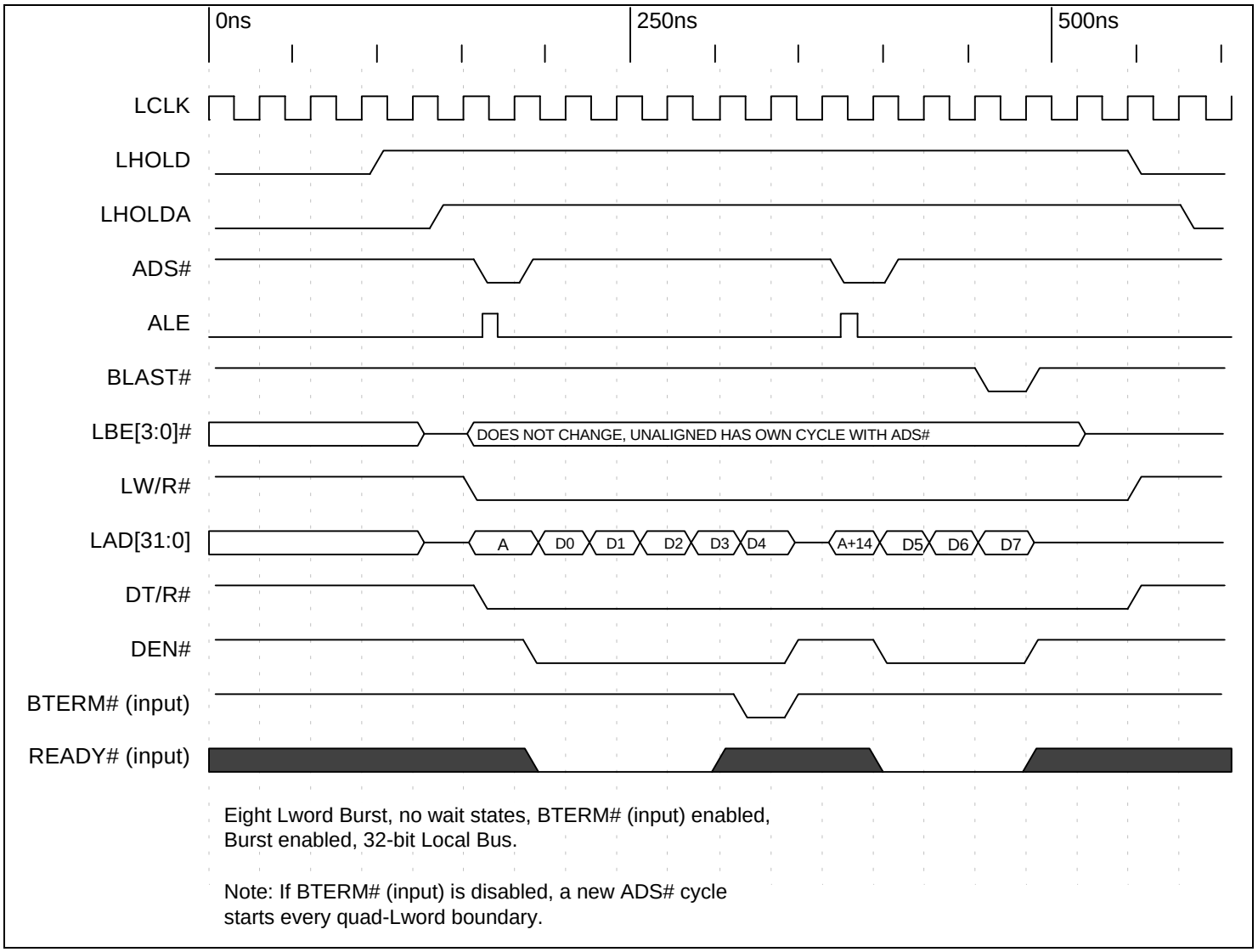


Timing Diagram 5-62. Direct Slave Burst Read with Prefetch Enabled (32-Bit Local Bus), Prefetech Counter Set to 8

5.7.3 J Mode DMA



Timing Diagram 5-63. DMA Aligned PCI Address to Aligned Local Address, Bterm Enabled, Burst Enabled



Timing Diagram 5-64. DMA Aligned Local Address to Aligned PCI Address, Bterm Enabled, Burst Enabled

6. PCI LOCAL INTERRUPTS AND USER I/O

6.1 Doorbell Registers

The PCI 9054 has two 32-bit Doorbell Interrupt/Status registers. One is assigned to the PCI Bus interface. The other is assigned to the Local Bus interface.

A Local processor can assert a PCI Bus interrupt by writing any number other than all zeroes to the PCI-to-Local Doorbell register bits (P2LDBELL[31:0]).

A PCI Host can assert a Local Bus interrupt by writing any number other than all zeroes to the Local-to-PCI Doorbell register bits (L2PDBELL[31:0]). The PCI Interrupt and Local Interrupt remain asserted until all bits are cleared to zero.

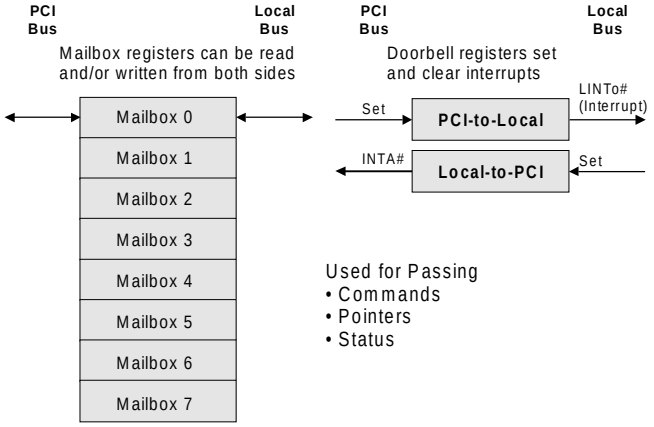


Figure 6-1. Mailbox and Doorbell Message Passing

6.2 Mailbox Registers

The PCI 9054 has eight 32-bit Mailbox registers that can be written to and read from both the PCI and Local buses. These registers can be used to pass command and status information directly between the PCI Bus and Local Bus devices.

A Local interrupt can be asserted, if enabled (INTCSR[3] and INTCSR[16]), when the PCI Host writes to one of the first four Mailbox registers (MBOX0, MBOX1, MBOX2, or MBOX3).

6.3 Interrupts

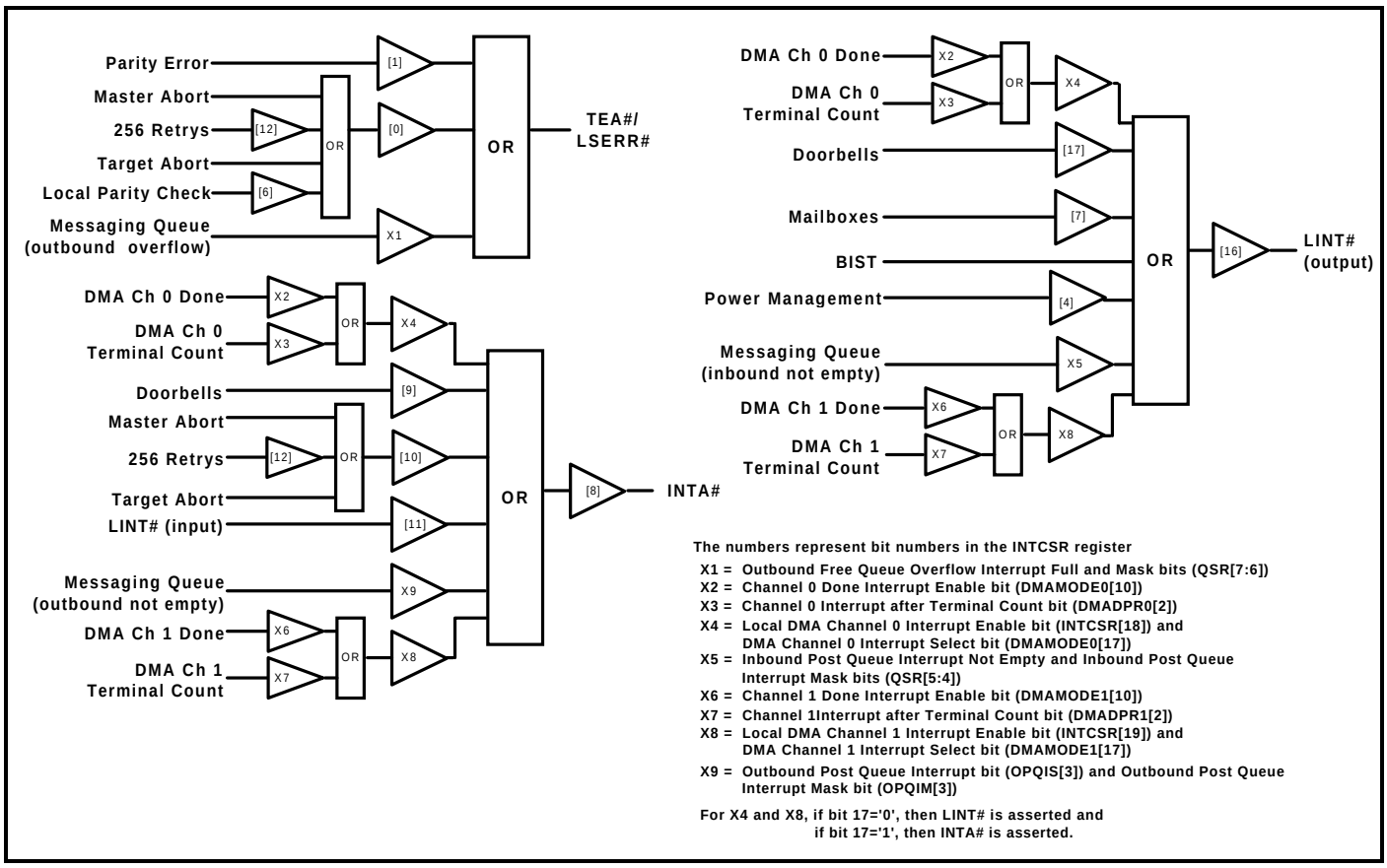


Figure 6-2. Interrupt and Error Sources

6.3.1 PCI Interrupts (INTA#)

A PCI 9054 PCI Interrupt (INTA#) can be asserted by one of the following:

- Local-to-PCI Doorbell register
- Local Interrupt input
- Master/Target Abort Status condition
- DMA Ch 0/Ch 1 Done
- DMA Ch 0/Ch 1 Terminal Count is reached
- Messaging Outbound Post Queue not empty
- 256 consecutive PCI Retrys

INTA#, or individual sources of an interrupt, can be enabled or disabled with the PCI 9054 Interrupt Control/Status register (INTCSR). This register also provides the interrupt status of each interrupt source.

The PCI 9054 PCI Bus interrupt is a level output. Disabling an interrupt enable bit or clearing the cause(s) of the interrupt can clear an interrupt.

6.3.1.1 Local Interrupt Input (LINT#)

Asserting the Local Bus input LINT# can assert a PCI Bus interrupt. The PCI Host processor can read the PCI 9054 Interrupt Control/Status register (INTCSR) to determine whether an interrupt is pending as a result of LINT# being asserted (INTCSR[15]).

The interrupt remains asserted as long as LINT# input is asserted and the Local Interrupt input is enabled. The PCI Host processor can take adapter-specific action to cause the Local Bus to release LINT#.

If the PCI Interrupt Enable bit is cleared (INTCSR[8]=0), the PCI interrupt (INTA#) is de-asserted; however, the Local interrupts (LINT#) and the status bit remain active.

6.3.1.2 Local Interrupt Output (LINT#)

The PCI 9054 Local Interrupt (LINT#) output can be asserted by one of the following:

- PCI-to-Local Doorbell/Mailbox register access
- PCI BIST interrupt
- DMA Ch 0/Ch 1 Done interrupt
- DMA Ch 0/Ch 1 Terminal Count is reached
- DMA Abort Interrupt or Messaging Outbound Post Queue is not empty

LINT#, or individual sources of an interrupt, can be enabled or disabled with the PCI 9054 Interrupt Control/Status register (INTCSR). This register also provides interrupt status for each interrupt source.

The PCI 9054 Local interrupt is a level output. Interrupts can be cleared by disabling the Interrupt Enable bit of a source or by clearing the cause of an interrupt.

The Local Interrupt Input Enable bit must be disabled (INTCSR[11]=0) when LINT# output is active; otherwise, the PCI interrupt becomes active. This could result in an unwanted PCI interrupt.

6.3.1.3 Master/Target Abort Interrupt

The PCI 9054 sets the Received Master Abort or Target Abort bit (PCISR[13, 11]=1, respectively) when it detects a Master or Target Abort. These status bits cause the PCI INTA# to be asserted if interrupts are enabled.

Interrupt remains set as long as the Receive Master Abort or Target Abort bits remain set and the Master/Target Abort interrupt is enabled. Use PCI Type 0 Configuration or Local accesses to clear the Received Master Abort and Target Abort interrupt bits (PCISR[13, 11]=0, respectively).

The Interrupt Control/Status Register bit(s) (INTCSR[26:24]) are latched at the time of a Master or Target Abort interrupt. These bits provide information such as which device was the Master when an abort occurred. The PCI 9054 updates these bits only when an abort occurs.

6.3.1.4 Local-to-PCI Doorbell Interrupt

A Local Bus Master can assert a PCI Bus interrupt by writing to the Local-to-PCI Doorbell Register bit(s) (L2PDBELL[31:0]). The PCI Host processor can read the PCI Doorbell Interrupt Active bit to determine whether a PCI Doorbell interrupt is pending (INTCSR[13]), and if so, read the PCI 9054 Local-to-PCI Doorbell register.

Each bit in the Local-to-PCI Doorbell register is individually controlled. The Local Bus can only set bits in the Local-to-PCI Doorbell register. From Local Bus, writing 1 to any bit position sets that bit and writing 0 has no effect. Bits in the Local-to-PCI Doorbell register can only be cleared from the PCI Bus. From the PCI Bus, writing 1 to any bit position clears that bit and writing 0 has no effect.

Interrupts remain set as long as any Local-to-PCI Doorbell register bits are set and the PCI Doorbell Interrupt Enable bit (INTCSR[9]) is set.

6.3.1.4.1 M Mode Local-to-PCI Doorbell Interrupt

To prevent race conditions when the PCI Bus is accessing the Local-to-PCI Doorbell register (or any Configuration register), the PCI 9054 automatically de-asserts TA# output to prevent Local Bus configuration accesses.

6.3.1.4.2 C and J Modes Local-to-PCI Doorbell Interrupt

To prevent race conditions when the PCI Bus is accessing the Local-to-PCI Doorbell register (or any Configuration register), the PCI 9054 automatically de-asserts READY# output to prevent Local Bus configuration accesses.

6.3.1.5 PCI-to-Local Doorbell Interrupt

A PCI Bus Master can assert a Local Bus interrupt by writing to the PCI-to-Local Doorbell Register bit(s) (P2LDBELL[31:0]). The Local processor can read the Local Doorbell Interrupt Active bit to determine whether a Local doorbell interrupt is pending (P2LDBELL[20]), and if so, read the PCI 9054 PCI-to-Local Doorbell register.

Each bit in the PCI-to-Local Doorbell register is individually controlled. The PCI Bus only sets bits in the PCI-to-Local Doorbell register. From the PCI Bus, writing 1 to any bit position sets that bit and writing 0 to a bit position has no effect. Bits in the PCI-to-Local Doorbell register can only be cleared from the Local Bus. From the Local Bus, writing 1 to any bit position clears that bit and writing 0 has no effect.

Note: *If the Local Bus cannot clear a Doorbell Interrupt, do not use the PCI-to-Local Doorbell register.*

Interrupts remain set as long as any PCI-to-Local Doorbell register bits are set and the Local Doorbell Interrupt Enable bit is set (INTCSR[17]=1).

To prevent race conditions when the Local Bus is accessing the PCI-to-Local Doorbell register (or any Configuration register), the PCI 9054 automatically issues a Retry to the PCI Bus.

6.3.1.6 Built-In Self Test Interrupt (BIST)

A PCI Bus Master can assert a Local Bus interrupt by performing a PCI Type 0 Configuration write to a bit in the PCI BIST register. A Local processor can read the BIST Interrupt Active bit (INTCSR[23]) to determine whether a BIST interrupt is pending.

Interrupts remain set as long as the bit is set and the PCI BIST Interrupt Enable bit is set (PCIBISTR[6]=1). The Local Bus then resets the bit when BIST completes. The PCI Host software may fail the device if the bit is not reset after two seconds.

Note: *The PCI 9054 does not have an internal BIST.*

6.3.1.7 DMA Channel 0/1 Interrupts

A DMA channel can assert a PCI Bus or Local Bus interrupt when done (transfer complete) or after a transfer is complete for the current descriptor in Scatter/Gather DMA mode. The DMA Channel Interrupt Select bit(s) determine whether to assert a PCI (DMAMODE0[17]=1 and/or DMAMODE1[17]=1) or Local (DMAMODE0[17]=0 and/or DMAMODE1[17]=0) interrupt. The Local or PCI processor can read the DMA Channel 0 Interrupt Active bits to determine whether a DMA Channel 0 (INTCSR[21]) or DMA Channel 1 (INTCSR[22]) interrupt is pending.

The Channel Done bit(s) (DMACSR0[4] and/or DMACSR1[4]) can be used to determine whether an interrupt is:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt

The Done Interrupt Enable bit(s) (DMAMODE0[10] and/or DMAMODE1[10]) enable a Done interrupt. In Scatter/Gather DMA mode, a bit in the Next Descriptor Pointer register of the channel (loaded from Local memory) specifies whether to assert an interrupt at the end of the transfer for the current descriptor.

A DMA Channel interrupt is cleared by the Channel Clear Interrupt bit(s) (DMACSR0[3]=1 and/or DMACSR1[3]=1).

6.3.2 All Modes PCI SERR# (PCI NMI)

The PCI 9054 asserts an SERR# pulse if parity checking is enabled (PCICR[6]=1) and it detects an address or 1 is written to the Generate PCI Bus SERR# Interrupt bit (INTCSR[2]) with a current value of 0.

SERR# output can be enabled or disabled with the SERR# Enable bit (PCICR[8]).

6.3.2.1 M Mode PCI SERR#

The PCI 9054 also asserts SERR# if the Local Bus responds with TEA# to the PCI 9054. The TEA# Input Interrupt Mask bit (LMISC[5]) masks out the SERR# interrupt assertion process.

6.3.3 Local NMI

If the Parity Error Response bit is set (PCICR[6]=1), the PCI 9054 sets the Master Data Parity Error Detected bit (PCISR[8]=1) when the following three conditions are met:

- The PCI 9054 asserted PERR# or acknowledged PERR# was asserted
- The PCI 9054 was the Bus Master for the operation in which the error occurred
- The Parity Error Response bit is set (PCICR[6]=1)

The PCI 9054 sets the Detected Parity Error bit (PCISR[15]=1) if it detects one of the following conditions:

- The PCI 9054 detected a parity error during a PCI Address phase
- The PCI 9054 detected a data parity error when it was the Target of a write
- The PCI 9054 detected a data parity error when performing Master Read operation

6.3.3.1 M Mode Local TEA# (Local NMI)

A TEA# interrupt is asserted if the following occurs:

- PCI Bus Target Abort bit is set (PCISR[11]=1) or Received Master Abort bit is set (PCISR[13]=1)
- Detected Parity Error bit is set (PCISR[15]=1)
- Direct Master Local Data Parity Check Error Status bit is set (INTCSR[7]=1)
- Messaging Outbound Free queue overflows

The Enable Local Bus TEA# bit (INTCSR[0]) can be used to enable or disable TEA# for an abort or parity error. TEA# is a level output that remains asserted as long as the Abort or Parity Error Status bits are set.

6.3.3.2 C and J Modes Local LSERR# (Local NMI)

An LSERR# interrupt is asserted if the following conditions occur:

- PCI Bus Target Abort bit is set (PCISR[11]=1) or Received Master Abort bit is set (PCISR[13]=1)
- Detected Parity Error bit is set (PCISR[15]=1)
- Direct Master Local Data Parity Check Error Status bit is set (INTCSR[7]=1)
- Messaging Outbound Free queue overflows

The Enable Local Bus LSERR# bit (INTCSR[0]) can be used to enable or disable LSERR# for an abort or parity error. LSERR# is a level output that remains asserted as long as the Abort or Parity Error Status bits are set.

6.4 User Input and Output

The PCI 9054 supports user input and output pins, USERi and USERo (PQFP—pins 159-158; PBGA—pins C7 and A7), respectively. Both are multiplexed with other functional pins. The PCI 9054-default condition is USERi and USERo functions. USERi is selected when CNTRL[18]=1. USERo is selected when CNTRL[19]=1. User output data can be logged by writing to the General Purpose Output bit (CNTRL[16]). User input data can be read from the General Purpose Input bit (CNTRL[17]).

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7. INTELLIGENT I/O (I_2O)

7.1 I_2O-Compatible Message Unit

The I_2O-compatible Messaging Unit supplies two paths for messages, two inbound FIFOs to receive messages from the primary PCI Bus, and two outbound FIFOs to pass messages to the primary PCI Bus. Refer to *I_2O Architecture Specification v1.5* for details.

Figure 7-1 and Figure 7-2 illustrate information about I_2O architecture.

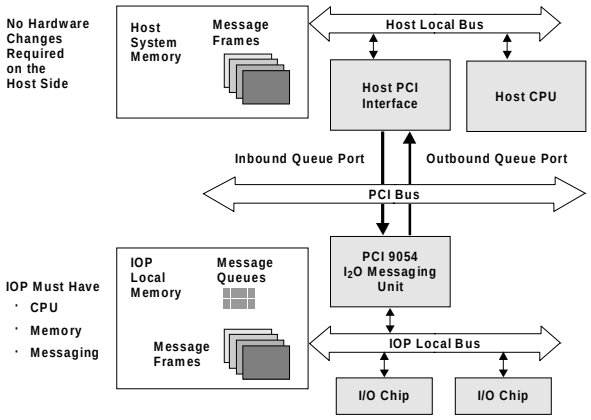

Figure 7-1. Typical I_2O Server/Adapter Card Design

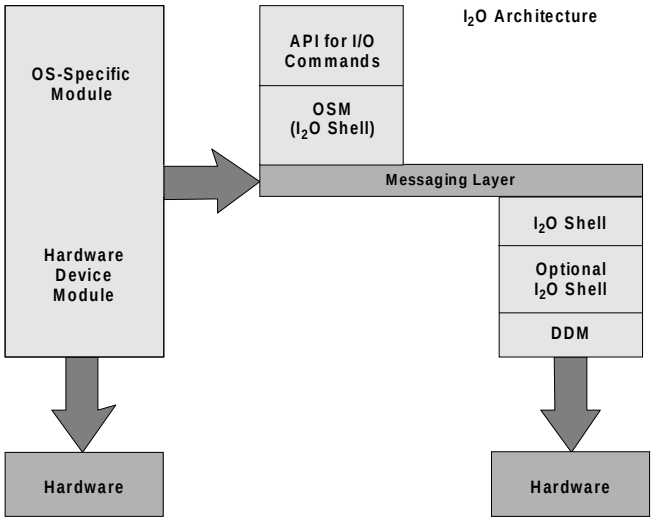

Figure 7-2. Driver Architecture Compared

7.1.1 Inbound Messages

Inbound messages reside in a pool of message frames (minimum 64-byte frames) allocated in the shared Local Bus (IOP) memory. The inbound message queue is comprised of a pair of rotating FIFOs implemented in Local memory. The Inbound Free List FIFO holds the message frame addresses (MFA) of available message frames in Local memory. The Inbound Post Queue FIFO holds the MFA of all currently posted messages.

Inbound circular FIFOs are accessed by external PCI agents, through the Inbound Queue Port location in PCI Address space. The Inbound Queue Port, when read by an external PCI agent, returns the Inbound Free List FIFO MFA. The external PCI agent places a message frame into the Inbound Post Queue FIFO by writing its MFA to the Inbound Queue Port location.

7.1.2 Outbound Messages

Outbound messages reside in a pool of message frames (minimum 64-byte frames) allocated in the shared PCI Bus (Host System) memory. The Outbound message queue is comprised of a pair of rotating FIFOs implemented in Local memory. The Outbound Free List FIFO holds the message frame addresses (MFA) of available message frames in system memory. The Outbound Post Queue FIFO holds the MFA of all currently posted messages.

Outbound circular FIFOs are accessed by external PCI agents, through the Outbound Queue Port location in PCI Address space. The Outbound Queue Port, when read by an external PCI agent, returns the Outbound Post Queue FIFO MFA. The External PCI agent places free message frames into the Outbound Free List FIFO by writing the free MFA into the Outbound Queue Port location.

Memory for the circular FIFOs themselves must be allocated in Local (IOP) memory. The base address of the queue is contained in the Queue Base Address bits (QBAR[31:20]). Each FIFO entry is a 32-bit data value. Each read and write of the queue must be a single 32-bit access.

Circular FIFOs range in size from 4-kilobit to 64-kilobit entries. All four FIFOs must be the same size and contiguous. Therefore, the total amount of Local memory needed for circular FIFOs ranges from 64 kilobits to 1 MB. A FIFO size is specified in the Circular Queue Size bits (MQCR[5:1]).

The starting address of each FIFO is based on the Queue Base Address and the FIFO Size, as listed in Table 7-1.

Table 7-1. Queue Starting Address

FIFO	Starting Address
Inbound Free List	QBAR
Inbound Post List	QBAR + (1 * FIFO Size)
Outbound Post List	QBAR + (2 * FIFO Size)
Outbound Free List	QBAR + (3 * FIFO Size)

7.1.3 I_2O Pointer Management

The FIFOs always reside in shared Local (IOP) memory and are allocated and initialized by the IOP. Before setting the Queue Enable bit (MQCR[0]=1), the Local processor must initialize the following registers, with the initial offset according to the configured FIFO size:

- Inbound Post and Free Head Pointer registers (IPHPR)
- Inbound Post and Free Tail Pointer registers (IPTPR)
- Outbound Post and Free Head Pointer registers (OFHPR)
- Outbound Post and Free Tail Pointer registers (OFTPR)

The Messaging Unit automatically adds the Queue Base Address to offset in each head and tail pointer register. The software can then enable I_2O. After initialization, the Local software should not write to the pointers managed by the MU hardware.

Empty flags are set if the queues are disabled (MQCR[0]=0) or head and tail pointers are equal. This occurs independent of how the head and tail pointers are set.

An empty flag is cleared, signifying not empty, only if the queues are enabled and pointers become not equal.

If an empty flag is cleared and the queues are enabled, the empty flag is set only if the tail pointer is incremented and the head and tail pointers become equal.

Full flags are always cleared when the queues are disabled or the head and tail pointers are not equal.

A full flag is set when the queues are enabled, the head pointer is incremented, and the head and tail pointers become equal.

Each circular FIFO has a head pointer and a tail pointer, which are offsets from the Queue Base Address. Writes to a FIFO occur at the head of the FIFO and reads occur from the tail. Head and tail pointers are incremented by either the Local processor or the MU hardware. The unit that writes to the FIFO also maintains the pointer. Pointers are incremented after a FIFO access. Both pointers wrap around to the first address of the circular FIFO when they reach the FIFO size, so that the head and tail pointers continuously "chase" each other around in the circular FIFO. The MU wraps the pointers automatically for the pointers that it maintains. IOP software must wrap the pointers that it maintains. Whenever they are equal, the FIFO is empty. To prevent overflow conditions, I_2O specifies that the number of message frames allocated should be less than or equal to the number of entries in a FIFO. (Refer to Figure 7-3.)

Each inbound MFA is specified by I_2O as the offset from the start of shared Local (IOP) memory region 0 to the start of the message frame. Each outbound MFA is specified as the offset from Host memory location 0x00000000h to the start of the message frame in shared Host memory. Because the MFA is an actual address, the message frames need not be contiguous. IOP allocates and initializes inbound message frames in shared IOP memory using any suitable memory allocation technique. Host allocates and initializes outbound message frames in shared Host memory using any suitable memory allocation technique. Message frames are a minimum of 64 bytes in length.

I_2O uses a "push" (write preferred) memory model. That means the IOP writes messages and data to the shared Host memory, and the Host writes messages and data to shared IOP memory. Software should make use of Burst and DMA transfers whenever possible to ensure efficient use of the PCI Bus for message passing.

Additional information on message passing implementation may be found in *I_2O Architecture Specification v1.5*.

7.1.4 Inbound Free List FIFO

The Local processor allocates inbound message frames in its shared memory and can place the address of a free (available) message frame into the Inbound Free List FIFO by writing its MFA into the FIFO location pointed to by the Queue Base register + Inbound Free Head Pointer register. The Local processor must then increment the Inbound Free Head Pointer register.

A PCI Master (Host or another IOP) can obtain the MFA of a free message frame by reading the Inbound Queue Port Address (40h of the first PCI Memory Base Address register). If the FIFO is empty (no free inbound message frames are currently available, head and tail pointers are equal), the MU returns -1 (FFFFFFFFh). If the FIFO is not empty (head and tail pointers are not equal), the MU reads the MFA pointed to by the Queue Base register + Inbound Free Tail Pointer register, returns its value and increments the Inbound Free Tail Pointer register. If the Inbound Free Queue is not empty, and the Inbound Free Queue Prefetch Enable bit is set (QSR[3]=1), the next

entry in the FIFO is read from the Local Bus into a prefetch register. The prefetch register then provides the data for the next PCI read from this queue, thus reducing the number of PCI wait states. (Refer to Figure 7-3.)

7.1.5 Inbound Post Queue FIFO

A PCI Master (Host or another IOP) can write a message into an available message frame in the shared Local (IOP) memory. It can then post that message by writing the Message Frame Address (MFA) to the Inbound Queue Port Address, IQP (40h of the first PCI Memory Base Address register). When the port is written, the MU writes the MFA to the Inbound Post Queue FIFO location pointed to by the Queue Base register + FIFO Size + Inbound Post Head Pointer register. After the MU writes the MFA to the Inbound Post Queue FIFO, it increments the Inbound Post Head Pointer register.

The Inbound Post Tail Pointer register points to the Inbound Post Queue FIFO location, which holds the MFA of the oldest posted message. The Local processor maintains the tail pointer. After a Local processor reads the oldest MFA, it can remove the MFA from the Inbound Post Queue FIFO by incrementing the Inbound Post Tail Pointer register.

The PCI 9054 asserts a Local Interrupt when the Inbound Post Queue FIFO is not empty. The Inbound Post Queue FIFO Interrupt bit in the Queue Status/Control register (QSR[5]) indicates the interrupt status. The interrupt clears when the Inbound Post Queue FIFO is empty. The interrupt can be masked by the Inbound Post Queue FIFO Interrupt Mask bit (QSR[4]).

To prevent racing between the time the PCI Write transaction is received until the data is written in Local memory and the Inbound Post Head Pointer register is incremented, any PCI Direct Slave access to the PCI 9054 is issued a Retry.

7.1.6 Outbound Post Queue FIFO

A Local Master (IOP) can write a message into an available message frame in shared Host memory. It can then post that message by writing the Message Frame Address (MFA) to the Outbound Post Queue FIFO location pointed to by the Queue Base register + Outbound Post Head Pointer register + (2 * FIFO Size). The Local processor should then increment the Outbound Post Head Pointer register.

A PCI Master can obtain the MFA of the oldest posted message by reading the Outbound Queue Port Address (44h of the first PCI Memory Base Address register). If the FIFO is empty (no more outbound messages are posted, head and tail pointers are equal), the MU returns -1 (FFFFFFFFh). If the Outbound Post Queue FIFO is not empty (head and tail pointers are not equal), the MU reads the MFA pointed to by the Queue Base register + (2 * FIFO Size) + outbound Post Tail Pointer register, returns its value and increments the Outbound Post Tail Pointer register.

The PCI 9054 asserts a PCI Interrupt when the Outbound Post Head Pointer register is not equal to the Outbound Post Tail Pointer register. The Outbound Post Queue FIFO Interrupt bit of the Outbound Post Queue Interrupt Status register (OPQIS) indicates the interrupt status. When the pointers become equal, both the interrupt and the Outbound Post Queue FIFO interrupt bit are automatically cleared. Pointers become equal when a PCI Master (Host or another IOP) reads sufficient FIFO entries to empty the FIFO. The Outbound Post Queue FIFO Interrupt Mask register (OPLFIM) can mask the Interrupt.

7.1.7 Outbound Post Queue

To reduce read latency, prefetching from the tail of the queue occurs whenever the queue is not empty and the tail pointer is incremented (queue has been read from), or when the queue is empty and the head pointer is incremented (queue has been written to). When the Host CPU reads the Outbound Post Queue, the data is immediately available.

7.1.8 Inbound Free Queue

To reduce read latency, prefetching from the tail of the queue occurs whenever the queue is not empty and the tail pointer is incremented (queue has been read from), or when the queue is empty and the head pointer is incremented (queue has been written to). When the Host CPU reads the Inbound Free Queue, the data is immediately available.

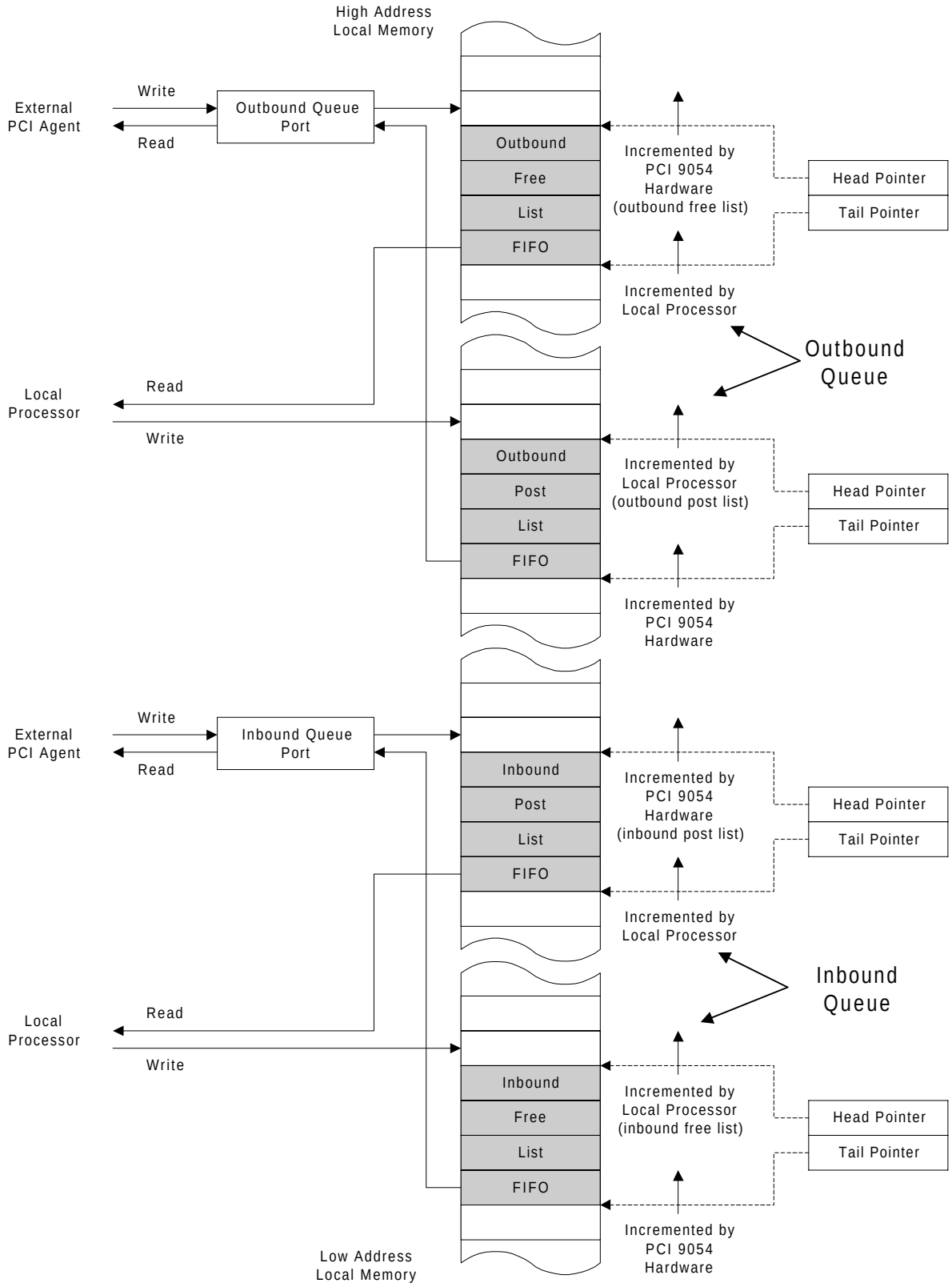

Figure 7-3. Circular FIFO Operation

7.1.9 Outbound Free List FIFO

The PCI Bus Master (Host or other IOP) allocates outbound message frames in its shared memory. The PCI Bus Master can place the address of a free (available) message frame into the Outbound Free List FIFO by writing a Message Frame Address (MFA) to the Outbound Queue Port Address (44h of the first PCI Memory Base Address register). When the port is written, the MU writes the MFA to the Outbound Free List FIFO location pointed to by the Queue Base register + (3 * FIFO Size) + Outbound Free Head Pointer register. After the MU writes the MFA to the Outbound Free List FIFO, it increments the Outbound Free Head Pointer register.

When the IOP needs a free outbound message frame, it must first check whether any free frames are available. If the Outbound Free List FIFO is empty (outbound free head and tail pointers are equal), the IOP must wait for the Host to place additional outbound free message frames in the Outbound Free List FIFO. If the Outbound Free List FIFO is not empty (head and tail pointers are not equal), the IOP can obtain the MFA of the oldest free outbound message frame by reading the location pointed to by the Queue Base register + (3 * FIFO Size) + Outbound Free Tail Pointer register. After the IOP reads the MFA, it must increment the Outbound Free Tail Pointer register. To prevent overflow conditions, I_2O specifies the number of message frames allocated should be less than or equal to the number of entries in a FIFO. The MU also checks for overflows of the Outbound Free List FIFO. When the head pointer is incremented and becomes equal to the tail pointer, the Outbound Free List FIFO is full, and the MU asserts a Local TEA#/LSERR# (NMI) interrupt. The interrupt is recorded in the Queue Status/Control register (QSR).

From the time the PCI Write transaction is received until the data is written into Local memory and the Outbound Free Head Pointer register is incremented, any PCI Direct Slave access to the PCI 9054 is issued a Retry.

7.1.10 I_2O Enable Sequence

To enable I_2O, the Local processor should perform the following:

- Initialize Space 1 address and range
- Initialize all FIFOs and Message Frame memory
- Set the PCI Base Class Code bits (PCICCR[23:16]) to be an I_2O device with programming interface 01h
- Set the I_2O Decode Enable bit (QSR[0])
- Set Local Init Status bit to “done” LMISC[2]=1)

Note: *The serial EEPROM must not set the Local Init Status bit so that the PCI 9054 issues retries to all PCI accesses until the Local Init Status bit is set to “done” by the Local processor.*

The I_2O Decode Enable bit (QSR[0]) causes remapping of resources for use in I_2O mode. When set, all Memory-Mapped Configuration registers (*for example*, queue ports 40h and 44h) and Space 1 share the PCIBAR0 register. PCI accesses to offset 00h-FFh of PCIBAR0 result in accesses to the PCI 9054 Internal Configuration registers.

Accesses above offset FFh of PCIBAR0 result in Local Space accesses, beginning at offset 100h from the Remap PCI Address to Local Address Space 1 into the Local Address Space bit(s) (LAS1BA[31:4]). Therefore, space located at offset 00h-FFh from LAS1BA is not addressable from the PCI Bus using PCIBAR0.

Note*: Because PCI accesses to offset 00h-FFh of PCIBAR0 result in internal configuration accesses, the Inbound Free MFAs must be greater than FFh.*

Table 7-2. Circular FIFO Summary

FIFO Name	PCI Port	Generate PCI Interrupt?	Generate Local Interrupt	Head Pointer Maintained by	Tail Pointer Maintained by
Inbound Free List FIFO	Inbound Queue Port (Host read)	No	No	Local processor	MU hardware
Inbound Post List FIFO	Inbound Queue Port (Host write)	No	Yes, when Port is written	MU hardware	Local processor
Outbound Post List FIFO	Outbound Queue Port (Host read)	Yes, when FIFO is not empty	No	Local processor	MU hardware
Outbound Free List FIFO	Outbound Queue Port (Host write)	No	Yes, (TEA#/LSERR#) when FIFO is full	MU hardware	Local processor

8. PCI POWER MANAGEMENT

8.1 Overview

The PCI Bus Power Management Interface Specification provides a standard mechanism for operating systems to control add-in cards for power management. The Specification defines four PCI functional power states—D_0, D_1, D_2, and D_3. States D_0 and D_3 are required, while states D_1 and D_2 are optional. State D_0 represents the highest power consumption and state D_3 the least.

- **D_0 (Uninitialized)**—Enters this state from Power-On Reset or from state D_{3hot}. Supports Direct Slave PCI transactions only.
- **D_0 (Active)**—All functions active.
- **D_1**—Uses less power than State D_0, and more than state D_2. Light Sleep State.
- **D_2**—Uses very little power.

  The functional states are defined by the allowed activites of the add-in card with the PCI 9054.

  The function supports PCI Configuration cycles to function if clock is running (Memory, I/O, Bus Mastering, and Interrupts are disabled). It also supports the Wakeup Event from function, but not standard PCI interrupts.
- **D_{3hot}**—Uses lower power than any other state. Supports PCI Configuration cycles to function if clock is running. Supports Wakeup Event from function, but not standard PCI interrupts. When programmed for state D_0, an internal soft reset occurs. The PCI Bus drivers must be disabled. PME# context must be retained during this soft reset.
- **D_{3cold}**—No power. Supports Bus reset only. All context is lost in this state.

From a power management perspective, the PCI Bus can be characterized at any point in time by one of four power management states—B_0, B_1, B_2, and B_3:

- **B_0 (Fully On)**—Bus is fully useable with full power and clock frequency, PCI v2.1 compliant. Fully operational bus activity. This is the only Power Management state in which data transactions can occur.
- **B_1**—Intermediate power management state. Full power with clock frequency, PCI v2.1 compliant. PME Event driven bus activity. Vcc is applied to all devices on the bus, and no transactions are allowed to occur on the bus.
- **B_2**—Intermediate power management state. Full power clock frequency stopped, PCI v2.1 compliant (in the low state). PME Event-driven bus activity. Vcc is applied to all devices on the bus; however, the clock is stopped and held in the Low state.
- **B_3 (Off)**—Power to the bus is switched off. PME Event-driven bus activity.Vcc is removed from all devices on the PCI Bus.

All system PCI Buses have an originating device, which can support one or more power states. In most cases, this creates a bridge (such as a Host-Bus-to-PCI-Bus or a PCI-to-PCI bridge).

Function States must be at the same or lower energy state than the bus on which they reside.

8.1.1 PCI Power Management Functional Description

The PCI 9054 passes power management information and has no inherent power-saving feature.

The PCI Status register (PCISR) and the New Capability Pointer register (CAP_PTR) indicate whether a new capability (the Power Management function) is available. The New Capability Functions Support bit (PCISR[4]) enables a PCI BIOS to identify a New Capability function support. This bit is executable for writes from the Local Bus, and reads from both the Local and PCI Buses. The CAP_PTR register provides an offset into PCI Configuration Space, the start location of the first item in a New Capabilities Linked List.

The Power Management Capability ID register (PMCAPID) specifies the Power Management Capability ID, 01h, assigned by the PCI SIG. The Power Management Next Capability Pointer register (PMNEXT) points to the first location of the next item in the capabilities linked list. If Power Management is the last item in the list, then this register should be set to 0. The default value for the PCI 9054 is 48h (Hot Swap).

For the PCI 9054 to change the power state and assert PME#, the Local Host or PCI Host should set the PME#_En bit (PMCSR[8]=1). The Local Host then determines to which power state the backplane should change by reading the Power_State bits (PMCSR[1:0]).

The Local Host sets up the following:

- D_2_Support and D_1_Support bits (PMC[10:9]) are used by the Local Host to identify power state support
- PME#_Support bits (PMC[14:11]) are used by the PCI 9054 to identify the PME# Support correspondent to a specific power state (PMCSR[1:0])

The Local Host then sets the PME#_Status bit (PMCSR[15]=1) and the PCI 9054 asserts PME#. To clear the PME#_Status bit, the PCI Host must write a 1 to the PME# Status bit (PMCSR[15]=1). To disable the PME# Interrupt signal, either Host can write a 0 to the PME#_En bit (PMCSR[8]=0).

LINT# output is asserted every time the power state in the PMCSR register changes. Transmission from state 11 (D_{3hot}) to state 00 (D_0) causes a soft reset. A soft reset should only be initiated from the PCI Bus because the Local Bus interface is reset during a soft reset. The PCI 9054 issues LRESETo# and resets all its internal registers to their default values. In state D_{3hot}, PCI Memory and I/O accesses are disabled, as well as PCI interrupts, and only configuration is allowed. Before making LINT# output work, set the Power Management Interrupt Enable bit (INTCSR[4]=1), and clear the interrupt by setting the Power Management Interrupt bit (INTCSR[5]=1).

The Data_Scale bits (PMCSR[14:13]) indicate the scaling factor to use when interpreting the value of the Power Management Data bits (PMDATA[7:0]). The value and meaning of the bits depend upon the data value specified in the Data_Select bits (PMCSR[12:9]). The Data_Scale bit value is unique for each Data_Select bit. For Data_Select values from 8 to 15, the Data_Scale bits always return a zero (PMCSR[14:13]=0).

PMDATA provides operating data, such as power consumed or heat dissipation.

8.1.2 System Changes Power Mode Example

1. The Host writes to the PCI 9054 PMCSR register to change the power states.
2. The PCI 9054 sends a local interrupt (LINT# output) to a Local CPU (LCPU).
3. The LCPU has 200 µs to read the power management information from the PCI 9054 PMCSR register to implement the power saving function.
4. After the LCPU implements the power saving function, the PCI 9054 disables all Direct Slave accesses and PCI Interrupt output (INTA#). In addition, the BIOS disables the PCI 9054 Master Access Enable bit (PCICR[2]).

***Notes**: In Power Saving mode, all PCI and Local Configuration cycles are granted.*

The PCI 9054 automatically performs a soft reset to a Local Bus on D_3-to-D_0 transitions.

8.1.3 Wake-Up Request Example

1. The add-in card (with a PCI 9054 chip installed) is in a powered-down state.
2. The Local CPU performs a write to the PCI 9054 PMCSR register to request a wake-up procedure.
3. As soon as the request is detected, the PCI 9054 drives PME# out to the PCI Bus.
4. The PCI Host accesses the PCI 9054 PMCSR register to disable the PME# output signal and restores the PCI 9054 to the D_0 power state.
5. The PCI 9054 completes the power management task by issuing the Local interrupt (LINT# output) to the Local CPU, indicating that the power mode has changed.

9. COMPACTPCI HOT SWAP

9.1 Hot Swap

The PCI 9054 is a CompactPCI Hot Swap-*Friendly*-compliant device.

9.1.1 Overview

Hot Swap is used for CompactPCI applications. Hot Swap functionality allows the orderly insertion and removal of boards without adversely affecting system operation. This is done for repair of faulty boards or system reconfiguration. Additionally, Hot Swap provides programmatic access to Hot Swap services allowing system reconfiguration and fault recovery to occur with no system down time and minimum operator interaction. Control of adapter insertion/removal logic resides on the individual adapters. The PCI 9054 uses two pins, ENUM# and LEDon/LEDin, to implement the hardware aspects of Hot Swap functionality. The PCI 9054 uses the Hot Swap Capabilities register to implement the software aspects of Hot Swap capabilities.

To avoid confusion in the industry, Hot Swap defines three levels of compatibility:

- Hot Swap-*Capable* devices contain the minimum requirements to operate in Hot Swap environment
- Hot Swap-*Friendly* devices contain additional functions to ease the job of the user
- Hot Swap-*Ready* devices contain all the necessary functions for Hot Swap

Hot Swap-*Capable* requirements are mandatory for a device to be used in Hot Swap environment. These requirements are attributes for which a system user must compensate using external circuitry, as follows:

- PCI Specification v2.1 compliant
- Tolerate Vcc from early power
- Tolerate precharge voltage
- Limited I/O pin leakage at precharge voltage

Hot Swap-*Friendly* silicon includes all the required *Capable* functions and adds some of the functions in the following list. These functions are possible to add externally to the device. The PCI 9054 has integrated them into the PCI silicon, thus reducing the amount of external circuitry that a user must add.

- **Incorporates Hot Swap Control/Status register (HS_CSR)**—Contained within the configuration space.
- **Incorporates an Extended Capability Pointer (ECP) mechanism**—Software must have a standard method of determining if a specific function is designed in accordance with the specification. The Capabilities Pointer is located within standard CSR space, using a bit in the PCI Status register (offset 04h).

The PCI 9054 has additional resources for software control of the ENUM# ejector switch and the blue LED to indicate insertion/removal.

The PCI 9054 is a Hot Swap-*Friendly* PCI silicon device. The PCI 9054 has incorporated all compliant functions defined by the CompactPCI Hot Swap specification. The PCI 9054 incorporates LEDon/LEDin and ENUM# and Hot Swap Capabilities registers—HS_CNTL, HS_NEXT, and HS_CSR.

9.1.2 Controlling Connection Processes

The following sections are excerpts from *CompactPCI Specification*. Please refer to the specification for more details.

9.1.2.1 Hardware Connection Control

Hardware Control provides a means for the platform to control the hardware connection process. The signals listed in the following sections must be supported on all Hot Swap boards for interoperability. Implementations on different platforms may vary.

9.1.2.1.1 Board Slot Control

BD_SEL# is one of the shortest pins. It is driven low to enable power-on. For systems not implementing hardware control, it is grounded on the backplane.

Systems implementing hardware control radially connect BD_SEL# to a Hot Swap Controller (HSC). The controller terminates the signal with a weak pulldown. The controller can detect board present when the board pullup overrides the pulldown. HSC can then control the power-on process by driving BD_SEL# low.

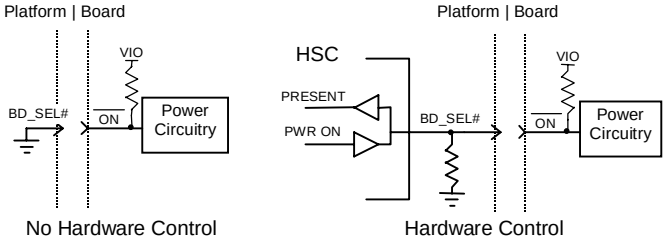

Figure 9-1. Redirection of BD_SEL#

9.1.2.1.2 Board Healthy

A second radial signal is used to acknowledge board health. It signals that a board is suitable to be released from reset and allowed onto the PCI Bus.

Minimally, this signal must be connected to the card's power controller "power good" status line. Use of HEALTHY# can be expanded for applications requiring additional conditions to be met for the board to be considered healthy.

On platforms that do not use Hardware Connection Control this line is not monitored. Platforms implementing this signaling route these signals radially to a Hot Swap Controller.

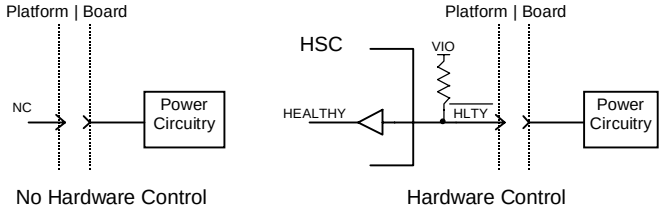

Figure 9-2. Board Healthy

9.1.2.1.3 Platform Reset

Reset (PCI_RST#), as defined by *CompactPCI Specification*, is a bused signal on the backplane, driven by the Host. Platforms may implement this signal as a radial signal from the Hot Swap Controller to further control the electrical connection process. To maintain function of the bused signal, platforms that do this must *OR* the Host reset signal with the slot-specific signal.

Locally, boards must not come out of reset until the H1 State is reached (healthy), but they must also honor the backplane reset. The Local board reset (Local_PCI_RST#) must be the logical *OR* of these two conditions. Local_PCI_RST# is connected to the PCI 9054 RST# input pin.

During a BIOS voltage precharge and platform reset, in insertion and extraction procedures, all PCI I/O buffers must be in a High Impedance state. The PCI 9054 supports this condition any time the Host RST# is asserted (PCI v2.1). To protect the Local board components from early power, the PCI 9054 floats the Local Bus I/Os. The TEST pin can be used to perform the High Impedance condition on the Local Bus. Both the RST# and TEST signals can be simultaneously asserted. The TEST signal is de-asserted some time before the Host RST# is de-asserted to ensure the PCI 9054 asserts the LRESETo# signal to complete a reset task of the Local board.

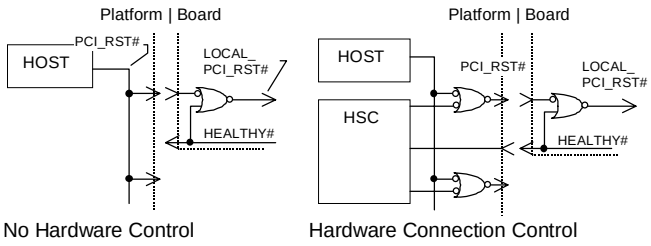

Figure 9-3. PCI Reset

9.1.2.2 Software Connection Control

Software Connection Control provides a means to control the Software Connection Process. Resources on the hot swap board facilitate software Connection Control. Access to these resources occurs by way of the bus, using PCI protocol transfers (in-band).

These resources consist of four elements:

- ENUM# driven active indicates the need to change the state of the Hot Swap board
- A switch, tied to the ejector, indicates the intent to remove a board
- LED indicates the status of the software connection process
- Control/Status register allows the software to interact with these resources

9.1.2.2.1 Ejector Switch and Blue LED

A microswitch (switch), located in the card-ejector mechanism of the Hot Swap CompactPCI board, is used to signal the impending removal of a board. This signal asserts ENUM#. The operator normally activates the switch, waits for the LED illumination to indicate it is okay to remove the board, and then removes the board. The PCI 9054 implements control logic for both the microswitch and the Blue LED in one pin (LEDon/LEDin).

When the ejector is opened or closed, the switch bounces for a time. The PCI 9054 uses internal debounce circuitry to clean the signal before the remainder of Hot Swap logic acknowledges it. The state of the switch is acknowledged six times, at 1 ms intervals, before it is assumed closed or open.

The Blue “Status” LED, located on the front of the Hot Swap CompactPCI board, is illuminated when it is permissible to remove a board. The hardware connection layer provides protection for the system during all insertions and extractions. This LED indicates the system software is in a state that tolerates board extraction.

Upon insertion, the LED is automatically illuminated by the hardware until the hardware connection process completes. The LED remains *OFF* until the software uses it to indicate extraction is once again permitted.

The PCI 9054 uses a tri-state I/O pin to drive the external LED. This pin is Time-Division Multiplexed (TDM) for input and output functionality. When an output, it drives the external LED. The LED state is driven from the LED Software On/Off Switch bit (HS_CSR[3]). When used as an input, it acknowledges the state of the ejector handle. With the implementation of TDM, this pin is usually driving the LED. A small portion of time is dedicated to acknowledging ejector status.

9.1.2.2.2 ENUM#

ENUM# is provided to notify the Host CPU that a board has been freshly inserted or is about to be removed. This signal informs the CPU that configuration of the system has changed. The CPU then performs any necessary maintenance such as installing a device driver upon board insertion, or quiescing a device driver prior to board extraction.

ENUM# is an open collector bused signal with a pull-up on the Host. It may drive an interrupt (preferred) or be polled by the system software at regular intervals. The CompactPCI Hot-Plug System Driver on the system Host manages the ENUM# sensing. Full Hot Swap Boards assert ENUM# until serviced by the Hot-Plug system driver.

When a board is inserted into the system and reset, the PCI 9054 acknowledges the state of the ejector switch. If this switch is open (ejector closed) the PCI 9054 asserts ENUM# interrupt and sets the ENUM# Status Indicator for Board Insertion bit (HS_CSR[7]). Once the Host CPU has installed the proper drivers, it can logically include this board by clearing the interrupt.

When a board is about to be removed, the PCI 9054 acknowledges the ejector switch is closed (ejector open), asserts ENUM# interrupt and sets the ENUM# Status Indicator for Board Removal bit (HS_CSR[6]). The Host then logically removes the board and turns on the LED. The operator can then remove the board completely.

9.1.2.2.3 Hot Swap Control/Status Register (HS_CSR)

The PCI 9054 supports Hot Swap directly, as a control/status register is provided in Configuration space. This register is accessed through the PCI Extended Capabilities Pointer (ECP) mechanism.

The Hot Swap Control/Status register (HS_CSR) provides status read-back for the Hot-Plug System Driver to determine which board is driving ENUM#. This register is also used to control the Hot Swap Status LED on the front panel of the board, and to de-assert ENUM#.

9.1.2.2.3.1 Hot Swap Capabilities Register Bit Definition

31 24	23 16	15 8	7 0
Reserved	Control	Next_Cap Pointer	Hot Swap ID

Figure 9-4. Hot Swap Capabilities Register Bit Definition

Hot Swap ID. Bits [7:0]. These bits are set to a default value of 0x00.

Next_Cap Pointer. Bits [15:8]. These bits either point to the next New Capability structure, or are set to 0 if this is the last capability in the structure.

Control. Bits [23:16]. This eight-bit control register is defined as follows (refer to Table 9-1).

Table 9-1. Hot Swap Control

Bit	Description
23	ENUM# status—Insertion (1 = board is inserted).
22	ENUM# status—Removal (1 = board is being removed).
21	Not used.
20	Not used.
19	LED state (1 = LED on, 0 = LED off).
18	Not used.
17	ENUM# interrupt enable (1 = de-assert, 0 = enable interrupt).
16	Not used.

10. PCI VITAL PRODUCT DATA (VPD)

10.1 Overview

The Vital Product Data (VPD) function in PCI Specification v2.2 defines a new location and access method. It also defines the Read Only and Read/Write bits. Currently Device ID, Vendor ID, Revision ID, Class Code, Subsystem ID, and Subsystem Vendor ID are required in the Configuration Space Header and are required for basic identification of the device and device configuration. Though this information allows a device to be configured, it is not sufficient to allow a device to be uniquely identified. With the addition of VPD, optional information is provided that allows a device to be uniquely identified and tracked. These additional bits enable current and/or future support tools and reduces the total cost of ownership of PCs and systems.

This provides an alternate access method other than Expansion ROM for VPD. VPD is stored in an external serial EEPROM, which is accessed using the Configuration Space New Capabilities function.

The VPD registers—PVPDCNTL, PVPD_NEXT, PVPDAD, and PVPDATA—are not accessible for reads from the Local Bus. It is recommended that the VPD function be exercised only from the PCI Bus.

10.1.1 VPD Capabilities Register

VPD ID. Bits [7:0]. These bits are assigned a value of 03h by the PCI SIG. The VPD ID is hardcoded.

Next_Cap Pointer. Bits [15:8]. These bits either point to the next New Capability structure, or are set to 0 if this is the last capability in the structure. The PCI 9054 defaults to 0x00. This value can be overwritten from the Local Bus.

VPD Address. Bits [24:16]. These bits specify the byte address of the VPD to be accessed. All accesses are 32-bit wide; bits [17:16] must be 0, with the maximum serial EEPROM size being 4 kilobits. Bits [30:25] are ignored.

F. Bit 31. This bit sets a flag to indicate when a serial EEPROM data operation is complete. For Write cycles, the four bytes of data are first written into the VPD Data bits, after which the VPD Address is written at the same time the F flag is set to 1. The F flag clears when the serial EEPROM Data transfer completes. For Read cycles, the VPD Address is written at the same time the F flag is cleared to 0. The F flag is set when four bytes of data are read from the serial EEPROM.

VPD Data. Bits [31:0]. The VPDDATA register is not a pure read/write register. The data read in the register depends upon the last Read operation performed in the VPDDAD[15]. VPD data is written or read through this register. Least-significant byte corresponding to VPD Byte at the address specified by the VPD Address register. Four bytes are always transferred between the register and the serial EEPROM.

31	30 16	15 8	7 0
F	VPD Address	Next_Cap Pointer (0X00)	VPD ID (0x03)
VPD Data			

Figure 10-1. VPD Capabilities Register

10.1.2 Serial EEPROM Partitioning for VPD

To support VPD, the serial EEPROM is partitioned into read only and read/write sections.

10.1.3 Sequential Read Only

The first 1456 bits, 182 bytes of the serial EEPROM contain read-only information. The read-only portion of the serial EEPROM is loaded into the PCI 9054, using a sequential Read command to serial EEPROM and occurs once after power-on.

10.1.4 Random Read and Write

The PCI 9054 can read and write the read/write portion of serial EEPROM. The Serial EEPROM Starting at Lword Boundary for VPD Accesses bits (PROT_AREA[6:0]) designates this portion. This register is loaded upon power-on and can be written with a desired value starting at location 0. This provides the capability of writing the entire serial EEPROM. Writes to serial EEPROM are comprised of the following three commands:

- Write Enable
- Write Enable, followed by Write data
- Write Disable

This is done to ensure against accidental write of the serial EEPROM. Random cycles allow VPD information to be written and read at any time.

To perform a simple VPD write to the serial EEPROM, the following steps are necessary:

1. Change the write-protected serial EEPROM address in PROT_AREA[6:0] to the desired address. 0x0000000 makes the serial EEPROM removable from the beginning.
2. Write desired data into the VPDDATA register.
3. Write destination serial EEPROM address and flag of operation, value of 1.
4. Probe a flag of operation until it changes to a 0 to ensure the write completes.

To perform a simple VPD read from serial EEPROM, the following steps are necessary:

1. Write a destination serial EEPROM address and flag of operation, value of 0.
2. Probe a flag of operation until it changes to a 1 to ensure the Read data is available.
3. Read back the VPDDATA register to see the requested data.

11. REGISTERS

11.1 New Register Definitions Summary (As Compared to the PCI 9080)

Refer to the descriptions in the following sections for a full explanation.

Table 11-1. New Registers Definitions Summary (As Compared to the PCI 9080)

PCI Offset	Local Offset	Register	Bits	Description
08h/ACh	88h/12Ch	Mode/DMA Arbitration Register	31	WAIT# enable. In M mode, the bit lets WAIT# be rerouted to BIGEND#. In C and J modes, the bit has no effect. When set to 1, WAIT# function is selected. When set to 0, BIGEND# input function is selected.
0Dh	8Dh	Local Miscellaneous Control Register	22:16 0 1 2 3 4 5 6	Write accessible Address Pointer in the serial EEPROM device for VPD support. I/O Base Address Register enable. I/O Base Address Register shift. Local Initialization Done. Serial EEPROM or Local Host sets bit. M-mode related. BDIP# input enabled during Direct Master accesses. M-mode related. Deferred Direct Master read. M-mode related. TEA# mask interrupt. M-mode related. Direct Master Write FIFO full RETRY# enable.
0Eh	8Eh	Serial EEPROM Write-Protected Address Boundary Register	6:0	Serial EEPROM starting at the Lword boundary for VPD accesses.
34h	34h	New Capability Pointer Register	7:0	Provides offset into PCI Configuration space for the location of the first item in the New Capability Linked List.
40h	180h	Power Management Register	30:0	Provides Power Management ID, Power Management Next Capability Pointer, and Power Management Capabilities.
44h	184h	Power Management Register	31:0	Provides Power Management Status, PMCSR Bridge Support Extensions, and Power Management Data.
48h	188h	CompactPCI Hot Swap Register	31:0	Hot Swap Control, Hot Swap Next Capability Pointer, and Hot Swap Control/Status Register.
4Ch	18Ch	PCI Vital Product Data Register	31:0	VPD ID, VPD Next Capability Pointer, and VPD Address Pointer.
50h	190h	PCI Vital Product Data Register	31:0	VPD Data.
68h	E8h	Interrupt Control/Status	7:6	Local Data Parity Error Check. Bit 7 is the Parity Error Check Status. Bit 6 is the Enable bit.
6Ch	ECh	USER I/O Control	19:18	Bit 18 is a select bit between USERi and LLOCKi#. Bit 19 is a select bit between USERo and LLOCKo#.
17Ch	FCh	Direct Master PCI Dual Address Cycle	31:0	Direct Master PCI Dual Address Cycle. When set to 0, the PCI 9054 performs a 32-bit PCI Address cycle.
94h	114h	DMA CH_1 Mode Register	12	The PCI 9054 does not support Demand Mode DMA by way of Channel 1. Bit is reserved.
B4h	134h	DMA0 PCI Dual Address Cycle	31:0	DMA0 PCI Dual Address Cycle. When set to 0, the PCI 9054 performs a 32-bit PCI Address cycle.
B8h	138h	DMA1 PCI Dual Address Cycle	31:0	DMA1 PCI Dual Address Cycle. When set to 0, the PCI 9054 performs a 32-bit PCI Address cycle.

11.2 Register Address Mapping

11.2.1 PCI Configuration Registers

Table 11-2. PCI Configuration Registers

PCI Configuration Register Address	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9054 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 24 23 16 15 8 7 0	PCI/Local Writable	Serial EEPROM Writable
00h	00h	Device ID | Vendor ID	Local	Y
04h	04h	Status | Command	Y	N
08h	08h	Class Code | Revision ID	Local	Y
0Ch	0Ch	BIST | Header Type | PCI Bus Latency Timer | Cache Line Size	Y [15:0], Local	N
10h	10h	PCI Base Address 0; used for Memory-Mapped Configuration Registers (PCIBAR0)	Y	N
14h	14h	PCI Base Address 1; used for I/O-Mapped Configuration Registers (PCIBAR1)	Y	N
18h	18h	PCI Base Address 2; used for Local Address Space 0 (PCIBAR2)	Y	N
1Ch	1Ch	PCI Base Address 3; used for Local Address Space 1 (PCIBAR3)	Y	N
20h	20h	Unused Base Address (PCIBAR4)	N	N
24h	24h	Unused Base Address (PCIBAR5)	N	N
28h	28h	Cardbus CIS Pointer (Not Supported)	N	N
2Ch	2Ch	Subsystem ID | Subsystem Vendor ID	Local	Y
30h	30h	PCI Base Address for Local Expansion ROM	Y	N
34h	34h	Reserved | New Capability Pointer	Local [7:0]	N
38h	38h	Reserved	N	N
3Ch	3Ch	Max_Lat | Min_Gnt | Interrupt Pin | Interrupt Line	Y [7:0], Local	Y
40h	180h	Power Management Capabilities | Next_Cap Pointer | Capability ID	Local	N
44h	184h	Data | PMCSR Bridge Support Extensions | Power Management Control/Status Register	Y [15, 12:8, 1:0]	N
48h	188h	Reserved | Control/Status Register | Next_Cap Pointer | Capability ID	PCI [23:16], Local [15:0]	Y [15:0]
4Ch	18Ch	F | VPD Address | Next_Cap Pointer | Capability ID	Y [31:16], Local [15:8]	N
50h	190h	VPD Data	Y	N

Note: *Refer to PCI Specification v2.1 for definitions of these registers.*

11.2.2 Local Configuration Registers

Table 11-3. Local Configuration Registers

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9054 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 24 23 16 15 8 7 0	PCI/Local Writable	Serial EEPROM Writable
00h	80h	Range for PCI-to-Local Address Space 0	Y	Y
04h	84h	Local Base Address (Remap) for PCI-to-Local Address Space 0	Y	Y
08h	88h	Mode/DMA Arbitration	Y	Y
0Ch	8Ch	Reserved | Serial EEPROM Write-Protected Address Boundary | Local Miscellaneous Control | Big/Little Endian Descriptor	Y	Y
10h	90h	Range for PCI-to-Local Expansion ROM	Y	Y
14h	94h	Local Base Address (Remap) for PCI-to-Local Expansion ROM and BREQo Control	Y	Y
18h	98h	Local Bus Region Descriptors (Space 0 and Expansion ROM) for PCI-to-Local Accesses	Y	Y
1Ch	9Ch	Range for Direct Master-to-PCI	Y	Y
20h	A0h	Local Base Address for Direct Master-to-PCI Memory	Y	Y
24h	A4h	Local Base Address for Direct Master-to-PCI I/O Configuration	Y	Y
28h	A8h	PCI Base Address (Remap) for Direct Master-to-PCI	Y	Y
2Ch	ACh	PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	Y	Y
F0h	170h	Range for PCI-to-Local Address Space 1	Y	Y
F4h	174h	Local Base Address (Remap) for PCI-to-Local Address Space 1	Y	Y
F8h	178h	Local Bus Region Descriptor (Space 1) for PCI-to-Local Accesses	Y	Y
FCh	17Ch	PCI Base Dual Address Cycle (Remap) for Direct Master-to-PCI (Upper 32 bits)	Y	N

11.2.3 Runtime Registers

Table 11-4. Runtime Registers

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9054 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 16 15 0		PCI/Local Writable	Serial EEPROM Writable
40h	C0h	Mailbox Register 0 (refer to Note)		Y	Y
44h	C4h	Mailbox Register 1 (refer to Note)		Y	Y
48h	C8h	Mailbox Register 2		Y	N
4Ch	CCh	Mailbox Register 3		Y	N
50h	D0h	Mailbox Register 4		Y	N
54h	D4h	Mailbox Register 5		Y	N
58h	D8h	Mailbox Register 6		Y	N
5Ch	DCh	Mailbox Register 7		Y	N
60h	E0h	PCI-to-Local Doorbell Register		Y	N
64h	E4h	Local-to-PCI Doorbell Register		Y	N
68h	E8h	Interrupt Control/Status		Y	N
6Ch	ECh	Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control		Y	N
70h	F0h	Device ID	Vendor ID	N	N
74h	F4h	Unused	Revision ID	N	N
78h	C0h	Mailbox Register (refer to Note)		Y	N
7Ch	C4h	Mailbox Register (refer to Note)		Y	N

Note: *Mailbox registers 0 and 1 are always accessible at addresses 78h/C0h and 7Ch/C4. When the I_2O function is disabled (QSR[0]=0), mailbox registers 0 and 1 are also accessible at PCI addresses 40h and 44h for PCI 9060 compatibility. When the I_2O function is enabled, the Inbound and Outbound Queue pointers are accessed at addresses 40 and 44, replacing mailbox registers in PCI Address space.*

11.2.4 DMA Registers

Table 11-5. DMA Registers

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9054 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 16 15 8 7 0			PCI/Local Writable	Serial EEPROM Writable
80h	100h	DMA Ch 0 Mode			Y	N
84h	104h	DMA Ch 0 PCI Address			Y	N
88h	108h	DMA Ch 0 Local Address			Y	N
8Ch	10Ch	DMA Ch 0 Transfer Byte Count			Y	N
90h	110h	DMA Ch 0 Descriptor Pointer			Y	N
94h	114h	DMA Ch 1 Mode			Y	N
98h	118h	DMA Ch 1 PCI Address			Y	N
9Ch	11Ch	DMA Ch 1 Local Address			Y	N
A0h	120h	DMA Ch 1 Transfer Byte Count			Y	N
A4h	124h	DMA Ch 1 Descriptor Pointer			Y	N
A8h	128h	Reserved	DMA Channel 1 Command/Status	DMA Channel 0 Command/Status	Y	N
ACh	12Ch	Mode/DMA Arbitration			Y	N
B0h	130h	DMA Threshold			Y	N
B4h	134h	DMA Ch 0 PCI Dual Address Cycle (Upper 32 bits)			Y	N
B8h	138h	DMA Ch 1 PCI Dual Address Cycle (Upper 32 bits)			Y	N

11.2.5 Messaging Queue Registers

Table 11-6. Messaging Queue Registers

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9054 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 0	PCI/Local Writable	Serial EEPROM Writable
30h	B0h	Outbound Post Queue Interrupt Status	N	N
34h	B4h	Outbound Post Queue Interrupt Mask	Y	N
40h	—	Inbound Queue Port	PCI	N
44h	—	Outbound Queue Port	PCI	N
C0h	140h	Messaging Unit Configuration	Y	N
C4h	144h	Queue Base Address	Y	N
C8h	148h	Inbound Free Head Pointer	Y	N
CCh	14Ch	Inbound Free Tail Pointer	Y	N
D0h	150h	Inbound Post Head Pointer	Y	N
D4h	154h	Inbound Post Tail Pointer	Y	N
D8h	158h	Outbound Free Head Pointer	Y	N
DCh	15Ch	Outbound Free Tail Pointer	Y	N
E0h	160h	Outbound Post Head Pointer	Y	N
E4h	164h	Outbound Post Tail Pointer	Y	N
E8h	168h	Queue Status/Control	Y	N

Notes: *When I_2O messaging is enabled (QSR[0]= 1), the PCI Master (Host or another IOP) uses the Inbound Queue Port to read Message Frame Addresses (MFAs) from the Inbound Free List FIFO and to write MFAs to the Inbound Post Queue FIFO. Uses the Outbound Queue Port to read MFAs from the Outbound Post Queue FIFO and to write MFAs to the Outbound Free List FIFO.*

Each Inbound MFA is specified by I_2O as an offset from the PCI Base Address 0 (programmed in PCIBAR0) to start of message frame. This means that all inbound message frames should reside in PCI Base Address 0 Memory space.

Each Outbound MFA is specified by I_2O as an offset from system address 0x00000000h. Outbound MFA is a physical
32-bit address of the frame in shared PCI system memory.

The Inbound and Outbound Queues may reside in Local Address Space 0 or 1 by programming QSR. The queues need not be in shared memory.

11.3 PCI Configuration Registers

All registers may be written to or read from in Byte, Word, or Lword accesses.

11.3.1 (PCIIDR; PCI:00h, LOC:00h) PCI Configuration ID Register

Table 11-7. (PCIIDR; PCI:00h, LOC:00h) PCI Configuration ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Vendor ID. Identifies manufacturer of device. Defaults to the PCI SIG-issued Vendor ID of PLX (10B5h) if blank or if no serial EEPROM is present.	Yes	Local/ Serial EEPROM	10B5h or 0
31:16	Device ID. Identifies particular device. Defaults to PLX part number for PCI interface chip (9054h) if blank or no serial EEPROM is present.	Yes	Local/ Serial EEPROM	9054h or 0

11.3.2 (PCICR; PCI:04h, LOC:04h) PCI Command Register

Table 11-8. (PCICR; PCI:04h, LOC:04h) PCI Command Register

Bit	Description	Read	Write	Value after Reset
0	I/O Space. Writing a 1 allows the device to respond to I/O space accesses. Writing a 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
1	Memory Space. Writing a 1 allows the device to respond to Memory Space accesses. Writing a 0 disables the device from responding to Memory Space accesses.	Yes	Yes	0
2	Master Enable. Writing a 1 allows device to behave as a Bus Master. Writing a 0 disables device from generating Bus Master accesses.	Yes	Yes	0
3	Special Cycle. **Not supported.**	Yes	No	0
4	Memory Write and Invalidate Enable. Writing a 1 enables the Memory Write and Invalidate mode for Direct Master and DMA. (Refer to the DMA Mode register(s), DMAMODE0[13] and/or DMAMODE1[13].)	Yes	Yes	0
5	VGA Palette Snoop. **Not supported.**	Yes	No	0
6	Parity Error Response. Writing a 0 indicates parity error is ignored and the operation continues. Writing a 1 indicates parity checking is enabled.	Yes	Yes	0
7	Wait Cycle Control. Controls whether a device does address/data stepping. Writing a 0 indicates the device never does stepping. Writing a 1 indicates the device always does stepping. ***Note:*** *Hardcoded to 0.*	Yes	No	0
8	SERR# Enable. Writing a 1 enables SERR# driver. Writing a 0 disables SERR# driver.	Yes	Yes	0
9	Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus. Writing a 1 indicates fast back-to-back transfers can occur to any agent on the bus. Writing a 0 indicates fast back-to-back transfers can only occur to the same agent as in the previous cycle. ***Note*:** *Hardcoded to 0.*	Yes	No	0
15:10	Reserved.	Yes	No	0h

11.3.3 (PCISR; PCI:06h, LOC:06h) PCI Status Register

Table 11-9. (PCISR; PCI:06h, LOC:06h) PCI Status Register

Bit	Description	Read	Write	Value after Reset
3:0	Reserved.	Yes	No	0h
4	New Capability Functions Support. Writing a 1 supports New Capabilities Functions. If enabled, the first New Capability Function ID is located at PCI Configuration offset [40h]. Can only be written from the Local Bus. Read-only from the PCI Bus.	Yes	Local	1
5	Reserved.	Yes	No	0
6	If set to 1, this device supports User Definable Functions. Can only be written from the Local Bus. Read-only from the PCI Bus.	Yes	Local	0
7	Fast Back-to-Back Capable. Writing a 1 indicates an adapter can accept fast back-to-back transactions. ***Note:*** *Hardcoded to 1.*	Yes	No	1
8	Master Data Parity Error Detected. Set to 1 when three conditions are met: 1) PCI 9054 asserted PERR# or acknowledged PERR# asserted; 2) PCI 9054 was Bus Master for operation in which error occurred; 3) Parity Error Response bit is set (PCICR[6]=1). Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0
10:9	DEVSEL# Timing. Indicates timing for DEVSEL# assertion. Writing a 01 sets this bit to medium. ***Note:*** *Hardcoded to 01.*	Yes	No	01
11	Target Abort. When set to 1, indicates the PCI 9054 has signaled a Target Abort. Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0
12	Received Target Abort. When set to 1, indicates the PCI 9054 has received a Target Abort signal. Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0
13	Received Master Abort. When set to 1, indicates the PCI 9054 has received a Master abort signal. Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0
14	Signaled System Error. When set to 1, indicates the PCI 9054 has reported a system error on SERR#. Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0
15	Detected Parity Error. When set to 1, indicates the PCI 9054 has detected a PCI Bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command register is clear). One of three conditions can cause this bit to be set: 1) PCI 9054 detected parity error during PCI Address phase; 2) PCI 9054 detected data parity error when it was the Target of a write; 3) PCI 9054 detected data parity error when performing Master Read operation. Writing a 1 clears this bit to 0.	Yes	Yes/Clr	0

11.3.4 (PCIREV; PCI:08h, LOC:08h) PCI Revision ID Register

Table 11-10. (PCIREV; PCI:08h, LOC:08h) PCI Revision ID Register

Bit	Description	Read	Write	Value after Reset
7:0	Revision ID. Silicon revision of the PCI 9054.	Yes	Local/ Serial EEPROM	Current Rev #

11.3.5 (PCICCR; PCI:09-0Bh, LOC:09-0Bh) PCI Class Code Register

Table 11-11. (PCICCR; PCI:09-0Bh, LOC:09-0Bh) PCI Class Code Register

Bit	Description	Read	Write	Value after Reset
7:0	Register Level Programming Interface. None defined.	Yes	Local/ Serial EEPROM	0h
15:8	Subclass Code (Other Bridge Device).	Yes	Local/ Serial EEPROM	80h
23:16	Base Class Code (Bridge Device).	Yes	Local/ Serial EEPROM	06h

11.3.6 (PCICLSR; PCI:0Ch, LOC:0Ch) PCI Cache Line Size Register

Table 11-12. (PCICLSR; PCI:0Ch, LOC:0Ch) PCI Cache Line Size Register

Bit	Description	Read	Write	Value after Reset
7:0	System Cache Line Size. Specified in units of 32-bit words (8 or 16 Lwords). If a size other than 8 or 16 is specified, the PCI 9054 performs Write transfers rather than Memory Write and Invalidate transfers.	Yes	Yes	0h

11.3.7 (PCILTR; PCI:0Dh, LOC:0Dh) PCI Bus Latency Timer Register

Table 11-13. (PCILTR; PCI:0Dh, LOC:0Dh) PCI Bus Latency Timer Register

Bit	Description	Read	Write	Value after Reset
7:0	PCI Bus Latency Timer. Specifies amount of time (in units of PCI Bus clocks) the PCI 9054, as a Bus Master, can burst data on the PCI Bus.	Yes	Yes	0h

11.3.8 (PCIHTR; PCI:0Eh, LOC:0Eh) PCI Header Type Register

Table 11-14. (PCIHTR; PCI:0Eh, LOC:0Eh) PCI Header Type Register

Bit	Description	Read	Write	Value after Reset
6:0	Configuration Layout Type. Specifies layout of bits 10h through 3Fh in configuration space. Only one encoding, 0h, is defined. All other encodings are reserved.	Yes	Local	0h
7	Header Type. Writing a 1 indicates multiple functions. Writing a 0 indicates single function.	Yes	Local	0

11.3.9 (PCIBISTR; PCI:0Fh, LOC:0Fh) PCI Built-In Self Test (BIST) Register

Table 11-15. (PCIBISTR; PCI:0Fh, LOC:0Fh) PCI Built-In Self Test (BIST) Register

Bit	Description	Read	Write	Value after Reset
3:0	Writing a 0h indicates a device passed its test. Non-0h values indicate a device failed its test. Device-specific failure codes can be encoded in a non-0h value.	Yes	Local	0h
5:4	Reserved.	Yes	No	00
6	PCI BIST Interrupt Enable. The PCI Bus writes 1 to enable BIST. Generates an interrupt to the Local Bus. The Local Bus resets this bit when BIST is complete. The software should fail device if BIST is not complete after two seconds. Refer to the Runtime registers for Interrupt Control/Status.	Yes	Yes	0
7	Returns 1 if device supports BIST. Returns 0 if device is not BIST compatible.	Yes	Local	0

11.3.10 (PCIBAR0; PCI:10h, LOC:10h) PCI Base Address Register for Memory Accesses to Local, Runtime, and DMA Registers

Table 11-16. (PCIBAR0; PCI:10h, LOC:10h) PCI Base Address Register for Memory Accesses to Local, Runtime, and DMA Registers

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. ***Note:*** *Hardcoded to 0.*	Yes	No	0
2:1	Location of Register. Values: 00—Locate anywhere in 32-bit Memory Address space 01—Locate below 1-MB Memory Address space 10—Locate anywhere in 64-bit Memory Address space 11—Reserved ***Note:*** *Hardcoded to 00.*	Yes	No	00
3	Prefetchable. Writing a 1 indicates there are no side effects on reads. Does not affect operation of the PCI 9054. ***Note:*** *Hardcoded to 0.*	Yes	No	0
7:4	Memory Base Address. Memory base address for access to Local, Runtime, and DMA registers (requires 256 bytes). ***Note:*** *Hardcoded to 0h.*	Yes	No	0h
31:8	Memory Base Address. Memory base address for access to Local, Runtime, and DMA registers.	Yes	Yes	0h

Note: *For I_2O, Inbound message frame pool must reside in address space pointed to by PCIBAR0. Message Frame Address (MFA) is defined by I_2O as offset from this base address to start of message frame.*

11.3.11 (PCIBAR1; PCI:14h, LOC:14h) PCI Base Address Register for I/O Accesses to Local, Runtime, and DMA Registers

Table 11-17. (PCIBAR1; PCI:14h, LOC:14h) PCI Base Address Register for I/O Accesses to Local, Runtime, and DMA Registers

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. ***Note:*** *Hardcoded to 1.*	Yes	No	1
1	Reserved.	Yes	No	0
7:2	I/O Base Address. Base Address for I/O access to Local, Runtime, and DMA registers (requires 256 bytes). ***Note:*** *Hardcoded to 0h.*	Yes	No	0h
31:8	I/O Base Address. Base Address for I/O access to Local, Runtime, and DMA registers. PCIBAR1 can be enabled or disabled by setting or clearing the Base Address Register 1 Enable bit (LMISC[0]).	Yes	Yes	0h

11.3.12 (PCIBAR2; PCI:18h, LOC:18h) PCI Base Address Register for Memory Accesses to Local Address Space 0

Table 11-18. (PCIBAR2; PCI:18h, LOC:18h) PCI Base Address Register for Memory Accesses to Local Address Space 0

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. (Specified in LAS0RR register.)	Yes	No	0
2:1	Location of Register (If Memory Space). Values: 00—Locate anywhere in 32-bit Memory Address space 01—Locate below 1-MB Memory Address space 10—Locate anywhere in 64-bit Memory Address space 11—Reserved (Specified in LAS0RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: bit 1 no, bit 2 yes	00
3	Prefetchable (If Memory Space). Writing a 1 indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect operation of the PCI 9054. Prefetching functions of this address space are controlled by the associated Bus Region Descriptor register. (Specified in LAS0RR register.) If I/O Space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Memory Base Address. Memory base address for access to Local Address Space 0. PCIBAR2 can be enabled or disabled by setting or clearing the Space 0 Enable bit (LAS0BA[0]).	Yes	Yes	0h

11.3.13 (PCIBAR3; PCI:1Ch, LOC:1Ch) PCI Base Address Register for Memory Accesses to Local Address Space 1

Table 11-19. (PCIBAR3; PCI:1Ch, LOC:1Ch) PCI Base Address Register for Memory Accesses to Local Address Space 1

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Writing a 0 indicates the register maps into Memory space. Writing a 1 indicates the register maps into I/O space. (Specified in LAS1RR register.)	Yes	No	0
2:1	Location of Register. Values: 00—Locate anywhere in 32-bit Memory Address space 01—Locate below 1-MB Memory Address space 10—Locate anywhere in 64-bit Memory Address space 11—Reserved (Specified in LAS1RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 No, Bit 2 Yes	00
3	Prefetchable (If Memory Space). Writing a 1 indicates there are no side effects on reads. Reflects value of LAS1RR[3] and only provides status to the system. Does not affect operation of the PCI 9054. Prefetching functions of this address space are controlled by the associated Bus Region Descriptor register. (Specified in LAS1RR register.) If I/O Space, bit 3 is included in base address.	Yes	Mem: No I/O: Yes	0
31:4	Memory Base Address. Memory base address for access to Local Address Space 1. PCIBAR3 can be enabled or disabled by setting or clearing the Space 1 Enable bit (LAS1BA[0]). If QSR[0]=1, PCIBAR3 returns 0h.	Yes	Yes	0h

11.3.14 (PCIBAR4; PCI:20h, LOC:20h) PCI Base Address Register

Table 11-20. (PCIBAR4; PCI:20h, LOC:20h) PCI Base Address Register

Bit	Description	Read	Write	Value after Reset
31:0	Reserved.	Yes	No	0h

11.3.15 (PCIBAR5; PCI:24h, LOC:24h) PCI Base Address Register

Table 11-21. (PCIBAR5; PCI:24h, LOC:24h) PCI Base Address Register

Bit	Description	Read	Write	Value after Reset
31:0	Reserved.	Yes	No	0h

11.3.16 (PCICIS; PCI:28h, LOC:28h) PCI Cardbus CIS Pointer Register

Table 11-22. (PCICIS; PCI:28h, LOC:28h) PCI Cardbus CIS Pointer Register

Bit	Description	Read	Write	Value after Reset
31:0	Cardbus Information Structure Pointer for PCMCIA. **Not supported.**	Yes	No	0h

11.3.17 (PCISVID; PCI:2Ch, LOC:2Ch) PCI Subsystem Vendor ID Register

Table 11-23. (PCISVID; PCI:2Ch, LOC:2Ch) PCI Subsystem Vendor ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Subsystem Vendor ID (unique add-in board Vendor ID).	Yes	Local/ Serial EEPROM	10B5h

11.3.18 (PCISID; PCI:2Eh, LOC:2Eh) PCI Subsystem ID Register

Table 11-24. (PCISID; PCI:2Eh, LOC:2Eh) PCI Subsystem ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Subsystem ID (unique add-in board Device ID).	Yes	Local/ Serial EEPROM	9054h

11.3.19 (PCIERBAR; PCI:30h, LOC:30h) PCI Expansion ROM Base Register

Table 11-25. (PCIERBAR; PCI:30h, LOC:30h) PCI Expansion ROM Base Register

Bit	Description	Read	Write	Value after Reset
0	Address Decode Enable. Writing a 1 indicates a device accepts accesses to the Expansion ROM address. Writing a 0 indicates a device does not accept accesses to Expansion ROM space. Should be set to 0 if there is no Expansion ROM. Works in conjunction with EROMRR[0].	Yes	Yes	0
10:1	Reserved.	Yes	No	0h
31:11	Expansion ROM Base Address (upper 21 bits).	Yes	Yes	0h

11.3.20 (CAP_PTR; PCI:34h, LOC:34h) New Capability Pointer Register

Table 11-26. (CAP_PTR; PCI:34h, LOC:34h) New Capability Pointer Register

Bit	Description	Read	Write	Value after Reset
7:0	Provides an offset into PCI Configuration Space for the location of the first item in the New Capabilities Linked List.	Yes	No	40h
31:8	Reserved.	Yes	No	0h

11.3.21 (PCIILR; PCI:3Ch, LOC:3Ch) PCI Interrupt Line Register

Table 11-27. (PCIILR; PCI:3Ch, LOC:3Ch) PCI Interrupt Line Register

Bit	Description	Read	Write	Value after Reset
7:0	Interrupt Line Routing Value. Value indicates which input of the system interrupt controller(s) is connected to each interrupt line of the device.	Yes	Yes	0h

11.3.22 (PCIIPR; PCI:3Dh, LOC:3Dh) PCI Interrupt Pin Register

Table 11-28. (PCIIPR; PCI:3Dh, LOC:3Dh) PCI Interrupt Pin Register

Bit	Description	Read	Write	Value after Reset
7:0	Interrupt Pin Register. Indicates which interrupt pin the device uses. The following values are decoded (the PCI 9054 supports only INTA#): 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	Local/ Serial EEPROM	1h

11.3.23 (PCIMGR; PCI:3Eh, LOC:3Eh) PCI Min_Gnt Register

Table 11-29. (PCIMGR; PCI:3Eh, LOC:3Eh) PCI Min_Gnt Register

Bit	Description	Read	Write	Value after Reset
7:0	Min_Gnt. Specifies how long a Burst period device needs, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 µs increments.	Yes	Local/ Serial EEPROM	0h

11.3.24 (PCIMLR; PCI:3Fh, LOC:3Fh) PCI Max_Lat Register

Table 11-30. (PCIMLR; PCI:3Fh, LOC:3Fh) PCI Max_Lat Register

Bit	Description	Read	Write	Value after Reset
7:0	Max_Lat. Specifies how often the device must gain access to the PCI Bus. Value is a multiple of 1/4 µs increments.	Yes	Local/ Serial EEPROM	0h

11.3.25 (PMCAPID; PCI:40h, LOC:180h) Power Management Capability ID Register

Table 11-31. (PMCAPID; PCI:40h, LOC:180h) Power Management Capability ID Register

Bit	Description	Read	Write	Value after Reset
7:0	Specifies Power Management Capability ID.	Yes	No	1h

11.3.26 (PMNEXT; PCI:41h, LOC:181h) Power Management Next Capability Pointer Register

Table 11-32. (PMNEXT; PCI:41h, LOC:181h) Power Management Next Capability Pointer Register

Bit	Description	Read	Write	Value after Reset
7:0	Next_Cap Pointer. Points to the first location of the next item in the capabilities linked list. If power management is the last item in the list, then this register should be set to 0.	Yes	Local	48h

11.3.27 (PMC; PCI:42h, LOC:182h) Power Management Capabilities Register

Table 11-33. (PMC; PCI:42h, LOC:182h) Power Management Capabilities Register

Bit	Description	Read	Write	Value after Reset
2:0	Version. Writing a 1 indicates this function complies with *PCI Power Management Interface Specification v1.0*.	Yes	Local	001
3	PCI Clock Required for PME# Signal. When set to 1, indicates a function relies on the presence of the PCI clock for PME# operation. The PCI 9054 does not require the PCI clock for PME#, so this bit should set to 0.	Yes	Local	0
4	Auxiliary Power Source. Because the PCI 9054 does not support PME# while in a $D3_{cold}$ state, this bit is always set to 0.	Yes	No	0
5	DSI. When set to 1, the PCI 9054 requires special initialization following a transition to a D_0 uninitialized state before a generic class device driver is able to use it.	Yes	Local	0
8:6	Reserved.	Yes	No	000
9	D_1_Support. When set to 1, the PCI 9054 supports the D_1 power state.	Yes	Local	0
10	D_2_Support. When set to 1, the PCI 9054 supports the D_2 power state.	Yes	Local	0
14:11	PME#_Support. Indicates power states in which the PCI 9054 may assert PME#. Value Description XXX1 PME# can be asserted from D_0 XX1X PME# can be asserted from D_1 X1XX PME# can be asserted from D_2 1XXX PME# can be asserted from D_{3hot}	Yes	Local	0h
15	Reserved.	Yes	No	0

11.3.28 (PMCSR; PCI:44h, LOC:184h) Power Management Control/Status Register

Table 11-34. (PMCSR; PCI:44h, LOC:184h) Power Management Control/Status Register

Bit	Description	Read	Write	Value after Reset
1:0	Power State. Determines or changes the current power state. Value State 00 D_0 01 D_1 10 D_2 11 D_{3hot} Transition from a D_{3hot} state to a D_0 state causes a soft reset. Should only be initiated from the PCI Bus because the Local Bus interface is reset during a soft reset. In a D_{3hot} state, PCI Memory and I/O accesses are disabled, as well as PCI interrupts, and only configuration is allowed. The same is true for the D_2 state if the corresponding D_2_Support pin is set.	Yes	Yes	00
7:2	Reserved.	Yes	No	0h
8	PME#_En. Writing a 1 enables PME# to be asserted.	Yes	Yes	0
12:9	Data_Select. Selects which data to report through the Data register and Data_Scale bits.	Yes	Yes	0h
14:13	Data_Scale. Indicates the scaling factor to use when interpreting the value of the Data register. Value and meaning of this bit depends on the data value selected by the Data_Select bit. When the Local CPU initializes the Data_Scale values, must use the Data_Select bit to determine which Data_Scale value it is writing. For Power Consumed and Power Dissipated data, the following scale factors are used. Unit values are in watts. Value Scale 0 Unknown 1 0.1x 2 0.01x 3 0.001x	Yes	Local	00
15	PME#_Status. Indicates PME# is being driven if the PME#_En bit is set (PMCSR[8]=1). Writing a 1 from the Local Bus sets this bit; writing a 1 from the PCI Bus clears this bit to 0. Depending on the current power state, set only if the appropriate PME#_Support bit(s) is set (PMC[15:11]=1).	Yes	Local/Set, PCI/Clr	0

11.3.29 (PMCSR_BSE; PCI:46h, LOC:186h) PMCSR Bridge Support Extensions Register

Table 11-35. (PMCSR_BSE; PCI:46h, LOC:186h) PMCSR Bridge Support Extensions Register

Bit	Description	Read	Write	Value after Reset
7:0	Reserved.	Yes	No	0h

11.3.30 (PMDATA; PCI:47h, LOC:187h) Power Management Data Register

Table 11-36. (PMDATA; PCI:47h, LOC:187h) Power Management Data Register

Bit	Description	Read	Write	Value after Reset
7:0	Power Management Data. Provides operating data, such as power consumed or heat dissipation. Data returned is selected by the Data_Select bit(s) (PMCSR[12:9]) and scaled by the Data_Scale bit(s) (PMCSR[14:13]). Data_Select — Description 0 — D_0 Power Consumed 1 — D_1 Power Consumed 2 — D_2 Power Consumed 3 — D_3 Power Consumed 4 — D_0 Power Dissipated 5 — D_1 Power Dissipated 6 — D_2 Power Dissipated 7 — D_{3hot} Power Dissipated	Yes	Local	0h

11.3.31 (HS_CNTL; PCI:48h, LOC:188h) Hot Swap Control Register

Table 11-37. (HS_CNTL; PCI:48h, LOC:188h) Hot Swap Control Register

Bit	Description	Read	Write	Value after Reset
7:0	Hot Swap ID.	Yes	Local/ Serial EEPROM	06h

11.3.32 (HS_NEXT; PCI:49h, LOC:189h) Hot Swap Next Capability Pointer Register

Table 11-38. (HS_NEXT; PCI:49h, LOC:189h) Hot Swap Next Capability Pointer Register

Bit	Description	Read	Write	Value after Reset
7:0	Next_Cap Pointer. Points to the first location of the next item in the capabilities linked list. If Hot Swap is the last item in the list, then this register should be set to zero.	Yes	Local/ Serial EEPROM	4Ch

11.3.33 (HS_CSR; PCI:4Ah, LOC:18Ah) Hot Swap Control/Status Register

Table 11-39. (HS_CSR; PCI:4Ah, LOC:18Ah) Hot Swap Control/Status Register

Bit	Description	Read	Write	Value after Reset
0	Reserved.	Yes	No	0
1	ENUM# Interrupt Clear. Writing a 0 enables the interrupt. Writing a 1 clears the interrupt.	Yes	PCI Yes/Clr	0
2	Reserved.	Yes	No	0
3	LED Software On/Off Switch. Writing a 1 turns on the LED. Writing a 0 turns off the LED.	Yes	PCI	0
4	Reserved.	Yes	No	0
5	Reserved.	Yes	No	0
6	ENUM# Status Indicator for Board Removal. Writing a 1 reports the ENUM# assertion for removal process.	Yes	PCI Only	0
7	ENUM# Status Indicator for Board Insertion. Writing a 1 reports the ENUM# assertion for insertion process.	Yes	PCI Only	0
15:8	Reserved.	Yes	No	0h

11.3.34 (PVPDCNTL; PCI:4Ch, LOC:18Ch) PCI Vital Product Data Control Register

Table 11-40. (PVPDCNTL; PCI:4Ch, LOC:18Ch) PCI Vital Product Data Control Register

Bit	Description	Read	Write	Value after Reset
7:0	VPD ID. Capability ID = 03h for VPD.	PCI	No	03h

11.3.35 (PVPD_NEXT; PCI:4Dh, LOC:18Dh) PCI Vital Product Data Next Capability Pointer Register

Table 11-41. (PVPD_NEXT; PCI:4Dh, LOC:18Dh) PCI Vital Product Data Next Capability Pointer Register

Bit	Description	Read	Write	Value after Reset
7:0	Next_Cap Pointer. Points to first location of next item in the capabilities linked list. VPD is the last item in the capabilities linked list. This register is set to 0h.	PCI	Local	0h

11.3.36 (PVPDAD; PCI:4Eh, LOC:18Eh) PCI Vital Product Data Address Register

Table 11-42. (PVPDAD; PCI:4Eh, LOC:18Eh) PCI Vital Product Data Address Register

Bit	Description	Read	Write	Value after Reset
14:0	VPD Address. Byte address of the VPD address to be accessed. Supports 2K or 4K bit serial EEPROM.	PCI	Yes	0h
15	F. Flag used to indicate when the transfer of data between PVPDATA and the storage component is complete. Writing a 0 along with the VPD address causes a read of VPD information into PVPDATA. The hardware sets this bit to 1 when the VPD Data transfer is complete. Writing a 1 along with the VPD address causes a write of VPD information from PVPDATA into a storage component. The hardware sets this bit to 0 after the Write operation is complete.	PCI	Yes	0

11.3.37 (PVPDATA; PCI:50h, LOC:190h) PVPDATA PCI VPD Data Register

Table 11-43. (PVPDATA; PCI:50h, LOC:190h) PVPDATA PCI VPD Data Register

Bit	Description	Read	Write	Value after Reset
31:0	VPD Data Register.	PCI	Yes	0h

11.4 Local Configuration Registers

11.4.1 (LAS0RR; PCI:00h, LOC:80h) Local Address Space 0 Range Register for PCI-to-Local Bus

Table 11-44. (LAS0RR; PCI:00h, LOC:80h) Local Address Space 0 Range Register for PCI-to-Local Bus

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Writing a 0 indicates Local Address Space 0 maps into PCI Memory space. Writing a 1 indicates address Space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI Address space 0 1 Locate below 1 MB in PCI Address space 1 0 Locate anywhere in 64-bit PCI Address space 1 1 Reserved When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [31:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect operation of the PCI 9054, but is used for system status). When mapped into I/O space, it is included with bits [31:2] to indicate the decoding range.	Yes	Yes	0
31:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 0. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits that must be included in decode and 0 to all others (used in conjunction with PCIBAR2). Default is 1 MB. ***Notes:*** *Range (**not** Range register) must be power of 2.* *"Range register value" is inverse of range.* *User should limit all I/O spaces to 256 bytes per PCI v2.1 spec.*	Yes	Yes	FFF0000h

11.4.2 (LAS0BA; PCI:04h, LOC:84h) Local Address Space 0 Local Base Address (Remap) Register

Table 11-45. (LAS0BA; PCI:04h, LOC:84h) Local Address Space 0 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 0 Enable. Writing a 1 enables decoding of PCI addresses for Direct Slave access to Local Bus Space 0. Writing a 0 disables decoding.	Yes	Yes	0
1	Reserved.	Yes	No	0
3:2	If Local Bus Space 0 is mapped into Memory space, bits are not used. When mapped into I/O space, included with bits [31:4] for remapping.	Yes	Yes	00
31:4	Remap PCI Address to Local Address Space 0 into Local Address Space. Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h

11.4.3 (MARBR; PCI:08h or ACh, LOC:88h or 12Ch) Mode/DMA Arbitration Register

Table 11-46. (MARBR; PCI:08h or ACh, LOC:88h or 12Ch) Mode/DMA Arbitration Register

Bit	Description	Read	Write	Value after Reset
7:0	Local Bus Latency Timer. The number of Local Bus clock cycles to occur before de-asserting HOLD and releasing the Local Bus.	Yes	Yes	0h
15:8	Local Bus Pause Timer. Number of Local Bus Clock cycles to occur before reasserting HOLD after releasing the Local Bus. The pause timer is valid only during DMA.	Yes	Yes	0h
16	Local Bus Latency Timer Enable. Writing a 1 enables the latency timer. Writing a 0 disables the latency timer.	Yes	Yes	0
17	Local Bus Pause Timer Enable. Writing a 1 enables the pause timer. Writing a 0 disables the pause timer.	Yes	Yes	0
18	Local Bus BREQ Enable. Writing a 1 enables the Local Bus BREQi. When BREQi is active, the PCI 9054 de-asserts HOLD and releases the Local Bus.	Yes	Yes	0
20:19	DMA Channel Priority. Writing a 00 indicates a rotational priority scheme. Writing a 01 indicates Channel 0 has priority. Writing a 10 indicates Channel 1 has priority. Writing a 11 is reserved.	Yes	Yes	00
21	Local Bus Direct Slave Release Bus Mode. When set to 1, the PCI 9054 de-asserts HOLD and releases the Local Bus when the Direct Slave Write FIFO becomes empty during a Direct Slave Write or when the Direct Slave Read FIFO becomes full during a Direct Slave Read.	Yes	Yes	1
22	Direct Slave LOCK# Enable. Writing a 1 enables PCI Direct Slave locked sequences. Writing a 0 disables Direct Slave locked sequences.	Yes	Yes	0
23	PCI Request Mode. Writing a 1 causes the PCI 9054 to de-assert REQ when it asserts FRAME during a Master cycle. Writing a 0 causes the PCI 9054 to leave REQ asserted for the entire Bus Master cycle.	Yes	Yes	0
24	Delayed Read Mode. When set to 1, the PCI 9054 operates in Delayed Transaction mode for Direct Slave reads. The PCI 9054 issues a Retry to the PCI Host and prefetches Read data.	Yes	Yes	0
25	PCI Read No Write Mode. Writing a 1 forces a Retry on writes if a read is pending. Writing a 0 allows writes to occur while a read is pending.	Yes	Yes	0
26	PCI Read with Write Flush Mode. Writing a 1 submits a request to flush a pending Read cycle if a Write cycle is detected. Writing a 0 submits a request to not effect pending reads when a Write cycle occurs (PCI Specification v2.1 compatible).	Yes	Yes	0
27	Gate Local Bus Latency Timer with BREQi. Applies to C and J modes only.	Yes	Yes	0
28	PCI Read No Flush Mode. Writing a 1 submits a request to not flush the Read FIFO if the PCI Read cycle completes (Read Ahead mode). Writing a 0 submits a request to flush the Read FIFO if a PCI Read cycle completes.	Yes	Yes	0
29	When set to 0, reads from the PCI Configuration Register address 00h return Device ID and Vendor ID. When set to 1, reads from the PCI Configuration register address 00h and returns Subsystem ID and Subsystem Vendor ID.	Yes	Yes	0
30	When set to 1, the Direct Master Write FIFO is almost full. Reflects the value of the DMPAF pin.	Yes	No	0
31	BIGEND#/WAIT# Input/Output Select (M mode only). Writing a 1 selects the wait functionality of the signal. Writing a 0 selects Big Endian input functionality.	Yes	Yes	0

11.4.4 (BIGEND; PCI:0Ch, LOC:8Ch) Big/Little Endian Descriptor Register

Table 11-47. (BIGEND; PCI:0Ch, LOC:8Ch) Big/Little Endian Descriptor Register

Bit	Description	Read	Write	Value after Reset
0	Configuration Register Big Endian Mode (Address Invariance). Writing a 1 specifies use of Big Endian data ordering for Local accesses to the Configuration registers. Writing a 0 specifies Little Endian ordering. Big Endian mode can be specified for Configuration register accesses by asserting BIGEND# during Address phase of access.	Yes	Yes	0
1	Direct Master Big Endian Mode (Address Invariance). Writing a 1 specifies use of Big Endian data ordering for Direct Master accesses. Writing a 0 specifies Little Endian ordering. Big Endian mode can be specified for Direct Master accesses by asserting BIGEND# input pin during Address phase of the access.	Yes	Yes	0
2	Direct Slave Address Space 0 Big Endian Mode (Address Invariance). Writing a 1 specifies use of Big Endian data ordering for Direct Slave accesses to Local Address Space 0. Writing a 0 specifies Little Endian ordering.	Yes	Yes	0
3	Direct Slave Address Expansion ROM 0 Big Endian Mode (Address Invariance). Writing a 1 specifies use of Big Endian data ordering for Direct Slave accesses to Expansion ROM. Writing a 0 specifies Little Endian ordering.	Yes	Yes	0
4	Big Endian Byte Lane Mode. Writing a 1 specifies that in any Endian mode, use byte lanes [31:16] for a 16-bit Local Bus and byte lanes [31:24] for an 8-bit Local Bus. Writing a 0 specifies that in any Endian mode, use byte lanes [15:0] for a 16-bit Local Bus and byte lanes [7:0] for an 8-bit Local Bus.	Yes	Yes	0
5	Direct Slave Address Space 1 Big Endian Mode (Address Invariance). Writing a 1 specifies use of Big Endian data ordering for Direct Slave accesses to Local Address Space 1. Writing a 0 specifies Little Endian ordering.	Yes	Yes	0
6	DMA Channel 1 Big Endian Mode (Address Invariance). Writing a 1 specifies use of Big Endian data ordering for DMA Channel 1 accesses to the Local Address space. Writing a 0 specifies Little Endian ordering.	Yes	Yes	0
7	DMA Channel 0 Big Endian Mode (Address Invariance). Writing a 1 specifies use of Big Endian data ordering for DMA Channel 0 accesses to the Local Address space. Writing a 0 specifies Little Endian ordering.	Yes	Yes	0

11.4.5 (LMISC; PCI:0Dh, LOC:8Dh) Local Miscellaneous Control Register

Table 11-48. (LMISC; PCI:0Dh, LOC:8Dh) Local Miscellaneous Control Register

Bit	Description	Read	Write	Value after Reset
0	Base Address Register 1 Enable. If set to 1, the Base Address 1 Register for I/O accesses to Configuration registers is enabled. If set to 0, the Base Address 1 Register for I/O accesses to Configuration registers is disabled.	Yes	Yes	1
1	Base Address Register 1 Shift. If Base Address Register 1 Enable is low, and this bit is set to 0, then PCIBAR2 and PCIBAR3 remain at PCI configuration addresses 18h and 1Ch. If Base Address Register 1 Enable is low, and this bit is set to 1, then PCIBAR2 (Local Address Space 0) and PCIBAR3 (Local Address Space 1) are shifted to become PCIBAR1 and PCIBAR2 at PCI configuration addresses 14h and 18h. Set if hole in Base Address Register Space could not be accepted by system BIOS.	Yes	Yes	0
2	Local Init Status. Writing a 1 indicates Local Init done. Responses to PCI accesses are Retrys until this bit is set. If the PCI 9054 has a blank serial EEPROM attached, the Local processor must set the Local Init Status bit to 1.	Yes	Local/ Serial EEPROM	0
3	Reserved.	Yes	No	0
4	M Mode Direct Master Deferred Read Enable. Writing a 1 enables the PCI 9054 to operate in Delayed Transaction mode for Direct Master reads. The PCI 9054 issues a RETRY# to the M mode Master and prefetches Read data from the PCI Bus.	Yes	Yes	0
5	TEA# Input Interrupt Mask. When set to 1, TEA# input causes SERR# output on the PCI Bus if enabled (PCICR[8]=1) and the Signaled System Error bit is set (PCISR[14]=1). Writing 0 masks the TEA# input to create SERR#. The SERR# Status bit is set in both cases.	Yes	Yes	0
6	Direct Master Write FIFO Almost Full RETRY# Output Enable. When set to 1, the PCI 9054 issues a RETRY# to the MPC850 or MPC860.	Yes	Yes	0
7	Reserved.	Yes	No	0

11.4.6 (PROT_AREA; PCI:0Eh, LOC:8Eh) Serial EEPROM Write-Protected Address Boundary Register

Table 11-49. (PROT_AREA; PCI:0Eh, LOC:8Eh) Serial EEPROM Write-Protected Address Boundary Register

Bit	Description	Read	Write	Value after Reset
6:0	Serial EEPROM Starting at Lword Boundary (48 Lwords = 192 bytes) for VPD Accesses. Any serial EEPROM address below this boundary is read-only. ***Note:*** *Anything below the programmed address may contain the PCI 9054 Configuration data.*	Yes	Yes	0110000
15:7	Reserved.	Yes	No	0h

11.4.7 (EROMRR; PCI:10h, LOC:90h) Expansion ROM Range Register

Table 11-50. (EROMRR; PCI:10h, LOC:90h) Expansion ROM Range Register

Bit	Description	Read	Write	Value after Reset
0	Address Decode Enable. Bit 0 can only be enabled from the serial EEPROM. To disable, set PCI Expansion ROM Address Decode Enable bit to 0 (PCIERBAR[0]=0).	Yes	Serial EEPROM Only	0
10:1	Reserved.	Yes	No	0h
31:11	Specifies which PCI Address bits to use for decoding a PCI-to-Local Bus Expansion ROM. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits that must be included in decode and 0 to all others (used in conjunction with PCIERBAR). Default is 64 kilobits. ***Note:*** *Range (**not** Range register) must be power of 2. "Range register value" is inverse of range.*	Yes	Yes	FFFF00h

11.4.8 (EROMBA; PCI:14h, LOC:94h) Expansion ROM Local Base Address (Remap) and BREQo Control Registers

Table 11-51. (EROMBA; PCI:14h, LOC:94h) Expansion ROM Local Base Address (Remap) and BREQo Control Registers

Bit	Description	Read	Write	Value after Reset
3:0	**M Mode:** RETRY# Signal Assertion Delay Clocks. Number of Local Bus clocks in which a Direct Slave BR# request is pending and a Local Direct Master access is in progress and not being granted the bus BG# before asserting RETRY#. Once asserted, RETRY# remains asserted until PCI 9054 samples de-assertion of BB# by the Local Arbiter (Least Significant Bit is 8 or 64 clocks). **C and J Modes:** Backoff Request Delay Clocks. Number of Local Bus clocks in which a Direct Slave HOLD request is pending and a Local Direct Master access is in progress and not being granted the bus (LHOLDA) before asserting BREQo (Backoff Request Out). BREQo remains asserted until PCI 9054 receives LHOLDA (Least Significant Bit is 8 or 64 clocks).	Yes	Yes	0h
4	Local Bus Backoff Enable. Writing a 1 enables the PCI 9054 to assert BREQo.	Yes	Yes	0
5	Backoff Timer Resolution. Writing a 1 changes the Least Significant Bit of the Backoff Timer from 8 to 64 clocks.	Yes	Yes	0
10:6	Reserved.	Yes	No	0h
31:11	Remap PCI Expansion ROM Space into Local Address Space. Bits in this register remap (replace) the PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h

11.4.9 (LBRD0; PCI:18h, LOC:98h) Local Address Space 0/Expansion ROM Bus Region Descriptor Register

Table 11-52. (LBRD0; PCI:18h, LOC:98h) Local Address Space 0/Expansion ROM Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
1:0	Memory Space 0 Local Bus Width. Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
5:2	Memory Space 0 Internal Wait States (data to data; 0-15 wait states).	Yes	Yes	0h
6	Memory Space 0 TA#/READY# Input Enable. Writing a 1 enables TA#/READY# input. Writing a 0 disables TA#/READY# input.	Yes	Yes	1
7	Memory Space 0 BTERM# Input Enable. Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.5 for M mode, or to Section 4.2.5 for C and J modes.	Yes	Yes	0
8	Memory Space 0 Prefetch Disable. When mapped into Memory space, writing a 0 enables Read prefetching. Writing a 1 disables prefetching. If prefetching is disabled, the PCI 9054 disconnects after each Memory read.	Yes	Yes	0
9	Expansion ROM Space Prefetch Disable. Writing a 0 enables Read prefetching. Writing a 1 disables prefetching. If prefetching is disabled, the PCI 9054 disconnects after each Memory read.	Yes	Yes	0
10	Prefetch Counter Enable. When set to 1 and Memory prefetching is enabled, the PCI 9054 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9054 ignores the count and continues prefetching until it is terminated by the PCI Bus.	Yes	Yes	0
14:11	Prefetch Counter. Number of Lwords to prefetch during Memory Read cycles (0-15). A count of zero selects a prefetch of 16 Lwords.	Yes	Yes	0h
15	Reserved.	Yes	No	0
17:16	Expansion ROM Space Local Bus Width. Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
21:18	Expansion ROM Space Internal Wait States (data to data; 0-15 wait states).	Yes	Yes	0h
22	Expansion ROM Space TA#/READY# Input Enable. Writing a 1 enables TA#/READY# input. Writing a 0 disables TA#/READY# input.	Yes	Yes	1
23	Expansion ROM Space BTERM# Input Enable. Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.5 for M mode or to Section 4.2.5 for C and J modes.	Yes	Yes	0
24	Memory Space 0 Burst Enable. Writing a 1 enables bursting. Writing a 0 disables bursting.	Yes	Yes	0
25	Extra Long Load from Serial EEPROM. Writing a 1 loads the Subsystem ID and Local Address Space 1 registers. Writing a 0 indicates not to load them.	Yes	Serial EEPROM Only	0
26	Expansion ROM Space Burst Enable. Writing a 1 enables bursting. Writing a 0 disables bursting.	Yes	Yes	0
27	Direct Slave PCI Write Mode. Writing a 0 indicates the PCI 9054 should disconnect when the Direct Slave Write FIFO is full. Writing a 1 indicates the PCI 9054 should de-assert TRDY# when the Direct Slave Write FIFO is full.	Yes	Yes	0
31:28	PCI Target Retry Delay Clocks. Contains the value (multiplied by 8) of the number of PCI Bus clocks after receiving a PCI-to-Local Read or Write access and not successfully completing a transfer. Pertains only to Direct Slave writes when the Direct Slave PCI Write Mode bit is set (LBRD0[27]=1).	Yes	Yes	4h (32 clocks)

11.4.10 (DMRR; PCI:1Ch, LOC:9Ch) Local Range Register for Direct Master-to-PCI

Table 11-53. (DMRR; PCI:1Ch, LOC:9Ch) Local Range Register for Direct Master-to-PCI

Bit	Description	Read	Write	Value after Reset
15:0	Reserved (64-kilobit increments).	Yes	No	0h
31:16	Specifies which Local Address bits to use for decoding a Local-to-PCI Bus access. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits that must be included in decode and 0h to all others. ***Note:*** *Range (**not** Range register) must be power of 2. "Range register value" is inverse of range.*	Yes	Yes	0h

11.4.11 (DMLBAM; PCI:20h, LOC:A0h) Local Bus Base Address Register for Direct Master-to-PCI Memory

Table 11-54. (DMLBAM; PCI:20h, LOC:A0h) Local Bus Base Address Register for Direct Master-to-PCI Memory

Bit	Description	Read	Write	Value after Reset
15:0	Reserved.	Yes	No	0h
31:16	Assigns a value to bits to use for decoding Local-to-PCI Memory accesses. ***Note:*** *Local Base Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h

11.4.12 (DMLBAI; PCI:24h, LOC:A4h) Local Base Address Register for Direct Master-to-PCI I/O Configuration

Table 11-55. (DMLBAI; PCI:24h, LOC:A4h) Local Base Address Register for Direct Master-to-PCI I/O Configuration

Bit	Description	Read	Write	Value after Reset
15:0	Reserved.	Yes	No	0h
31:16	Assigns a value to bits to use for decoding Local-to-PCI I/O or Configuration accesses. ***Notes:*** *Local Base Address value must be a multiple of the Range (**not** the Range register).* *Refer to DMPBAM[13] for the I/O Remap Address option.*	Yes	Yes	0h

11.4.13 (DMPBAM; PCI:28h, LOC:A8h) PCI Base Address (Remap) Register for Direct Master-to-PCI Memory

Table 11-56. (DMPBAM; PCI:28h, LOC:A8h) PCI Base Address (Remap) Register for Direct Master-to-PCI Memory

Bit	Description	Read	Write	Value after Reset
0	Direct Master Memory Access Enable. Writing a 1 enables decode of Direct Master Memory accesses. Writing a 0 disables decode of Direct Master Memory accesses.	Yes	Yes	0
1	Direct Master I/O Access Enable. Writing a 1 enables decode of Direct Master I/O accesses. Writing a 0 disables decode of Direct Master I/O accesses.	Yes	Yes	0
2	Direct Master Cache Enable. Writing a 1 causes prefetch to occur infinitely.	Yes	Yes	0
12, 3	Direct Master Read Prefetch Size Control. Values: 00 = PCI 9054 continues to prefetch Read data from the PCI Bus until the Direct Master access is finished. This may result in an additional four unneeded Lwords being prefetched from the PCI Bus. 01 = Prefetch up to four Lwords from the PCI Bus 10 = Prefetch up to eight Lwords from the PCI Bus 11 = Prefetch up to 16 Lwords from the PCI Bus Direct Master Burst reads should not exceed programmed limit.	Yes	Yes	00
4	Direct Master PCI Read Mode. Writing a 0 indicates the PCI 9054 should release the PCI Bus when the Read FIFO becomes full. Writing a 1 indicates the PCI 9054 should keep the PCI Bus and de-assert IRDY when the Read FIFO becomes full.	Yes	Yes	0
10, 8:5	Programmable Almost Full Flag. When the number of entries in the 32-word Direct Master Write FIFO exceeds this value, the MDREQ#/DMPAF signal is asserted high.	Yes	Yes	00000
9	Memory Write and Invalidate Mode. When set to 1, the PCI 9054 waits for 8 or 16 Lwords to be written from the Local Bus before starting PCI access. In addition, all Memory Write and Invalidate cycles to the PCI Bus must be 8 or 16 Lword bursts.	Yes	Yes	0
11	Direct Master Prefetch Limit. Writing a 1 causes the PCI 9054 to not prefetch past 4-KB boundaries.	Yes	Yes	0
13	I/O Remap Select. Writing a 1 forces PCI Address bits [31:16] to all zeros. Writing a 0 uses bits [31:16] of this register as PCI Address bits [31:16].	Yes	Yes	0
15:14	Direct Master Write Delay. Delays PCI Bus request after Direct Master Burst Write cycle has started. Values: 00 = No delay; start cycle immediately 01 = Delay 4 PCI clocks 10 = Delay 8 PCI clocks 11 = Delay 16 PCI clocks	Yes	Yes	00
31:16	Remap Local-to-PCI Space into PCI Address Space. Bits in these register remap (replace) Local Address bits used in decode as the PCI Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h

11.4.14 (DMCFGA; PCI:2Ch, LOC:ACh) PCI Configuration Address Register for Direct-Master-to-PCI I/O Configuration

Table 11-57. (DMCFGA; PCI:2Ch, LOC:ACh) PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration

Bit	Description	Read	Write	Value after Reset
1:0	Configuration Type (00=Type 0, 01=Type 1).	Yes	Yes	00
7:2	Register Number.	Yes	Yes	0
10:8	Function Number.	Yes	Yes	0
15:11	Device Number.	Yes	Yes	0
23:16	Bus Number.	Yes	Yes	0h
30:24	Reserved.	Yes	No	0h
31	Configuration Enable. Writing a 1 allows Local-to-PCI I/O accesses to be converted to a PCI Configuration cycle. Parameters in this table are used to assert the PCI Configuration address. ***Note:*** *For more information, refer to the Direct Master Configuration Cycle example in Section 3.4.1.7.1 for M mode, or in Section 5.4.1.6.1 for C and J modes.*	Yes	Yes	0

11.4.15 (LAS1RR; PCI:F0h, LOC:170h) Local Address Space 1 Range Register for PCI-to-Local Bus

Table 11-58. (LAS1RR; PCI:F0h, LOC:170h) Local Address Space 1 Range Register for PCI-to-Local Bus

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Writing a 0 indicates Local Address Space 1 maps into PCI Memory space. Writing a 1 indicates Address Space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 2/1 Meaning 0 0 Locate anywhere in 32-bit PCI Address space 0 1 Locate below 1 MB in PCI Address space 1 0 Locate anywhere in 64-bit PCI Address space 1 1 Reserved When mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [31:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory space, writing a 1 indicates reads are prefetchable (does not affect operation of the PCI 9054, but is used for system status). When mapped into I/O space, included with bits [31:2] to indicate the decoding range.	Yes	Yes	0
31:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 1. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write 1 to all bits that must be included in decode and 0 to all others. (Used in conjunction with PCIBAR3.) Default is 1 MB. ***Notes:*** *Range (**not** Range register) must be power of 2.* *"Range register value" is inverse of range.* *User should limit all I/O spaces to 256 bytes per PCI Specification v2.1.* *If QSR[0]=1, defines PCI Base Address 0.*	Yes	Yes	FFF0000h

11.4.16 (LAS1BA; PCI:F4h, LOC:174h) Local Address Space 1 Local Base Address (Remap) Register

Table 11-59. (LAS1BA; PCI:F4h, LOC:174h) Local Address Space 1 Local Base Address (Remap) Register

Bit	Description	Read	Write	Value after Reset
0	Space 1 Enable. Writing a 1 enables decoding of PCI addresses for Direct Slave access to Local Bus Space 1. Writing a 0 disables decoding.	Yes	Yes	0
1	Reserved.	Yes	No	0
3:2	Not used if Local Bus Space 1 is mapped into Memory space. Included with bits [31:4] for remapping when mapped into I/O space.	Yes	Yes	00
31:4	Remap PCI Address to Local Address Space 1 into Local Address Space. Bits in this register remap (replace) the PCI Address bits used in decode as Local Address bits. ***Note:*** *Remap Address value must be a multiple of the Range (**not** the Range register).*	Yes	Yes	0h

11.4.17 (LBRD1; PCI:F8h, LOC:178h) Local Address Space 1 Bus Region Descriptor Register

Table 11-60. (LBRD1; PCI:F8h, LOC:178h) Local Address Space 1 Bus Region Descriptor Register

Bit	Description	Read	Write	Value after Reset
1:0	Memory Space 1 Local Bus Width. Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
5:2	Memory Space 1 Internal Wait States (data to data; 0-15 wait states).	Yes	Yes	0h
6	Memory Space 1 TA#/READY# Input Enable. Writing a 1 enables TA#/READY# input. Writing a 0 disables TA#/READY# input.	Yes	Yes	1
7	Memory Space 1 BTERM# Input Enable. Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.5 for M mode, or to Section 4.2.5 for C and J modes.	Yes	Yes	0
8	Memory Space 1 Burst Enable. Writing a 1 enables bursting. Writing a 0 disables bursting.	Yes	Yes	0
9	Memory Space 1 Prefetch Disable. When mapped into Memory space, writing a 0 enables Read prefetching. Writing a 1 disables prefetching. If prefetching is disabled, the PCI 9054 disconnects after each Memory read.	Yes	Yes	0
10	Read Prefetch Count Enable. When set to 1 and Memory prefetching is enabled, the PCI 9054 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9054 ignores the count and continues prefetching until it is terminated by the PCI Bus.	Yes	Yes	0
14:11	Pread Prefetch Count. Number of Lwords to prefetch during Memory Read cycles (0-15).	Yes	Yes	0h
31:15	Reserved.	Yes	No	0h

11.4.18 (DMDAC; PCI:FCh, LOC:17Ch) Direct Master PCI Dual Address Cycle Register

Table 11-61. (DMDAC; PCI:FCh, LOC:17Ch) Direct Master PCI Dual Address Cycle Register

Bit	Description	Read	Write	Value after Reset
31:0	Upper 32 bits of PCI Dual Address Cycle PCI address during Direct Master cycles. If set to 0, the PCI 9054 performs 32-bit Direct Master address access.	Yes	Yes	0h

11.5 Runtime Registers

11.5.1 (MBOX0; PCI:40h or 78h, LOC:C0h) Mailbox Register 0

Table 11-62. (MBOX0; PCI:40h or 78h, LOC:C0h) Mailbox Register 0

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register. ***Note:*** *Inbound Queue Port replaces Mailbox Register 0 when the I_2O function is enabled (QSR[0]=1). Mailbox Register 0 is always accessible at PCI address 78h and Local address C0h*	Yes	Yes	0h

11.5.2 (MBOX1; PCI:44h or 7Ch, LOC:C4h) Mailbox Register 1

Table 11-63. (MBOX1; PCI:44h or 7Ch, LOC:C4h) Mailbox Register 1

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register. ***Note:*** *Mailbox Register 1 is replaced by Outbound Queue Port when the I_2O function is enabled (QSR[0]=1). Mailbox Register 1 is always accessible at PCI address 7Ch and Local address C4h.*	Yes	Yes	0h

11.5.3 (MBOX2; PCI:48h, LOC:C8h) Mailbox Register 2

Table 11-64. (MBOX2; PCI:48h, LOC:C8h) Mailbox Register 2

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0h

11.5.4 (MBOX3; PCI:4Ch, LOC:CCh) Mailbox Register 3

Table 11-65. (MBOX3; PCI:4Ch, LOC:CCh) Mailbox Register 3

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0h

11.5.5 (MBOX4; PCI:50h, LOC:D0h) Mailbox Register 4

Table 11-66. (MBOX4; PCI:50h, LOC:D0h) Mailbox Register 4

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0h

11.5.6 (MBOX5; PCI:54h, LOC:D4h) Mailbox Register 5

Table 11-67. (MBOX5; PCI:54h, LOC:D4h) Mailbox Register 5

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0h

11.5.7 (MBOX6; PCI:58h, LOC:D8h) Mailbox Register 6

Table 11-68. (MBOX6; PCI:58h, LOC:D8h) Mailbox Register 6

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0h

11.5.8 (MBOX7; PCI:5Ch, LOC:DCh) Mailbox Register 7

Table 11-69. (MBOX7; PCI:5Ch, LOC:DCh) Mailbox Register 7

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0h

11.5.9 (P2LDBELL; PCI:60h, LOC:E0h) PCI-to-Local Doorbell Register

Table 11-70. (P2LDBELL; PCI:60h, LOC:E0h) PCI-to-Local Doorbell Register

Bit	Description	Read	Write	Value after Reset
31:0	Doorbell Register. The PCI Bus Master can write to this register and assert a Local interrupt to the Local processor. The Local processor can then read this register to determine which doorbell bit was set. The PCI Bus Master sets the doorbell by writing a 1 to a particular bit. The Local processor can clear a doorbell bit by writing a 1 to that bit position.	Yes	Yes/Clr	0h

11.5.10 (L2PDBELL; PCI:64h, LOC:E4h) Local-to-PCI Doorbell Register

Table 11-71. (L2PDBELL; PCI:64h, LOC:E4h) Local-to-PCI Doorbell Register

Bit	Description	Read	Write	Value after Reset
31:0	Doorbell Register. The Local processor can write to this register and assert a PCI interrupt. The PCI Bus Master can then read this register to determine which doorbell bit was set. The Local processor sets the doorbell by writing a 1 to a particular bit. The PCI Bus Master can clear a doorbell bit by writing a 1 to that bit position.	Yes	Yes/Clr	0h

11.5.11 (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status Register

Table 11-72. (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status Register

Bit	Description	Read	Write	Value after Reset
0	Enable Local Bus TEA#/LSERR#. Writing a 1 enables PCI 9054 to assert TEA#/LSERR# interrupt when the PCI Bus Target Abort bit is set (PCISR[11]=1) or the Received Master Abort bit is set (PCISR[13]=1 or INTCSR[6]=1).	Yes	Yes	0
1	Enable Local Bus TEA#/LSERR# when a PCI parity error occurs during a PCI 9054 Master Transfer or a PCI 9054 Slave access.	Yes	Yes	0
2	Generate PCI Bus SERR# Interrupt. When set to 0, writing 1 asserts the PCI Bus SERR# interrupt.	Yes	Yes	0
3	Mailbox Interrupt Enable. Writing a 1 enables a Local Interrupt to be asserted when the PCI Bus writes to MBOX0 through MBOX3. To clear a Local Interrupt, the Local Bus Master must read the Mailbox. Used in conjunction with the Local Interrupt Output Enable bit (INTCSR[16]).	Yes	Yes	0
4	Power Management Interrupt Enable. Writing a 1 enables a Local Interrupt to be asserted when the Power Management Power State changes.	Yes	Yes	0
5	Power Management Interrupt. When set to 1, indicates a Power Management Interrupt is pending. A Power Management interrupt is caused by a change in the Power State register (PMCSR). Writing a 1 clears the interrupt.	Yes	Yes/Clr	0
6	Direct Master Write/Direct Slave Read Local Data Parity Check Error Enable. Writing a 1 enables a Local Data Parity error signal to be asserted through the LSERR#/TEA# pin. INTCSR[0] must be enabled for this to have an effect.	Yes	Yes	0
7	Direct Master Write/Direct Slave Read Local Data Parity Check Error Status. When set to 1, indicates the PCI 9054 has detected a Local Data Parity check error, even if the Check Parity Error bit is disabled. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
8	PCI Interrupt Enable. Writing a 1 enables PCI interrupts.	Yes	Yes	1
9	PCI Doorbell Interrupt Enable. Writing a 1 enables doorbell interrupts. Used in conjunction with the PCI Interrupt Enable bit (INTCSR[8]). Clearing the doorbell interrupt bits that caused the interrupt also clears the interrupt.	Yes	Yes	0
10	PCI Abort Interrupt Enable. Values of 1 enables Master abort or Master detect of a Target Abort to assert a PCI interrupt. Used in conjunction with the PCI Interrupt Enable bit (INTCSR[8]). Clearing the abort status bits also clears the PCI interrupt.	Yes	Yes	0
11	Local Interrupt Input Enable. Writing a 1 enables a Local interrupt input to assert a PCI interrupt. Used in conjunction with the PCI Interrupt Enable bit (INTCSR[8]). Clearing the Local Bus cause of the interrupt also clears the interrupt.	Yes	Yes	0
12	Retry Abort Enable. Writing a 1 enables the PCI 9054 to treat 256 Master consecutive Retrys to a Target as a Target Abort. Writing a 0 enables the PCI 9054 to attempt Master Retrys indefinitely.	Yes	Yes	0
13	PCI Doorbell Interrupt Active. When set to 1, indicates the PCI Doorbell interrupt is active.	Yes	No	0
14	PCI Abort Interrupt Active. When set to 1, indicates the PCI Abort interrupt is active.	Yes	No	0
15	Local Input Interrupt Active. When set to 1, indicates the Local Input interrupt is active.	Yes	No	0
16	Local Interrupt Output Enable. Writing a 1 enables Local interrupt output. Used in conjunction with the Mailbox Interrupt Enable bit (INTCSR[3]).	Yes	Yes	1
17	Local Doorbell Interrupt Enable. Writing a 1 enables Doorbell interrupts. Used in conjunction with the Local Interrupt Enable bit. Clearing the Local Doorbell Interrupt bits that caused the interrupt also clears the interrupt.	Yes	Yes	0

Table 11-72. (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status (continued)

Bit	Description	Read	Write	Value after Reset
18	Local DMA Channel 0 Interrupt Enable. Writing a 1 enables DMA Channel 0 interrupts. Used in conjunction with the Local Interrupt Enable bit. Clearing the DMA status bits also clears the interrupt.	Yes	Yes	0
19	Local DMA Channel 1 Interrupt Enable. Writing a 1 enables DMA Channel 1 interrupts. Used in conjunction with the Local Interrupt Enable bit. Clearing the DMA status bits also clears the interrupt.	Yes	Yes	0
20	Local Doorbell Interrupt Active. Reading a 1 indicates the Local Doorbell interrupt is active.	Yes	No	0
21	DMA Channel 0 Interrupt Active. Reading a 1 indicates the DMA Ch 0 interrupt is active.	Yes	No	0
22	DMA Channel 1 Interrupt Active. Reading a 1 indicates the DMA Ch 1 interrupt is active.	Yes	No	0
23	BIST Interrupt Active. Reading a 1 indicates the BIST interrupt is active. The BIST (built-in self test) interrupt is asserted by writing a 1 to bit 6 of the PCI Configuration BIST register. Clearing bit 6 clears the interrupt. Refer to the PCIBISTR register for a description of the self test.	Yes	No	0
24	Reading a 0 indicates the Direct Master was the Bus Master during a Master or Target Abort.	Yes	No	1
25	Reading a 0 indicates DMA CH 0 was the Bus Master during a Master or Target Abort.	Yes	No	1
26	Reading a 0 indicates DMA CH 1 was the Bus Master during a Master or Target Abort.	Yes	No	1
27	Reading a 0 indicates a Target Abort was asserted by the PCI 9054 after 256 consecutive Master retries to a Target.	Yes	No	1
28	Reading a 1 indicates the PCI Bus wrote data to MBOX0. Enabled only if the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
29	Reading a 1 indicates the PCI Bus wrote data to MBOX1. Enabled only if the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
30	Reading a 1 indicates the PCI Bus wrote data to MBOX2. Enabled only if the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
31	Reading a 1 indicates the PCI Bus wrote data to MBOX3. Enabled only if the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0

11.5.12 (CNTRL; PCI:6Ch, LOC:ECh) Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control Register

Table 11-73. (CNTRL; PCI:6Ch, LOC:ECh) Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control Register

Bit	Description	Read	Write	Value after Reset
3:0	PCI Read Command Code for DMA.	Yes	Yes	1110
7:4	PCI Write Command Code for DMA.	Yes	Yes	0111
11:8	PCI Memory Read Command Code for Direct Master.	Yes	Yes	0110
15:12	PCI Memory Write Command Code for Direct Master.	Yes	Yes	0111
16	General Purpose Output. Writing a 1 causes USERo output to go high. Writing a 0 causes USERo output to go low.	Yes	Yes	1
17	General Purpose Input. Writing a 1 indicates the USERi input pin is high. Writing a 0 indicates the USERi pin is low.	Yes	No	—
18	Writing a 1 selects USERi to be an input to the chip. Writing a 0 selects LLOCKi as an input. Enables the user to select between the USERi and LLOCKi# functions when USERi is chosen to be an input. DMAMODE0[12] and/or DMAMODE1[12] are select bit(s) for the pin.	Yes	Yes	1
19	Writing a 1 selects USERo to be an output from the chip. Writing a 0 selects LLOCKo# as an output. Enables the user to select between the USERo and LLOCKo# functions when USERo is chosen to be an output. DMAMODE0[12] and/or DMAMODE1[12] are select bit(s) for the pin.	Yes	Yes	1
23:20	Reserved.	Yes	No	0h
24	Serial EEPROM Clock for Local or PCI Bus Reads or Writes to Serial EEPROM. Toggling this bit asserts the serial EEPROM clock. (Refer to manufacturer's data sheet for particular serial EEPROM being used.)	Yes	Yes	0
25	Serial EEPROM Chip Select. For Local or PCI Bus reads or writes to the serial EEPROM, setting this bit to 1 provides the serial EEPROM chip select.	Yes	Yes	0
26	Write Bit to Serial EEPROM. For writes, this output bit is input to the serial EEPROM. Clocked into the serial EEPROM by the serial EEPROM clock.	Yes	Yes	0
27	Reserved. Refer to Section 2.4.2.1 for M mode, or to Section 4.4.2.1 for C and J modes.	Yes	No	—
28	Programmed Serial EEPROM Present. When set to 1, indicates that a programmed serial EEPROM is present.	Yes	No	0
29	Reload Configuration Registers. When set to 0, writing a 1 causes the PCI 9054 to reload the Local Configuration registers from the serial EEPROM.	Yes	Yes	0
30	PCI Adapter Software Reset. Writing a 1 holds the PCI 9054 Local Bus logic in a reset state, and asserts LRESETo# output. Contents of the PCI Configuration registers and the Shared Runtime registers are not reset. A software reset can only be cleared from the PCI Bus.	Yes	Yes	0
31	Reserved.	Yes	No	0

11.5.13 (PCIHIDR; PCI:70h, LOC:F0h) PCI Hardcoded Configuration ID Register

Table 11-74. (PCIHIDR; PCI:70h, LOC:F0h) PCI Hardcoded Configuration ID Register

Bit	Description	Read	Write	Value after Reset
15:0	Vendor ID. Identifies manufacturer of device. Hardcoded to the PCI SIG issued Vendor ID of PLX (10B5h).	Yes	No	10B5h
31:16	Device ID. Identifies particular device. Hardcoded to the PLX part number for PCI interface chip 9054h.	Yes	No	9054h

11.5.14 (PCIHREV; PCI:74h, LOC:F4h) PCI Hardcoded Revision ID Register

Table 11-75. (PCIHREV; PCI:74h, LOC:F4h) PCI Hardcoded Revision ID Register

Bit	Description	Read	Write	Value after Reset
7:0	Revision ID. Hardcoded silicon revision of the PCI 9054.	Yes	No	Current Rev #

11.6 DMA Registers

11.6.1 (DMAMODE0; PCI:80h, LOC:100h) DMA Channel 0 Mode Register

Table 11-76. (DMAMODE0; PCI:80h, LOC:100h) DMA Channel 0 Mode Register

Bit	Description	Read	Write	Value after Reset
1:0	Local Bus Width. Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
5:2	Internal Wait States (data to data).	Yes	Yes	0h
6	TA#/READY# Input Enable. Writing a 1 enables TA#/READY# input. Writing a 0 disables TA#/READY# input.	Yes	Yes	1
7	BTERM# Input Enable. Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.5 for M mode, or to Section 4.2.5 for C and J modes.	Yes	Yes	0
8	Local Burst Enable. Writing a 1 enables Local bursting. Writing a 0 disables Local bursting.	Yes	Yes	0
9	Scatter/Gather Mode. Writing a 1 indicates Scatter/Gather mode is enabled. For Scatter/Gather mode, DMA source address, destination address, and byte count are loaded from memory in PCI or Local Address spaces. Writing a 0 indicates Block mode is enabled.	Yes	Yes	0
10	Done Interrupt Enable. Writing a 1 enables an interrupt when done. Writing a 0 disables an interrupt when done. If DMA Clear Count mode is enabled, the interrupt does not occur until the byte count is cleared.	Yes	Yes	0
11	Local Addressing Mode. Writing a 1 holds the Local address bus constant. Writing a 0 indicates the Local address is incremented.	Yes	Yes	0
12	Demand Mode. Writing a 1 causes the DMA controller to operate in Demand mode, as well as to make USERo/DREQ0#/LLOCKo# to be an input (DREQ0#) and USERi/DACK0#/LLOCKi# to be an output (DACK0#). In Demand mode, the DMA controller transfers data when its DREQ0# input is asserted. Asserts DACK0# to indicate the current Local Bus transfer is in response to DREQ0# input. DMA controller transfers Lwords (32 bits) of data. This may result in multiple transfers for an 8- or 16-bit bus.	Yes	Yes	0
13	Memory Write and Invalidate Mode for DMA Transfers. When set to 1, the PCI 9054 performs Memory Write and Invalidate cycles to the PCI Bus. The PCI 9054 supports Memory Write and Invalidate sizes of 8 or 16 Lwords. Size is specified in the System Cache Line Size bits (PCICLSR[7:0]). If a size other than 8 or 16 is specified, the PCI 9054 performs Write transfers rather than Memory Write and Invalidate transfers. Transfers must start and end at Cache Line Boundaries.	Yes	Yes	0
14	DMA EOT# Enable. Writing a 1 enables the EOT# input pin. Writing a 0 disables the EOT# input pin.	Yes	Yes	0
15	Fast/Slow Terminate Mode Select. Writing a 0 sets PCI 9054 into the Slow Terminate mode. As a result in C or J modes, BLAST# is asserted on the last Data transfer to terminate DMA transfer. In M mode, BDIP# is de-asserted at the nearest 16-byte boundary and stops the DMA transfer. Writing a 1 indicates that if EOT# is asserted or DREQ0# is de-asserted in Demand mode during DMA will immediately terminate the DMA transfer. In M mode, writing a 1 indicates BDIP# output is disabled. As a result, the PCI 9054 DMA transfer terminates immediately when EOT# is asserted or when DREQ0# is de-asserted in Demand mode.	Yes	Yes	0
16	DMA Clear Count Mode. Writing a 1 clears the byte count in each Scatter/Gather descriptor when corresponding DMA transfer is complete.	Yes	Yes	0
17	DMA Channel 0 Interrupt Select. Writing a 1 routes the DMA Channel 0 interrupt to the PCI Bus interrupt. Writing a 0 routes the DMA Channel 0 interrupt to the Local Bus interrupt.	Yes	Yes	0
18	DAC Chain Load. When set to 1, enables the descriptor to load the PCI Dual Address Cycle value. Otherwise, it uses the contents of the register.	Yes	Yes	0
31:19	Reserved.	Yes	No	0

11.6.2 (DMAPADR0; PCI:84h, LOC:104h) DMA Channel 0 PCI Address Register

Table 11-77. (DMAPADR0; PCI:84h, LOC:104h) DMA Channel 0 PCI Address Register

Bit	Description	Read	Write	Value after Reset
31:0	PCI Address Register. Indicates from where in PCI Memory space DMA transfers (reads or writes) start.	Yes	Yes	0h

11.6.3 (DMALADR0; PCI:88h, LOC:108h) DMA Channel 0 Local Address Register

Table 11-78. (DMALADR0; PCI:88h, LOC:108h) DMA Channel 0 Local Address Register

Bit	Description	Read	Write	Value after Reset
31:0	Local Address Register. Indicates from where in Local Memory space DMA transfers (reads or writes) start.	Yes	Yes	0h

11.6.4 (DMASIZ0; PCI:8Ch, LOC:10Ch) DMA Channel 0 Transfer Size (Bytes) Register

Table 11-79. (DMASIZ0; PCI:8Ch, LOC:10Ch) DMA Channel 0 Transfer Size (Bytes) Register

Bit	Description	Read	Write	Value after Reset
22:0	DMA Transfer Size (Bytes). Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	0h
31:23	Reserved.	Yes	No	0h

11.6.5 (DMADPR0; PCI:90h, LOC:110h) DMA Channel 0 Descriptor Pointer Register

Table 11-80. (DMADPR0; PCI:90h, LOC:110h) DMA Channel 0 Descriptor Pointer Register

Bit	Description	Read	Write	Value after Reset
0	Descriptor Location. Writing a 1 indicates PCI Address space. Writing a 0 indicates Local Address space.	Yes	Yes	0
1	End of Chain. Writing a 1 indicates end of chain. Writing a 0 indicates not end of chain descriptor. (Same as Block mode.)	Yes	Yes	0
2	Interrupt after Terminal Count. Writing a 1 causes an interrupt to be asserted after the terminal count for this descriptor is reached. Writing a 0 disables interrupts from being asserted.	Yes	Yes	0
3	Direction of Transfer. Writing a 1 indicates transfers from the Local Bus to the PCI Bus. Writing a 0 indicates transfers from the PCI Bus to the Local Bus.	Yes	Yes	0
31:4	Next Descriptor Address. Quad word aligned (bits [3:0]=0000).	Yes	Yes	0h

11.6.6 (DMAMODE1; PCI:94h, LOC:114h) DMA Channel 1 Mode Register

Table 11-81. (DMAMODE1; PCI:94h, LOC:114h) DMA Channel 1 Mode Register

Bit	Description	Read	Write	Value after Reset
1:0	Local Bus Width. Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
5:2	Internal Wait States (data to data).	Yes	Yes	0h
6	TA#/READY# Input Enable. Writing a 1 enables TA#/READY# input. Writing a 0 disables TA#/READY# input.	Yes	Yes	1
7	BTERM# Input Enable. Writing a 1 enables BTERM# input. Writing a 0 disables BTERM# input. For more information, refer to Section 2.2.5 for M mode, or to Section 4.2.5 for C and J modes.	Yes	Yes	0
8	Local Burst Enable. Writing a 1 enables Local bursting. Writing a 0 disables Local bursting.	Yes	Yes	0
9	Scatter/Gather Mode. Writing a 1 indicates Scatter/Gather mode is enabled. For Scatter/Gather mode, the DMA source address, destination address, and byte count are loaded from memory in PCI or Local Address spaces. Writing a 0 indicates Block mode is enabled.	Yes	Yes	0
10	Done Interrupt Enable. Writing a 1 enables interrupt when done. Writing a 0 disables the interrupt when done. If DMA Clear Count mode is enabled, the interrupt does not occur until the byte count is cleared.	Yes	Yes	0
11	Local Addressing Mode. Writing a 1 holds the Local address bus constant. Writing a 0 indicates the Local address is incremented.	Yes	Yes	0
12	Reserved.	Yes	No	0
13	Memory Write and Invalidate Mode for DMA Transfers. When set to 1, the PCI 9054 performs Memory Write and Invalidate cycles to the PCI Bus. The PCI 9054 supports Memory Write and Invalidate sizes of 8 or 16 Lwords. Size is specified in the System Cache Line Size bits (PCICLSR[7:0]). If a size other than 8 or 16 is specified, the PCI 9054 performs Write transfers rather than Memory Write and Invalidate transfers. Transfers must start and end at Cache Line Boundaries.	Yes	Yes	0
14	DMA EOT# Enable. Writing a 1 enables the EOT# input pin. Writing a 0 disables the EOT# output pin.	Yes	Yes	0
15	Fast/Slow Terminate Mode Select. Writing a 0 sets the PCI 9054 into the Slow Terminate mode. As a result in C or J modes, BLAST# is asserted to terminate the DMA transfer. In M mode, BDIP# is de-asserted at the nearest 16-byte boundary and stops the DMA transfer. Writing a 1 indicates that asserting EOT# during DMA will terminate the DMA transfer. In M mode, writing a 1 indicates BDIP# output is disabled. As a result, the PCI 9054 DMA transfer terminates immediately when EOT# is asserted.	Yes	Yes	0
16	DMA Clear Count Mode. When set to 1, the byte count in each Scatter/Gather descriptor is cleared when the corresponding DMA transfer is complete.	Yes	Yes	0
17	DMA Channel 1 Interrupt Select. Writing a 1 routes the DMA Channel 1 interrupt to the PCI Bus interrupt. Writing a 0 routes the DMA Channel 1 interrupt to the Local Bus interrupt.	Yes	Yes	0
18	DAC Chain Load. When set to 1, enables the descriptor to load the PCI Dual Address Cycle value. Otherwise, it uses the contents of the register.	Yes	Yes	0
31:19	Reserved.	Yes	No	0h

11.6.7 (DMAPADR1; PCI:98h, LOC:118h) DMA Channel 1 PCI Address Register

Table 11-82. (DMAPADR1; PCI:98h, LOC:118h) DMA Channel 1 PCI Address Register

Bit	Description	Read	Write	Value after Reset
31:0	PCI Data Address Register. Indicates from where in PCI Memory space DMA transfers (reads or writes) start.	Yes	Yes	0h

11.6.8 (DMALADR1; PCI:9Ch, LOC:11Ch) DMA Channel 1 Local Address Register

Table 11-83. (DMALADR1; PCI:9Ch, LOC:11Ch) DMA Channel 1 Local Address Register

Bit	Description	Read	Write	Value after Reset
31:0	Local Data Address Register. Indicates from where in Local Memory space DMA transfers (reads or writes) start.	Yes	Yes	0h

11.6.9 (DMASIZ1; PCI:A0h, LOC:120h) DMA Channel 1 Transfer Size (Bytes) Register

Table 11-84. (DMASIZ1; PCI:A0h, LOC:120h) DMA Channel 1 Transfer Size (Bytes) Register

Bit	Description	Read	Write	Value after Reset
22:0	DMA Transfer Size (Bytes). Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	0h
31:23	Reserved.	Yes	No	0h

11.6.10 (DMADPR1; PCI:A4h, LOC:124h) DMA Channel 1 Descriptor Pointer Register

Table 11-85. (DMADPR1; PCI:A4h, LOC:124h) DMA Channel 1 Descriptor Pointer Register

Bit	Description	Read	Write	Value after Reset
0	Descriptor Location. Writing a 1 indicates PCI Address space. Writing a 0 indicates Local Address space.	Yes	Yes	0
1	End of Chain. Writing a 1 indicates end of chain. Writing a 0 indicates not end of chain descriptor. (Same as Block mode.)	Yes	Yes	0
2	Interrupt after Terminal Count. Writing a 1 causes an interrupt to be asserted after the terminal count for this descriptor is reached. Writing a 0 disables interrupts from being asserted.	Yes	Yes	0
3	Direction of Transfer. Writing a 1 indicates transfers from the Local Bus to the PCI Bus. Writing a 0 indicates transfers from the PCI Bus to the Local Bus.	Yes	Yes	0
31:4	Next Descriptor Address. Quad word aligned (bits [3:0]=0000).	Yes	Yes	0h

11.6.11 (DMACSR0; PCI:A8h, LOC:128h) DMA Channel 0 Command/Status Register

Table 11-86. (DMACSR0; PCI:A8h, LOC:128h) DMA Channel 0 Command/Status Register

Bit	Description	Read	Write	Value after Reset
0	Channel 0 Enable. Writing a 1 enables channel to transfer data. Writing a 0 disables the channel from starting a DMA transfer and if in the process of transferring data suspend transfer (pause).	Yes	Yes	0
1	Channel 0 Start. Writing a 1 causes the channel to start transferring data if the channel is enabled.	No	Yes/Set	0
2	Channel 0 Abort. Writing a 1 causes the channel to abort current transfer. Channel 0 Enable bit must be cleared (bit [0]=0). Sets Channel 1 Done bit when abort is complete.	No	Yes/Set	0
3	Channel 0 Clear Interrupt. Writing a 1 clears Channel 0 interrupts.	No	Yes/Clr	0
4	Channel 0 Done. Reading a 1 indicates a channel transfer is complete. Reading a 0 indicates a channel transfer is not complete.	Yes	No	1
7:5	Reserved.	Yes	No	000

11.6.12 (DMACSR1; PCI:A9h, LOC:129h) DMA Channel 1 Command/Status Register

Table 11-87. (DMACSR1; PCI:A9h, LOC:129h) DMA Channel 1 Command/Status Register

Bit	Description	Read	Write	Value after Reset
0	Channel 1 Enable. Writing a 1 enables channel to transfer data. Writing a 0 disables the channel from starting a DMA transfer and if in the process of transferring data suspend transfer (pause).	Yes	Yes	0
1	Channel 1 Start. Writing a 1 causes channel to start transferring data if the channel is enabled.	No	Yes/Set	0
2	Channel 1 Abort. Writing a 1 causes channel to abort current transfer. Channel 1 Enable bit must be cleared (bit [0]=0). Sets Channel 1 Done bit when abort is complete.	No	Yes/Set	0
3	Channel 1 Clear Interrupt. Writing a 1 clears Channel 1 interrupts.	No	Yes/Clr	0
4	Channel 1 Done. Reading a 1 indicates a channel transfer is complete. Reading a 0 indicates a channel transfer is not complete.	Yes	No	1
7:5	Reserved.	Yes	No	000

11.6.13 (DMAARB; PCI:ACh, LOC:12Ch) DMA Arbitration Register

Same as Mode/Arbitration register (MARBR).

11.6.14 (DMATHR; PCI:B0h, LOC:130h) DMA Threshold Register

Table 11-88. (DMATHR; PCI:B0h, LOC:130h) DMA Threshold Register

Bit	Description	Read	Write	Value after Reset
3:0	DMA Channel 0 PCI-to-Local Almost Full (C0PLAF). Number of full entries (divided by two, minus one) in the FIFO before requesting the Local Bus for writes. (C0PLAF+1) + (C0PLAE+1) should be ≤ a FIFO Depth of 32.	Yes	Yes	0h
7:4	DMA Channel 0 Local-to-PCI Almost Empty (C0LPAE). Number of empty entries (divided by two, minus one) in the FIFO before requesting the Local Bus for reads. (C0LPAF+1) + (C0LPAE+1) should be ≤ a FIFO depth of 32.	Yes	Yes	0h
11:8	DMA Channel 0 Local-to-PCI Almost Full (C0LPAF). Number of full entries (divided by two, minus one) in the FIFO before requesting the PCI Bus for writes.	Yes	Yes	0h
15:12	DMA Channel 0 PCI-to-Local Almost Empty (C0PLAE). Number of empty entries (divided by two, minus one) in the FIFO before requesting the PCI Bus for reads.	Yes	Yes	0h
19:16	DMA Channel 1 PCI-to-Local Almost Full (C1PLAF). Number of full entries, minus one, in the FIFO before requesting the Local Bus for writes. (C1PLAF+1) + (C1PLAE+1) should be ≤ a FIFO depth of 16.	Yes	Yes	0h
23:20	DMA Channel 1 Local-to-PCI Almost Empty (C1LPAE). Number of empty entries, minus one, in the FIFO before requesting the Local Bus for reads. (C1PLAF) + (C1PLAE) should be ≤ a FIFO depth of 16.	Yes	Yes	0h
27:24	DMA Channel 1 Local-to-PCI Almost Full (C1LPAF). Number of full entries, minus one, in the FIFO before requesting the PCI Bus for writes.	Yes	Yes	0h
31:28	DMA Channel 1 PCI-to-Local Almost Empty (C1PLAE). Number of empty entries, minus one, in the FIFO before requesting the PCI Bus for reads.	Yes	Yes	0h

Note for DMA Channel 0 Only: *If number of entries needed is x, then the value is one less than half the number of entries (that is, x/2 - 1).*

11.6.15 (DMADAC0; PCI:B4h, LOC:134h) DMA 0 PCI Dual Address Cycle Address Register

Table 11-89. (DMADAC0; PCI:B4h, LOC:134h) DMA 0 PCI Dual Address Cycle Address Register

Bit	Description	Read	Write	Value after Reset
31:0	Upper 32 bits of the PCI Dual Address Cycle PCI address during DMA Channel 0 cycles. If set to 0h, the PCI 9054 performs a 32-bit DMA Channel 0 Address access.	Yes	Yes	0h

11.6.16 (DMADAC1; PCI:B8h, LOC:138h) DMA 1 PCI Dual Address Cycle Address Register

Table 11-90. (DMADAC1; PCI:B8h, LOC:138h) DMA 1 PCI Dual Address Cycle Address Register

Bit	Description	Read	Write	Value after Reset
31:0	Upper 32 bits of the PCI Dual Address Cycle PCI address during DMA Channel 1 cycles. If set to 0h, the PCI 9054 performs a 32-bit DMA Channel 1 Address access.	Yes	Yes	0h

11.7 Messaging Queue Registers

11.7.1 (OPQIS; PCI:30h, LOC:B0h) Outbound Post Queue Interrupt Status Register

Table 11-91. (OPQIS; PCI:30h, LOC:B0h) Outbound Post Queue Interrupt Status Register

Bit	Description	Read	Write	Value after Reset
2:0	Reserved.	Yes	No	000
3	Outbound Post Queue Interrupt. Set when the Outbound Post Queue is not empty. Not affected by the Interrupt Mask bit.	Yes	No	0
31:4	Reserved.	Yes	No	0h

11.7.2 (OPQIM; PCI:34h, LOC:B4h) Outbound Post Queue Interrupt Mask Register

Table 11-92. (OPQIM; PCI:34h, LOC:B4h) Outbound Post Queue Interrupt Mask Register

Bit	Description	Read	Write	Value after Reset
2:0	Reserved.	Yes	No	000
3	Outbound Post Queue Interrupt Mask. Writing a 1 masks the interrupt.	Yes	Yes	1
31:4	Reserved.	Yes	No	0h

11.7.3 (IQP; PCI:40h) Inbound Queue Port Register

Table 11-93. (IQP; PCI:40h) Inbound Queue Port Register

Bit	Description	Read	Write	Value after Reset
31:0	Value written by the PCI Master is stored into the Inbound Post Queue, which is located in Local memory at the address pointed to by the Queue Base Address + Queue Size + Inbound Post Head Pointer. From the time of the PCI write until the Local Memory write and update of the Inbound Post Queue Head Pointer, further accesses to this register result in a Retry. A Local interrupt is asserted when the Inbound Post Queue is not empty. When the port is read by the PCI Master, the value is read from the Inbound Free Queue, which is located in Local memory at the address pointed to by the Queue Base Address + Inbound Free Tail Pointer. If the queue is empty, FFFFFFFh is returned.	PCI	PCI	0h

11.7.4 (OQP; PCI:44h) Outbound Queue Port Register

Table 11-94. (OQP; PCI:44h) Outbound Queue Port Register

Bit	Description	Read	Write	Value after Reset
31:0	Value written by the PCI Master is stored into the Outbound Free Queue, which is located in Local memory at the address pointed to by the Queue Base Address + 3*Queue Size + Outbound Free Head Pointer. From the time of the PCI write until the Local Memory write and update of the Outbound Free Queue Head Pointer, further accesses to this register result in a Retry. If the queue fills up, a Local NMI interrupt is asserted. When the port is read by the PCI Master, the value is read from the Outbound Post Queue, which is located in Local memory at the address pointed to by the Queue Base Address + 2*Queue Size + Outbound Post Tail Pointer. If the queue is empty, FFFFFFFh is returned. A PCI interrupt is asserted if the Outbound Post Queue is not empty.	PCI	PCI	0h

11.7.5 (MQCR; PCI:C0h, LOC:140h) Messaging Queue Configuration Register

Table 11-95. (MQCR; PCI:C0h, LOC:140h) Messaging Queue Configuration Register

Bit	Description	Read	Write	Value after Reset
0	Queue Enable. Writing a 1 allows accesses to the Inbound and Outbound Queue ports. If cleared to 0, writes are accepted but ignored and reads return FFFFFFFFh.	Yes	Yes	0
5:1	Circular Queue Size. Contains the size of one of the circular FIFO queues. Each of the four queues are the same size. Queue Size Encoding values: Bits [5:1] — Number of entries — Total size 00001 — 4-kilobit entries — 64 kilobits 00010 — 8-kilobit entries — 128 kilobits 00100 — 16-kilobit entries — 256 kilobits 01000 — 32-kilobit entries — 512 kilobits 10000 — 64-kilobit entries — 1 MB	Yes	Yes	00001
31:6	Reserved.	Yes	No	0h

11.7.6 (QBAR; PCI:C4h, LOC:144h) Queue Base Address Register

Table 11-96. (QBAR; PCI:C4h, LOC:144h) Queue Base Address Register

Bit	Description	Read	Write	Value after Reset
19:0	Reserved.	Yes	No	0h
31:20	Queue Base Address. Local Memory base address of circular queues. Queues must be aligned on a 1 MB boundary.	Yes	Yes	0h

11.7.7 (IFHPR; PCI:C8h, LOC:148h) Inbound Free Head Pointer Register

Table 11-97. (IFHPR; PCI:C8h, LOC:148h) Inbound Free Head Pointer Register

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	00
19:2	Inbound Free Head Pointer. Local Memory Offset for the Inbound Free Queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	Queue Base Address.	Yes	No	0h

11.7.8 (IFTPR; PCI:CCh, LOC:14Ch) Inbound Free Tail Pointer Register

Table 11-98. (IFTPR; PCI:CCh, LOC:14Ch) Inbound Free Tail Pointer Register

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	00
19:2	Inbound Free Tail Pointer. Local Memory offset for the Inbound Free Queue. Maintained by the hardware and incremented modulo the queue size.	Yes	Yes	0h
31:20	Queue Base Address.	Yes	No	0h

11.7.9 (IPHPR; PCI:D0h, LOC:150h) Inbound Post Head Pointer Register

Table 11-99. (IPHPR; PCI:D0h, LOC:150h) Inbound Post Head Pointer Register

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	00
19:2	Inbound Post Head Pointer. Local Memory offset for the Inbound Post Queue. Maintained by the hardware and incremented modulo the queue size.	Yes	Yes	0h
31:20	Queue Base Address.	Yes	No	0h

11.7.10 (IPTPR; PCI:D4h, LOC:154h) Inbound Post Tail Pointer Register

Table 11-100. (IPTPR; PCI:D4h, LOC:154h) Inbound Post Tail Pointer Register

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	00
19:2	Inbound Post Tail Pointer. Local Memory offset for the Inbound Post Queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	Queue Base Address.	Yes	No	0h

11.7.11 (OFHPR; PCI:D8h, LOC:158h) Outbound Free Head Pointer Register

Table 11-101. (OFHPR; PCI:D8h, LOC:158h) Outbound Free Head Pointer Register

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	00
19:2	Outbound Free Head Pointer. Local Memory offset for the Outbound Free Queue. Maintained by the hardware and incremented modulo the queue size.	Yes	Yes	0h
31:20	Queue Base Address.	Yes	No	0h

11.7.12 (OFTPR; PCI:DCh, LOC:15Ch) Outbound Free Tail Pointer Register

Table 11-102. (OFTPR; PCI:DCh, LOC:15Ch) Outbound Free Tail Pointer Register

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	00
19:2	Outbound Free Tail Pointer. Local Memory offset for the Outbound Free Queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	Queue Base Address.	Yes	No	0h

11.7.13 (OPHPR; PCI:E0h, LOC:160h) Outbound Post Head Pointer Register

Table 11-103. (OPHPR; PCI:E0h, LOC:160h) Outbound Post Head Pointer Register

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	00
19:2	Outbound Post Head Pointer. Local Memory offset for the Outbound Post Queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	Queue Base Address.	Yes	No	0h

11.7.14 (OPTPR; PCI:E4h, LOC:164h) Outbound Post Tail Pointer Register

Table 11-104. (OPTPR; PCI:E4h, LOC:164h) Outbound Post Tail Pointer Register

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	00
19:2	Outbound Post Tail Pointer. Local Memory offset for the Outbound Post Queue. Maintained by the hardware and incremented modulo the queue size.	Yes	Yes	0h
31:20	Queue Base Address.	Yes	No	0h

11.7.15 (QSR; PCI:E8h, LOC:168h) Queue Status/Control Register

Table 11-105. (QSR; PCI:E8h, LOC:168h) Queue Status/Control Register

Bit	Description	Read	Write	Value after Reset
0	I_2O Decode Enable. When set, replaces the MBOX0 and MBOX1 registers with the Inbound and Outbound Queue Port registers and redefines Space 1 as PCI Base Address 0 to be accessed by PCIBAR0. Former Space 1 registers F0, F4, and F8 should be programmed to configure their shared I_2O Memory space, defined as PCI Base Address 0.	Yes	Yes	0
1	Queue Local Space Select. When set to 0, use the Local Address Space 0 Bus Region descriptor for Queue accesses. When set to 1, use the Local Address Space 1 Bus Region descriptor for Queue accesses.	Yes	Yes	0
2	Outbound Post Queue Prefetch Enable. Writing a 1 causes prefetching to occur from the Outbound Post Queue if it is not empty.	Yes	Yes	0
3	Inbound Free Queue Prefetch Enable. Writing a 1 causes prefetching to occur from the Inbound Free Queue if it is not empty.	Yes	Yes	0
4	Inbound Post Queue Interrupt Mask. Writing a 1 masks the interrupt.	Yes	Yes	1
5	Inbound Post Queue Interrupt Not Empty. Set when the Inbound Post Queue is not empty. Not affected by the Interrupt Mask bit.	Yes	No	0
6	Outbound Free Queue Overflow Interrupt Mask. Masks the interrupt when set.	Yes	Yes	1
7	Outbound Free Queue Overflow Interrupt Full. Set when the Outbound Free Queue becomes full. A Local TEA#/LSERR# (NMI) interrupt is asserted. Writing a 1 clears the interrupt.	Yes	Yes/Clr	0
31:8	Unused.	Yes	No	0h

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12. PIN DESCRIPTION

12.1 Pin Summary

Tables in this section describe each PCI 9054 pin. Table 12-2 through Table 12-6 provide pin information common to all Local Bus modes of operation:

- Power and Ground Pin Description
- Serial EEPROM Interface Pin Description
- PCI System Bus Interface Pin Description
- Local Bus Mode and Processor Independent Interface Pin Description

Pins in Table 12-7 through Table 12-9 correspond to the PCI 9054 Local Bus modes—M, C, and J:

- M Bus Mode Interface Pin Description (32-bit address/32-bit data, non-multiplexed)
- C Bus Mode Interface Pin Description (32-bit address/32-bit data, non-multiplexed)
- J Bus Mode Interface Pin Description (32-bit address/32-bit data, multiplexed)

For a visual view of the chip pinout, refer to Section 14.

The following pins have internal pull-ups:

ADS#, BDIP#, BI#, BIGEND#/WAIT#, BLAST#, BTERM#, BURST#, CCS#, DMPAF/EOT#, DP[3:0]#, EEDI/EEDO, LA[31:30], LA[28:0], LAD[31:0], LBE[3:0]#, LINT#, LRESETo#, LSERR#, LW/R#, RD/WR#, MDREQ#/DMPAF/EOT#, MODE[1:0], READY#, TA#, TEA#, TS#, TSIZ[0:1], WAIT#.

The TEST pin has an internal pull-down.

***Notes**: Due to the complexity of pin multiplexing, LA[29] requires an external pull-up in M and C modes. This pin requires a pull-down in J mode.*

The BB# pin requires a 510 ohm external pull-up resistor in M mode only.

Table 12-1 lists abbreviations used in this section to represent various pin types.

Table 12-1. Pin Type Abbreviations

Abbreviation	Pin Type
I/O	Input and output pin
I	Input pin only
O	Output pin only
TS	Tri-state pin
OC	Open collector pin
TP	Totem pole pin
STS	Sustained tri-state pin, driven high for one CLK before float
DTS	Driven tri-state pin, driven high for one-half CLK before float

All Local Bus internal pull-ups go through a 100k-ohm resistor. All Local Bus internal pull-downs go through a 50k-ohm resistor.

All Local I/O pins should have external pull-ups or pull-downs, which depend upon the application and polarity of the pin. (Use approximately 3k to 10k ohms.) This is recommended due to the weak value of the internal pull-ups and pull-downs.

Unspecified pins are not connected (NC).

***Note for PCI pins:** DO NOT pull up or down on any pins unless the PCI 9054 is being used in an embedded design. Refer to PCI Local Bus Specification, v2.1, page 123.*

12.2 Pinout Common to All Bus Modes

Table 12-2. Power and Ground Pins (176-Pin PQFP)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	Function
TEST	Test Pin	1	I	155	Pulled high for test and low for normal operation. When pulled high: All outputs except USERo/DREQ0#/LLOCKo# and LEDon/LEDin are placed in tri-state. USERo/DREQ0#/LLOCKo# provide NANDTREE output.
VDD	Power (+3.3V)	15	I	1, 20, 28, 35, 45, 62, 70, 89, 99, 109, 116, 133, 141, 147, 162	Three-volt power supply pins for core and I/O buffers. Liberal .01 µF to .1 µF decoupling capacitors should be placed near the PCI 9054.
VSS	Ground	12	I	19, 27, 44, 61, 69, 88, 108, 115, 132, 140, 161, 176	Ground pins.

Note: *The die contains 224 pads. Power and Grounds are double bounded in the PQFP package to meet proper drive strength of the buffers.*

Table 12-3. Power and Ground Pins (225-Pin PBGA)

Symbol	Signal Name	Total Die Pads	Total Pins	Pin Type	PBGA Pin Number	Function
TEST	Test Pin	1	1	I	A8	Pulled high for test, low for normal operation. When pulled high: All outputs except USERo/DREQ0#/LLOCKo# and LEDon/LEDin are placed in tri-state. USERo/DREQ0#/LLOCKo# provide NANDTREE output.
VDD (Core)	Power (+3.3V)	34	34	I	A1, E2, G2, G5, H5, J4, J5, L2, K5, R1, P5, R6, P7, L8, R9, P10, N11, R15, L13, K11, J13, J11, H12, G12, E15, A15, B12, C11, C10, D9, D8, A6, B6, D6	Three-volt power supply pins for core and I/O buffers. Liberal .01 µF to .1 µF decoupling capacitors should be placed near the PCI 9054.
VSS	Ground	39	13	I	F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8	Ground pins.

Table 12-4. Serial EEPROM Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
EECS	Serial EEPROM Chip Select	1	O TP 6 mA	164	F7	Serial EEPROM Chip Select.
EEDI/EEDO	Serial EEPROM Data IN/ Serial EEPROM Data OUT	1	I/O TP 6 mA	166	C5	Multiplexed Write/Read data to serial EEPROM pin.
EESK	Serial DataClock	1	O TP 6 mA	165	B5	Serial EEPROM clock pin.

Note: *The serial EEPROM interface operates at core voltage (+3.3V). The PCI 9054 requires use of a serial EEPROM that can operate up to 1 MHz.*

Table 12-5. PCI System Bus Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS PCI	173-175, 2-5, 8-15, 31-34, 36-40, 42-43, 46-51	F6, A2, C3, D4, B1, C2, E5, D2, G6, D1, E3, F5, F4, F3, F2, J6, L1, K4, M1, M2, L4, N1, M3, N2, P1, N3, M4, R2, P3, L5, N4, R3	All multiplexed on the same PCI pins. The Bus transaction consists of an Address phase, followed by one or more Data phases. The PCI 9054 supports both Read and Write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I/O TS PCI	6, 16, 30, 41	D3, G4, K3, K6	All multiplexed on the same PCI pins. During the Address phase of a transaction, defines the bus command. During the Data phase, used as byte enables. Refer to the PCI spec for further detail if needed.
DEVSEL#	Device Select	1	I/O STS PCI	22	H1	When actively driven, indicates the driving device has decoded its address as Target of current access. As an input, indicates whether any device on the bus is selected.
ENUM#	Enumeration	1	O OC PCI	52	P4	Interrupt output set when an adapter using the PCI 9054 is freshly inserted or ready to be removed from a PCI slot.
FRAME#	Cycle Frame	1	I/O STS PCI	17	G3	Driven by the current Master to indicate the beginning and duration of an access. FRAME# is asserted to indicate the bus transaction is beginning. While FRAME# is asserted, Data transfers continue. When FRAME# is de-asserted, the transaction is in the final Data phase.
GNT#	Grant	1	I	171	C4	Indicates to the agent that access to the bus is granted. Every Master has its own REQ# and GNT#.
RST#	Reset	1	I	169	D5	Used to bring PCI-specific registers, sequencers, and signals to a consistent state.
IDSEL	Initialization Device Select	1	I	7	C1	Used as a chip select during Configuration Read and Write transactions.
INTA#	Interrupt A	1	O OC PCI	168	B4	PCI Interrupt request.

Table 12-5. PCI System Bus Interface Pins (continued)

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
IRDY#	Initiator Ready	1	I/O STS PCI	18	G1	Indicates ability of the initiating agent (Bus Master) to complete the current Data phase of the transaction.
LOCK#	Lock	1	I/O STS PCI	24	J2	Indicates an atomic operation that may require multiple transactions to complete.
PAR	Parity	1	I/O TS PCI	29	K1	Even parity across AD[31:0] and C/BE[3:0]#. All PCI agents require parity generation. PAR is stable and valid one clock after the Address phase. For Data phases, PAR is stable and valid one clock after either IRDY# is asserted on a Write transaction or TRDY# is asserted on a Read transaction. Once PAR is valid, it remains valid until one clock after current Data phase completes.
PCLK	Clock	1	I	170	A3	Provides timing for all transactions on PCI and is an input to every PCI device. The PCI 9054 operates up to 33 MHz.
PERR#	Parity Error	1	I/O STS PCI	25	J1	Reports data parity errors during all PCI transactions, except during a special cycle.
PME#	Power Management Event	1	O OC PCI	167	A4	Wake-up event interrupt.
REQ#	Request	1	O STS PCI	172	B3	Indicates to arbiter that this agent must use the bus. Every Master has its own GNT# and REQ#.
SERR#	Systems Error	1	O OC PCI	26	J3	Reports address parity errors, data parity errors on the Special Cycle command, or any other system error where the result is catastrophic.
STOP#	Stop	1	I/O STS PCI	23	H4	Indicates the current Target is requesting that the Master stop the current transaction.
TRDY#	Target Ready	1	I/O STS PCI	21	H3	Indicates ability of the Target agent (selected device) to complete the current Data phase of the transaction.

Table 12-6. Local Bus Mode and Processor Independent Interface Pins

Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
CCS#	Configuration Register Select	1	I	160	E7	Internal PCI 9054 registers are selected when CCS# is asserted low.
LCLK	Local processor Clock	1	I	142	D11	Local clock input.
LEDon/ LEDin	LEDon/LEDin	1	I/O TS 24 mA	53	K7	As an output, acts as the Hot Swap board indicator LED. As an input, monitors the CompactPCI board latch status.
LFRAME#	PCI Buffered FRAME# Signal	1	O TP 6 mA	—	G13	Could be used to monitor PCI Bus activity. *Available only on the PBGA package.*
LINT#	Local Interrupt	1	I/O TP 12 mA	154	B8	As an input to the PCI 9054, when asserted low, causes PCI interrupt. As an output, a synchronous level output that remains asserted as long as an interrupt condition exists. If edge level interrupt is required, disabling and then enabling Local interrupts through INTCSR creates an edge if an interrupt condition still exists or a new interrupt condition occurs.
LRESETo#	Local Bus Reset Out	1	O TP 12 mA	152	A9	Asserted when the PCI 9054 chip is reset. Can be used to drive RESET# input of a Local processor.
MODE[1:0]	Bus Mode	2	I	157-156	B7, E8	Selects the PCI 9054 bus operation mode: Mode 0 / Mode 1 / Bus Mode 1 / 1 / M 1 / 0 / J 0 / 1 / Reserved 0 / 0 / C
USERi/	User Input	1	I	159	C7	Multiplexed input/output pin. USERi: General-purpose input that can be read by way of the PCI 9054 Configuration registers.
DACK0#/	Demand Mode DMA Acknowledge		O TS 12 mA			DACK0#: When a channel is programmed through the Configuration registers to operate in Demand mode, this output indicates a DMA transfer is being executed. DACK0# corresponds to PCI 9054 DMA Ch 0.
LLOCKi#	Local Lock Input		I			LLOCKi#: Indicates an atomic operation that may require multiple transactions to complete. Used by the PCI 9054 for direct Local access to the PCI Bus.
USERo/	User Output	1	O TS 12 mA	158	A7	Multiplexed input/output pin. USERo: General-purpose output controlled from the PCI 9054 Configuration registers.
DREQ0#/	Demand DMA Request		I			DREQ0#: When a channel is programmed through the Configuration registers to operate in Demand mode, this input serves as a DMA request. DREQ0# corresponds to the PCI 9054 DMA Ch 0.
LLOCKo#	Local Lock Output		O			LLOCKo#: Indicates an atomic operation for a Direct Slave PCI-to-Local Bus access may require multiple transactions to complete.

12.3 M Bus Mode Pinout

Table 12-7. M Bus Mode Interface Pins

M Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
BB#	Bus Busy	1	I/O TP 12 mA	150	C9	As an input, the PCI 9054 monitors this signal to determine whether the external Master has ended a Bus cycle. As an output, the PCI 9054 asserts this signal after an external arbiter has granted ownership of the Local Bus and BB# is inactive from another Master. Signal requires an external pull-up resistor value of 510Ω be applied to guarantee a fast transition to the inactive state when the PCI 9054 relinquishes ownership of the Local Bus.
BDIP#	Burst Data in Progress	1	I/O TS 12 mA	151	B9	As an input, driven by the Bus Master during a Burst transaction. The Master de-asserts before the last Data phase on the bus. As an output, driven by the PCI 9054 during the Data phase of a Burst transaction. The PCI 9054 de-asserts before the last Burst Data phase on the bus.
BG#	Bus Grant	1	I	144	B11	Asserted by the Local Bus arbiter in response to BR#. Indicates the requesting Master is next.
BI#	Burst Inhibit	1	I	134	D12	Whenever BR# is asserted, indicates that the Target device does not support Burst transactions.
BIGEND#/ WAIT#	Big Endian Select WAIT input/output Select (*WAIT# is available at this location only in M mode)*	1	I I/O TS 12 mA	163	C6	Multiplexed input/output pin. Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. Big Endian Byte order for Direct Master transfers or Configuration register accesses is also programmable through the Configuration registers. If wait is selected, then PCI 9054 issues WAIT# when it is a Master on the Local Bus and has internal wait states setup. As a Slave, the PCI 9054 accepts WAIT# as an input from the Bus Master.
BR#	Bus Request	1	O TP 12 mA	143	A12	Asserted by the Master to request use of the Local Bus. The Local Bus arbiter asserts BG# when the Master is next in line for bus ownership.
BURST#	Burst	1	I/O TS 12 mA	148	B10	As an input, driven by the Master along with address and data indicating a Burst transfer is in progress. As an output, driven by the PCI 9054 along with address and data indicating a Burst transfer is in progress.
DP[0:3]	Data Parity	4	I/O TS 12 mA	136-139	B13, E11, C12, A13	Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for writes or reads to the PCI 9054. Parity is asserted for reads from or writes by the PCI 9054. DP0 is the most significant bit of the Bus address.

Table 12-7. M Bus Mode Interface Pins (continued)

M Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PGFP Pin Number	PBGA Pin Number	Function
LA[0:31]	Address Bus	32	I/O TS 12 mA	54-60, 63-68, 71-87, 93-94	R4, N5, L6, M6, N6, P6, M7, R7, L7, N8, R8, M8, P9, N9, L9, R10, N10, K9, R11, M10, R12, L10, M11, R13, N12, P13, K10, R14, N13, P14, L11, M13	Carries the 32 bits of the physical Address Bus. LA0 is most significant bit of bus address.
LD[0:31]	Data Bus	32	I/O TS 12 mA	95-98, 100-107, 110-114, 117-131	N15, M14, J10, M15, L14, L15, K12, K13, K15, J12, J14, J15, H14, H15, H11, G14, G15, G11, F14, F13, G10, E14, E13, D15, D14, E12, C15, D13, C14, F10, B15, C13	Carries 8-, 16-, or 32-bit data quantities, depending upon the bus-width configuration. All Master accesses to the PCI 9054 are 32 bits only. LD0 is most significant bit of bus address.
MDREQ#/	IDMA Data Transfer Request *(MDREQ# is available at this location in M mode only)*	1	0 TS 12 mA	153	E9	Multiplexed input or output pin. MDREQ#: IDMA M mode Data transfer request start. Always asserted, indicating Data transfer should start. De-asserted only when the Direct Master FIFO becomes full. Programmable through a Configuration register.
DMPAF/	Direct Master Programmable Almost Full		O TS 12 mA			DMPAF: Direct Master Write FIFO Almost Full status output. Programmable through a Configuration register.
EOT#	End of Transfer for Current DMA Channel		I			EOT#: Terminates the current DMA transfer. ***Note:*** *EOT# serves as a general purpose EOT. Before asserting EOT#, user should be aware of DMA channel activity.*
RD/WR#	Read/Write	1	I/O TS 12 mA	90	M12	Asserted high for reads and low for writes.
RETRY#	Retry	1	O TP 12 mA	149	A10	Driven by the PCI 9054 when it is a Slave to indicate a Local Master must back off and restart the cycle. In Deferred Read mode, indicates a Local Master should return for the requested data.

Table 12-7. M Bus Mode Interface Pins (continued)

M Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PGFP Pin Number	PBGA Pin Number	Function
TA#	Transfer Acknowledge	1	I/O DTS 12 mA	135	A14	As an input, when a Local Bus access is made to the PCI 9054, indicates a Write Data transfer can complete or that Read data on the bus is valid. As an output, when the PCI 9054 is a Bus Master, indicates a Write Data transfer is complete or that Read data on the bus is valid.
TEA#	Transfer Error Acknowledge	1	I/O OC 12 mA	146	D10	Driven by the Target device, indicating an error condition occurred during a Bus cycle.
TS#	Address Strobe	1	I/O TS 12 mA	145	A11	Indicates the valid address and start of a new Bus access. Asserted for the first clock of a Bus access.
TSIZ[0:1]	Transfer Size	2	I/O TS 12 mA	92-91	N14, P15	Driven by the current Master along with the address, indicating the data-transfer size. TSIZ0 is most significant bit of bus address. Refer to Section 3.4.3.5.3 for more information.

12.4 C Bus Mode Pinout

Table 12-8. C Bus Mode Interface Pins

C Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
ADS#	Address Strobe	1	I/O TS 12 mA	145	A11	Indicates the valid address and start of a new Bus access. Asserted for the first clock of a Bus access.
BIGEND#	Big Endian Select	1	I	163	C6	Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. Big Endian Byte order for Direct Master transfers or Configuration register accesses is also programmable through Configuration registers.
BLAST#	Burst Last	1	I/O TS 12 mA	148	B10	Driven by the current Local Bus Master to indicate the last transfer in a Bus access.
BREQi	Bus Request	1	I	150	C9	Asserted to indicate the Local Bus Master requires the bus. If enabled through the PCI 9054 Configuration registers, the PCI 9054 releases the bus during a DMA transfer if this signal is asserted.
BREQo	Bus Request Out	1	O TP 12 mA	149	A10	Asserted to indicate the PCI 9054 requires the bus to perform a Direct Slave PCI-to-Local Bus access while a Direct Master access is pending on the Local Bus. Can be used with external logic to assert backoff to a Local Bus Master. Operational parameters are set up by way of the PCI 9054 Configuration registers.
BTERM#	Burst Terminate	1	I/O DTS 12 mA	134	D12	As input to the PCI 9054: For processors that burst up to four Lwords. If the Bterm Mode bit is disabled through the PCI 9054 Configuration registers, the PCI 9054 also bursts up to four Lwords. If enabled, the PCI 9054 continues to burst until BTERM# input is asserted. BTERM# is a Ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9054 programmable wait state generator. As output from the PCI 9054: Asserted, along with READY#, to request break up of a burst and start of a new Address cycle (PCI Aborts only).
DMPAF/ EOT#	Direct Master Programmable Almost Full End of Transfer for Current DMA Channel	1	O TS 12 mA I	153	E9	Multiplexed input or output pin. DMPAF: Direct Master Write FIFO Almost Full status output. Programmable through a Configuration register. EOT#: Terminates the current DMA transfer. ***Note:*** *EOT# serves as a general purpose EOT. Before asserting EOT, user should be aware of DMA channel activity.*
DP[3:0]	Data Parity	4	I/O TS 12 mA	136-139	B13, E11, C12, A13	Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for writes or reads to the PCI 9054. Parity is asserted for reads from or writes by the PCI 9054.

Table 12-8. C Bus Mode Interface Pins (continued)

C Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
LA[31:2]	Address Bus	30	I/O TS 12 mA	54-60, 63-68, 71-87	R4, N5, L6, M6, N6, P6, M7, R7, L7, N8, R8, M8, P9, N9, L9, R10, N10, K9, R11, M10, R12, L10, M11, R13, N12, P13, K10, R14, N13, P14	Carries the upper 30 bits of the physical Address Bus. During bursts, LA[31:2] increment to indicate successive Data cycles.
LBE[3:0]#	Byte Enables	4	I/O TS 12 mA	92, 91, 93, 94	N14, P15, L11, M13	Encoded, based on the bus-width configuration, as follows: **32-Bit Bus**: The four byte enables indicate which of the four bytes are active during a Data cycle: BE3# Byte Enable 3—LD[31:24] BE2# Byte Enable 2—LD[23:16] BE1# Byte Enable 1—LD[15:8] BE0# Byte Enable 0—LD[7:0] **16-Bit Bus:** BE3#, BE1# and BE0# are encoded to provide BHE#, LA1, and BLE#, respectively: BE3# Byte High Enable (BHE#)—LD[15:8] BE2# not used BE1# Address bit 1 (LA1) BE0# Byte Low Enable (BLE#)—LD[7:0] **8-Bit Bus:** BE1# and BE0# are encoded to provide LA1 and LA0, respectively: BE3# not used BE2# not used BE1# Address bit 1 (LA1) BE0# Address bit 0 (LA0)
LD[31:0]	Data Bus	32	I/O TS 12 mA	95-98, 100-107, 110-114, 117-131	N15, M14, J10, M15, L14, L15, K12, K13, K15, J12, J14, J15, H14, H15, H11, G14, G15, G11, F14, F13, G10, E14, E13, D15, D14, E12, C15, D13, C14, F10, B15, C13	Carries 8-, 16-, or 32-bit data quantities, depending upon a Target bus-width configuration. All Master accesses to the PCI 9054 are 32 bits only.
LHOLD	Hold Request	1	O TP 12 mA	143	A12	Asserted to request use of the Local Bus. The Local Bus arbiter asserts LHOLDA when control is granted.

Table 12-8. C Bus Mode Interface Pins (continued)

C Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
LHOLDA	Hold Acknowledge	1	I	144	B11	Asserted by the Local Bus arbiter when control is granted in response to LHOLD. Bus should not be granted to the PCI 9054 unless requested by LHOLD.
LSERR#	System Error Interrupt Output	1	O OC 12 mA	146	D10	Synchronous level output asserted PCI Bus Target Abort bit is set (PCISR[11]=1) or Received Master Abort bit is set (PCISR[13]=1). If edge level interrupt is required, disabling and then enabling LSERR# interrupts through the interrupt/control status creates an edge if an interrupt condition still exists or a new interrupt condition occurs.
LW/R#	Write/Read	1	I/O TS 12 mA	90	M12	Asserted low for reads and high for writes.
READY#	Ready Input/Output	1	I/O DTS 12 mA	135	A14	When the PCI 9054 is a Bus Master, indicates Read data on the bus is valid or a Write Data transfer is complete. Used in conjunction with the PCI 9054 programmable wait state generator. When a Local Bus access is made to the PCI 9054, indicates the bus Read data is valid or a Write Data transfer is complete.
WAIT#	Wait Input/Output	1	I/O TS 12 mA	151	B9	As an input, can be asserted to cause the PCI 9054 to insert wait states for Local Direct Master accesses to the PCI Bus. Can be thought of as a Ready input from an external Master for Direct Master accesses. As an output, asserted by the PCI 9054 when the internal wait state generator causes wait states. Can be thought of as an output providing PCI 9054 Ready status.

12.5 J Bus Mode Pinout

Table 12-9. J Bus Mode Interface Pins

J Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
ADS#	Address Strobe	1	I/O TS 12 mA	145	A11	Indicates the valid address and start of a new Bus access. Asserted for the first clock of a Bus access.
ALE	Address Latch Enable	1	I/O TS 12 mA	56	L6	Asserted during the Address phase and de-asserted before the Data phase and before the next LCLK rising edge.
BIGEND#	Big Endian Select	1	I	163	C6	Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. Big Endian Byte order for Direct Master transfers or Configuration register accesses is also programmable through the Configuration registers.
BLAST#	Burst Last	1	I/O TS 12 mA	148	B10	Driven by the current Local Bus Master to indicate the last transfer in a Bus access.
BREQi	Bus Request	1	I	150	C9	Asserted to indicate the Local Bus Master requires the bus. If enabled through the PCI 9054 Configuration registers, the PCI 9054 releases the bus during a DMA transfer if this signal is asserted.
BREQo	Bus Request Out	1	O TP 12 mA	149	A10	Asserted to indicate the PCI 9054 requires the bus to perform a Direct Slave PCI-to-Local Bus access while a Direct Master access is pending on the Local Bus. Can be used with external logic to assert backoff to a Local Bus Master. Operational parameters are set up through the PCI 9054 Configuration registers.
BTERM#	Burst Terminate	1	I/O DTS 12 mA	134	D12	As input to the PCI 9054: For processors that burst up to four Lwords. If the Bterm Mode bit is disabled through the PCI 9054 Configuration registers, the PCI 9054 also bursts up to four Lwords. If enabled, the PCI 9054 continues to burst until a BTERM# input is asserted. BTERM# is a Ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9054 programmable wait state generator. As output from the PCI 9054: Asserted, along with READY#, to request break up of a burst and start of a new Address cycle (PCI Aborts only).
DEN#	Data Enable	1	O TS 12 mA	55	N5	Used in conjunction with DT/R# to provide control for data transceivers attached to the Local Bus.
DMPAF/ EOT#	Direct Master Programmable Almost Full End of Transfer for Current DMA Channel	1	O TS 12 mA I	153	E9	Multiplexed input or output pin. DMPAF: Direct Master Write FIFO Almost Full status output. Programmable through a Configuration register. EOT#: Terminates the current DMA transfer. ***Note:*** *EOT# serves as a general purpose EOT. Before asserting EOT#, user should be aware of DMA channel activity.*

Table 12-9. J Bus Mode Interface Pins (continued)

J Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
DP[3:0]	Data Parity	4	I/O TS 12 mA	136-139	B13, E11, C12, A13	Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for writes or reads to the PCI 9054. Parity is asserted for reads from or writes by the PCI 9054.
DT/R#	Data Transmit/Receive	1	O TS 12 mA	54	R4	Used in conjunction with DEN# to provide control for data transceivers attached to the Local Bus. When asserted, indicates the PCI 9054 receives data.
LA[28:2]	Local Address Bus	27	I/O TS 12 mA	57-60, 63-68, 71-87	M6, N6, P6, M7, R7, L7, N8, R8, M8, P9, N9, L9, R10, N10, K9, R11, M10, R12, L10, M11, R13, N12, P13, K10, R14, N13, P14	Carries the upper 27 bits of the physical Address Bus. During bursts, it is incremented to indicate successive Data cycles. The lowest two bits, LA[3:2], carry the word address of the 32-bit Memory Address. The bits are incremented during a Burst access.
LAD[31:0]	Address/Data Bus	32	I/O TS 12 mA	95-98, 100-107, 110-114, 117-131	N15, M14, J10, M15, L14, L15, K12, K13, K15, J12, J14, J15, H14, H15, H11, G14, G15, G11, F14, F13, G10, E14, E13, D15, D14, E12, C15, D13, C14, F10, B15, C13	During an Address phase, the bus carries the upper 30 bits of the physical Address Bus. During a Data phase, the bus carries 32 bits of data.

Table 12-9. J Bus Mode Interface Pins (continued)

J Bus Mode Symbol	Signal Name	Total Pins	Pin Type	PQFP Pin Number	PBGA Pin Number	Function
LBE[3:0]#	Byte Enables	4	I/O TS 12 mA	92, 91, 93, 94	N14, P15, L11, M13	Encoded, based on the bus-width configuration, as follows: **32-Bit Bus:** The four byte enables indicate which of the four bytes are active during a Data cycle: BE3# Byte Enable 3—LAD[31:24] BE2# Byte Enable 2—LAD[23:16] BE1# Byte Enable 1—LAD[15:8] BE0# Byte Enable 0—LAD[7:0] **16-Bit Bus:** BE3#, BE1# and BE0# are encoded to provide BHE#, LAD1, and BLE#, respectively: BE3# Byte High Enable (BHE#)—LAD[15:8] BE2# not used BE1# Address bit 1 (LAD1) BE0# Byte Low Enable (BLE#)—LAD[7:0] **8-Bit Bus:** BE1# and BE0# are encoded to provide LAD1 and LAD0, respectively: BE3# not used BE2# not used BE1# Address bit 1 (LAD1) BE0# Address bit 0 (LAD0)
LHOLD	Hold Request	1	O TP 12 mA	143	A12	Asserted to request use of the Local Bus. The Local Bus arbiter asserts LHOLDA when control is granted.
LHOLDA	Hold Acknowledge	1	I	144	B11	Asserted by the Local Bus arbiter when control is granted in response to LHOLD. The bus should not be granted to the PCI 9054 unless requested by LHOLD.
LW/R#	Write/Read	1	I/O TS 12 mA	90	M12	Asserted low for reads and high for writes.
LSERR#	System Error Interrupt Output	1	O OC 12 mA	146	D10	Synchronous level output asserted the PCI Bus Target Abort bit is set (PCISR[11]=1) or the Received Master Abort bit is set (PCISR[13]=1). If the edge level interrupt is required, disabling and then enabling LSERR# interrupts through the interrupt/control status creates an edge if an interrupt condition still exists or a new interrupt condition occurs.
READY#	Ready Input/Output	1	I/O DTS 12 mA	135	A14	When the PCI 9054 is Bus Master, indicates the Read data on the bus is valid or a Write Data transfer is complete. Used in conjunction with the PCI 9054 programmable wait state generator. When a Local Bus access is made to the PCI 9054, indicates the bus Read data is valid or a Write Data transfer is complete.
WAIT#	Wait Input/Output	1	I/O TS 12 mA	151	B9	As an input, can be asserted to cause the PCI 9054 to insert wait states for Local Direct Master accesses to the PCI Bus. Can be thought of as a Ready input from an external Master for Direct Master accesses. As an output, asserted by the PCI 9054 when the internal wait state generator causes wait states. Can be thought of as an output providing PCI 9054 Ready status.

12.6 NANDTREE Test Access Method

Manufacturing Test (the proper soldering of components to a board) is the first step toward a successful product release. Some silicon vendors provide Joint Test Action Group (JTAG), while other silicon vendors provide an alternative method, NANDTREE, to achieve the same goal. NANDTREE, as well JTAG, provide users with a methodology to verify connectivity between the board and the components.

NANDTREE, the method used by PLX, is a serial interconnection of NAND gates that are used only for testing shorts, opens, and bridging faults of installed devices on a board.

JTAG, by comparison, is a boundary-scan test, or Design for Test (DFT) technique, that simplifies printed circuit board testing, using a standard chip-board test interface. This standard is known as the IEEE Standard Test Access Port and Boundary Scan Architecture. JTAG is a group that initiated the standardization of this test interface.

The PCI 9054 supports the NANDTREE method for this verification methodology. The PCI 9054 NANDTREE is an internal, serial interconnection of all functional pins to provide a convenient method for board manufacturers to check connectivity of package pins to the board. To perform a NANDTREE check, all NANDTREE-connected pins must be forced high “1”, as well as a TEST pin, to enable NANDTREE functionality. Whenever TEST pin is connected high “1”, the PCI 9054 goes to quiescent state, meaning all NANDTREE-connected pins are tri-stated. Sequentially toggling one pin at a time to low “0”, the output of a NANDTREE, USERo/DREQ0#/ LLOCKo# pin, changes its state from high to low or vice-versa, dependent on what input signal is toggled. If the NANDTREE output state remains unchanged during the input toggle procedure, it identifies a bad connection with the toggling pin.

Table 12-10 provides the NANDTREE interconnection sequence.

Note: *IN2 is an inverter. NA2 is a two-input NAND gate.*

Table 12-10. Sequential Interconnection of the PCI 9054 NANDTREE (Pin Definition)

Component Name	Input #1	Input #2	Output
IN2 _INV1	(.A(LA[31]),	—	.X(NAN0));
NA2 _NAND1	(.A1(LA[30]),	.A2(NAN0),	.X(NAN1));
NA2 _NAND2	(.A1(LA[29]),	.A2(NAN1),	.X(NAN2));
NA2 _NAND3	(.A1(LA[28]),	.A2(NAN2),	.X(NAN3));
NA2 _NAND4	(.A1(LA[27]),	.A2(NAN3),	.X(NAN4));
NA2 _NAND5	(.A1(LA[26]),	.A2(NAN4),	.X(NAN5));
NA2 _NAND6	(.A1(LA[25]),	.A2(NAN5),	.X(NAN6));
NA2 _NAND7	(.A1(LA[24]),	.A2(NAN6),	.X(NAN7));
NA2 _NAND8	(.A1(LA[23]),	.A2(NAN7),	.X(NAN8));
NA2 _NAND9	(.A1(LA[22]),	.A2(NAN8),	.X(NAN9));
NA2 _NAND10	(.A1(LA[21]),	.A2(NAN9),	.X(NAN10));
NA2 _NAND11	(.A1(LA[20]),	.A2(NAN10),	.X(NAN11));
NA2 _NAND12	(.A1(LA[19]),	.A2(NAN11),	.X(NAN12));
NA2 _NAND13	(.A1(LA[18]),	.A2(NAN12),	.X(NAN13));
NA2 _NAND14	(.A1(LA[17]),	.A2(NAN13),	.X(NAN14));
NA2 _NAND15	(.A1(LA[16]),	.A2(NAN14),	.X(NAN15));
NA2 _NAND16	(.A1(LA[15]),	.A2(NAN15),	.X(NAN16));
NA2 _NAND17	(.A1(LA[14]),	.A2(NAN16),	.X(NAN17));
NA2 _NAND18	(.A1(LA[13]),	.A2(NAN17),	.X(NAN18));
NA2 _NAND19	(.A1(LA[12]),	.A2(NAN18),	.X(NAN19));
NA2 _NAND20	(.A1(LA[11]),	.A2(NAN19),	.X(NAN20));
NA2 _NAND21	(.A1(LA[10]),	.A2(NAN20),	.X(NAN21));
NA2 _NAND22	(.A1(LA[9]),	.A2(NAN21),	.X(NAN22));
NA2 _NAND23	(.A1(LA[8]),	.A2(NAN22),	.X(NAN23));
NA2 _NAND24	(.A1(LA[7]),	.A2(NAN23),	.X(NAN24));
NA2 _NAND25	(.A1(LA[6]),	.A2(NAN24),	.X(NAN25));
NA2 _NAND26	(.A1(LA[5]),	.A2(NAN25),	.X(NAN26));
NA2 _NAND27	(.A1(LA[4]),	.A2(NAN26),	.X(NAN27));
NA2 _NAND28	(.A1(LA[3]),	.A2(NAN27),	.X(NAN28));
NA2 _NAND29	(.A1(LA[2]),	.A2(NAN28),	.X(NAN29));
NA2 _NAND30	(.A1(LBE[1]#/LA[1]),	.A2(NAN29),	.X(NAN30));
NA2 _NAND31	(.A1(LBE[0]#/LA[0]),	.A2(NAN30),	.X(NAN31));
NA2 _ NAND32	(.A1(LAD[31]/LD[31]),	.A2(NAN31),	.X(NAN32));
NA2 _NAND33	(.A1(LAD[30]/LD[30]),	.A2(NAN32),	.X(NAN33));
NA2 _NAND34	(.A1(LAD[29]/LD[29]),	.A2(NAN33),	.X(NAN34));

Table 12-10. Sequential Interconnection of the PCI 9054 NANDTREE (Pin Definition) (continued)

Component Name	Input #1	Input #2	Output
NA2 _NAND35	(.A1(LAD[28]/LD[28]),	.A2(NAN34),	.X(NAN35));
NA2 _NAND36	(.A1(LAD[27]/LD[27]),	.A2(NAN35),	.X(NAN36));
NA2 _NAND37	(.A1(LAD[26]/LD[26]),	.A2(NAN36),	.X(NAN37));
NA2 _NAND38	(.A1(LAD[25]/LD[25]),	.A2(NAN37),	.X(NAN38));
NA2 _NAND39	(.A1(LAD[24]/LD[24]),	.A2(NAN38),	.X(NAN39));
NA2 _NAND40	(.A1(LAD[23]/LD[23]),	.A2(NAN39),	.X(NAN40));
NA2 _NAND41	(.A1(LAD[22]/LD[22]),	.A2(NAN40),	.X(NAN41));
NA2 _NAND42	(.A1(LAD[21]/LD[21]),	.A2(NAN41),	.X(NAN42));
NA2 _NAND43	(.A1(LAD[20]/LD[20]),	.A2(NAN42),	.X(NAN43));
NA2 _NAND44	(.A1(LAD[19]/LD[19]),	.A2(NAN43),	.X(NAN44));
NA2 _NAND45	(.A1(LAD[18]/LD[18]),	.A2(NAN44),	.X(NAN45));
NA2 _NAND46	(.A1(LAD[17]/LD[17]),	.A2(NAN45),	.X(NAN46));
NA2 _NAND47	(.A1(LAD[16]/LD[16]),	.A2(NAN46),	.X(NAN47));
NA2 _NAND48	(.A1(LAD[15]/LD[15]),	.A2(NAN47),	.X(NAN48));
NA2 _NAND49	(.A1(LAD[14]/LD[14]),	.A2(NAN48),	.X(NAN49));
NA2 _NAND50	(.A1(LAD[13]/LD[13]),	.A2(NAN49),	.X(NAN50));
NA2 _NAND51	(.A1(LAD[12]/LD[12]),	.A2(NAN50),	.X(NAN51));
NA2 _NAND52	(.A1(LAD[11]/LD[11]),	.A2(NAN51),	.X(NAN52));
NA2 _NAND53	(.A1(LAD[10]/LD[10]),	.A2(NAN52),	.X(NAN53));
NA2 _NAND54	(.A1(LAD[9]/LD[9]),	.A2(NAN53),	.X(NAN54));
NA2 _NAND55	(.A1(LAD[8]/LD[8]),	.A2(NAN54),	.X(NAN55));
NA2 _NAND56	(.A1(LAD[7]/LD[7]),	.A2(NAN55),	.X(NAN56));
NA2 _NAND57	(.A1(LAD[6]/LD[6]),	.A2(NAN56),	.X(NAN57));
NA2 _NAND58	(.A1(LAD[5]/LD[5]),	.A2(NAN57),	.X(NAN58));
NA2 _NAND59	(.A1(LAD[4]/LD[4]),	.A2(NAN58),	.X(NAN59));
NA2 _NAND60	(.A1(LAD[3]/LD[3]),	.A2(NAN59),	.X(NAN60));
NA2 _NAND61	(.A1(LAD[2]/LD[2]),	.A2(NAN60),	.X(NAN61));
NA2 _NAND62	(.A1(LAD[1]/LD[1]),	.A2(NAN61),	.X(NAN62));
NA2 _NAND63	(.A1(LAD[0]/LD[0]),	.A2(NAN62),	.X(NAN63));
NA2 _NAND64	(.A1(AD[31]),	.A2(NAN63),	.X(NAN64));
NA2 _NAND65	(.A1(AD[30]),	.A2(NAN64),	.X(NAN65));
NA2 _NAND66	(.A1(AD[29]),	.A2(NAN65),	.X(NAN66));
NA2 _NAND67	(.A1(AD[28]),	.A2(NAN66),	.X(NAN67));
NA2 _NAND68	(.A1(AD[27]),	.A2(NAN67),	.X(NAN68));
NA2 _NAND69	(.A1(AD[26]),	.A2(NAN68),	.X(NAN69));
NA2 _NAND70	(.A1(AD[25]),	.A2(NAN69),	.X(NAN70));
NA2 _NAND71	(.A1(AD[24]),	.A2(NAN70),	.X(NAN71));
NA2 _NAND72	(.A1(AD[23]),	.A2(NAN71),	.X(NAN72));
NA2 _NAND73	(.A1(AD[22]),	.A2(NAN72),	.X(NAN73));
NA2 _NAND74	(.A1(AD[21]),	.A2(NAN73),	.X(NAN74));
NA2 _NAND75	(.A1(AD[20]),	.A2(NAN74),	.X(NAN75));

Table 12-10. Sequential Interconnection of the PCI 9054 NANDTREE (Pin Definition) (continued)

Component Name	Input #1	Input #2	Output
NA2 _NAND76	(.A1(AD[19]),	.A2(NAN75),	.X(NAN76));
NA2 _NAND77	(.A1(AD[18]),	.A2(NAN76),	.X(NAN77));
NA2 _NAND78	(.A1(AD[17]),	.A2(NAN77),	.X(NAN78));
NA2 _NAND79	(.A1(AD[16]),	.A2(NAN78),	.X(NAN79));
NA2 _NAND80	(.A1(AD[15]),	.A2(NAN79),	.X(NAN80));
NA2 _NAND81	(.A1(AD[14]),	.A2(NAN80),	.X(NAN81));
NA2 _NAND82	(.A1(AD[13]),	.A2(NAN81),	.X(NAN82));
NA2 _NAND83	(.A1(AD[12]),	.A2(NAN82),	.X(NAN83));
NA2 _NAND84	(.A1(AD[11]),	.A2(NAN83),	.X(NAN84));
NA2 _NAND85	(.A1(AD[10]),	.A2(NAN84),	.X(NAN85));
NA2 _NAND86	(.A1(AD[9]),	.A2(NAN85),	.X(NAN86));
NA2 _NAND87	(.A1(AD[8]),	.A2(NAN86),	.X(NAN87));
NA2 _NAND88	(.A1(AD[7]),	.A2(NAN87),	.X(NAN88));
NA2 _NAND89	(.A1(AD[6]),	.A2(NAN88),	.X(NAN89));
NA2 _NAND90	(.A1(AD[5]),	.A2(NAN89),	.X(NAN90));
NA2 _NAND91	(.A1(AD[4]),	.A2(NAN90),	.X(NAN91));
NA2 _NAND92	(.A1(AD[3]),	.A2(NAN91),	.X(NAN92));
NA2 _NAND93	(.A1(AD[2]),	.A2(NAN92),	.X(NAN93));
NA2 _NAND94	(.A1(AD[1]),	.A2(NAN93),	.X(NAN94));
NA2 _NAND95	(.A1(AD[0]),	.A2(NAN94),	.X(NAN95));
NA2 _NAND96	(.A1(RETRY#/BREQo),	.A2(NAN95),	.X(NAN96));
NA2 _NAND97	(.A1(BB#/BREQi),	.A2(NAN96),	.X(NAN97));
NA2 _NAND98	(.A1(BI#/BTERM#),	.A2(NAN97),	.X(NAN98));
NA2 _NAND99	(.A1(TA#/READY#),	.A2(NAN98),	.X(NAN99));
NA2 _NAND100	(.A1(LINT#),	.A2(NAN99),	.X(NAN100));
NA2 _NAND101	(.A1(BG#/LHOLDA),	.A2(NAN100),	.X(NAN101));
NA2 _NAND102	(.A1(RDWR#/LW/R#),	.A2(NAN101),	.X(NAN102));
NA2 _NAND103	(.A1(TS#/ADS#),	.A2(NAN102),	.X(NAN103));
NA2 _NAND104	(.A1(BURST#/BLAST#),	.A2(NAN103),	.X(NAN104));
NA2 _NAND105	(.A1(USERi/DACK0#/LLOCKi#),	.A2(NAN104),	.X(NAN105));
NA2 _NAND106	(.A1(CCS#),	.A2(NAN105),	.X(NAN106));
NA2 _NAND107	(.A1(MODE0),	.A2(NAN106),	.X(NAN107));
NA2 _NAND108	(.A1(MODE1),	.A2(NAN107),	.X(NAN108));
NA2 _NAND109	(.A1(TSIZ[1]/LBE[2]#),	.A2(NAN108),	.X(NAN109));
NA2 _NAND110	(.A1(TSIZ[0]/LBE[3]#),	.A2(NAN109),	.X(NAN110));
NA2 _NAND111	(.A1(WAIT#/BDIP#),	.A2(NAN110),	.X(NAN111));
NA2 _NAND112	(.A1(DP[0]),	.A2(NAN111),	.X(NAN112));
NA2 _NAND113	(.A1(DP[1]),	.A2(NAN112),	.X(NAN113));
NA2 _NAND114	(.A1(DP[2]),	.A2(NAN113),	.X(NAN114));
NA2 _NAND115	(.A1(DP[3]),	.A2(NAN114),	.X(NAN115));
NA2 _NAND116	(.A1(MDREQ#/DMPAF/EOT#),	.A2(NAN115),	.X(NAN116));

Table 12-10. Sequential Interconnection of the PCI 9054 NANDTREE (Pin Definition) (continued)

Component Name	Input #1	Input #2	Output
NA2 _NAND117	(.A1(BR#/LHOLD),	.A2(NAN116),	.X(NAN117));
NA2 _NAND118	(.A1(LRESETo#),	.A2(NAN117),	.X(NAN118));
NA2 _NAND119	(.A1(TEA#/LSERR#),	.A2(NAN118),	.X(NAN119));
NA2 _NAND120	(.A1(FRAME#),	.A2(NAN119),	.X(NAN120));
NA2 _NAND121	(.A1(IRDY#),	.A2(NAN120),	.X(NAN121));
NA2 _NAND122	(.A1(DEVSEL#),	.A2(NAN121),	.X(NAN122));
NA2 _NAND123	(.A1(TRDY#),	.A2(NAN122),	.X(NAN123));
NA2 _NAND124	(.A1(STOP#),	.A2(NAN123),	.X(NAN124));
NA2 _NAND125	(.A1(PAR),	.A2(NAN124),	.X(NAN125));
NA2 _NAND126	(.A1(SERR#),	.A2(NAN125),	.X(NAN126));
NA2 _NAND127	(.A1(LOCK#),	.A2(NAN126),	.X(NAN127));
NA2 _NAND128	(.A1(GNT#),	.A2(NAN127),	.X(NAN128));
NA2 _NAND129	(.A1(IDSEL),	.A2(NAN128),	.X(NAN129));
NA2 _NAND130	(.A1(CBE[0]#),	.A2(NAN129),	.X(NAN130));
NA2 _NAND131	(.A1(CBE[1]#),	.A2(NAN130),	.X(NAN131));
NA2 _NAND132	(.A1(CBE[2]#),	.A2(NAN131),	.X(NAN132));
NA2 _NAND133	(.A1(CBE[3]#),	.A2(NAN132),	.X(NAN133));
NA2 _NAND134	(.A1(REQ#),	.A2(NAN133),	.X(NAN134));
NA2 _NAND135	(.A1(RST#),	.A2(NAN134),	.X(NAN135));
NA2 _NAND136	(.A1(INTA#),	.A2(NAN135),	.X(NAN136));
NA2 _NAND137	(.A1(PME#),	.A2(NAN136),	.X(NAN137));
NA2 _NAND138	(.A1(BIGEND#/WAIT#),	.A2(NAN137),	.X(NAN138));
NA2 _NAND139	(.A1(PERR#),	.A2(NAN138),	.X(NAN139));
NA2 _NAND140	(.A1(EECS),	.A2(NAN139),	.X(NAN140));
NA2 _NAND141	(.A1(EESK),	.A2(NAN140),	.X(NAN141));
NA2 _NAND142	(.A1(EEDI/EEDO),	.A2(NAN141),	.X(NAN142));
NA2 _NAND143	(.A1(ENUM#),	.A2(NAN142),	.X(USERo/DREQ0#/LLOCKo#));

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13. ELECTRICAL SPECIFICATIONS

13.1 General Electrical Specifications

Table 13-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage Temperature	-55 °C to +125 °C
Ambient Temperature with Power Applied	-40 °C to +85 °C
Supply Voltage to Ground	-0.5V to +4.6V
Input Voltage (VIN)	VSS -0.5V to 5.5V
Output Voltage (VOUT)	VSS -0.5V to VDD +0.5
Maximum Package Power Dissipation (176-Pin PQFP)	1.0W
Maximum Package Power Dissipation (225-Pin PBGA)	1.0W

Table 13-2. Operating Ranges

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)	
		Min	Max
-40 °C to +85 °C	3.0V to 3.6V	VSS	VDD

Table 13-3. Capacitance (Sample Tested Only)

Parameter	Test Conditions	Pin Type	Value		Units
			Typical	Maximum	
CIN	VIN = 0V	Input	4	6	pF
COUT	VOUT = 0V	Output	6	10	pF

Table 13-4. Thermal Resistance of Packages (Θ_{j-a})

Package Type	Air Flow			
	0m/sec	1m/sec	2m/sec	3m/sec
176-Pin PQFP	65 (°C/W)	45	35	30
225-Pin PBGA	72 (°C/W)	46	37	32

Table 13-5. Electrical Characteristics over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min VIN = VIH or VIL	IOH = -12.0 mA	2.4	—	V
VOL	Output Low Voltage		IOL = 12 mA	—	0.4	V
VIH	Input High Level	—	—	2.0	5.5	V
VIL	Input Low Level	—	—	-0.5	0.8	V
VOH3	PCI 3.3V Output High Voltage	VDD = Min VIN = VIH or VIL	IOH = -500 µA	0.9 VDD	—	V
VOL3	PCI 3.3V Output Low Voltage		IOL = 1500 µA	—	0.1 VDD	V
VIH3	PCI 3.3V Input High Level	—	—	0.5 VDD	VDD +0.5	V
VIL3	PCI 3.3V Input Low Level	—	—	-0.5	0.3 VDD	V
IIL	Input Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	µA
ILPC	DC Current Per Pin During Pre-Charge	VP = 0.8V to 1.2V		—	1.0	mA
IOZ	Tri-State Output Leakage Current	VDD = Max		-10	+10	µA
ICC	Power Supply Current [2]	VDD=3.6V, PCLK = 33 MHz, LCLK = 50 MHz 120 outputs switching simultaneously		—	250	mA
ICCL ICCH ICCZ	Quiescent Power Supply Current	VCC = Max VIN = GND or VCC		—	50	µA

Notes:

1 *ILPC is the DC current flowing from VDD to Ground during precharge, as both PMOS and NMOS devices remain on during precharge. It is not the leakage current flowing into or out of the pin under precharge.*

2 *Maximum value based upon I_2O simultaneously switching outputs.*

13.2 Local Inputs

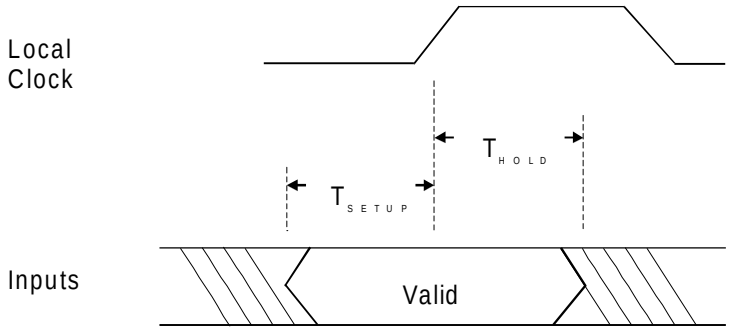

Figure 13-1. PCI 9054 Local Input Setup and Hold Waveform

Table 13-6. AC Electrical Characteristics (Local Inputs) over Operating Range (M Mode)

Signals (Synchronous Inputs) C_L = 50 pF, Vcc = 3.0V, Ta = 85 °C	T_{SETUP} (ns) (WORST CASE)	T_{HOLD} (ns) (WORST CASE)
BB#	5.0	2
BDIP#/WAIT#	6.0	2
BG#	7.0	2
BI#	9.0	2
BIGEND#/WAIT#	7.0	2
BURST#	6.0	2
CCS#	1.5	2
DP[0:3]	3.0	2
LA[0:31]	6.0	2
LD[0:31]	3.5	2
MDREQ#/DMPAF/EOT#	8.5 (EOT#)	2
RD/WR#	6.0	2
TA#	8.0	2
TS#	5.0	2
TSIZ[0:1]	6.0	2
USERi//DACK0#/LLOCKi#	7.0 (LLOCKi#)	2
USERo/DREQ0#/LLOCKo#	7.0 (DREQ0#)	2
Input Clocks	Min	Max
Local Clock Input Frequency	0	50 MHz
PCI Clock Input Frequency	0	33 MHz

Note: *These values are provided only for example purposes and are representative of general performance characteristics of the PLX PCI Bus Masters.*

Table 13-7. AC Electrical Characteristics (Local Inputs) over Operating Range (C and J Modes)

Signals (Synchronous Inputs) C_L = 50 pF, Vcc = 3.0V, Ta = 85 °C	Bus Mode	T_{SETUP} (ns) (WORST CASE)	T_{HOLD} (ns) (WORST CASE)
ADS#	C, J	5.0	2
ALE	J	3.5	2
BIGEND#	C, J	7.0	2
BLAST#	C, J	6.5	2
BREQi	C, J	5.0	2
BTERM#	C, J	9.5	2
CCS#	C, J	1.5	2
DMPAF/EOT#	C, J	8.5 (EOT#)	2
DP[3:0]	C, J	3.0	2
LAD[31:0]	J	6.5	2
LBE[3:0]#	C, J	9.0	2
LD[31:0]	C	3.5	2
LHOLDA	C, J	7.0	2
LW/R#	C, J	8.5	2
READY#	C, J	9.5	2
USERi//DACK0#/LLOCKi#	C, J	7.0 (LLOCKi#)	2
USERo/DREQ0#/LLOCKo#	C, J	7.0 (DREQ0#)	2
WAIT#	C, J	7.0	2
Input Clocks	**Bus Mode**	**Min**	**Max**
Local Clock Input Frequency	C, J	0	50 MHz
PCI Clock Input Frequency	C, J	0	33 MHz

Note: *These values are provided only for example purposes and are representative of general performance characteristics of the PLX PCI Bus Masters.*

13.3 Local Outputs

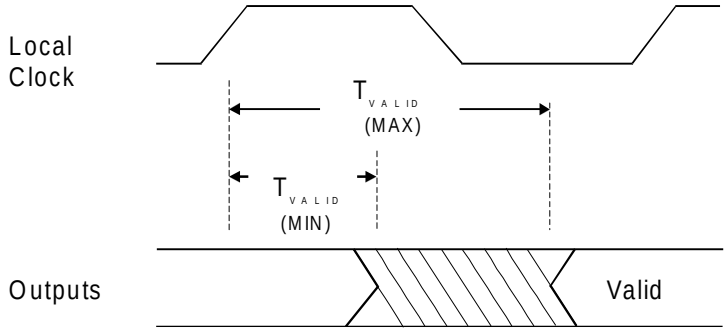

Figure 13-2. PCI 9054 Local Output Delay

Table 13-8. AC Electrical Characteristics (Local Outputs) over Operating Range (M Mode)

Signals (Synchronous Outputs) C_L = 50 pF, Vcc = 3.0V, Ta = 85 °C	Clock to Out Worst Case (ns) T_{VALID} (Max)
BB#	9.5
BDIP#	10.5
BI#	9.0
BIGEND#/WAIT#	10.5 (WAIT#)
BR#	10.0
BURST#	10.5
DP[0:3]	10.0
LA[0:31]	10.0
LD[0:31]	11.0
MDREQ#/DMPAF/EOT#	13.0 (MDREQ#/DMPAF)
RD/WR#	12.0
RETRY#	9.0
TA#	9.0
TEA#	8.5
TS#	10.0
TSIZ[0:1]	10.0
USERi//DACK0#/LLOCKi#	10.5 (DACK0#)
USERo/DREQ0#/LLOCKo#	9.5 (USERo/LLOCKo#)

Notes: *All T_{VALID} (Mins) values are greater than 5 ns.*

Timing derating for loading is ±35 PS/PF.

These values are provided only for example purposes and are representative of general performance characteristics of the PLX PCI Bus Masters.

Table 13-9. AC Electrical Characteristics (Local Outputs) over Operating Range (C and J Modes)

Signals (Synchronous Outputs) C_L = 50 pF, Vcc = 3.0V, Ta = 85 °C	Bus Mode	Output T_{VALID} (Max)
ADS#	C, J	10.0
BLAST#	C, J	12.5
BREQo	C, J	8.5
BTERM#	C, J	10.0
DEN#	J	10.0
DMPAF/EOT#	C, J	13.0 (DMPAF)
DP[3:0]	C, J	10.0
DT/R#	J	12.5
LA[31:2]	C	10.0
LA[28:2]	J	9.5
LAD[31:0]	J	11.0
LBE[3:0]#	C, J	10.0
LD[31:0]	C	11.0
LHOLD	C, J	10.0
LSERR#	C, J	8.5
LW/R#	C, J	12.0
READY#	C, J	9.5
USERi/DACK0#/LLOCKi#	C, J	10.5 (DACK0#)
USERo/DREQ0#/LLOCKo#	C, J	9.5 (USERo/LLOCKo#)
WAIT#	C, J	10.5

Notes: *All T_{VALID} (Mins) values are greater than 5 ns.*

Timing derating for loading is ±35 PS/PF.

These values are provided only for example purposes and are representative of general performance characteristics of PLX PCI Bus Masters.

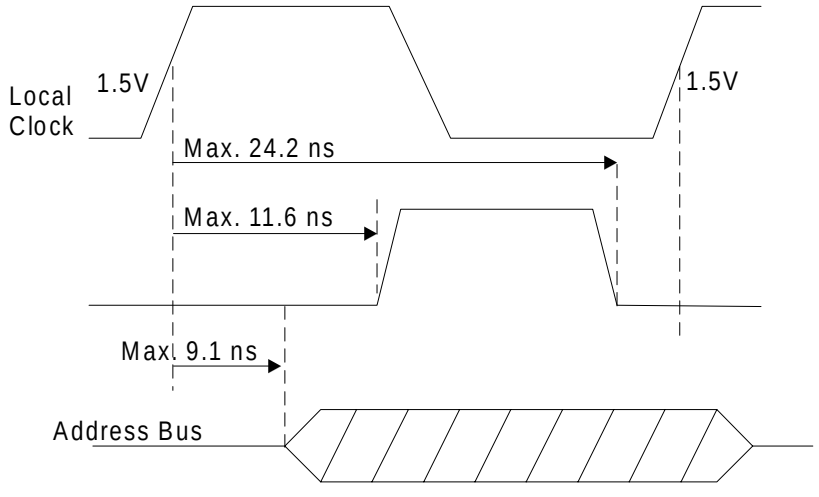

Figure 13-3. PCI 9054 ALE Output Delay to the Local Clock

14. PACKAGE, SIGNAL, AND PINOUT SPECS

14.1 176-Pin PQFP

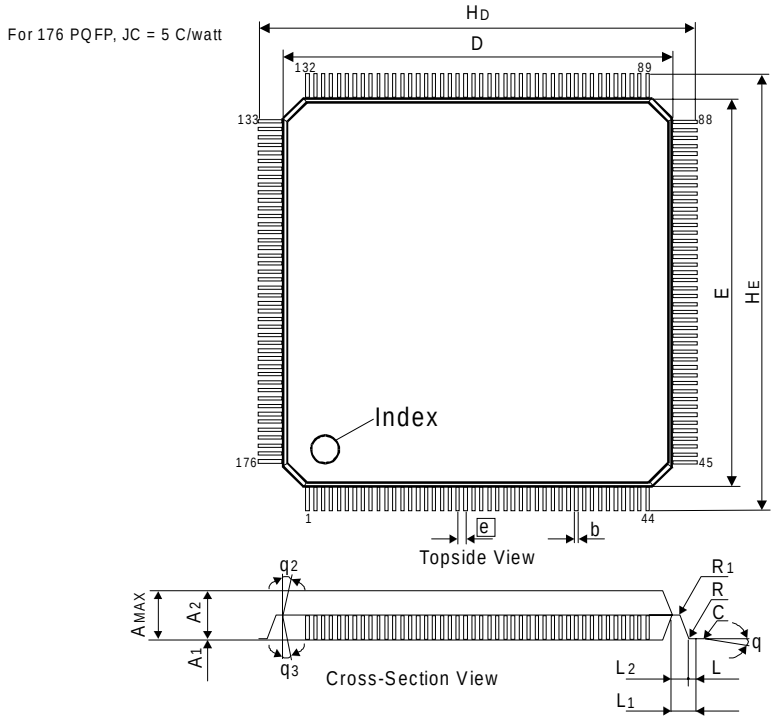

Figure 14-1. 176-Pin PQFP Package Mechanical Dimensions

Table 14-1. 176-Pin PQFP Package Mechanical Dimensions

Lead Type STD (QfP18-176 Pin STD)			
Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
E	23.9	24	24.1
D	23.9	24	24.1
A	—	—	3
A1	—	0.1	—
A2	2.6	2.7	2.8
e	—	0.5	—
b	0.15	0.2	0.3
C	0.1	0.15	0.2
θ	0°	—	10°
L	0.3	0.5	0.7
L1	—	1	—
L2	—	0.5	—
HE	25.6	26	26.4
HD	25.6	26	26.4
θ2	—	15°	—
θ3	—	15°	—
R	—	0.2	—
R1	—	0.2	—

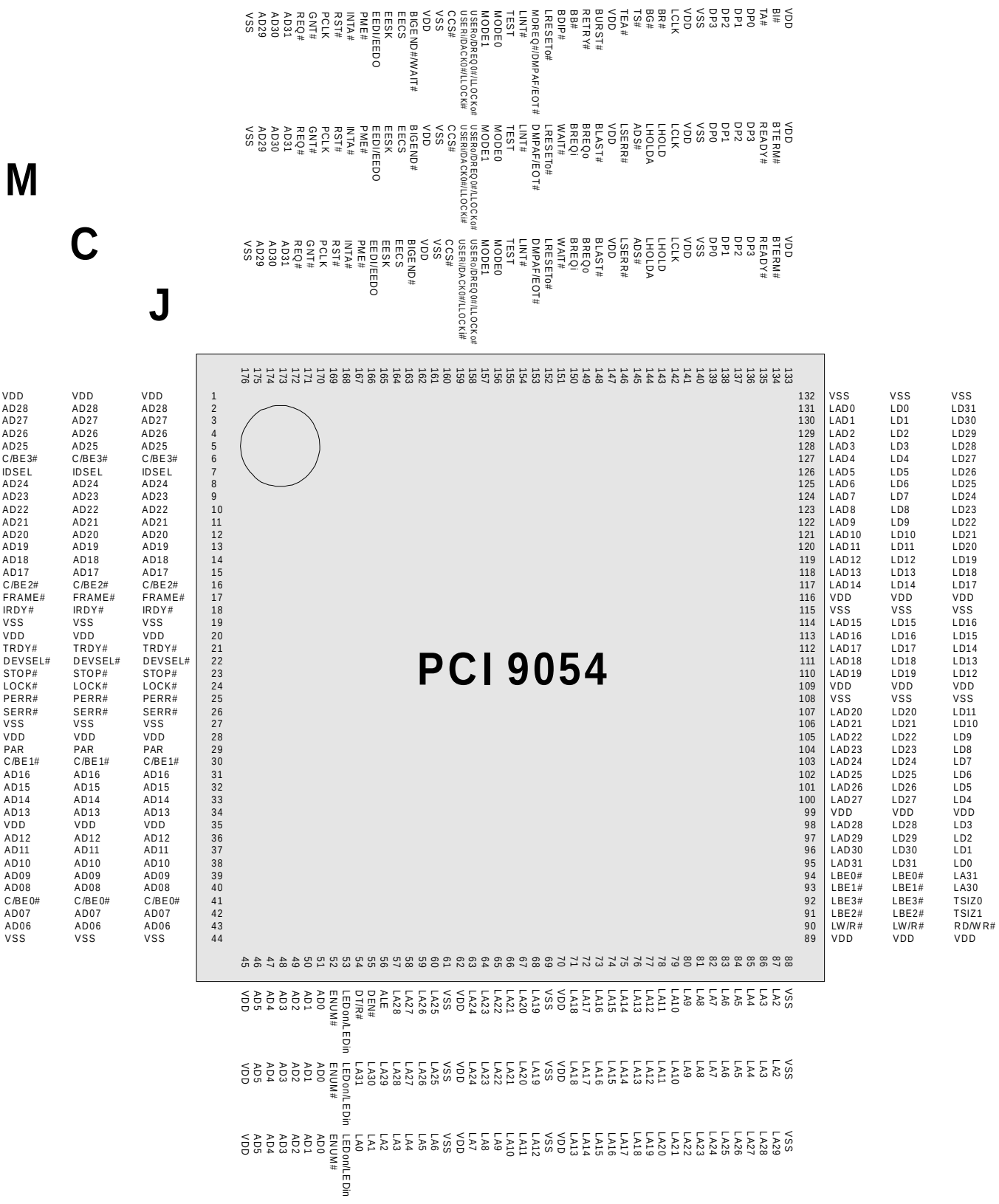

Figure 14-2. 176-Pin PQFP PCI 9054 Pinout

14.2 225-Pin PBGA

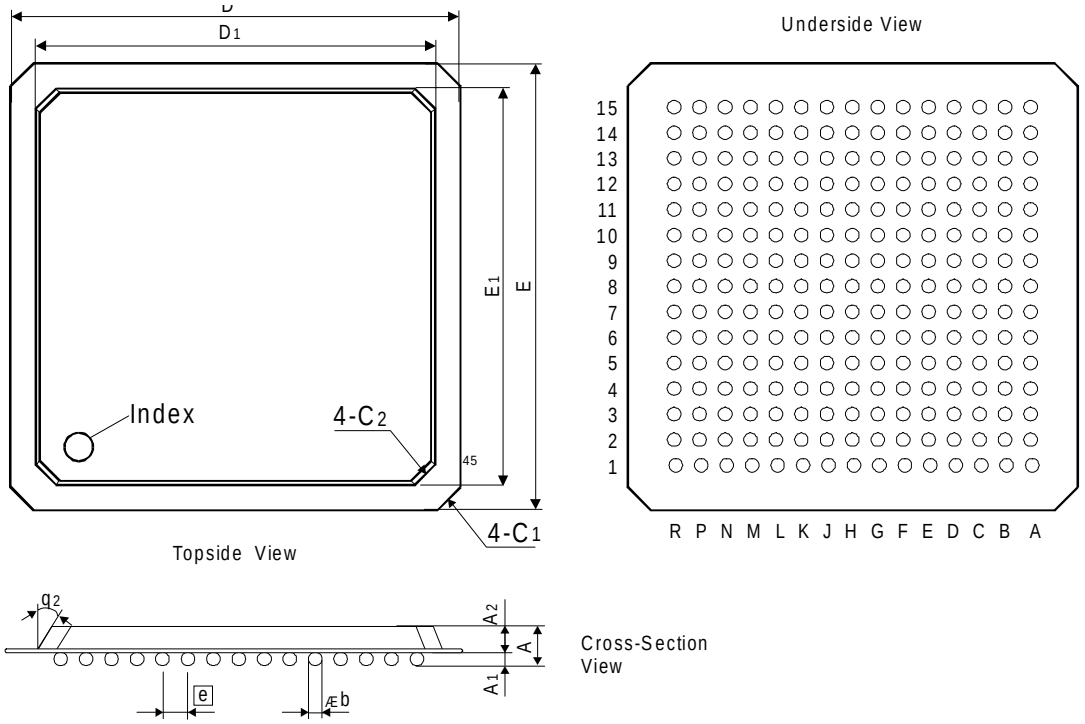

Figure 14-3. 225-Pin PBGA Package Mechanical Dimensions

Table 14-2. 225-Pin PBGA Package Mechanical Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
ø b	0.6	0.75	0.90
A	—	2.13	—
A1	0.5	0.6	0.7
A2	1.43	1.53	1.63
θ2	—	25°	—
C1	—	1.5	—
C2	—	1.2	—
e	—	1.5	—
D1	23.9	24	24.1
E1	23.9	24	24.1
D	—	27	—
E	—	27	—

G = GND

	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
15	R15	P15	N15	M15	L15	K15	J15	H15	G15	F15	E15	D15	C15	B15	A15
14	R14	P14	N14	M14	L14	K14	J14	H14	G14	F14	E14	D14	C14	B14	A14
13	R13	P13	N13	M13	L13	K13	J13	H13	G13	F13	E13	D13	C13	B13	A13
12	R12	P12	N12	M12	L12	K12	J12	H12	G12	F12	E12	D12	C12	B12	A12
11	R11	P11	N11	M11	L11	K11	J11	H11	G11	F11	E11	D11	C11	B11	A11
10	R10	P10	N10	M10	L10	K10	J10	H10	G10	F10	E10	D10	C10	B10	A10
9	R9	P9	N9	M9	L9	K9	J9	H9	G9	F9	E9	D9	C9	B9	A9
8	R8	P8	N8	M8	L8	K8	J8	H8	G8	F8	E8	D8	C8	B8	A8
7	R7	P7	N7	M7	L7	K7	J7	H7	F7	F7	E7	D7	C7	B7	A7
6	R6	P6	N6	M6	L6	K6	J6	H6	G6	F6	E6	D6	C6	B6	A6
5	R5	P5	N5	M5	L5	K5	J5	H5	G5	F5	E5	D5	C5	B5	A5
4	R4	P4	N4	M4	L4	K4	J4	H4	G4	F4	E4	D4	C4	B4	A4
3	R3	P3	N3	M3	L3	K3	J3	H3	G3	F3	E3	D3	C3	B3	A3
2	R2	P2	N2	M2	L2	K2	J2	H2	G2	F2	E2	D2	C2	B2	A2
1	R1	P1	N1	M1	L1	K1	J1	H1	G1	F1	E1	D1	C1	B1	A1

13 Connected Grounds (40 Total Grounds)

28 No Connects (NC)

Figure 14-4. 225-Pin PBGA Package Layout (Underside View)

Table 14-3. 225-Pin PBGA PCI 9054 Pinout

Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode
A1	VDD (Core)	All	C1	IDSEL	All	E1	NC	All	G1	IRDY#	All
A2	AD30	All	C2	AD26	All	E2	VDD (Core)	All	G2	VDD (Core)	All
A3	PCLK	All	C3	AD29	All	E3	AD21	All	G3	FRAME#	All
A4	PME#	All	C4	GNT#	All	E4	NC	All	G4	C/BE2#	All
A5	NC	All	C5	EEDI/EEDO	All	E5	AD25	All	G5	VDD (Core)	All
A6	VDD (Core)	All	C6	BIGEND#/WAIT# BIGEND#	M C, J	E6	NC	All	G6	AD23	All
A7	USERo/DREQ0#/ LLOCKo#	All	C7	USERi/DACK0#/ LLOCKi#	All	E7	CCS#	All	G7	VSS	All
A8	TEST	All	C8	NC	All	E8	MODE0	All	G8	VSS	All
A9	LRESETo#	All	C9	BB# BREQi	M C, J	E9	MDREQ#/DMPAF/EOT# DMPAF/EOT#	M C, J	G9	VSS	All
A10	RETRY# BREQo	M C, J	C10	VDD (Core)	All	E10	NC	All	G10	LD20 LD11 LAD11	M C J
A11	TS# ADS#	M C, J	C11	VDD (Core)	All	E11	DP1 DP2	M C, J	G11	LD17 LD14 LAD14	M C J
A12	BR# LHOLD	M C, J	C12	DP2 DP1	M C, J	E12	LD25 LD6 LAD6	M C J	G12	VDD (Core)	All
A13	DP3 DP0	M C, J	C13	LD31 LD0 LAD0	M C J	E13	LD22 LD9 LAD9	M C J	G13	LFRAME#	All
A14	TA# READY#	M C, J	C14	LD28 LD3 LAD3	M C J	E14	LD21 LD10 LAD10	M C J	G14	LD15 LD16 LAD16	M C J
A15	VDD (Core)	All	C15	LD26 LD5 LAD5	M C J	E15	VDD (Core)	All	G15	LD16 LD15 LAD15	M C J
B1	AD27	All	D1	AD22	All	F1	NC	All	H1	DEVSEL#	All
B2	NC	All	D2	AD24	All	F2	AD17	All	H2	NC	All
B3	REQ#	All	D3	C/BE3#	All	F3	AD18	All	H3	TRDY#	All
B4	INTA#	All	D4	AD28	All	F4	AD19	All	H4	STOP#	All
B5	EESK	All	D5	RST#	All	F5	AD20	All	H5	VDD (Core)	All
B6	VDD (Core)	All	D6	VDD (Core)	All	F6	AD31	All	H6	VSS	All
B7	MODE1	All	D7	NC	All	F7	EECS	All	H7	VSS	All
B8	LINT#	All	D8	VDD (Core)	All	F8	VSS	All	H8	VSS	All
B9	BDIP# WAIT#	M C	D9	VDD (Core)	All	F9	NC	All	H9	VSS	All
B10	BURST# BLAST#	M C, J	D10	TEA# LSERR#	M C, J	F10	LD29 LD2 LAD2	M C J	H10	VSS	All
B11	BG# LHOLDA	M C, J	D11	LCLK	All	F11	NC	All	H11	LD14 LD17 LAD17	M C J
B12	VDD (Core)	All	D12	BI# BTERM#	M C, J	F12	NC	All	H12	VDD (Core)	All
B13	DP0 DP3	M C, J	D13	LD27 LD4 LAD4	M C J	F13	LD19 LD12 LAD12	M C J	H13	NC	All
B14	NC	All	D14	LD24 LD7 LAD7	M C J	F14	LD18 LD13 LAD13	M C J	H14	LD12 LD19 LAD19	M C J
B15	LD30 LD1 LAD1	M C J	D15	LD23 LD8 LAD8	M C J	F15	NC	All	H15	LD13 LD18 LAD18	M C J

Table 14-3. 225-Pin PBGA PCI 9054 Pinout (continued)

Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode	Pin #	Symbol	Bus Mode
J1	PERR#	All	L1	AD15	All	N1	AD10	All	R1	VDD (Core)	All
J2	LOCK#	All	L2	VDD (Core)	All	N2	AD8	All	R2	AD4	All
J3	SERR#	All	L3	NC	All	N3	AD6	All	R3	AD0	All
J4	VDD (Core)	All	L4	AD11	All	N4	AD1	All	R4	LA0 LA31 DT/R#	M C J
J5	VDD (Core)	All	L5	AD2	All	N5	LA1 LA30 DEN#	M C J	R5	NC	All
J6	AD16	All	L6	LA2 LA29 ALE	M C J	N6	LA4 LA27	M C, J	R6	VDD (Core)	All
J7	VSS	All	L7	LA8 LA23	M C, J	N7	NC	All	R7	LA7 LA24	M C, J
J8	VSS	All	L8	VDD (Core)	All	N8	LA9 LA22	M C, J	R8	LA10 LA21	M C, J
J9	VSS	All	L9	LA14 LA17	M C, J	N9	LA13 LA18	M C, J	R9	VDD (Core)	All
J10	LD2 LD29 LAD29	M C J	L10	LA21 LA10	M C, J	N10	LA16 LA15	M C, J	R10	LA15 LA16	M C, J
J11	VDD (Core)	All	L11	LA30 LBE1#	M C, J	N11	VDD (Core)	All	R11	LA18 LA13	M C, J
J12	LD9 LD22 LAD22	M C J	L12	NC	All	N12	LA24 LA7	M C, J	R12	LA20 LA11	M C, J
J13	VDD (Core)	All	L13	VDD (Core)	All	N13	LA28 LA3	M C, J	R13	LA23 LA8	M C, J
J14	LD10 LD21 LAD21	M C J	L14	LD4 LD27 LAD27	M C J	N14	TSIZ0 LBE3#	M C, J	R14	LA27 LA4	M C, J
J15	LD11 LD20 LAD20	M C J	L15	LD5 LD26 LAD26	M C J	N15	LD0 LD31 LAD31	M C J	R15	VDD (Core)	All
K1	PAR	All	M1	AD13	All	P1	AD7	All			
K2	NC	All	M2	AD12	All	P2	NC	All			
K3	C/BE1#	All	M3	AD9	All	P3	AD3	All			
K4	AD14	All	M4	AD5	All	P4	ENUM#	All			
K5	VDD (Core)	All	M5	NC	All	P5	VDD (Core)	All			
K6	C/BE0#	All	M6	LA3 LA28	M C, J	P6	LA5 LA26	M C, J			
K7	LEDon/LEDin	All	M7	LA6 LA25	M C, J	P7	VDD (Core)	All			
K8	VSS	All	M8	LA11 LA20	M C, J	P8	NC	All			
K9	LA17 LA14	M C, J	M9	NC	All	P9	LA12 LA19	M C, J			
K10	LA26 LA5	M C, J	M10	LA19 LA12	M C, J	P10	VDD (Core)	All			
K11	VDD (Core)	All	M11	LA22 LA9	M C, J	P11	NC	All			
K12	LD6 LD25 LAD25	M C J	M12	RD/WR# LW/R#	M C, J	P12	NC	All			
K13	LD7 LD24 LAD24	M C J	M13	LA31 LBE0#	M C, J	P13	LA25 LA6	M C, J			
K14	NC	All	M14	LD1 LD30 LAD30	M C J	P14	LA29 LA2	M C, J			
K15	LD8 LD23 LAD23	M C J	M15	LD3 LD28 LAD28	M C J	P15	TSIZ1 LBE2#	M C, J			

15. ORDERING INSTRUCTIONS

The PCI 9054 is a 32-bit 33-MHz PCI Bus Master I/O Accelerator featuring advanced Data Pipe Architecture technology, which includes two DMA engines, programmable Target and Initiator Data Transfer modes, and PCI messaging functions. The PCI 9054 offers 3.3V, 5V tolerant PCI and Local signaling supports Universal PCI Adapter designs, 3.3V core, low-power CMOS offered in two package options, a 176-pin PQFP and 225-pin (ball) PBGA. The device is designed to operate at Industrial Temperature range.

Table 15-1. Available Packages

Package	Ordering Part Number
176-pin PQFP	PCI 9054-AA50PI
225-pin PBGA	PCI 9054-AA50BI