

FEATURES

- Low V_{OS} **$25\mu\text{V}$ Max**
- Low V_{OS} Drift **$0.6\mu\text{V}/^\circ\text{C}$ Max**
- Ultra-Stable vs Time **$1.0\mu\text{V}/\text{Month}$ Max**
- Low Noise **$0.6\mu\text{V}_{p-p}$ Max**
- Wide Input Voltage Range **$\pm 14\text{V}$**
- Wide Supply Voltage Range **$\pm 3\text{V}$ to $\pm 18\text{V}$**
- Fits 725, 108A/308A, 741, AD510 Sockets
- 125°C Temperature-Tested Dice

ORDERING INFORMATION [†]

| $T_A = +25^\circ\text{C}$ V_{OS} MAX (μV) | PACKAGE | | | | OPERATING TEMPERATURE RANGE |
|--|---------|-----------------|----------------------|-------------------|-----------------------------------|
| | TO-99 | CERDIP 8-PIN | PLASTIC 8-PIN | LCC 20-CONTACT | |
| 25 | OP07AJ* | OP07AZ* | — | — | MIL |
| 75 | OP07EJ | OP07EZ | OP07EP | — | COM |
| 75 | OP07J* | OP07Z* | — | OP07RC/883 | MIL |
| 150 | OP07CJ | OP07CZ | OP07CP | — | XIND |
| 150 | — | — | OP07CS ^{††} | — | XIND |
| 150 | OP07DJ | — | OP07DP | — | XIND |

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

^{††} For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-07 has very low input offset voltage ($25\mu\text{V}$ max for OP-07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current ($\pm 2\text{nA}$ for OP-07A) and high open-loop gain ($300\text{V}/\text{mV}$ for OP-07A). The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain instrumentation applications.

The wide input voltage range of $\pm 13\text{V}$ minimum combined with high CMRR of 110dB (OP-07A) and high input impedance provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained

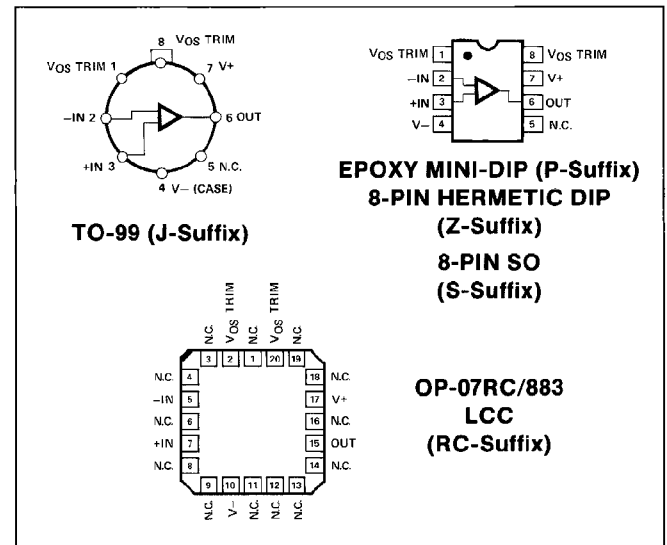
even at high closed-loop gains.

Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP-07, even at high gain, combined with the freedom from external nulling have made the OP-07 a new industry standard for instrumentation and military applications.

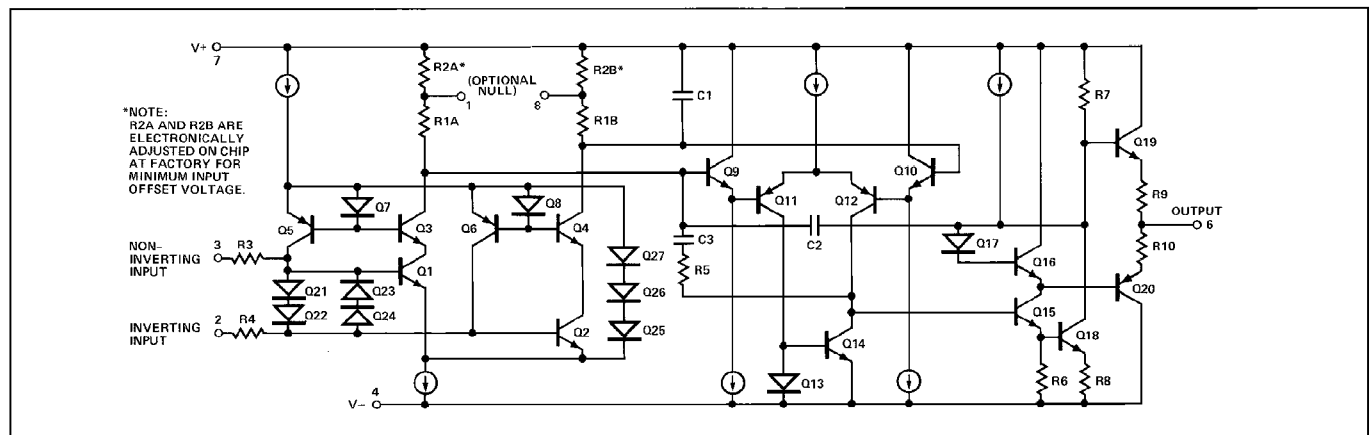
The OP-07 is available in five standard performance grades. The OP-07A and the OP-07 are specified for operation over the full military range of -55°C to $+125^\circ\text{C}$; the OP-07E is specified for operation over the 0°C to $+70^\circ\text{C}$ range, and OP-07C and D over the -40°C to $+85^\circ\text{C}$ temperature range.

The OP-07 is available in hermetically-sealed TO-99 metal can or ceramic 8-pin Mini-DIP, and in epoxy 8-pin Mini-DIP. It is a direct replacement for 725, 108A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. The OP-207, a dual OP-07, is available for applications requiring close matching of two OP-07 amplifiers. For improved specifications, see the OP-77/OP-177.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OP07

ABSOLUTE MAXIMUM RATINGS (Note 1)

| | |
|--|-----------------|
| Supply Voltage | ±22V |
| Differential Input Voltage | ±30V |
| Input Voltage (Note 2) | ±22V |
| Output Short-Circuit Duration | Indefinite |
| Storage Temperature Range | |
| J, RC and Z Packages | −65°C to +150°C |
| P Package | −65°C to +125°C |
| Operating Temperature Range | |
| OP-07A, OP-07, OP-07RC | −55°C to +125°C |
| OP-07E | 0°C to +70°C |
| OP-07C, OP-07D | −40°C to +85°C |
| Lead Temperature (Soldering, 60 sec) | +300°C |
| Junction Temperature (T _J) | +150°C |

| PACKAGE TYPE | θ _{JA} (Note 3) | θ _{JC} | UNITS |
|------------------------|--------------------------|-----------------|-------|
| TO-99 (J) | 150 | 18 | °C/W |
| 8-Pin Hermetic DIP (Z) | 148 | 16 | °C/W |
| 8-Pin Plastic DIP (P) | 103 | 43 | °C/W |
| 20-Contact LCC | 98 | 38 | °C/W |
| 8-Pin SO (S) | 158 | 43 | °C/W |

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-07A | | | OP-07 | | | UNITS |
|--|------------------------|--|--------|-------|------|-------|-------|------|-------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input Offset Voltage | V _{OS} | (Note 1) | — | 10 | 25 | — | 30 | 75 | μV |
| Long-Term Input Offset Voltage Stability | ΔV _{OS} /Time | (Note 2) | — | 0.2 | 1.0 | — | 0.2 | 1.0 | μV/Mo |
| Input Offset Current | I _{OS} | | — | 0.3 | 2.0 | — | 0.4 | 2.8 | nA |
| Input Bias Current | I _B | | — | ±0.7 | ±2.0 | — | ±1.0 | ±3.0 | nA |
| Input Noise Voltage | e _{np-p} | 0.1Hz to 10Hz (Note 3) | — | 0.35 | 0.6 | — | 0.35 | 0.6 | μV _{p-p} |
| Input Noise Voltage Density | e _n | f _O = 10Hz (Note 3) | — | 10.3 | 18.0 | — | 10.3 | 18.0 | nV/√Hz |
| | | f _O = 100Hz (Note 3) | — | 10.0 | 13.0 | — | 10.0 | 13.0 | |
| | | f _O = 1000Hz (Note 3) | — | 9.6 | 11.0 | — | 9.6 | 11.0 | |
| Input Noise Current | i _{np-p} | 0.1Hz to 10Hz (Note 3) | — | 14 | 30 | — | 14 | 30 | pA _{p-p} |
| Input Noise Current Density | i _n | f _O = 10Hz (Note 3) | — | 0.32 | 0.80 | — | 0.32 | 0.80 | pA/√Hz |
| | | f _O = 100Hz (Note 3) | — | 0.14 | 0.23 | — | 0.14 | 0.23 | |
| | | f _O = 1000Hz (Note 3) | — | 0.12 | 0.17 | — | 0.12 | 0.17 | |
| Input Resistance — Differential-Mode | R _{IN} | (Note 4) | 30 | 80 | — | 20 | 60 | — | MΩ |
| Input Resistance — Common-Mode | R _{INCM} | | — | 200 | — | — | 200 | — | GΩ |
| Input Voltage Range | IVR | | ±13 | ±14 | — | ±13 | ±14 | — | V |
| Common-Mode Rejection Ratio | CMRR | V _{CM} = ±13V | 110 | 126 | — | 110 | 126 | — | dB |
| Power Supply Rejection Ratio | PSRR | V _S = ±3V to ±18V | — | 4 | 10 | — | 4 | 10 | μV/V |
| Large-Signal Voltage Gain | A _{VO} | R _L ≥ 2kΩ, V _O = ±10V | 300 | 500 | — | 200 | 500 | — | V/mV |
| | | R _L ≥ 500Ω, V _O = ±0.5V, V _S = ±3V (Note 4) | 150 | 400 | — | 150 | 400 | — | |
| Output Voltage Swing | V _O | R _L ≥ 10kΩ | ±12.5 | ±13.0 | — | ±12.5 | ±13.0 | — | V |
| | | R _L ≥ 2kΩ | ±12.0 | ±12.8 | — | ±12.0 | ±12.8 | — | |
| | | R _L ≥ 1kΩ | ±10.5 | ±12.0 | — | ±10.5 | ±12.0 | — | |
| Slew Rate | SR | R _L ≥ 2kΩ (Note 3) | 0.1 | 0.3 | — | 0.1 | 0.3 | — | V/μs |
| Closed-Loop Bandwidth | BW | A _{VCL} = +1 (Note 3) | 0.4 | 0.6 | — | 0.4 | 0.6 | — | MHz |
| Open-Loop Output Resistance | R _O | V _O = 0, I _O = 0 | — | 60 | — | — | 60 | — | Ω |
| Power Consumption | P _d | V _S = ±15V, No Load | — | 75 | 120 | — | 75 | 120 | mW |
| | | V _S = ±3V, No Load | — | 4 | 6 | — | 4 | 6 | |
| Offset Adjustment Range | | R _P = 20kΩ | — | ±4 | — | — | ±4 | — | mV |

NOTES:

1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation.

Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.

3. Sample tested.
4. Guaranteed by design.

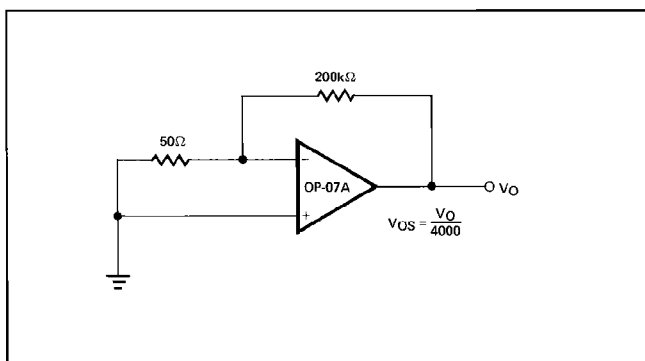
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-07A | | | OP-07 | | | UNITS |
|--|-------------|---------------------------------------|----------|------------|---------|----------|------------|---------|------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input Offset Voltage | V_{OS} | (Note 1) | — | 25 | 60 | — | 60 | 200 | μV |
| Average Input Offset Voltage Drift Without External Trim | TCV_{OS} | (Note 2) | — | 0.2 | 0.6 | — | 0.3 | 1.3 | $\mu V/^\circ C$ |
| With External Trim | TCV_{OSn} | $R_P = 20k\Omega$ (Note 3) | — | 0.2 | 0.6 | — | 0.3 | 1.3 | $\mu V/^\circ C$ |
| Input Offset Current | I_{OS} | | — | 0.8 | 4 | — | 1.2 | 5.6 | nA |
| Average Input Offset Current Drift | TCI_{OS} | (Note 2) | — | 5 | 25 | — | 8 | 50 | $pA/^\circ C$ |
| Input Bias Current | I_B | | — | ± 1 | ± 4 | — | ± 2 | ± 6 | nA |
| Average Input Bias Current Drift | TCI_B | (Note 2) | — | 8 | 25 | — | 13 | 50 | $pA/^\circ C$ |
| Input Voltage Range | IVR | | ± 13 | ± 13.5 | — | ± 13 | ± 13.5 | — | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = \pm 13V$ | 106 | 123 | — | 106 | 123 | — | dB |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 3V$ to $\pm 18V$ | — | 5 | 20 | — | 5 | 20 | $\mu V/V$ |
| Large-Signal Voltage Gain | A_{VO} | $R_L \geq 2k\Omega$, $V_O = \pm 10V$ | 200 | 400 | — | 150 | 400 | — | V/mV |
| Output Voltage Swing | V_O | $R_L \geq 2k\Omega$ | ± 12 | ± 12.6 | — | ± 12 | ± 12.6 | — | V |

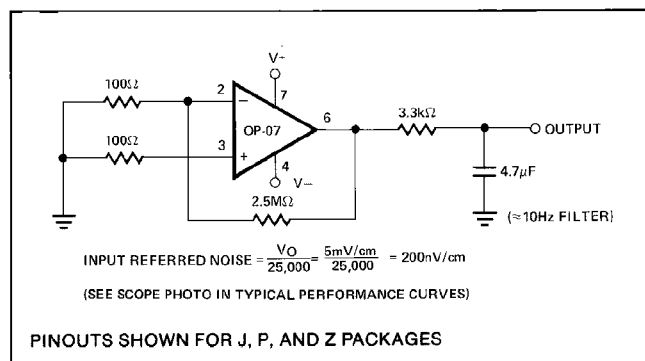
NOTES:

1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT

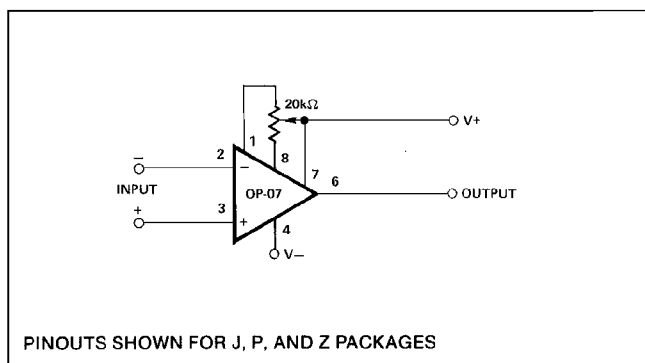


TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT

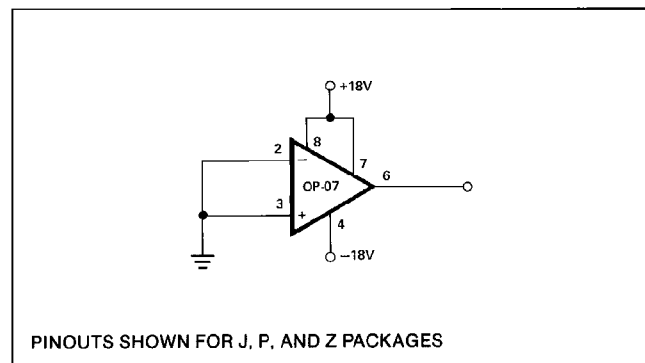


PINOUTS SHOWN FOR J, P, AND Z PACKAGES

OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-07E | | | OP-07C | | | OP-07D | | | UNITS |
|--------------------------------------|----------------------|---|------------|------------|-----------|------------|------------|-----------|------------|------------|----------|-----------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input Offset Voltage | V_{OS} | (Note 1) | — | 30 | 75 | — | 60 | 150 | — | 60 | 150 | μV |
| Long-Term V_{OS} Stability | V_{OS}/Time | (Note 2) | — | 0.3 | 1.5 | — | 0.4 | 2.0 | — | 0.5 | 3.0 | $\mu V/\text{Mo}$ |
| Input Offset Current | I_{OS} | | — | 0.5 | 3.8 | — | 0.8 | 6.0 | — | 0.8 | 6.0 | nA |
| Input Bias Current | I_B | | — | ± 1.2 | ± 4.0 | — | ± 1.8 | ± 7.0 | — | ± 2.0 | ± 12 | nA |
| Input Noise Voltage | e_{np-p} | 0.1Hz to 10Hz (Note 3) | — | 0.35 | 0.6 | — | 0.38 | 0.65 | — | 0.38 | 0.65 | μV_{p-p} |
| Input Noise Voltage Density | e_n | $f_O = 10\text{Hz}$ | — | 10.3 | 18.0 | — | 10.5 | 20.0 | — | 10.5 | 20.0 | $nV/\sqrt{\text{Hz}}$ |
| | | $f_O = 100\text{Hz}$ (Note 3) | — | 10.0 | 13.0 | — | 10.2 | 13.5 | — | 10.3 | 13.5 | |
| | | $f_O = 1000\text{Hz}$ | — | 9.6 | 11.0 | — | 9.8 | 11.5 | — | 9.8 | 11.5 | |
| Input Noise Current | i_{np-p} | 0.1Hz to 10Hz (Note 3) | — | 14 | 30 | — | 15 | 35 | — | 15 | 35 | pA_{p-p} |
| Input Noise Current Density | i_n | $f_O = 10\text{Hz}$ | — | 0.32 | 0.80 | — | 0.35 | 0.90 | — | 0.35 | 0.90 | $pA/\sqrt{\text{Hz}}$ |
| | | $f_O = 100\text{Hz}$ (Note 3) | — | 0.14 | 0.23 | — | 0.15 | 0.27 | — | 0.15 | 0.27 | |
| | | $f_O = 1000\text{Hz}$ | — | 0.12 | 0.17 | — | 0.13 | 0.18 | — | 0.13 | 0.18 | |
| Input Resistance — Differential-Mode | R_{IN} | (Note 4) | 15 | 50 | — | 8 | 33 | — | 7 | 31 | — | M Ω |
| Input Resistance — Common-Mode | R_{INCM} | | — | 160 | — | — | 120 | — | — | 120 | — | G Ω |
| Input Voltage Range | IVR | | ± 13 | ± 14 | — | ± 13 | ± 14 | — | ± 13 | ± 14 | — | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = \pm 13V$ | 106 | 123 | — | 100 | 120 | — | 94 | 110 | — | dB |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 3V$ to $\pm 18V$ | — | 5 | 20 | — | 7 | 32 | — | 7 | 32 | $\mu V/V$ |
| Large-Signal Voltage Gain | A_{VO} | $R_L \geq 2k\Omega$, $V_O = \pm 10V$ | 200 | 500 | — | 120 | 400 | — | 120 | 400 | — | V/mV |
| | | $R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 4) | 150 | 400 | — | 100 | 400 | — | — | 400 | — | |
| Output Voltage Swing | V_O | $R_L \geq 10k\Omega$ | ± 12.5 | ± 13.0 | — | ± 12.0 | ± 13.0 | — | ± 12.0 | ± 13.0 | — | V |
| | | $R_L \geq 2k\Omega$ | ± 12.0 | ± 12.8 | — | ± 11.5 | ± 12.8 | — | ± 11.5 | ± 12.8 | — | |
| | | $R_L \geq 1k\Omega$ | ± 10.5 | ± 12.0 | — | — | ± 12.0 | — | — | ± 12.0 | — | |
| Slew Rate | SR | $R_L \geq 2k\Omega$ (Note 3) | 0.1 | 0.3 | — | 0.1 | 0.3 | — | 0.1 | 0.3 | — | V/ μs |
| Closed-Loop Bandwidth | BW | $A_{VCL} = +1$ (Note 5) | 0.4 | 0.6 | — | 0.4 | 0.6 | — | 0.4 | 0.6 | — | MHz |
| Open-Loop Output Resistance | R_O | $V_O = 0, I_O = 0$ | — | 60 | — | — | 60 | — | — | 60 | — | Ω |
| Power Consumption | P_d | $V_S = \pm 15V$, No Load | — | 75 | 120 | — | 80 | 150 | — | 80 | 150 | mW |
| | | $V_S = \pm 3V$, No Load | — | 4 | 6 | — | 4 | 8 | — | 4 | 8 | |
| Offset Adjustment Range | | $R_P = 20k\Omega$ | — | ± 4 | — | — | ± 4 | — | — | ± 4 | — | mV |

NOTES:

- Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
- Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves. Parameter is sample tested.
- Sample tested.
- Guaranteed by design.
- Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-07E, and $-40^\circ C \leq T_A \leq +85^\circ C$ for OP-07C/D, unless otherwise noted.

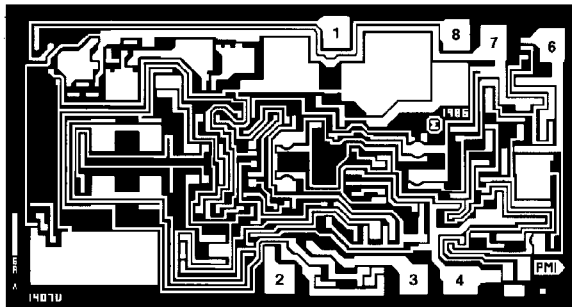
| PARAMETER | SYMBOL | CONDITIONS | OP-07E | | | OP-07C | | | OP-07D | | | UNITS |
|--|-------------|--|------------|------------|-----------|------------|------------|-----------|------------|------------|----------|------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| Input Offset Voltage | V_{OS} | (Note 1) | — | 45 | 130 | — | 85 | 250 | — | 85 | 250 | μV |
| Average Input Offset Voltage Drift Without External Trim | TCV_{OS} | (Note 3) | — | 0.3 | 1.3 | — | 0.5 | 1.8 | — | 0.7 | 2.5 | $\mu V/^\circ C$ |
| With External Trim | TCV_{OSn} | $R_P = 20k\Omega$ (Note 3) | — | 0.3 | 1.3 | — | 0.4 | 1.6 | — | 0.7 | 2.5 | $\mu V/^\circ C$ |
| Input Offset Current | I_{OS} | | — | 0.9 | 5.3 | — | 1.6 | 8.0 | — | 1.6 | 8.0 | nA |
| Average Input Offset Current Drift | TCI_{OS} | (Note 2) | — | 8 | 35 | — | 12 | 50 | — | 12 | 50 | $pA/^\circ C$ |
| Input Bias Current | I_B | | — | ± 1.5 | ± 5.5 | — | ± 2.2 | ± 9.0 | — | ± 3.0 | ± 14 | nA |
| Average Input Bias Current Drift | TCI_B | (Note 2) | — | 13 | 35 | — | 18 | 50 | — | 18 | 50 | $pA/^\circ C$ |
| Input Voltage Range | IVR | | ± 13.0 | ± 13.5 | — | ± 13.0 | ± 13.5 | — | ± 13.0 | ± 13.5 | — | V |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = \pm 13V$ | 103 | 123 | — | 97 | 120 | — | 94 | 106 | — | dB |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 3V$ to $\pm 18V$ | — | 7 | 32 | — | 10 | 51 | — | 10 | 51 | $\mu V/V$ |
| Large-Signal Voltage Gain | A_{VO} | $R_L \geq 2k\Omega$ $V_O = \pm 10V$ | 180 | 450 | — | 100 | 400 | — | 100 | 400 | — | V/mV |
| Output Voltage Swing | V_O | $R_L \geq 2k\Omega$ | ± 12 | ± 12.6 | — | ± 11 | ± 12.6 | — | ± 11 | ± 12.6 | — | V |

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

OP07

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
6. OUTPUT
7. V+
8. BALANCE

DIE SIZE 0.100 × 0.055 inch, 5500 sq. mils
(2.54 × 1.40 mm, 3.56 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-07N, OP-07G and OP-07GR devices; $T_A = 125^\circ C$ for OP-07NT and OP-07GT devices, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | OP-07NT LIMIT | OP-07N LIMIT | OP-07GT LIMIT | OP-07G LIMIT | OP-07GR LIMIT | UNITS |
|---------------------------------------|----------|-------------------------------------|------------------|-----------------|------------------|-----------------|------------------|----------------|
| Input Offset Voltage | V_{OS} | | 140 | 40 | 210 | 80 | 150 | μV MAX |
| Input Offset Current | I_{OS} | | 4.0 | 2.0 | 5.6 | 2.8 | 6.0 | nA MAX |
| Input Bias Current | I_B | | ± 4 | ± 2 | ± 6 | ± 3 | ± 7 | nA MAX |
| Input Resistance Differential-Mode | R_{IN} | (Note 2) | — | 20 | — | 20 | 8 | M Ω MIN |
| Input Voltage Range | IVR | | ± 13 | ± 13 | ± 13 | ± 13 | ± 13 | V MIN |
| Common-Mode Rejection Ratio | CMRR | $V_{CM} = \pm 13V$ | 100 | 110 | 100 | 110 | 100 | dB MIN |
| Power Supply Rejection Ratio | PSRR | $V_S = \pm 3V$ to $\pm 18V$ | 20 | 10 | 20 | 10 | 30 | $\mu V/V$ MAX |
| Output Voltage Swing | V_O | $R_L = 10k\Omega$ | — | ± 12.5 | — | ± 12.0 | ± 12.0 | V MIN |
| | | $R_L = 2k\Omega$ | ± 12.0 | ± 12.0 | ± 12.0 | ± 11.5 | ± 11.5 | |
| | | $R_L = 1k\Omega$ | — | ± 10.5 | — | ± 10.5 | — | |
| Large-Signal Voltage Gain | A_{VO} | $R_L = 2k\Omega$ $V_O = \pm 10V$ | 200 | 200 | 150 | 120 | 120 | V/mV MIN |
| Differential Input Voltage | | | ± 30 | ± 30 | ± 30 | ± 30 | ± 30 | V MAX |
| Power Consumption | P_d | $V_{OUT} = 0V$ | — | 120 | — | 120 | 150 | mW MAX |

NOTES:

1. For 25°C characteristics of OP-07NT and OP-07GT, see OP-07N and OP-07G characteristics, respectively.
2. Guaranteed by design.

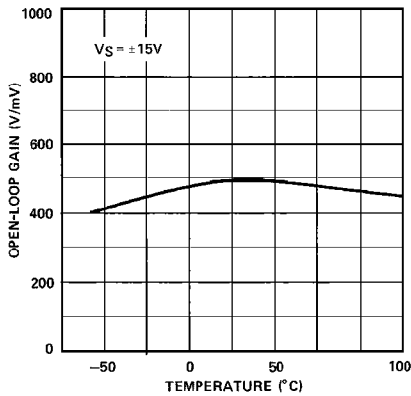
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

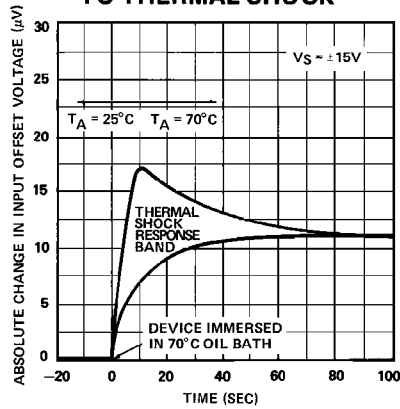
| PARAMETER | SYMBOL | CONDITIONS | OP-07NT TYPICAL | OP-07N TYPICAL | OP-07GT TYPICAL | OP-07G TYPICAL | OP-07GR TYPICAL | UNITS |
|---------------------------------------|-------------|--------------------------------------|--------------------|-------------------|--------------------|-------------------|--------------------|------------------|
| Average Input Offset Voltage Drift | TCV_{OS} | $R_S = 50\Omega$ | 0.2 | 0.2 | 0.3 | 0.3 | 0.7 | $\mu V/^\circ C$ |
| Nullled Input Offset Voltage Drift | TCV_{OSn} | $R_S = 50\Omega$, $R_P = 20k\Omega$ | 0.2 | 0.2 | 0.3 | 0.3 | 0.7 | $\mu V/^\circ C$ |
| Average Input Offset Current Drift | TCI_{OS} | | 5 | 5 | 8 | 8 | 12 | pA/°C |
| Slew Rate | SR | $R_L \geq 2k\Omega$ | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | V/ μs |
| Closed-Loop Bandwidth | BW | $A_{VCL} = +1$ | 0.6 | 0.6 | 0.6 | 0.6 | 0.6 | MHz |

TYPICAL PERFORMANCE CHARACTERISTICS

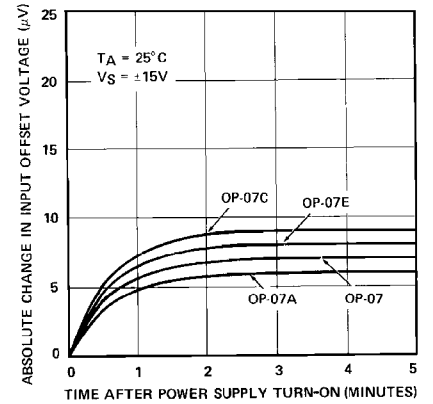
OPEN-LOOP GAIN vs TEMPERATURE



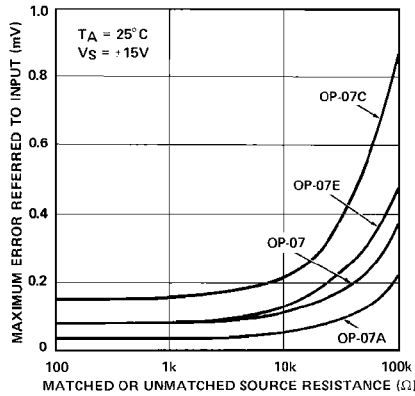
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



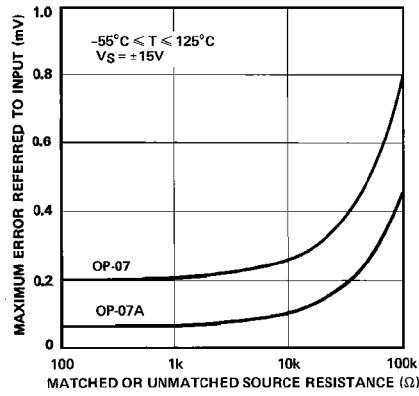
WARM-UP DRIFT



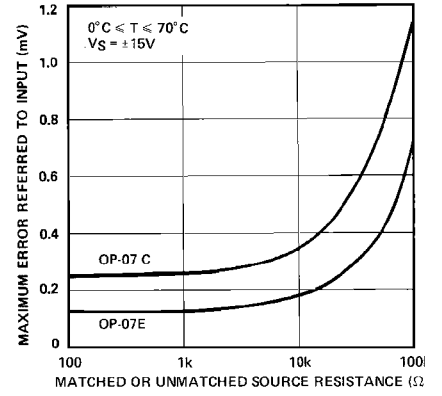
MAXIMUM ERROR vs SOURCE RESISTANCE



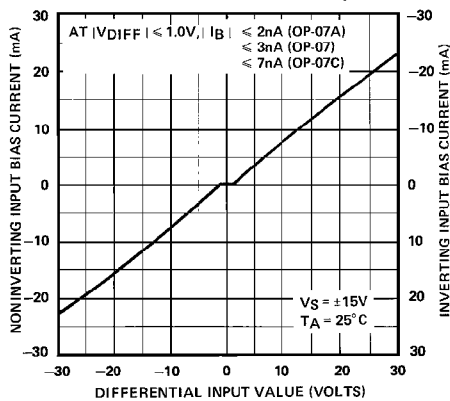
MAXIMUM ERROR vs SOURCE RESISTANCE



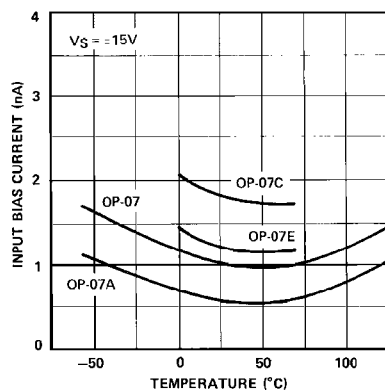
MAXIMUM ERROR vs SOURCE RESISTANCE



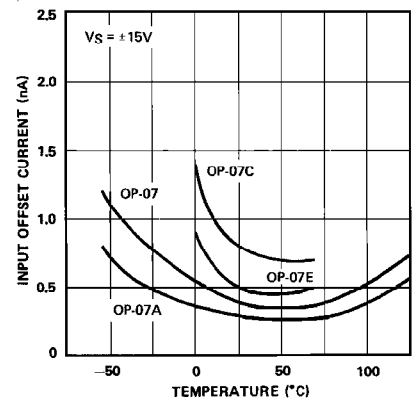
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

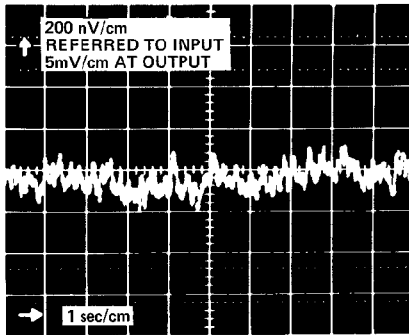


INPUT OFFSET CURRENT vs TEMPERATURE

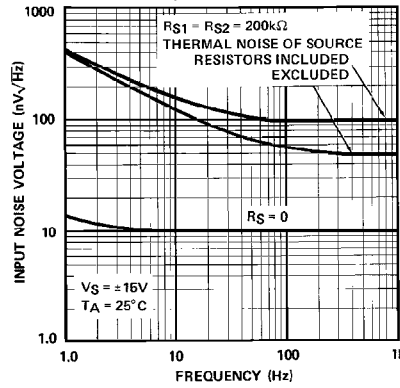


TYPICAL PERFORMANCE CHARACTERISTICS

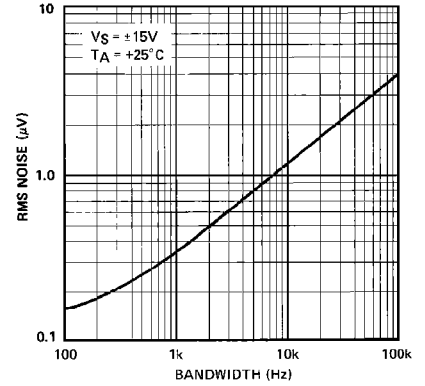
OP-07 LOW FREQUENCY NOISE



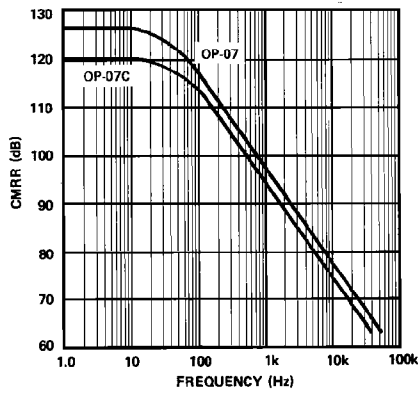
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



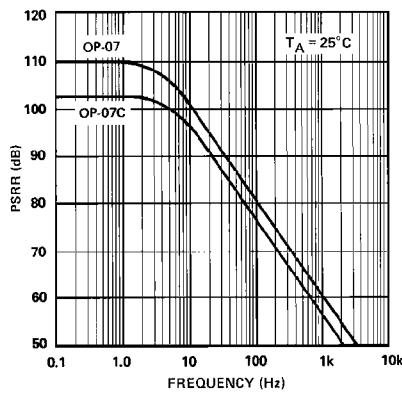
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



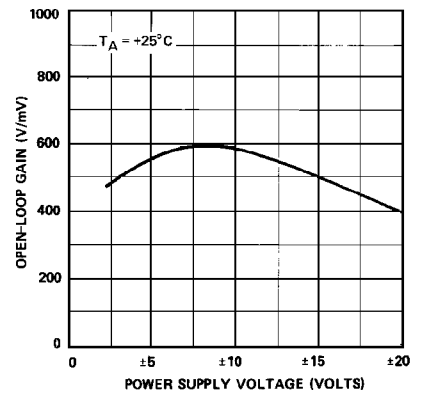
CMRR vs FREQUENCY



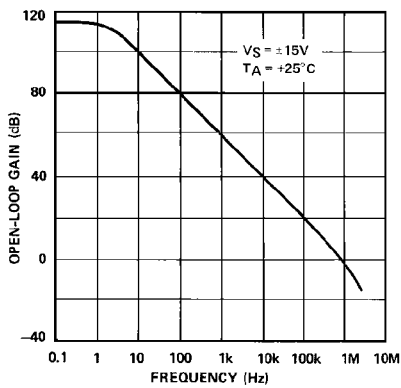
PSRR vs FREQUENCY



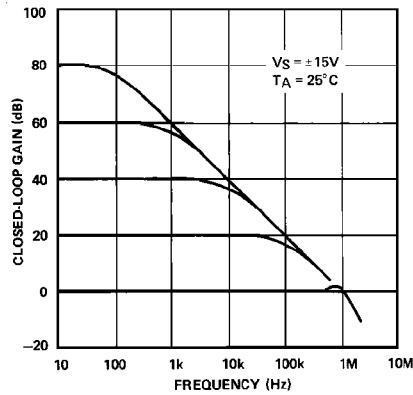
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



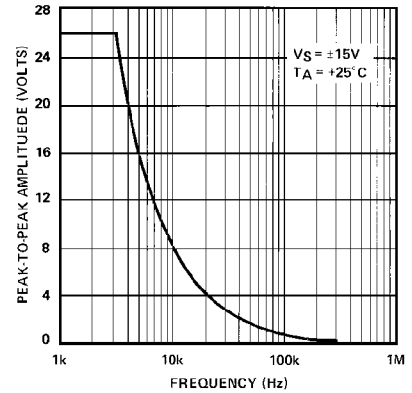
OPEN-LOOP FREQUENCY RESPONSE



CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

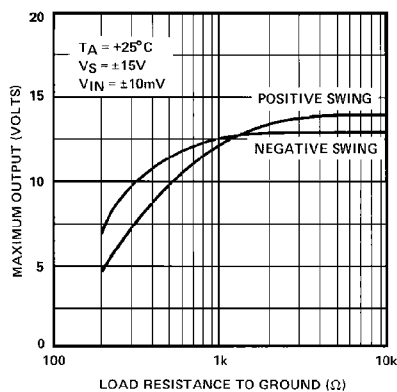


MAXIMUM OUTPUT SWING vs FREQUENCY

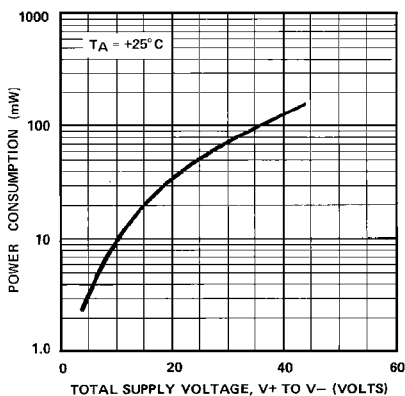


TYPICAL PERFORMANCE CHARACTERISTICS

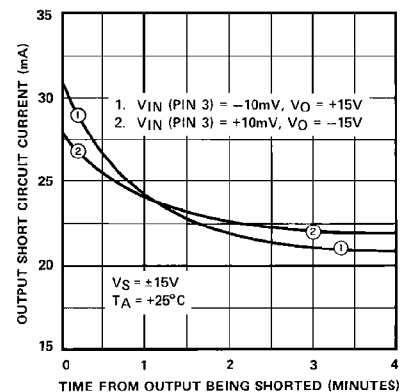
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



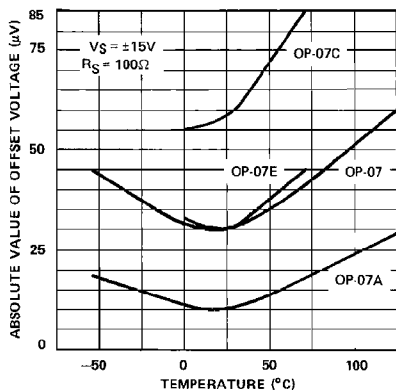
POWER CONSUMPTION vs POWER SUPPLY



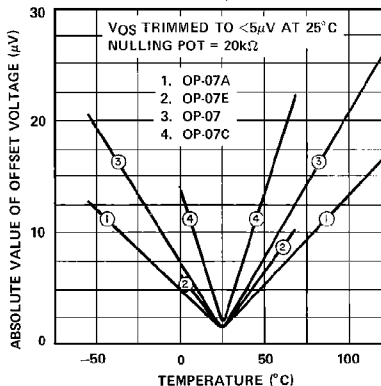
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



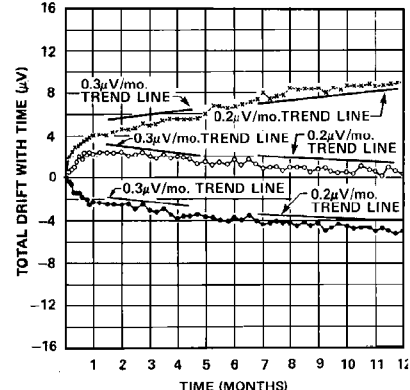
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



TRIMMED OFFSET VOLTAGE vs TEMPERATURE

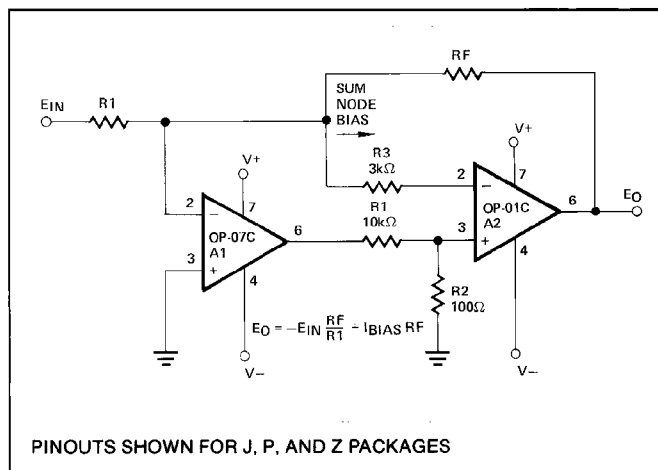


OFFSET VOLTAGE STABILITY vs TIME

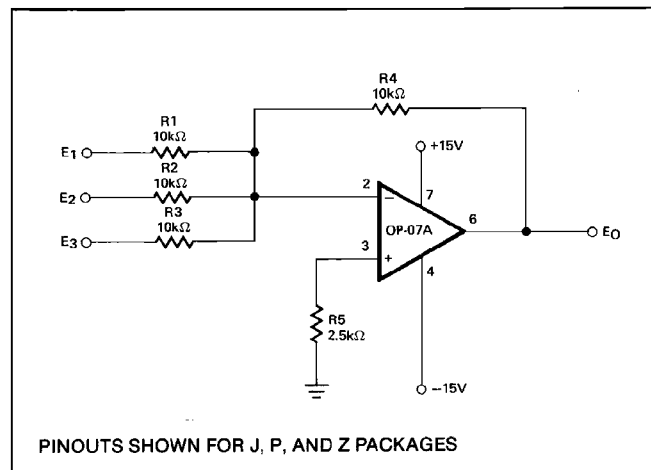


TYPICAL APPLICATIONS

HIGH SPEED, LOW VOS, COMPOSITE AMPLIFIER



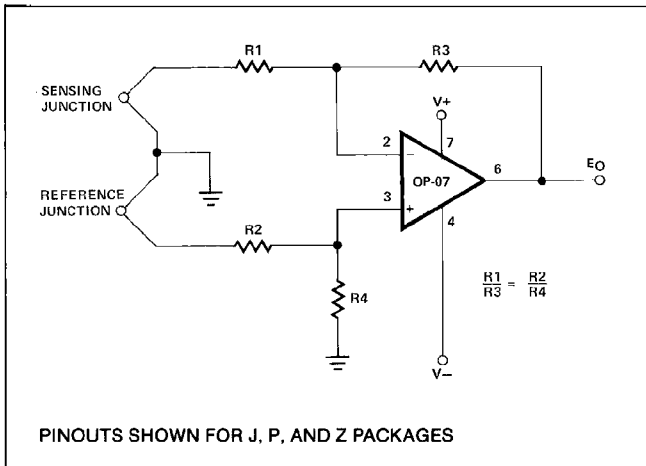
ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER



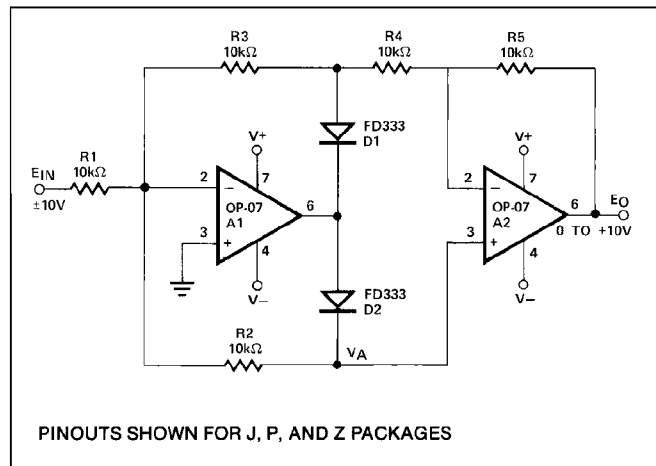
OP07

TYPICAL APPLICATIONS

HIGH-STABILITY THERMOCOUPLE AMPLIFIER



PRECISION ABSOLUTE-VALUE CIRCUIT



APPLICATIONS INFORMATION

OP-07 series units may be substituted directly into 725, 108A/308A* and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-07 may be used in unnulling 741-type sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram).

The OP-07 provides stable operation with load capacitance of up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

*TO-99 Package only