NPC

OVERVIEW

The NR8576 series devices are serial-interface type real-time clock modules with built-in crystal oscillator elements. They feature timer counter circuits that keep track of time from the current second to the current year, automatic leap-year adjustment, and a supply voltage detect function. Also, a 32.768kHz/1Hz select output function is incorporated for independent hardware control.

FEATURES

- Crystal oscillator element built-in for adjustment-free use
- Timer counters for second, minute, hour, day, day of the week, month, and year
- 2.5 to 5.5V operating voltage range
- 1.7 ± 0.3V supply voltage detection threshold
- 1.0μA at 3.0V (typ) current consumption
- Automatic leap-year calendar adjustment
- 32.768kHz and 1Hz output selectable
- Package: 14-pin SOP

SERIES CONFIGURATION

Device	Package	Frequency deviation
NR8576AA	14-pin SOP	5 ± 12 ppm
NR8576AB		5 ± 23 ppm

PINOUT

(Top view)
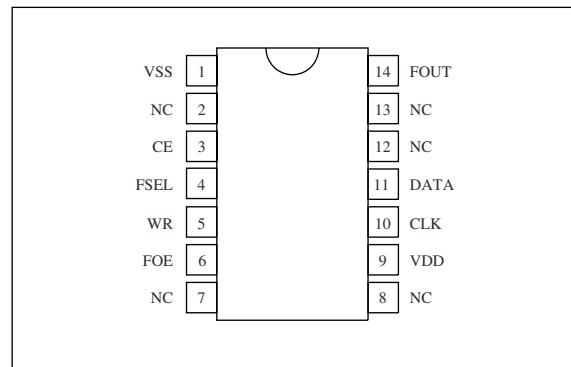
PACKAGE DIMENSIONS

(Unit: mm)
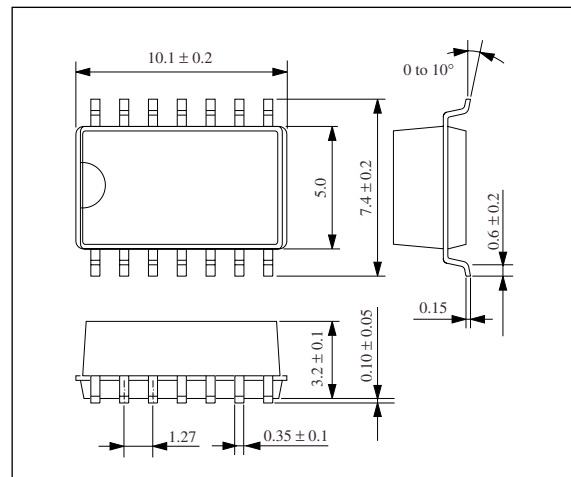
BLOCK DIAGRAM
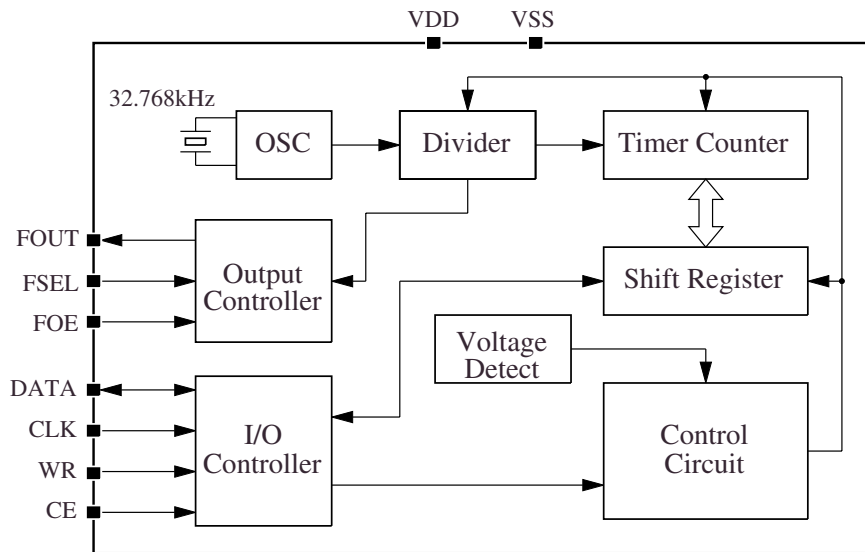
PIN DESCRIPTION

Number	Name	I/O	Description
1	VSS	–	Ground Connect a ≥ 0.1μF capacitor between VDD and VSS.
2	NC	–	No connection. Leave open for normal use.
3	CE	I	Chip enable. HIGH: Enable LOW: DATA goes high impedance; input on WR, CLK, and DATA stops; and the TM bit is cleared.
4	FSEL	I	FOUT output frequency select. HIGH: 1Hz LOW: 32.768kHz
5	WR	I	DATA input/output control switch. HIGH: Data input mode (RTC write) LOW: Data output mode (RTC read)
6	FOE	I	FOUT output enable control. HIGH: The frequency selected by FSEL is output on FOUT. LOW: FOUT goes high impedance.
7	NC	–	No connection. Leave open for normal use.
8	NC	–	No connection. Leave open for normal use.
9	VDD	–	Supply voltage. Connect a ≥ 0.1μF capacitor between VDD and VSS.
10	CLK	I	System clock input. Data is input (RTC write mode) and output (RTC read mode) on the rising edge of CLK.
11	DATA	I/O	Data read and write input/output
12	NC	–	No connection. Leave open for normal use.
13	NC	–	No connection. Leave open for normal use.
14	FOUT	O	Frequency output (output controlled by FOE and frequency selected by FSEL). In 1Hz output mode, the 1Hz signal is synchronized to the internal 1 second signal. FOUT output is not affected by the CE signal.

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0V$ unless otherwise noted.

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}	Ta = 25°C	−0.3 to 7.0	V
Input voltage range	V_{IN}	Ta = 25°C	V_{SS} − 0.3 to V_{DD} + 0.3	V
Output voltage range	V_{OUT}	Ta = 25°C	V_{SS} − 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{STG}		−55 to 125	°C

Recommended Operating Conditions

$V_{SS} = 0V$ unless otherwise noted.

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		2.5 to 5.5	V
Clock supply voltage range	V_{CLK}		1.4 to 5.5	V
Operating temperature range	T_{OPR}		−40 to 85	°C

Oscillator Characteristics

$V_{SS} = 0V$ unless otherwise noted.

Parameter	Symbol	Condition		Rating	Unit
Frequency deviation	$\Delta f/f_O$	Ta = 25°C, V_{DD} = 5.0V	NR8576AA	5 ± 12	ppm
			NR8576AB	5 ± 23	ppm
Frequency temperature characteristic	T_{OP}	Ta = −10 to 70°C, V_{DD} = 5.0V, 25°C std		+10/−120	ppm
Frequency voltage characteristic	f/V	Ta = 25°C, V_{DD} = 2.0 to 5.5V		±2 max	ppm/V
Oscillator start time	t_{STA}	Ta = 25°C, V_{DD} = 2.5V		3 max	sec
Aging	f_A	Ta = 25°C, V_{DD} = 5.0V, first year		±5 max	ppm/year

DC Electrical Characteristics

V_{SS} = 0V, V_{DD} = 5.0V ± 10%, Ta = −40 to 85°C unless otherwise noted.

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
Current consumption	I_{DD1}	V_{DD} = 5.0V	CE = V_{SS}, FOE = V_{SS}, FSEL = V_{DD}, FOUT: floating	–	1.5	3.0	μA
	I_{DD2}	V_{DD} = 3.0V		–	1.0	2.0	μA
	I_{DD3}	V_{DD} = 2.0V		–	0.5	1.0	μA
	I_{DD4}	V_{DD} = 5.0V	CE = V_{SS}, FOE = V_{DD}, FSEL = V_{SS}, FOUT: 32kHz output	–	4.0	10.0	μA
	I_{DD5}	V_{DD} = 3.0V		–	2.5	6.5	μA
	I_{DD6}	V_{DD} = 2.0V		–	1.5	4.0	μA
HIGH-level input voltage	V_{IH}	CE, FSEL, WR, FOE, CLK, DATA		$0.8V_{DD}$	–	–	V
LOW-level input voltage	V_{IL}	CE, FSEL, WR, FOE, CLK, DATA		–	–	$0.2V_{DD}$	V
Input OFF leakage current	I_{OFF}	CE, FSEL, WR, FOE, CLK; V_{IN} = V_{DD} or V_{SS}		–	–	0.5	μA
HIGH-level output voltage	V_{OH1}	V_{DD} = 5.0V	I_{OH} = −1.0mA; DATA, FOUT	4.5	–	–	V
	V_{OH2}	V_{DD} = 3.0V		2.0	–	–	V
LOW-level output voltage	V_{OL1}	V_{DD} = 5.0V	I_{OL} = 1.0mA; DATA, FOUT	–	–	0.5	V
	V_{OL2}	V_{DD} = 3.0V		–	–	0.8	V
Output load fanout	N/CL	FOUT		2 LSTTL/30pF max			
Output leakage current	I_{OZH}	V_{OUT} = 5.5V; DATA, FOUT		−1.0	–	1.0	μA
	I_{OZL}	V_{OUT} = 0V; DATA, FOUT		−1.0	–	1.0	μA
Supply voltage detect threshold voltage	V_{DT}			1.4	1.7	2.0	V

AC Characteristics

Ta = −40 to 85°C, CL = 50pF unless otherwise noted.

Parameter	Symbol	Rating				Unit
		V_{DD} = 5V ± 10%		V_{DD} = 3V ± 10%		
		min	max	min	max	
CLK clock period	t_{CLK}	0.75	7800	1.5	7800	µs
CLK LOW-level pulsewidth	t_{CLKL}	0.375	3900	0.75	3900	µs
CLK HIGH-level pulsewidth	t_{CLKH}	0.375	3900	0.75	3900	µs
CE setup time	t_{CES}	0.375	3900	0.75	3900	µs
CE hold time	t_{CEH}	0.375	–	0.75	–	µs
CE enable time	t_{CE}	–	0.9	–	0.9	sec
Write data setup time	t_{SD}	0.1	–	0.2	–	µs
Write data hold time	t_{HD}	0.1	–	0.1	–	µs
WR setup time	t_{WRS}	100	–	100	–	ns
WR hold time	t_{WRH}	100	–	100	–	ns
DATA output delay time	t_{DATD}	–	0.2	–	0.4	µs
DATA output floating time	t_{DZ}	–	0.1	–	0.2	µs
Clock rise time	t_{r1}	–	50	–	100	ns
Clock fall time	t_{f1}	–	50	–	100	ns
FOUT rise time (CL = 30pF)	t_{r2}	–	100	–	200	ns
FOUT fall time (CL = 30pF)	t_{f2}	–	100	–	200	ns
Disable time (CL = 30pF)	t_{HZ}	–	100	–	200	ns
	t_{LZ}	–	100	–	200	ns
Enable time (CL = 30pF)	t_{ZH}	–	100	–	200	ns
	t_{ZL}	–	100	–	200	ns
FOUT duty cycle (CL = 30pF)	Duty	40	60	40	60	%
Wait time	t_{RCV}	0.95	–	1.9	–	µs

Timing Diagrams

Data read

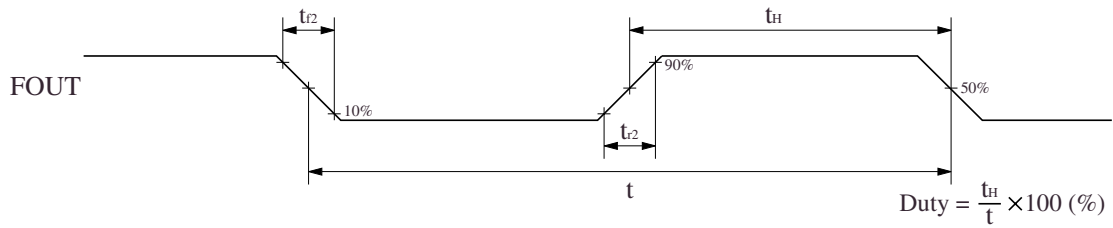### Data write
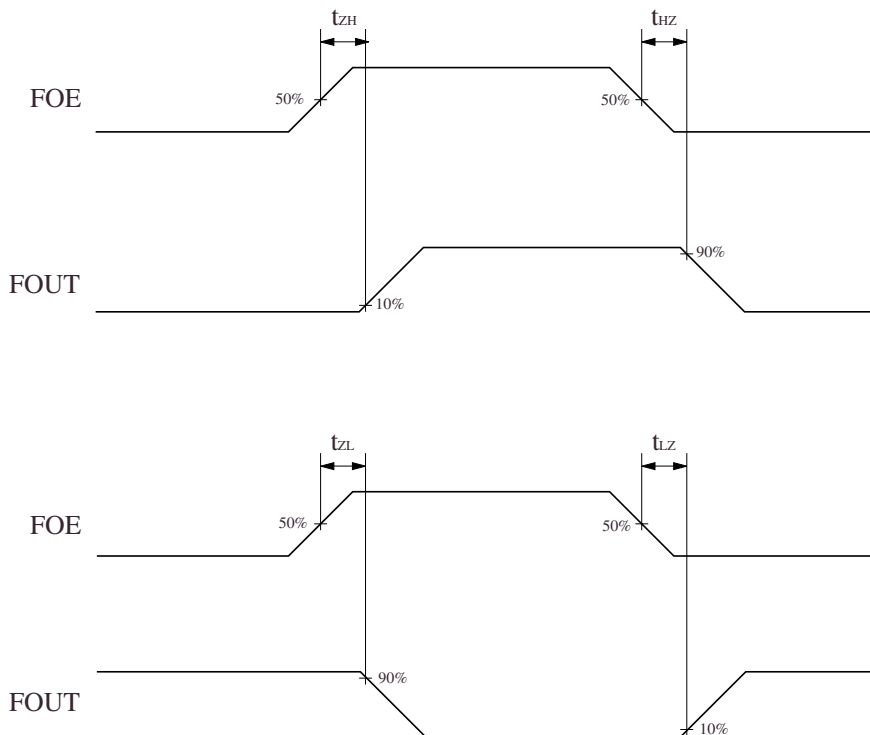
FOUT

$$\text{Duty} = \frac{t_H}{t} \times 100 \ (\%)$$
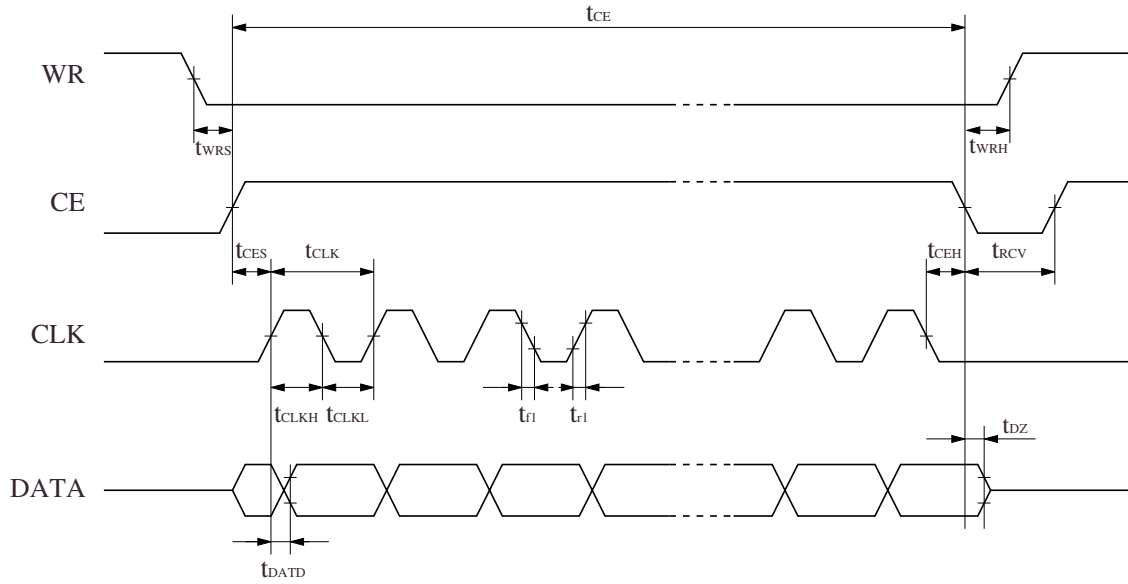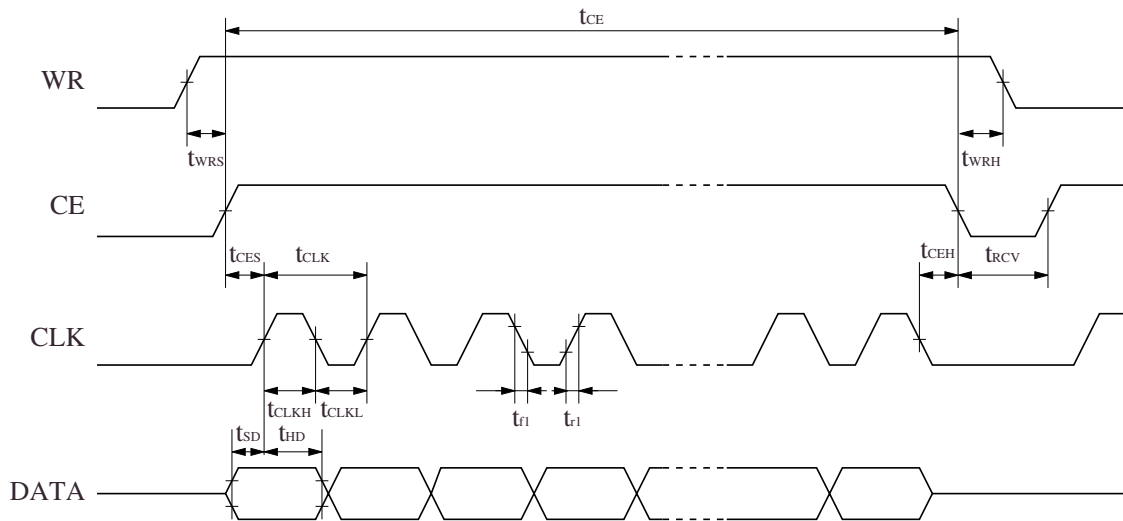
Disable/Enable

Note that FOE and FSEL do not have chatter elimination circuits. Consequently, switching either FOE or FSEL during 32kHz mode operation may generate chatter noise on the FOUT output. Also, note that the 1Hz and 32kHz oscillators are not synchronized to each other, so switching intervals shortens the duty cycle. Accordingly, a wait time ($\geq$ chattering time + output frequency period) should be incorporated when switching intervals.

FUNCTIONAL DESCRIPTION

Timer data configuration

- Counter data in BCD code format
- Automatic long/short month and leap-year adjustment
- 24-hour time display
- LSB first write and read data

	MSB						LSB
Second (0 to 59)	FDT	S40	S20	S10	S8	S4	S2	S1

Second (0 to 59): FDT, S40, S20, S10, S8, S4, S2, S1

Minute (0 to 59): *, mi40, mi20, mi10, mi8, mi4, mi2, mi1

Hour (0 to 23): *, *, h20, h10, h8, h4, h2, h1

Week (1 to 7): *, w4, w2, w1

Day (1 to 31): *, *, d20, d10, d8, d4, d2, d1

Month (1 to 12): TM, *, *, mo10, mo8, mo4, mo2, mo1

Year (0 to 99): y80, y40, y20, y10, y8, y4, y2, y1

Field	MSB							LSB
Second (0 to 59)	FDT	S40	S20	S10	S8	S4	S2	S1
Minute (0 to 59)	*	mi40	mi20	mi10	mi8	mi4	mi2	mi1
Hour (0 to 23)	*	*	h20	h10	h8	h4	h2	h1
Week (1 to 7)					*	w4	w2	w1
Day (1 to 31)	*	*	d20	d10	d8	d4	d2	d1
Month (1 to 12)	TM	*	*	mo10	mo8	mo4	mo2	mo1
Year (0 to 99)	y80	y40	y20	y10	y8	y4	y2	y1

1. * bit: Optional write bits.
2. FDT bit: Supply voltage detect bit
   - The FDT bit is set to 1 when the voltage between VDD and VSS falls below 1.7 ± 0.3V.
   - The FDT bit is reset to 0 for data reads longer than 48 bits. Note that the FDT bit is not reset to 0 for data reads of 47 bits or less.
   - The read/write data bits should be should be set to 0. After the supply voltage is applied, the FDT bit should be set to 0.
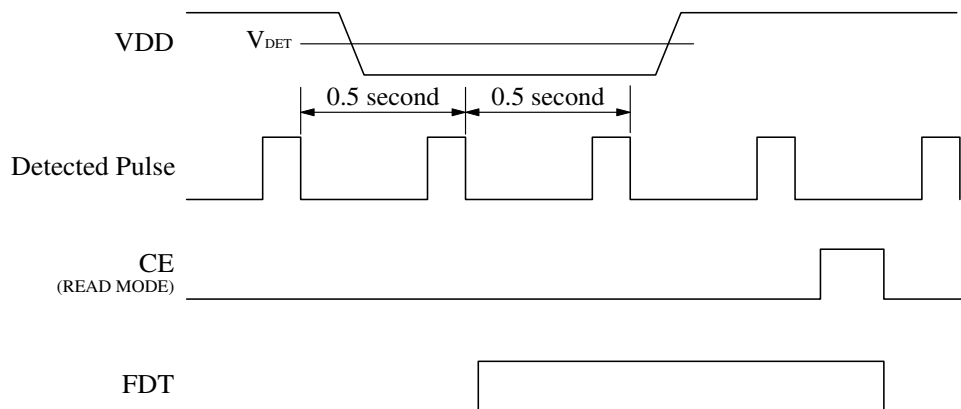
3. TM bit: Factory test bit. Should be set to 0 for normal use.

Data Read
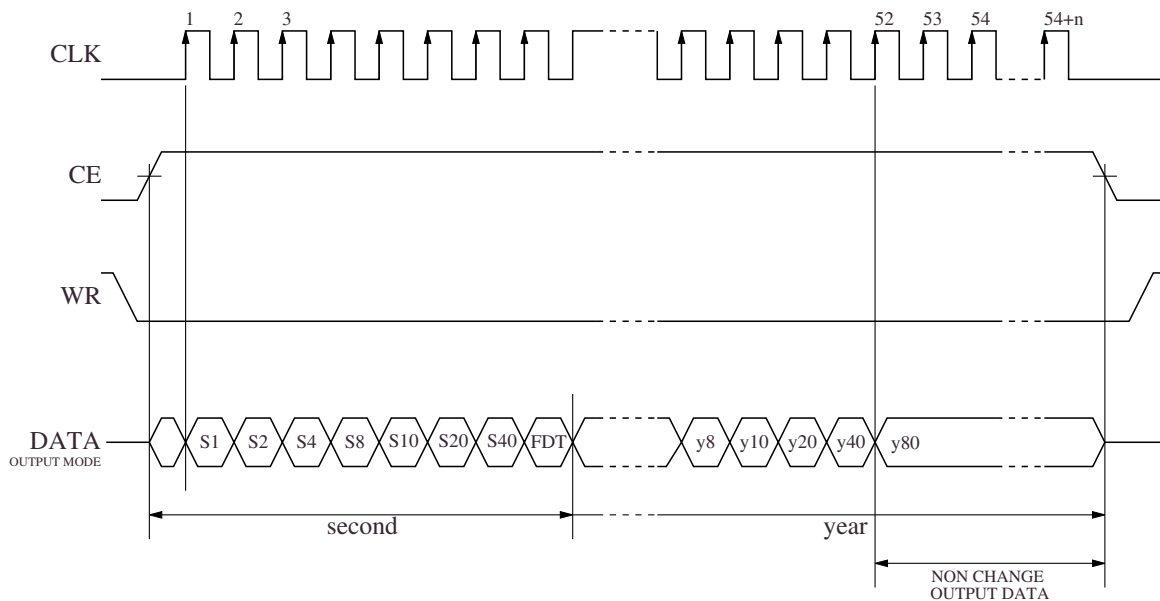
Data is output when WR is LOW and CE is HIGH.

Time and calendar data is loaded into shift registers on the first rising edge of the clock CLK, and the seconds' digit LSB is output on DATA.

The data is then loaded and shifted in the sequence second, minute, hour, week, day, and month on the rising edge of CLK, and output on DATA. The output data is valid after 52 rising edges of the clock; data input after 52 cycles does not alter the first 52 bits of valid data.

Within the 52 cycles of valid data, data already input can be output if there is a falling edge of CE after the corresponding number of cycles. For example, the data comprising the second-to-week is output is CE goes LOW after 28 clock cycles.

For continuous data reads, a wait time (t_{RCV}) is required before the next data cycle if CE has gone LOW.

Note that if an update operation (a 1s carry) occurs during a data read, an error of −1s in the read data is generated.

The data read time should be completed after $t_{CE} \leq 0.9$s.

Data Write
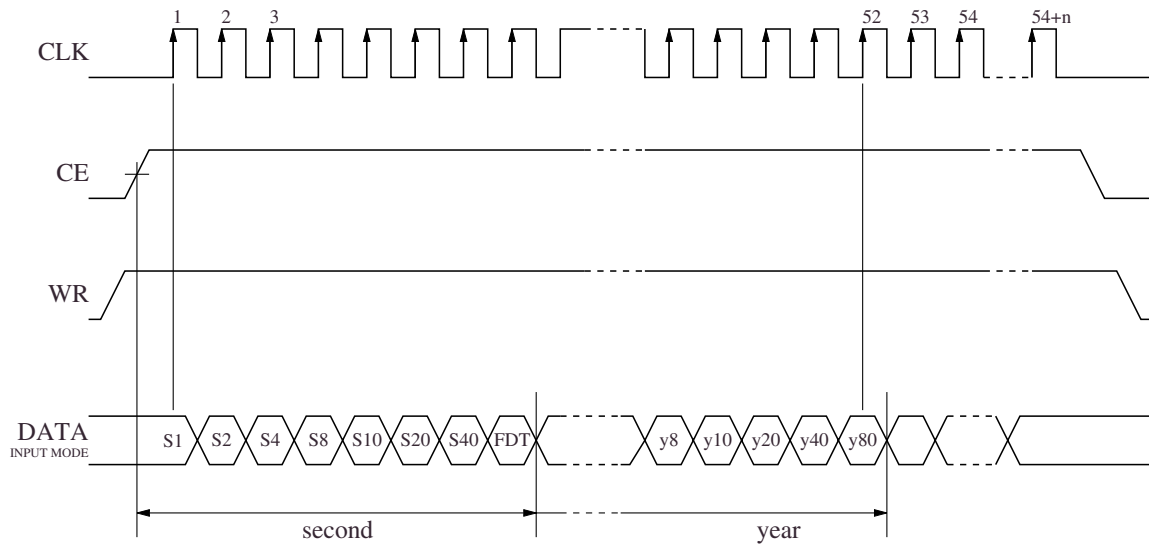
Data is input when WR is HIGH and CE is HIGH.

The seconds' digit signal to the timer counter stops on the first falling edge of CLK and the counter remains stopped until the next rising edge of CE. The 1Hz to 128Hz frequency divider step counters are reset during the interval between the first and second rising edges of CLK.

The data is then input on DATA into the shift register, starting with seconds' digit LSB synchronized with the rising edge of CLK.

After the final data is input into the shift register following 52 cycles, the shift register contents are transferred to the timer counters. Note that a data write must contain 52 bits of input data. If CE goes LOW before 52 bits are input, the input data is invalid. If the input data exceeds 52 bits, data from the 53rd bit is ignored (the first 52 bits remain valid).

The data write time should be completed after $t_{CE} \leq 0.9s$.

If a data read occurs immediately after a data write, a wait time (t_{RCV}) is required if CE has gone LOW.

Note that writing null data will cause incorrect operation. All bits must be valid data bits.

Please pay your attention to the following points at time of using the products shown in this document.