MTC-20146

ADSL
DMT Transceiver
with ATM Framer and
integrated controller

Data Sheet

Preliminary Information
Rev. 0.9 - November 1998

Features

- ANSI TI.413 issue 2 standard DMT modem with embedded , bypassable, ATM framer
- Standard Utopia level 1 and level 2 ATM interfaces
- Main functions:
  - Receive Direction:
    - Rotor and Adaptive Frequency domain Equalizing
    - Demapping of DMT carriers into a digital bitstream, including 4D trellis coding
    - Error and noise monitoring on individual carriers and pilot tones
    - Reed-Solomon decoding and deinterleaving
    - ADSL Deframing
    - ATM cell-specific Deframing
    - 176 TQFP package for ATU-R
    - 208 DQFP package for ATU-C
    - Power consumption 1.3 Watt at 3.3V
  - Transmit Direction:
    - ATM cell-specific Framing
    - ADSL Framing
    - Reed-Solomon encoding
    - Mapping of digital bit stream onto DMT carriers
    - Rotor and frequency domain gain correction
  - Performs ADSL control functions compliant with ANSI T1.413 issue 2
    - Initialization procedure
    - Line monitoring during operation
    - Rate adaptive modes
  - Supports the modem control interface protocol (CTRLE)
  - Embedded high speed ARM microcore
  - Parallel or serial modem control interface (CTRLE) for glueless connection to management entities
  - Embedded UART
  - Supports code download
  - External Bus Interface for 16-bit SDRAM

General Description

The MTC-20146 is the DMT modem, ATM Framer and controller chip of the MTK-20140 Rate adaptive ADSL Dyna-MiTe chipset.

When used in conjunction with the MTC-20144 analog front-end, the product supports ANSI TI.413 release 2 ADSL specification.

The MTC-20146 may be used in both central office (ATU-C) and remote (ATU-R) applications. It provides both a cell based UTOPIA Level 1 and 2 ATM data interface.

Ordering Information

Part number	Package	Temp
MTC-20146DQ-I	208 pin DQFP	-40 + 85°C
MTC-20146TQ-C	176 pin TQFP	0 + 70°C

Can also be ordered using kit number MTK-20140

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Pin Description

Nr	Name	Type	Description
1	TDI	in	test data in
2	CTRL_RST	in	carm reset signal, active low
3	CS_ 0	out	CS signal for flash eprom
4	VSS		
5	VDD		
6	T_ACK	out	test acknowledge
7	T_REQB	in	test request signal
8	T_REQA	in	test request signal
9	TROM	in	boot from test Rom select
10	PA_1	inout	port A bit[1]
11	PA_0	inout	port A bit[0]
12	VSS		
13	VDD		
14	BOOT-M1	inout	download mode select (CTRL-E or UART)
15	BOOT-M0	inout	download mode select (UART baudrate)
16	E_CLK	inout	EBI clock (SDRAM)
17	S_WE	out	control signal SDRAM
18	S_RAS	out	control signal SDRAM
19	VSS		
20	VDD		
21	S_CAS	out	control signal SDRAM
22	S_LDQM	out	control signal SDRAM
23	S_UDQM	out	control signal SDRAM
24	E_A_15	inout	address bus / testbus MSB
25	E_A_14	inout	address bus / testbus MSB
26	VSS		
27	VDD		
28	E_A_13	inout	address bus / testbus MSB
29	E_A_12	inout	address bus / testbus MSB
30	E_A_11	inout	address bus / testbus MSB
31	E_A_10	inout	address bus / testbus MSB
32	E_A_9	inout	address bus / testbus MSB
33	VSS		
34	VDD		
35	E_A_8	inout	address bus / testbus MSB
36	E_A_7	inout	address bus / testbus MSB
37	E_A_6	inout	address bus / testbus MSB
38	E_A_5	inout	address bus / testbus MSB
39	E_A_4	inout	address bus / testbus MSB
40	VSS		
41	VDD		
42	E_A_3	inout	address bus / testbus MSB
43	E_A_2	inout	address bus / testbus MSB
44	E_A_1	inout	address bus / testbus MSB
45	E_A_0	inout	address bus / testbus MSB
46	E_D_0	inout	data bus / testbus LSB
47	E_D_1	inout	data bus / testbus LSB

48	VSS		
49	VDD		
50	E_D_2	inout	data bus / testbus LSB
51	E_D_3	inout	data bus / testbus LSB
52	E_D_4	inout	data bus / testbus LSB
53	E_D_5	inout	data bus / testbus LSB
54	E_D_6	inout	data bus / testbus LSB
55	VSS		
56	VDD		
57	E_D_7	inout	data bus / testbus LSB
58	E_D_8	inout	data bus / testbus LSB
59	E_D_9	inout	data bus / testbus LSB
60	E_D_10	inout	data bus / testbus LSB
61	E_D_11	inout	data bus / testbus LSB
62	VSS		
63	VDD		
64	E_D_12	inout	data bus / testbus LSB
65	E_D_13	inout	data bus / testbus LSB
66	E_D_14	inout	data bus / testbus LSB
67	E_D_15	inout	data bus / testbus LSB
68	S_OE	out	output enable, active low
69	S_CS	out	chip select signal (SDRAM), active low
70	VSS		
71	VDD		
72	AFTXD_3	out	transmit data nibble
73	AFTXD_2	out	transmit data nibble
74	AFTXD_1	out	transmit data nibble
75	AFTXD_0	out	transmit data nibble
76	DMT_IDDq	in	test pin, active high
77	VSS		
78	VDD		
79	CTRLDATA	inout	serial data transmit channel
80	MCLK	in	master clock
81	CLWD	in	start of word indication
82	AFRXD_3	in	receive data nibble
83	AFRXD_2	in	receive data nibble
84	VSS		
85	VDD		
86	AFRXD_1	in	receive data nibble
87	AFRXD_0	in	receive data nibble
88	POWER_LOWB	inout	Power down analog front end
89	U_TxADDR_0	in	utopia tx address bit
90	U_TxData_0	in	utopia tx data bus
91	U_TxData_1	in	utopia tx data bus
92	VSS		
93	VDD		
94	U_TxData_2	in	utopia tx data bus
95	U_TxData_3	in	utopia tx data bus
96	U_TxData_4	in	utopia tx data bus
97	U_TxData_5	in	utopia tx data bus
98	U_TxData_6	in	utopia tx data bus
99	VSS		

100	VDD		
101	U_TxData_7	in	utopia tx data bus
102	U_TxENB	in	utopia tx control signal
103	U_TxCLAV	inout	utopia tx control signal
104	U_TxSOC	in	transmit interface start of cell indication
105	U_TxCLK	in	transmit interface utopia clock
106	VSS		
107	VDD		
108	U_RxENB	in	utopia rx control signal
109	U_RxCLAV	inout	utopia rx control signal
110	U_RxSOC	inout	receive interface start of cell indication
111	U_RxCLK	in	receive interface utopia clock
112	U_TxRefB	in	8 kHz clock from network
113	U_RxRefB	inout	8 kHz clock to ATM device
114	VSS		
115	VDD		
116	U_RxADDR_0	in	Utopia rx address bit
117	U_RxData_7	outZ	Utopia rx data bus
118	U_RxData_6	outZ	Utopia rx data bus
119	U_RxData_5	outZ	Utopia rx data bus
120	U_RxData_4	outZ	Utopia rx data bus
121	VSS		
122	VDD		
123	U_RxData_3	outZ	Utopia rx data bus
124	U_RxData_2	outZ	Utopia rx data bus
125	U_RxData_1	outZ	Utopia rx data bus
126	U_RxData_0	outZ	Utopia rx data bus
127	DMT_RESET	in	DMT Engine reset, active low
128	VSS		
129	VDD		
130	C_A_8	inout	Ctrl_E address bus
131	C_A_7	inout	Ctrl_E address bus
132	C_A_6	inout	Ctrl_E address bus
133	C_A_5	inout	Ctrl_E address bus
134	C_A_4	inout	Ctrl_E address bus
135	C_A_3	inout	Ctrl_E address bus
136	VSS		
137	VDD		
138	C_A_2	inout	Ctrl_E address bus
139	C_A_1	inout	Ctrl_E address bus
140	C_A_0	inout	Ctrl_E address bus
141	C_D_7	inout	Ctrl_E data bus
142	C_D_6	inout	Ctrl_E data bus
143	VSS		
144	VDD		
145	C_D_5	inout	Ctrl_E data bus
146	C_D_4	inout	Ctrl_E data bus
147	C_D_3	inout	Ctrl_E data bus
148	C_D_2	inout	Ctrl_E data bus
149	C_D_1	inout	Ctrl_E data bus
150	VSS		
151	VDD		

152	C_D_0	inout	Ctrl_E data bus
153	C_clk	in	Ctrl_E serial input clock
154	C_CS	in	Ctrl_E chip select
155	C_Wr	in	Ctrl_E write indication
156	C_Rd	inout	Ctrl_E read indication
157	VSS		
158	VDD		
159	C_Rdy	out_Hiz	Ctrl_E ready indication
160	C_Int	out_Hiz	Ctrl_E interface interrupt
161	Mode_1	in	select functional and test mode
162	Mode_0	in	select functional and test mode
163	SCAN_CLK	in	scan clock
164	VSS		
165	VDD		
166	TESTSE	in	test scan enable
167	RSRXD2	inout	serial Rx port
168	RSTXD2	inout	serial Tx port
169	C_mode	inout	Ctrl-E mode signal: 0=motorola, 1=intel
170	GP	inout	carm iddq pin
171	TCK	in	jtag clock
172	VSS		
173	VDD		
174	TRST	in	reset jtag interface
175	TMS	in	test mode select
176	TDO	out	test data out

Package

For detailed mechanical data, please refer to the 176 Pins Thin Plastic Quad Flat Package Data Sheet. Ref : 01/97-DS0240b

Prototypes: TQFP176
Production: TQFP176

MTC-20146

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