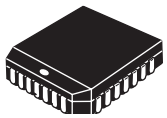
Low Skew CMOS PLL Clock Drivers, 3-State

MC88915T

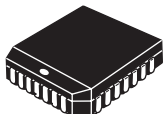
55, 70, 100, 133, and 160 MHz Versions

MC88915TFN55
MC88915TFN70
MC88915TFN100
MC88915TFN133
MC88915TFN160

LOW SKEW CMOS PLL CLOCK DRIVER



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 766-02



EI SUFFIX
28-LEAD PLCC PACKAGE
Pb-FREE PACKAGE
CASE 766-02

The MC88915T Clock Driver utilizes phase-locked loop (PLL) technology to lock its low skew outputs frequencies and phase onto an input reference clock. It is designed to provide clock distribution for high performance PCs and workstations. For a 3.3 V version, see the MC88LV915T data sheet.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it to multiple components on a board. The PLL also allows the MC88915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915s can lock onto a single reference clock, ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 9).

Five “Q” outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the “Q” outputs. The 2X_Q output runs at twice the “Q” output frequency, while the Q/2 runs at 1/2 the “Q” frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q f_{max} specification. The wiring diagrams in Figure 7 detail the different feedback configurations, creating specific input/output frequency relationships. Possible frequency ratios of the “Q” outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide-by in the feedback path of the PLL. It selects between divide-by-1 and divide-by-2 of the VCO before its signal reaches the internal clock distribution section of the chip (see [2]). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) allows the VCO to run in its optimal range (>20 MHz and >40 MHz for the TFN133 version).

In normal phase-locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88915 in a static “test mode.” In this mode, there is no frequency limitation on the input clock, necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board-level testing (see APPLICATIONS INFORMATION FOR ALL VERSIONS on page 12).

Pulling the $\overline{OE}/\overline{RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 into a high impedance state (3-state). After the $\overline{OE}/\overline{RST}$ pin goes back high Q0–Q4, $\overline{Q5}$, and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady-state phase and frequency lock. The LOCK output will go low if phase-lock is lost, or when the PLL_EN pin is low. The LOCK output will go high no later than 10 ms after the 88915 sees a SYNC signal and full 5.0 V V_{CC}.

Features

- Five outputs (Q0–Q4) with output-output skew < 500 ps, each being phase and frequency locked to the SYNC input
- The phase variation from part-to-part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, defining the part-to-part skew).
- Input/output phase-locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5 MHz – 2X_Q f_{max} specification (10 MHz – 2X_Q f_{max} for the TFN133 version)
- Additional outputs available at 2X and +2 the system “Q” frequency. Also, a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL-level compatible. ±88 mA I_{OL}/I_{OH} specifications guarantee 50 Ω transmission line switching on the incident edge.
- Test mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3-state) for board test purposes.
- Lock indicator (LOCK) accuracy indicates a phase-locked state.
- 28-lead Pb-free package available.

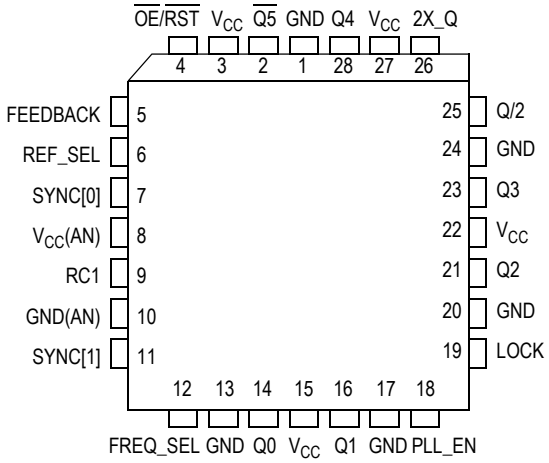


Figure 1. Pinout: 28-Lead PLCC (Top View)

Table 1. Pin Summary

Pin Name	Number	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between SYNC[0] and SYNC[1]
FREQ_SEL	1	Input	Doubles VCO internal frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0–4)	5	Output	Clock output (locked to SYNC)
$\overline{Q5}$	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output (Q) frequency ÷ 2 (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
$\overline{OE}/\overline{RST}$	1	Input	Output enable/asynchronous reset (active low)
PLL_EN	1	Input	Disables phase-lock for low frequency testing
V_{CC}, GND	11		Power and ground pins (note pins 8 and 10 are “analog” supply pins for internal PLL only)

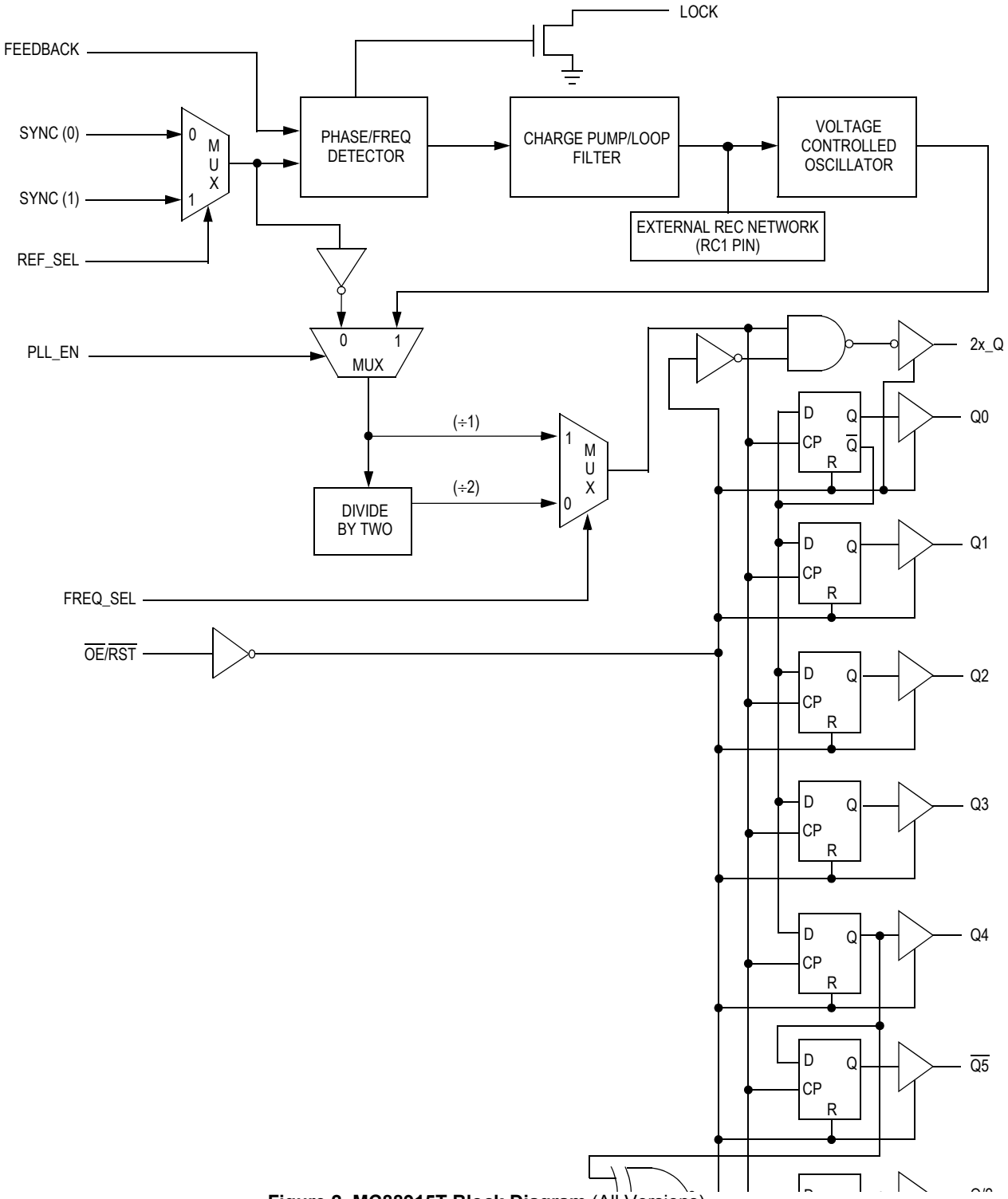


Figure 2. MC88915T Block Diagram (All Versions)

MC88915TFN55 AND MC88915TFN70

Table 2. SYNC Input Timing Requirements

Symbol	Parameter	Minimum		Maximum	Unit
		TFN70	TFN55		
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs from 0.8 to 2.0 V	—	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	28.5(1)	36.0(1)	200(2)	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ± 25%			

1. These t_{CYCLE} minimum values are valid when "Q" output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 7**b**.
2.Information in Table 22 and in Note 3 of the AC specification notes describe this specification with its limits depending on what output is fed back, and if FREQ_SEL is high or low.

Table 3. DC Electrical Characteristics (Voltages Referenced to GND)
T_A = –40°C to +85°C for 55 MHz Version; T_A = 0°C to +70°C for 70 MHz Version; V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA(1)	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = 36 mA(1)	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	± 1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	2.0	mA
I_{OLD}	Minimum Dynamic Output Current	V_{OLD} = 1.0 V Maximum	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Minimum	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.25	± 50	µA

1. Maximum test duration is 2.0 ms, one output loaded at a time.

Table 4. Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1(1)	Power Dissipation @ 50 MHz with 50 Ω Thevenin Termination	23 mW/Output 184 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2(1)	Power Dissipation @ 50 MHz with 50 Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0 V T = 25°C

1. PD_1 nd PD_2 mW/Output numbers are for a "Q" output.

MC88915TFN55 AND MC88915TFN70 (Continued)

Table 5. Frequency Specifications (T_A = –40°C to +85 °C, V_{CC} = 5.0 V ± 5%)

Symbol	Parameter	Guaranteed Minimum		Unit
		TFN70	TFN55	
f_{max}(1)	Maximum Operating Frequency (2X_Q Output)	70	55	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	35	27.5	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to V_{CC}/2.

Table 6. AC Characteristics (T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%, Load = 50 Ω Terminated to V_{CC}/2)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})	1.0	2.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time into a 20 pF Load, with Termination Specified in Note(2)	0.5	1.6	ns	t_{RISE}: 0.8 V – 2.0 V t_{FALL}: 2.0 V – 0.8 V
$t_{PULSEWIDTH}$(1) (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q4, Q4, $\overline{Q5}$, Q/2 @ V_{CC}/2	0.5 t_{CYCLE} – 0.5(2)	0.5 t_{CYCLE} + 0.5(2)	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{PULSEWIDTH}$(1) (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5 V 66 MHz 50 MHz 40 MHz	0.5 t_{CYCLE} – 0.5(2) 0.5 t_{CYCLE} – 1.0 0.5 t_{CYCLE} – 1.5	0.5 t_{CYCLE} + 0.5(2) 0.5 t_{CYCLE} + 1.0 0.5 t_{CYCLE} + 1.5	ns	Must Use Termination Specified in Note(2)
$t_{PULSEWIDTH}$(1) (2X_Q Output)	Output Pulse Width: 2X_Q @ V_{CC}/2 50 – 65 MHz 40 – 49 MHz 66 – 70 MHz	0.5 t_{CYCLE} – 1.0(2) 0.5 t_{CYCLE} – 1.5 0.5 t_{CYCLE} – 0.5	0.5 t_{CYCLE} + 1.0(2) 0.5 t_{CYCLE} + 1.5 0.5 t_{CYCLE} + 0.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
t_{PD}(1),(3) SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note(4) and Figure 4 for Detailed Explanation
		–1.05	–0.40		
		(With 1 MΩ from RC1 to An GND)			
		+1.25	+3.25		
t_{SKEWr}(4) (Rising)(5)	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{SKEWf}(1),(4) (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
$t_{SKEWall}$(1),(4)	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{LOCK}(5)	Time Required to Acquire Phase-Lock from Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low

1. These specifications are not tested. They are guaranteed by statistical characterization. See AC specification Note 1.
2. t_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The t_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.

MC88915TFN100

Table 7. SYNC Input Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs from 0.8 to 2.0 V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	20.0(1)	200(2)	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ± 25%		

1. These t_{CYCLE} minimum values are valid when "Q" output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 7**b**.
2. Information in Table 22 and in Note 3 of the AC specification notes describe this specification with its limits depending on what output is fed back, and if FREQ_SEL is high or low.

Table 8. DC Electrical Characteristics (Voltages Referenced to GND) T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA(1)	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = 36 mA1	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	± 1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} –2.1 V	5.25	2.0(2)	mA
I_{OLD}	Minimum Dynamic Output Current(3)	V_{OLD} = 1.0 V Maximum	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Minimum	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.25	± 50	µA

1. I_{OL} and I_{OH} are 12 mA and –12 mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0 ms, one output loaded at a time.

Table 9. Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1(1)	Power Dissipation @ 50 MHz with 50 Ω Thevenin Termination	23 mW/Output 184 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2(1)	Power Dissipation @ 50 MHz with 50 Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0 V T = 25°C

1. PD_1 nd PD_2 mW/Output numbers are for a "Q" output.

Table 10. Frequency Specifications (T_A = –40°C to +85 °C, V_{CC} = 5.0 V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN100	
f_{max}(1)	Maximum Operating Frequency (2X_Q Output)	100	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	50	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to V_{CC}/2.

MC88915TFN100 (Continued)

Table 11. AC Characteristics (T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%, Load = 50 Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})	1.0	2.5	ns	Into a 50 Ω Load Terminated to $V_{CC}/2$
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time into a 20 pF Load, with Termination Specified in Note(2)	0.5	1.6	ns	t_{RISE}: 0.8 V – 2.0 V t_{FALL}: 2.0 V – 0.8 V
$t_{PULSEWIDT}$(1) (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q4, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$	0.5 t_{CYCLE} – 0.5(2)	0.5 t_{CYCLE} + 0.5(2)	ns	Into a 50 Ω Load Terminated to $V_{CC}/2$
$t_{PULSEWIDTH}$(1) (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5 V	0.5 t_{CYCLE} – 0.5(2)	0.5 t_{CYCLE} + 0.5(2)	ns	Must Use Termination Specified in Note(2)
$t_{PULSEWIDTH}$(1) (2X_Q Output)	Output Pulse Width: 40 – 49 MHz 2X_Q @ $V_{CC}/250$ – 65 MHz 66 – 100 MHz	0.5 t_{CYCLE} – 1.5(2) 0.5 t_{CYCLE} – 1.0 0.5 t_{CYCLE} – 0.5	0.5 t_{CYCLE} + 1.5(2) 0.5 t_{CYCLE} + 1.0 0.5 t_{CYCLE} + 0.5	ns	Into a 50 Ω Load Terminated to $V_{CC}/2$
t_{PD}(1),(3) SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note(4) and Figure 4 for Detailed Explanation
		–1.05	–0.30		
		(With 1 MΩ from RC1 to An GND)			
		+1.25	+3.25		
t_{SKEWr}(4) (Rising)(5)	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to $V_{CC}/2$
t_{SKEWf}(1),(4) (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to $V_{CC}/2$
$t_{SKEWall}$(1),(4)	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs into a Matched 50 Ω Load Terminated to $V_{CC}/2$
t_{LOCK}(5)	Time Required to Acquire Phase-Lock from Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low

1. These specifications are not tested. They are guaranteed by statistical characterization. See AC specification Note 1.
2. t_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The t_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.

MC88915TFN133

Table 12. SYNC Input Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs from 0.8 to 2.0 V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	15.0(1)	100(2)	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ± 25%		

1. These t_{CYCLE} minimum values are valid when "Q" output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 7**b**.
2. Information in Table 22 and in Note 3 of the AC specification notes describe this specification with its limits depending on what output is fed back, and if FREQ_SEL is high or low.

Table 13. DC Electrical Characteristics (Voltages Referenced to GND) T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA(1)	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = 36 mA(1)	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	± 1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} –2.1 V	5.25	2.0(2)	mA
I_{OLD}	Minimum Dynamic Output Current(3)	V_{OLD} = 1.0 V Maximum	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Minimum	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.25	± 50	µA

1. I_{OL} and I_{OH} are 12 mA and –12 mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0 ms, one output loaded at a time.

Table 14. Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1(1)	Power Dissipation @ 50 MHz with 50 Ω Thevenin Termination	23 mW/Output 184 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2(1)	Power Dissipation @ 50 MHz with 50 Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0 V T = 25°C

1. PD_1 nd PD_2 mW/Output numbers are for a "Q" output.

Table 15. Frequency Specifications (T_A = –40°C to +85 °C, V_{CC} = 5.0 V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN133	
f_{max}(1)	Maximum Operating Frequency (2X_Q Output)	133	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	66	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to V_{CC}/2.

MC88915TFN133 (Continued)

Table 16. AC Characteristics (T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%, Load = 50 Ω Terminated to V_{CC}/2)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})	1.0	2.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time into a 20 pF Load, with Termination Specified in Note(2)	0.5	1.6	ns	t_{RISE}: 0.8 V – 2.0 V t_{FALL}: 2.0 V – 0.8 V
$t_{PULSEWIDTH}$(1) (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q4, Q4, $\overline{Q5}$, Q/2 @ V_{CC}/2	0.5 t_{CYCLE} – 0.5(2)	0.5 t_{CYCLE} + 0.5(2)	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{PULSEWIDTH}$(1) (2X_Q Output)	Output Pulse Width: 66 – 133 MHz 2X_Q @ 1.5 V 40 – 65 MHz	0.5 t_{CYCLE} – 0.5(2) 0.5 t_{CYCLE} – 0.9	0.5 t_{CYCLE} + 0.5(2) 0.5 t_{CYCLE} + 0.9	ns	Must Use Termination Specified in Note(2)
$t_{PULSEWIDTH}$(1) (2X_Q Output)	Output Pulse Width:66 – 133 MHz 2X_Q @ V_{CC}/2 40 – 65 MHz	0.5 t_{CYCLE} – 0.5(2) 0.5 t_{CYCLE} – 0.9	0.5 t_{CYCLE} + 0.5(2) 0.5 t_{CYCLE} + 0.9	ns	Into a 50 Ω Load Terminated to V_{CC}/2
t_{PD}(1),(3) SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note(4) and Figure 4 for Detailed Explanation
		–1.05	–0.25		
		(With 1 MΩ from RC1 to An GND)			
		+1.25	+3.25		
t_{SKEWr}(4) (Rising)(5)	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{SKEWf}(1),(4) (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
$t_{SKEWall}$(1),(4)	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{LOCK}(5)	Time Required to Acquire Phase-Lock from Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low

1. These specifications are not tested. They are guaranteed by statistical characterization. See AC specification Note 1.
2. t_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The t_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.

MC88915TFN160

Table 17. SYNC Input Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs from 0.8 to 2.0 V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	12.5(1)	100(2)	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ± 25%		

1. These t_{CYCLE} minimum values are valid when "Q" output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 7**b**.
2. Information in Table 22 and in Note 3 of the AC specification notes describe this specification with its limits depending on what output is fed back, and if FREQ_SEL is high or low.

Table 18. DC Electrical Characteristics (Voltages Referenced to GND) T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} –0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA(1)	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = 36 mA(1)	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	± 1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} –2.1 V	5.25	2.0(2)	mA
I_{OLD}	Minimum Dynamic Output Current(3)	V_{OLD} = 1.0 V Maximum	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Minimum	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.25	± 50	µA

1. I_{OL} and I_{OH} are 12 mA and –12 mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0 ms, one output loaded at a time.

Table 19. Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1(1)	Power Dissipation @ 50 MHz with 50 Ω Thevenin Termination	15 mW/Output 120 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2(1)	Power Dissipation @ 50 MHz with 50 Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0 V T = 25°C

1. PD_1 nd PD_2 mW/Output numbers are for a "Q" output.

Table 20. Frequency Specifications (T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN160	
f_{max}(1)	Maximum Operating Frequency (2X_Q Output)	160	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	80	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to V_{CC}/2.

MC88915TFN160 (Continued)

Table 21. AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 5%, Load = 50 Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})	1.0	2.5	ns	Into a 50 Ω Load Terminated to $V_{CC}/2$
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time	0.5	1.6	ns	t_{RISE}: 0.8 V – 2.0 V t_{FALL}: 2.0 V – 0.8 V
$t_{PULSEWIDTH}$ (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q4, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$	0.5 t_{CYCLE} – 0.5(2)	0.5 t_{CYCLE} + 0.5(2)	ns	Into a 50 Ω Load Terminated to $V_{CC}/2$
$t_{PULSEWIDTH}$ (2X_Q Output)	Output Pulse Width: 80 MHz 2X_Q @ 1.5 V100 MHz 133 MHz 160 MHz	0.5 t_{CYCLE} – 0.7 0.5 t_{CYCLE} – 0.5 0.5 t_{CYCLE} – 0.5 TBD	0.5 t_{CYCLE} + 0.7 0.5 t_{CYCLE} + 0.5 0.5 t_{CYCLE} + 0.5 TBD	ns	
t_{PD}(1) SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note(2) and Figure 4 for Detailed Explanation
	133 MHz 160 MHz	–1.05 –0.9	–0.25 –0.10		
t_{CYCLE} (2x_Q Output)	Cycle-to-Cycle Variation133 MHz 160 MHz	t_{CYCLE} – 300 ps t_{CYCLE} – 300 ps	t_{CYCLE} + 300 ps t_{CYCLE} + 300 ps		
t_{SKEWr}(3) (Rising)(4)	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to $V_{CC}/2$
t_{SKEWf}(3) (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to $V_{CC}/2$
$t_{SKEWall}$(3)	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs into a Matched 50 Ω Load Terminated to $V_{CC}/2$
t_{LOCK}(4)	Time Required to Acquire Phase-Lock from Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low

1. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
2. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
3. Under equally loaded conditions and at a fixed temperature and voltage.
4. With V_{CC} fully powered on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.

APPLICATIONS INFORMATION FOR ALL VERSIONS

General AC Specification Notes

1. Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88915 devices were fabricated with key transistor properties intentionally varied to create a 14-cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area, to set performance limits of ATE testable specifications within those to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non-tested specifications limits.
2. These two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output) guarantee the MC88915T meets the 40 MHz and 33 MHz MC68040 P-Clock input specification (at 80 MHz and 66 MHz, respectively). For these two specs to be guaranteed by Freescale Semiconductor, the termination scheme shown below in Figure 3 must be used.
3. The wiring diagrams and explanations in Figure 7 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether FREQ_SEL is high or low. Although not shown, it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the "Q" outputs. Table 22 below summarizes the allowable SYNC frequency range for each possible configuration.

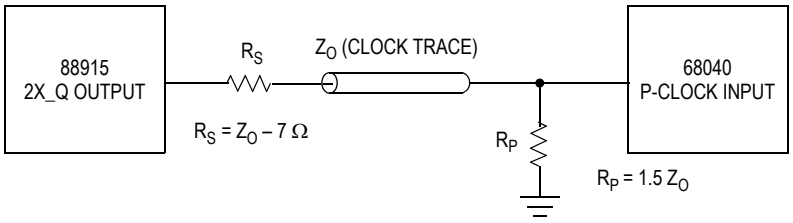


Figure 3. MC68040 P-Clock Input Termination Scheme

Table 22. Allowable SYNC Input Frequency Ranges for Different Feedback Configurations

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHz)	Corresponding VCO Frequency Range	Phase Relationships of the "Q" Outputs to Rising SYNC Edge
HIGH	Q/2	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
HIGH	Any "Q" (Q0–Q4)	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°
HIGH	$\overline{Q5}$	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	180°
HIGH	2X_Q	20 to (2X_Q FMAX Spec)	20 to (2X_Q FMAX Spec)	0°
LOW	Q/2	2.5 to (2X_Q FMAX Spec)/8	20 to (2X_Q FMAX Spec)	0°
LOW	Any "Q" (Q0–Q4)	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
LOW	$\overline{Q5}$	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	180°
LOW	2X_Q	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°

4. A 1 MΩ resistor tied to either Analog V_{CC} or Analog GND, depicted in Figure 4, is required to ensure no jitter is present on the MC88915T outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were determined by measuring the phase relationship for the 14 lots described in Note 1 while the part was in phase-locked operation. The actual measurements were made with a 10 MHz SYNC input (1.0 ns edge rate from 0.8 V – 2.0 V) with the Q/2 output fed back. The phase measurements were made at 1.5 V. The Q/2 output was terminated at the FEEDBACK input with 100 Ω to V_{CC} and 100 Ω to ground.

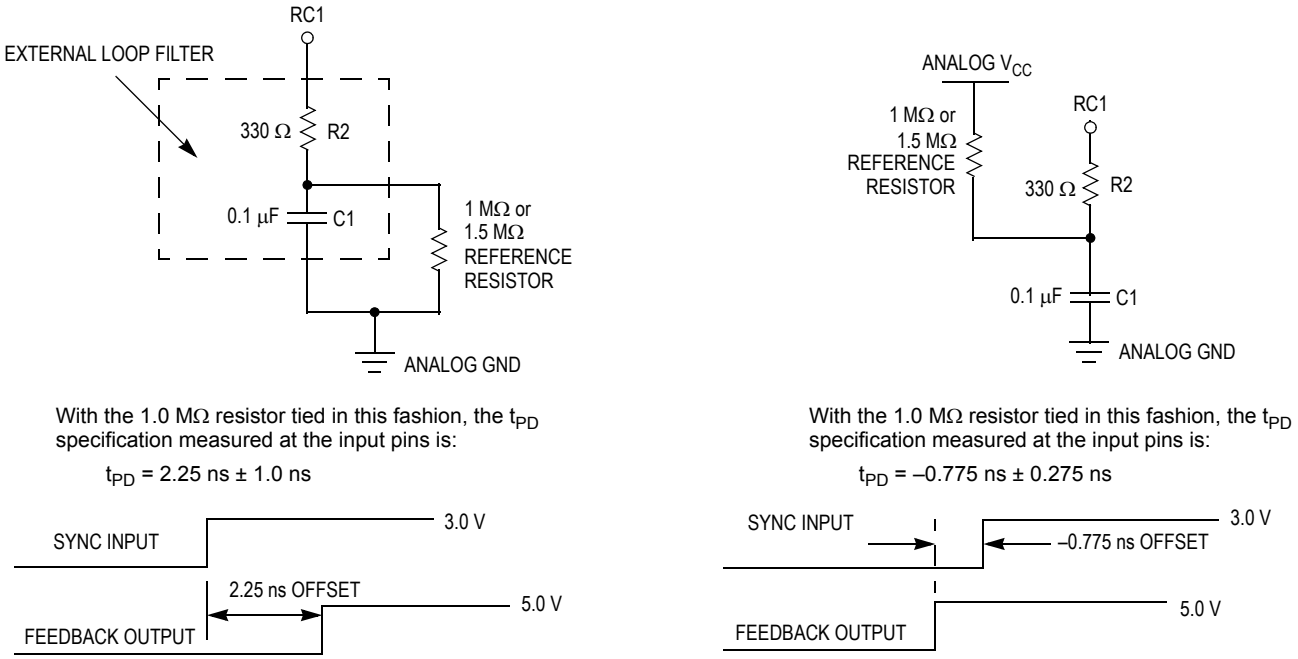


Figure 4. Depiction of the Fixed SYNC to Feedback Offset (t_{PD}) Which Is Present When a 1 mΩ Resistor is Tied to V_{CC} or Ground

5. The t_{SKEWr} specification guarantees the rising edges of outputs Q/2, Q0, Q1, Q2, Q3, and Q4 will always fall within a 500 ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the t_{PD} specification limits to calculate the total part-to-part skew. For this reason, the absolute distribution of these outputs are provided in Table 23. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 23 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

Table 23. Relative Positions of Outputs Q/2, Q0–Q4, 2X_Q Within the 500 ps t_{SKEWr} Spec Window

Output	– (ps)	+ (ps)
Q0	0	0
Q1	–72	40
Q2	–44	276
Q3	–40	255
Q4	–274	–34
Q/2	–16	250
2X_Q	–633	–35

6. **Calculation of Total Output-to-Skew Between Multiple Parts (Part-to-Part Skew)**

   By combining the t_{PD} specification and the information in Note 5, the worst case output-to-output skew between multiple 88915s connected in parallel can be calculated. This calculation assumes all parts have a common SYNC input clock with equal delay of input signal to each part. This skew value is valid at the 88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.

   With a 1.0 MΩ resistor tied to analog V_{CC} as shown in Note 4, the t_{PD} spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are –1.05 ns and –0.5 ns. To calculate the skew of any given output between two or more parts, the absolute value of the distribution of the output given in Table 23 must be subtracted and added to the lower and upper t_{PD} spec limits respectively. For output Q2, [276 – (–44)] = 320 ps is the absolute value of the distribution. Therefore, [–1.05 ns – 0.32 ns] = –1.37 ns is the lower t_{PD} limit, and [–0.5 ns + 0.32 ns] = –0.18 ns is the upper limit. Therefore, the worst case skew of output Q2 between any number of parts is |(–1.37) – (–0.18)| = 1.19 ns. Q2 has the worst case skew distribution of any output, so 1.2 ns is the absolute worst case output-to-output skew between multiple parts.

7. Note 4 explains the t_{PD} specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10 MHz. The fixed offset (t_{PD}) as described above has some dependence on the input frequency and at what frequency the VCO is running. The graphs of Figure 5 demonstrate this dependence.

   The data presented in Figure 5 is from devices representing process extremes, and the measurements were also taken at the voltage extremes (V_{CC} = 5.25 V and 4.75 V). Therefore, the data in Figure 5 is a realistic representation of the variation of t_{PD}.

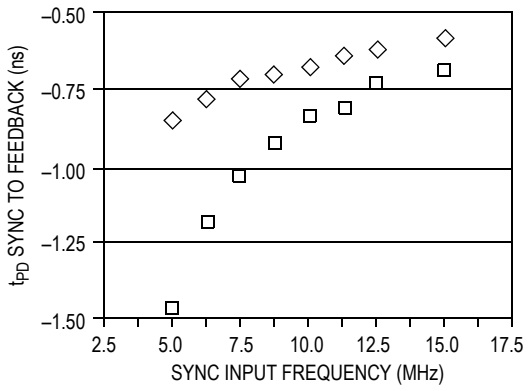


Figure 5a

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (with 1.0 MΩ Resistor Tied to Analog V_{CC})

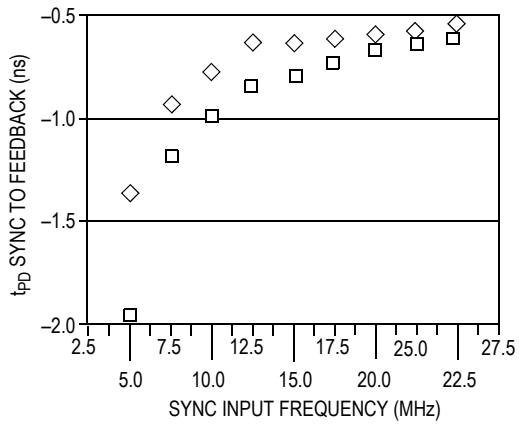


Figure 5b

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (with 1.0 MΩ Resistor Tied to Analog V_{CC})

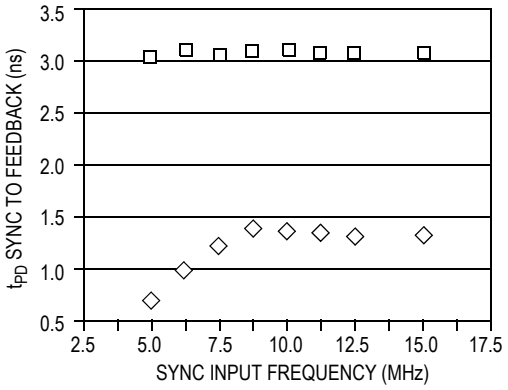


Figure 5c

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (with 1.0 MΩ Resistor Tied to Analog GND)

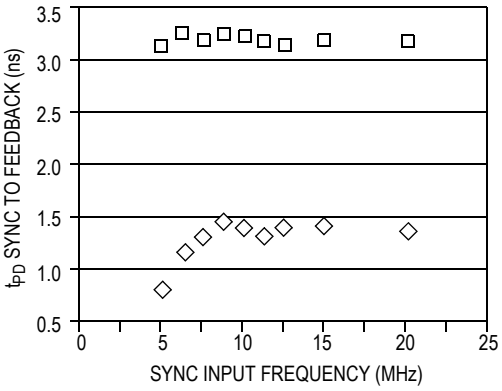


Figure 5d

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (with 1.0 MΩ Resistor Tied to Analog GND)

Figure 5. Graphs

8. The lock indicator pin (LOCK) will reliably indicate a phase-locked condition at SYNC input frequencies down to 10 MHz. At frequencies below 10 MHz, the frequency of correction pulses going into the phase detector form the SYNC and FEEDBACK pins may not be sufficient to allow the lock indicator circuitry to accurately predict a phase-locked condition. The MC88915T is guaranteed to provide stable phase-locked operation down to the appropriate minimum input frequency given in Table 22, even though the LOCK pin may be LOW at frequencies below 10 MHz.

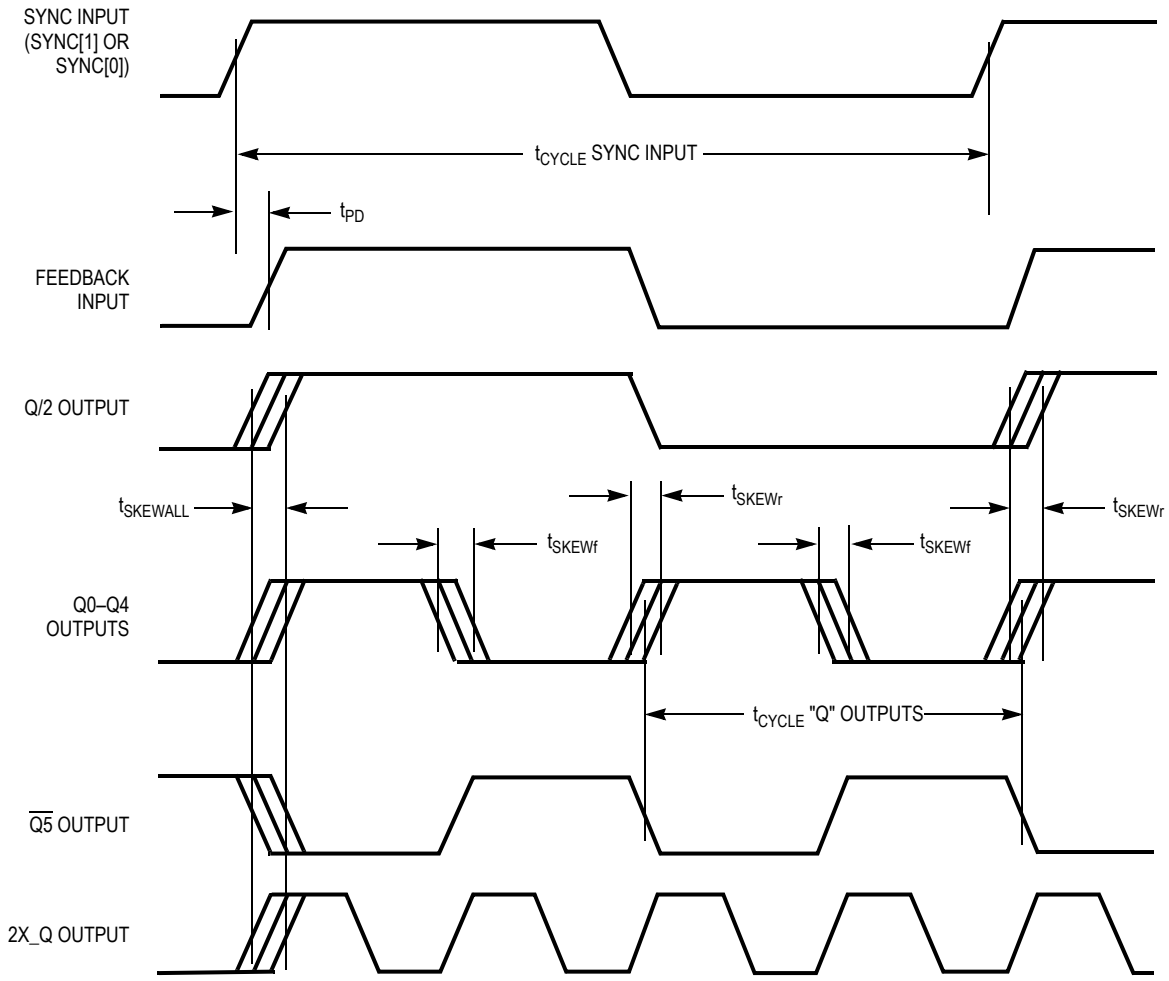
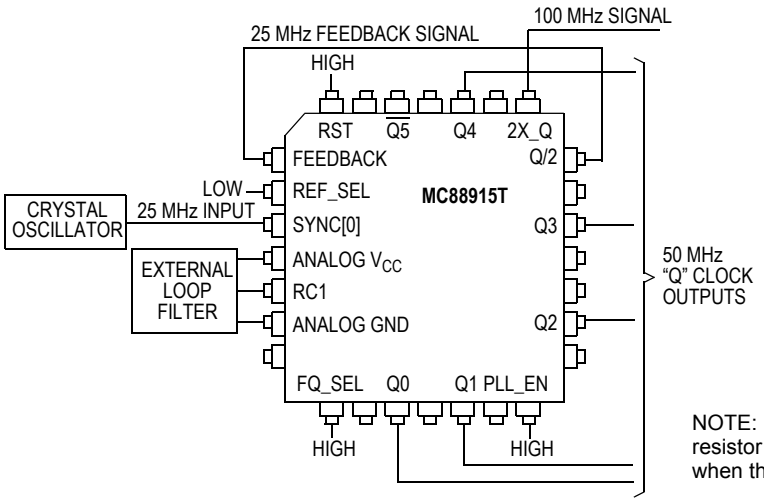


Figure 6. Output/Input Switching Waveforms and Timing Diagrams
(These waveforms represent the hook-up configuration of **Figure 7a**)

TIMING NOTES:

1. The MC88915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the VCC/2 crossing point of the appropriate output edges. All skews are specified as “windows,” not as a ± deviation around a center point.
3. If a “Q” output is connected to the FEEDBACK input (this situation is not shown), the “Q” output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.

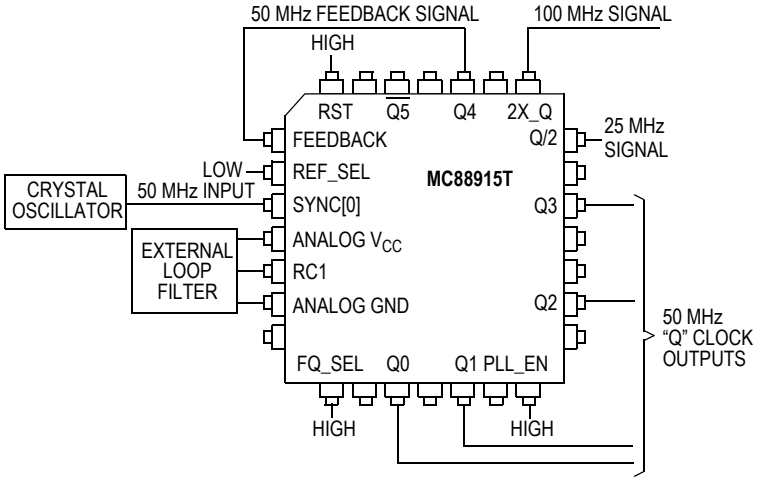


1:2 Input to "Q" Output Frequency Relationship
In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

Allowable Input Frequency Range:
5 MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL HIGH)
2.5 MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

NOTE: If the $\overline{OE}$/$\overline{RST}$ input is active, a pullup or pull-down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3-state.

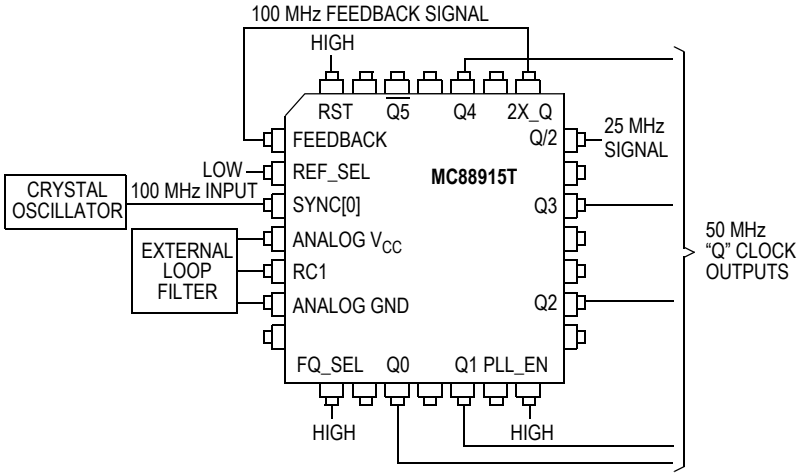
Figure 7a. Wiring Diagram and Frequency Relationships with Q/2 Output Feedback



1:1 Input to "Q" Output Frequency Relationship
In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always rn at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

Allowable Input Frequency Range:
10 MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL HIGH)
5 MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

Figure 7b. Wiring Diagram and Frequency Relationships with Q4 Output Feedback



2:1 Input to "Q" Output Frequency Relationship
In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/3 the 2X_Q frequency, and the "Q" outputs will run at 1/2 the 2X_Q frequency.

Allowable Input Frequency Range:
20 MHz to (2X_Q FMAX Spec) (for FREQ_SEL HIGH)
10 MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 7c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feedback

Figure 7. Wiring Diagrams

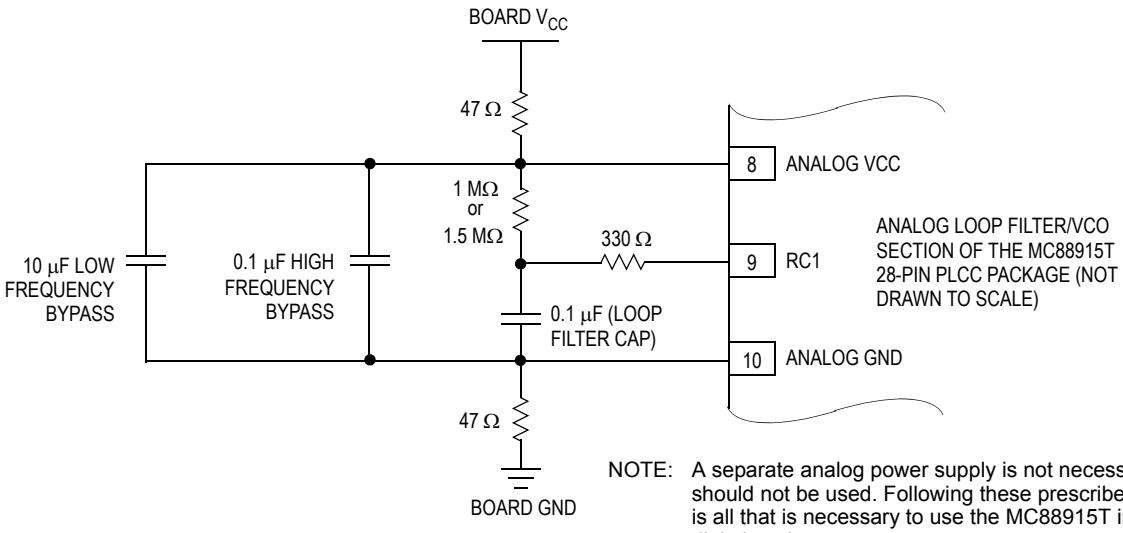


Figure 8. Recommended Loop Filter and Analog Isolation Scheme for the MC88915T

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 8 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:
   a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.
   b. The 47 Ω resistors, the 10 μF low frequency bypass capacitor, and the 0.1 μF high frequency bypass capacitor form a wide bandwidth filter minimizing the 88915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure a 100 mV step deviation on the digital V_{CC} supply, causing no more than a 100 ps phase deviation o the 88915T outputs. A 250 mV step deviation on VCC using the recommended filter values should cause no more than 250 ps phase deviation; if a 25 μF bypass capacitor is used (instead of 10 μF) a 250 mV V_{CC} step should cause no more than a 100 ps phase deviation.
   If good bypass techniques are used on a board design near components potentially causing digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 8 is to give the 88915T additional protection from the power supply and ground plane transients potentially occurring in a high frequency, high speed digital system.
   c. There are no special requirements set forth for the loop filter resistors (1.0 MΩ and 330 Ω). The loop filter capacitor (0.1 μF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.
   d. The 1.0 M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X_Q output) is running above 40 MHz, the 1.0 MΩ resistor provides the correct amount of current injection into the charge pump (2–3 μA). For the TFN55, 70 or 100, if the VCO is running below 40 MHz, a 1.5 MΩ reference resistor should be used (instead of 1 MΩ).
2. In addition to the bypass capacitors used in the analog filter of Figure 8, there should be a 0.1 μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88915T outputs. In addition to reducing potential for noise in the "analog" section of the chip. These bypass capacitors should also be tied as close to the 88915T package as possible.

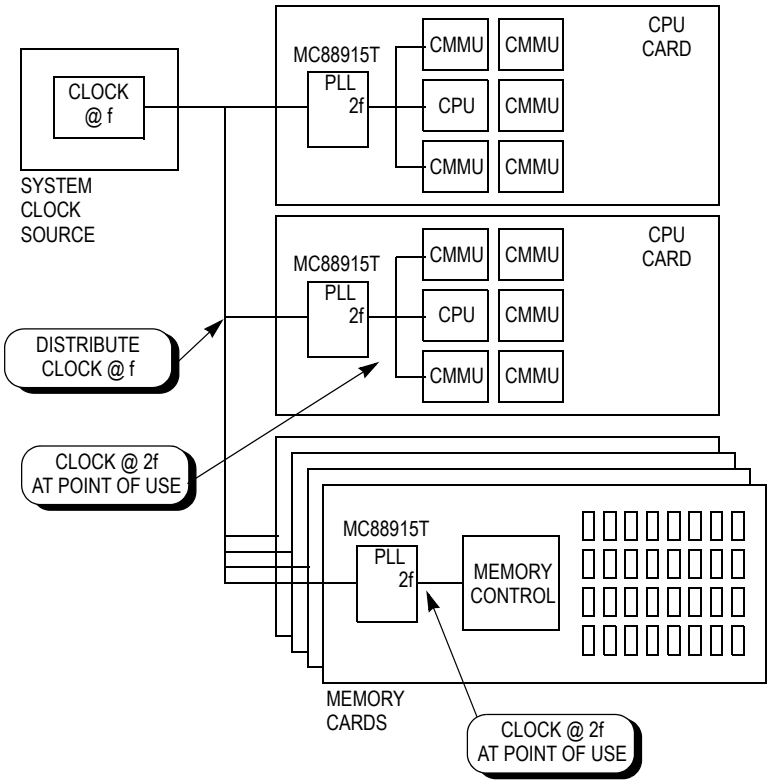


Figure 9. Representation of a Potential Multi-Processing Application Utilizing the MC88915T for Frequency Multiplication and Low Board-to-Board Skew

MC88915T System Level Testing Functionality

Three-state functionality was added to the 100 MHz version of the MC88915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0–Q4, $\overline{Q5}$, and the Q/2 outputs will remain in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output is the inverse of the SYNC signal in this mode. If the 3-state functionality is used, a pull-up or pull-down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the fed back output goes into high impedance.

With the PLL_EN pin low the selected SNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

NOTE: If the outputs are put into 3-state during normal PLL operation, the loop will be broken and phase-lock will be lost. It will take a maximum of 10 ms (t_{LOCK} spec) to regain phase-lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

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