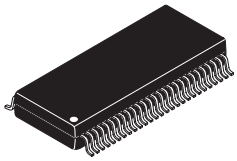
Document Number: MM908E624
Rev. 8.0, 3/2007

Integrated Triple High-Side Switch with Embedded MCU and LIN Serial Communication for Relay Drivers

908E624

HIGH-SIDE SWITCH



DWB SUFFIX
EW (Pb-FREE) SUFFIX
98ASA99294D
54-TERMINAL SOICW

The 908E624 is an integrated single-package solution that includes a high-performance HC08 microcontroller with a *SMARTMOS*™ analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), serial peripheral interface (SPI) (only internal), and an internal clock generator module. The analog control die provides three high-side outputs with diagnostic functions, voltage regulator, watchdog, current sense operational amplifier, and local interconnect network (LIN) physical layer.

The single-package solution, together with LIN, provides optimal application performance adjustments and space-saving PCB design. It is well suited for the control of automotive high-current motors applications using relays (e.g., window lifts, fans, and sun roofs).

Features

- High-Performance M68HC908EY16 Core
- 16 K Bytes of On-Chip Flash Memory, 512 Bytes of RAM
- Internal Clock Generator Module
- Two 16-Bit, 2-Channel Timers
- 10-Bit Analog-to-Digital Converter (ADC)
- LIN Physical Layer Interface
- Low Dropout Voltage Regulator
- Three High-Side Outputs
- Two Wake-Up Inputs
- 16 Microcontroller I/Os
- Pb-Free Packaging Designated by Suffix Code EW

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MM908E624ACDWB/R2	-40°C to 85°C	54 SOICW
*MM908E624ACEW/R2		
*MM908E624AYEW/R2	-40°C to 125°C	

Notes* Recommended for new designs

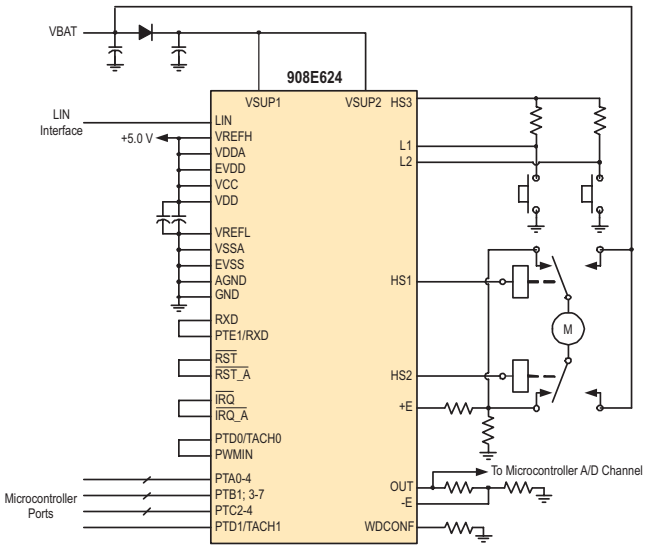


Figure 1. 908E624 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

INTERNAL BLOCK DIAGRAM

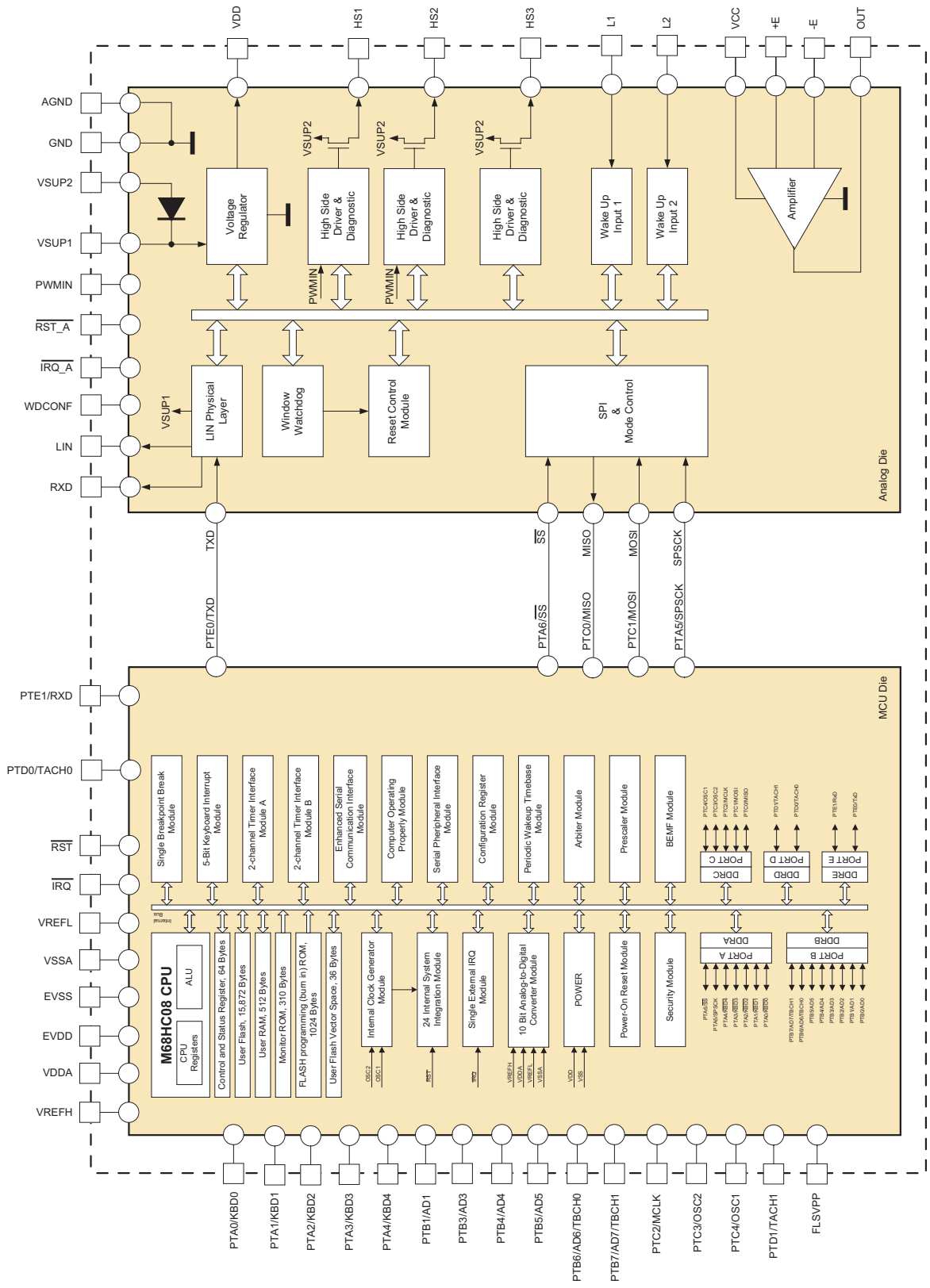


Figure 2. 908E624 Simplified Internal Block Diagram

TERMINAL CONNECTIONS

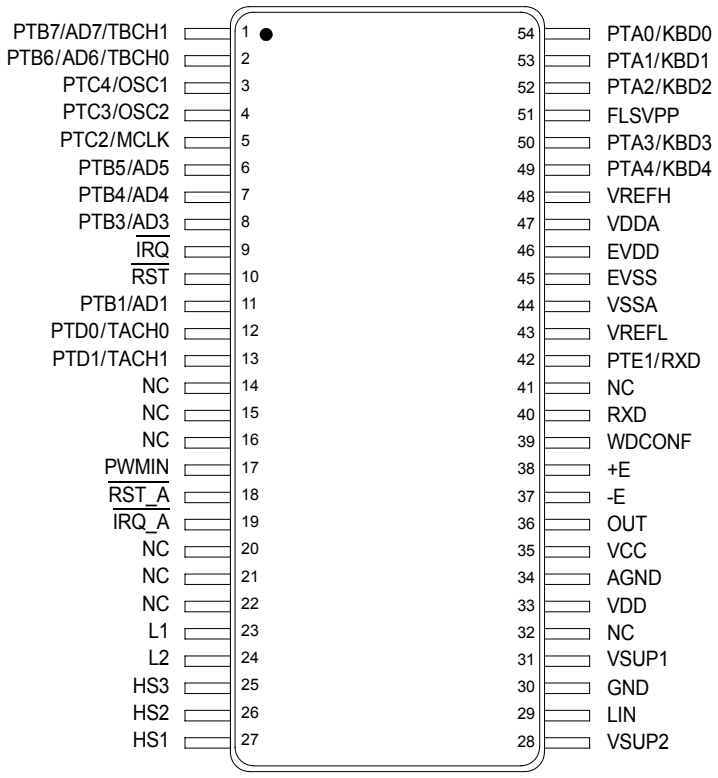


Figure 3. Terminal Connections

Table 1. Terminal Definitions

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 18.

Die	Terminal	Terminal Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	9	IRQ	External Interrupt Input	This terminal is an asynchronous external interrupt input terminal.
MCU	10	RST	External Reset	This terminal is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0 PTD1/TACH1	Port D I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
—	14, 15, 16, 20, 21, 22, 32, 41	NC	No Connect	Not connected.
MCU	42	PTE1/RXD	Port E I/O	This terminal is a special-function, bidirectional I/O port terminal that can is shared with other functional modules in the MCU.

Table 1. Terminal Definitions (continued)

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 18.

Die	Terminal	Terminal Name	Formal Name	Definition
MCU	43 48	VREFL VREFH	ADC References	These terminals are the reference voltage terminals for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Terminals	These terminals are the power supply terminals for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Terminals	These terminals are the ground and power supply terminals, respectively. The MCU operates from a single-power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Terminal	For test purposes only. Do not connect in the application.
Analog	17	PWMIN	Direct High-Side Control Input	This terminal allows the enabling and PWM control of the high-side HS1 and HS2 terminals.
Analog	18	RST_A	Internal Reset Output	This terminal is the reset output terminal of the analog die.
Analog	19	IRQ_A	Internal Interrupt Output	This terminal is the interrupt output terminal of the analog die indicating errors or wake-up events.
Analog	23 24	L1 L2	Wake-Up Inputs	These terminals are the wake-up inputs of the analog chip.
Analog	25 26 27	HS3 HS2 HS1	High-Side Output	These output terminals are low $R_{DS(ON)}$ high-side switches.
Analog	31 28	VSUP1 VSUP2	Power Supply Terminals	These terminals are device power supply terminals.
Analog	29	LIN	LIN Bus	This terminal represents the single-wire bus transmitter and receiver.
Analog	30 34	GND AGND	Power Ground Terminals	These terminals are device power ground connections.
Analog	33	VDD	Voltage Regulator Output	The +5.0 V voltage regulator output terminal is intended to supply the embedded microcontroller.
Analog	35	VCC	Amplifier Power Supply	This terminal is the single +5.0 V power supply for the current sense operational amplifier.
Analog	36	OUT	Amplifier Output	This terminal is the output of the current sense operational amplifier.
Analog	37 38	-E +E	Amplifier Inputs	These terminals are the current sense operational amplifier inverted and non-inverted inputs.
Analog	39	WDCONF	Window Watchdog Configuration Terminal	This input terminal is for configuration of the watchdog period and allows the disabling of the watchdog.
Analog	40	RXD	LIN Transceiver Output	This terminal is the output of LIN transceiver.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any terminal may cause permanent damage to the device.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Supply Voltage			V
Analog Chip Supply Voltage under Normal Operation (Steady-State)	$V_{SUP(SS)}$	-0.3 to 27	
Analog Chip Supply Voltage under Transient Conditions	$V_{SUP(PK)}$	-0.3 to 40	
MCU Chip Supply Voltage	V_{DD}	-0.3 to 5.5	
Input Terminal Voltage			V
Analog Chip	$V_{IN(ANALOG)}$	-0.3 to V_{DD}+0.3	
Microcontroller Chip	$V_{IN(MCU)}$	V_{SS}-0.3 to V_{DD}+0.3	
Maximum Microcontroller Current per Terminal			mA
All Terminals except VDD, VSS, PTA0:PTA6, PTC0:PTC1	$I_{PIN(1)}$	±15	
PTA0:PTA6, PTC0:PTC1 Terminals	$I_{PIN(2)}$	±25	
Maximum Microcontroller VSS Output Current	I_{MVSS}	100	mA
Maximum Microcontroller VDD Input Current	I_{MVDD}	100	mA
Current Sense Operational Amplifier			
Maximum Input Voltage, +E, -E Terminals	V_{+E-E}	-0.3 to 7.0	V
Maximum Input Current, +E, -E Terminals	I_{+E-E}	±20	mA
Maximum Output Voltage, OUT Terminal	V_{OUT}	-0.3 to V_{CC}+0.3	V
Maximum Output Current, OUT Terminal	I_{OUT}	±20	mA
LIN Supply Voltage			V
Normal Operation (Steady-State)	$V_{BUS(SS)}$	-18 to 40	
Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 15)	$V_{BUS(PK)}$	-150 to 100	
L1 and L2 Terminal Voltage			V
Normal Operation with a 33 kΩ resistor (Steady-State)	$V_{WAKE(SS)}$	-18 to 40	
Transient Input Voltage (per ISO7637 Specification) and with External Components (Figure 4, page 15)	$V_{WAKE(PK)}$	-100 to 100	
ESD Voltage			V
Human Body Model (1)	V_{ESD1}	±2000	
Machine Model (1)	V_{ESD2}	±100	
Charge Device Model (1)	V_{ESD3}	±500	

Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any terminal may cause permanent damage to the device.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Package Operating Ambient Temperature (4) MM908E624ACDWB and MM908E624ACEW MM908E624AYEW	T_A	 -40 to 85 -40 to 125	°C
Operating Junction Temperature (2)(4) MM908E624ACDWB and MM908E624ACEW MM908E624AYEW	T_J	 -40 to 125 -40 to 125	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Peak Package Reflow Temperature During Solder Mounting (3) DWB Suffix EW (Pb-Free) Suffix	T_{SOLDER}	 245 260	°C

Notes

2. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation of the analog die. The analog die junction temperature must not exceed 150°C under these conditions.
3. Terminal soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. Independent of $T_{A,}$ device parametrics are only guaranteed for -40 < T_J < 125°C . Please see note 2. T_J is a factor of power dissipation, package thermal resistance, and available heat sinking.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE RANGE					
Nominal Operating Voltage	V_{SUP}	5.5	—	18	V
Functional Operating Voltage (5)	V_{SUPOP}	—	—	27	V
SUPPLY CURRENT RANGE					
Normal Mode (6) V_{SUP} = 13.5 V, Analog Chip in Normal Mode, MCU Operating Using Internal Oscillator at 32 MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	—	20	—	mA
Stop Mode (6), (7) V_{SUP} = 13.5 V, LIN in recessive state	I_{STOP}	—	60	75	µA
Sleep Mode (6), (7) V_{SUP} = 13.5 V, LIN in recessive state	I_{SLEEP}	—	35	45	µA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Terminal $\overline{RST\_A}$					
Low-State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	—	—	0.4	V
High-State Output Current (V_{OUT} > 3.5 V)	I_{OH}	—	250	—	µA
Pulldown Current Limitation	I_{OL_MAX}	-1.5	—	-8.0	mA
Output Terminal $\overline{IRQ\_A}$					V
Low-State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	—	—	0.4	
High-State Output Voltage (I_{OUT} = 250 µA)	V_{OH}	3.85	—	—	
Output Terminal RXD					
Low-State Output Voltage (I_{OUT} = -1.5 mA)	V_{OL}	—	—	0.4	V
High-State Output Voltage (I_{OUT} = 250 µA)	V_{OH}	3.85	—	—	V
Capacitance (8)	C_{IN}	—	4.0	—	pF
Input Terminal PWMIN					
Input Logic Low Voltage	V_{IL}	—	—	1.5	V
Input Logic High Voltage	V_{IH}	3.5	—	—	V
Input Current	I_{IN}	-10	—	10	µA
Capacitance (8)	C_{IN}	—	4.0	—	pF
Terminal TXD, $\overline{SS}$–Pullup Current	I_{PU}	—	40	—	µA

Notes

5. Device is fully functional. All functions are operating. Overtemperature may occur.
6. Total current (I_{VSUP1} + I_{VSUP2}) measured at GND terminal.
7. Stop and Sleep mode current will increase if V_{SUP} exceeds 15 V.
8. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
Low-Voltage Reset (LVR) Threshold	V_{LVRON}	 3.6	 4.0	 4.4	V
Low-Voltage Interrupt (LVI) Threshold Hysteresis	 V_{LVI} V_{LVI_HYS}	 5.7 —	 6.0 1.0	 6.6 —	V
High-Voltage Interrupt (HVI) Threshold Hysteresis	 V_{HVI} V_{HVI_HYS}	 18 —	 19.25 220	 20.5 —	 V mV
VOLTAGE REGULATOR (9)					
Normal Mode Output Voltage 2.0 mA < I_{DD} < 50 mA, 5.5 V < V_{SUP} < 27 V	V_{DDRUN}	 4.75	 5.0	 5.25	V
Normal Mode Output Current Limitation (10)	I_{DDRUN}	50	110	200	mA
Dropout Voltage V_{SUP} = 4.9 V, I_{DD} = 50 mA	V_{DDDROP}	 —	 0.1	 0.2	V
Stop Mode Output Voltage (11)	V_{DDSTOP}	4.75	5.0	5.25	V
Stop Mode Regulator Current Limitation	I_{DDSTOP}	4.0	8.0	14	mA
Line Regulation Normal Mode, 5.5 V < V_{SUP} < 27 V, I_{DD} = 10 mA Stop Mode, 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	 V_{LRRUN} V_{LRSTOP}	 — —	 20 10	 150 100	mV
Load Regulation Normal Mode, 1.0 mA < I_{DD} < 50 mA, V_{SUP} = 18 V Stop Mode, 1.0 mA < I_{DD} < 5.0 mA, V_{SUP} = 18 V	 V_{LRRUN} V_{LDSTOP}	 — —	 40 40	 150 150	mV
Overtemperature Pre-Warning (Junction) (12)	T_{PRE}	120	135	160	°C
Thermal Shutdown Temperature (Junction) (12)	T_{SD}	155	170	—	°C
Temperature Threshold Difference T_{SD}-T_{PRE}	ΔT_{SD}-T_{PRE} 	 20	 30	 45	°C

Notes

9. Specification with external capacitor 2.0 μF< C < 10 μF and 200 mΩ ≤ ESR ≤ 10 Ω. Capacitor value up to 47 μF can be used.
10. Total V_{DD} regulator current. A 5.0 mA current for current sense operational amplifier is included. Digital output supplied from VDD.
11. When switching from Normal to Stop mode or from Stop mode to Normal mode, the output voltage can vary within the output voltage specification.
12. This parameter is guaranteed by process monitoring but not production tested

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW WATCHDOG CONFIGURATION TERMINAL (WDCONF)					
External Resistor Range	R_{EXT}	10	—	100	kΩ
Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy) (13)	WD_{CACC}	-15	—	15	%
LIN PHYSICAL LAYER					
LIN Transceiver Output Voltage					V
Recessive State, TXD HIGH, I_{OUT} = 1.0 μA	V_{LIN_REC}	V_{SUP}-1	—	—	
Dominant State, TXD LOW, 500 Ω External Pullup Resistor	V_{LIN_DOM}	—	—	1.4	
Normal Mode Pullup Resistor to VSUP	R_{PU}	20	30	60	kΩ
Stop, Sleep Mode Pullup Current Source	I_{PU}	—	2.0	—	μA
Output Current Shutdown Threshold	$I_{OV\text{-}CUR}$	50	75	150	mA
Leakage Current to GND	I_{BUS}				μA
VSUP Disconnected, V_{BUS} at 18 V		—	1.0	10	
Recessive State, 8.0 V ≤ V_{SUP} ≤ 18 V, 8.0 V≤ V_{BUS} ≤ 18 V, V_{BUS} ≥ V_{SUP}		0.0	3.0	20	
GND Disconnected, V_{GND} = V_{SUP}, V_{BUS} at -18 V		-1.0	—	1.0	
LIN Receiver					V_{SUP}
Receiver Threshold Dominant	V_{BUS_DOM}	—	—	0.4	
Receiver Threshold Recessive	V_{BUS_REC}	0.6	—	—	
Receiver Threshold Center	V_{BUS_CNT}	0.475	0.5	0.525	
Receiver Threshold Hysteresis	V_{BUS_HYS}	—	—	0.175	

Notes

13. Watchdog timing period calculation formula: P_{WD} = 0.991 * R_{EXT}+0.648 (R_{EXT} in kΩ and P_{WD} in ms).

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HIGH-SIDE OUTPUTS HS1 AND HS2					
Switch On Resistance	$R_{DS(ON)}$				Ω
T_J = 25°C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V		—	2.0	2.5	
T_J = 125°C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V		—	—	4.5	
T_J = 125°C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} > 9.0 V		—	3.0	—	
Output Current Limit	I_{LIM}	300	—	600	mA
Overtemperature Shutdown (14), (15)	T_{HSSD}	155	—	190	°C
Leakage Current	I_{LEAK}	—	—	10	μA
Output Clamp Voltage	V_{CL}				V
I_{OUT} = -100 mA		-6.0	—	—	
HIGH-SIDE OUTPUT HS3					
Switch On Resistance	$R_{DS(ON)}$				Ω
T_J = 25°C, I_{LOAD} = 50 m A, V_{SUP} > 9.0 V		—	—	7.0	
T_J = 125°C, I_{LOAD} = 50 mA, V_{SUP} > 9.0 V		—	—	10	
T_J = 125°C, I_{LOAD} = 30 mA, 5.5 V < V_{SUP} > 9.0 V		—	—	14	
Output Current Limitation	I_{LIM}	60	100	200	mA
Overtemperature Shutdown (14), (15)	T_{HSSD}	155	—	190	°C
Leakage Current	I_{LEAK}	—	—	10	μA

Notes

14. This parameter is guaranteed by process monitoring but it is not production tested
15. When overtemperature occurs, switch is turned off and latched off. Flag is set in SPI.

Table 3. Static Electrical Characteristics (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE OPERATIONAL AMPLIFIER					
Rail-to-Rail Input Voltage	V_{IMC}	-0.1	—	V_{CC}+0.1	V
Output Voltage Range					V
Output Current ±1.0 mA	V_{OUT1}	0.1	—	V_{CC}-0.1	
Output Current ±5.0 mA	V_{OUT2}	0.3	—	V_{CC}-0.3	
Input Bias Current	I_B	—	—	250	nA
Input Offset Current	I_O	-100	—	100	nA
Input Offset Voltage	V_{IO}	-25	—	25	mV
L1 AND L2 INPUTS					
Low Detection Threshold	V_{THL}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.5	
18 V < V_{SUP} < 27 V		2.7	3.2	3.7	
High Detection Threshold	V_{THH}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.5	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Hysteresis	V_{HYS}				V
5.5 V < V_{SUP} < 27 V		0.5	—	1.3	
Input Current	I_{IN}				μA
-0.2 V < V_{IN} < 40 V		-10	—	10	

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Driver Characteristics for Normal Slew Rate (16), (17)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	50	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	50	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	50	µs
Propagation Delay Symmetry: $t_{DOM-MIN}$ - $t_{REC-MAX}$	dt1	-10.44	—	—	µs
Propagation Delay Symmetry: $t_{DOM-MAX}$ - $t_{REC-MIN}$	dt2	—	—	11	µs
Driver Characteristics for Slow Slew Rate (16), (18)					
Dominant Propagation Delay TXD to LIN	$t_{DOM-MIN}$	—	—	100	µs
Dominant Propagation Delay TXD to LIN	$t_{DOM-MAX}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MIN}$	—	—	100	µs
Recessive Propagation Delay TXD to LIN	$t_{REC-MAX}$	—	—	100	µs
Propagation Delay Symmetry: $t_{DOM-MIN}$ - $t_{REC-MAX}$	dt1s	-22	—	—	µs
Propagation Delay Symmetry: $t_{DOM-MAX}$ - $t_{REC-MIN}$	dt2s	—	—	23	µs
Driver Characteristics for Fast Slew Rate					
LIN High Slew Rate (Programming Mode)	SR_{FAST}	—	15	—	V/µs
Receiver Characteristics and Wake-Up Timings					
Receiver Dominant Propagation Delay (19)	t_{RL}	—	3.5	6.0	µs
Receiver Recessive Propagation Delay (19)	t_{RH}	—	3.5	6.0	µs
Receiver Propagation Delay Symmetry	t_{R-SYM}	-2.0	—	2.0	µs
Bus Wake-Up Deglitcher	t_{PROPWL}	35	—	150	µs
Bus Wake-Up Event Reported (20)	t_{WAKE}	—	20	—	µs

Notes

16. V_{SUP} from 7.0 V to 18 V, bus load R0 and C0 1.0 nF/1.0 kΩ, 6.8 nF/660 Ω, 10 nF/500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
17. See Figure 6, page 15.
18. See Figure 7, page 16.
19. Measured between LIN signal threshold V_{IL} or V_{IH} and 50% of RXD signal.
20. t_{WAKE} is typically 2 internal clock cycles after LIN rising edge detected. See Figure 8 and Figure 9, page 16. In Sleep mode the V_{DD} rise time is strongly dependent upon the decoupling capacitor at VDD terminal.

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER (CONTINUED)					
Output Current Shutdown Delay	$t_{OV-DELAY}$	—	10	—	µs
SPI INTERFACE TIMING					
SPI Operating Recommended Frequency	f_{SPIOP}	0.25	—	4.0	MHz
L1 AND L2 INPUTS					
Wake-Up Filter Time (21)	t_{WUF}	8.0	20	38	µs
WINDOW WATCHDOG CONFIGURATION TERMINAL (WDCONF)					
Watchdog Period	t_{PWD}				ms
External Resistor R_{EXT} = 10 kΩ (1%)		—	10.558	—	
External Resistor R_{EXT} = 100 kΩ (1%)		—	99.748	—	
Without External Resistor R_{EXT} (WDCONF Terminal Open)		97	150	205	
STATE MACHINE TIMING					
Reset Low-Level Duration after V_{DD} High (25)	$t_{\overline{RST}}$	0.65	1.0	1.35	ms
Interrupt Low-Level Duration	$t_{\overline{INT}}$	7.0	10	13	µs
Normal Request Mode Timeout (25)	t_{NRTOUT}	97	150	205	ms
Delay Between SPI Command and HS1/HS2/HS3 Turn On (22), (23)	t_{S-HSON}	—	3.0	10	µs
Delay Between SPI Command and HS1/HS2/HS3 Turn Off (22), (23)	$t_{S-HSOFF}$	—	3.0	10	µs
Delay Between Normal Request and Normal Mode After W/D Trigger Command (24)	t_{S-NR2N}	6.0	35	70	µs
Delay Between $\overline{SS}$ Wake-Up ($\overline{SS}$ LOW to HIGH) and Normal Request Mode (VDD On and Reset High)	$t_{W-\overline{SS}}$	15	40	80	µs
Delay Between $\overline{SS}$ Wake-Up ($\overline{SS}$ LOW to HIGH) and First Accepted SPI Command	t_{W-SPI}	90	—	N/A	µs
Delay Between Interrupt Pulse and First SPI Command Accepted	$t_{S-1STSPI}$	30	—	N/A	µs
Minimum Time Between Two Rising Edges on $\overline{SS}$	$t_{2\overline{SS}}$	15	—	—	µs

Notes
21. This parameter is guaranteed by process monitoring but is not production tested.
22. Delay between turn-on or turn-off command and high-side on or high-side off, excluding rise or fall time due to external load.
23. Delay between the end of the SPI command (rising edge of the $\overline{SS}$) and start of device activation/deactivation.
24. This parameter is guaranteed by process monitoring but it is not production tested.
25. Also see Figure 10 on page 17

Table 4. Dynamic Electrical Characteristics (continued)

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 data sheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0 V ≤ V_{SUP} ≤ 16 V, -40°C ≤ T_J ≤ 125°C unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE OPERATIONAL AMPLIFIER					
Supply Voltage Rejection Ratio (26)	SVR	60	—	—	dB
Common Mode Rejection Ratio (26)	CMR	70	—	—	dB
Gain Bandwidth (26)	GBP	1.0	—	—	MHz
Slew Rate	SR	0.5	—	—	V/μs
Phase Margin (for Gain = 1, Load 100 pF/ 5.0 kΩ (26)	PHMO	40	—	—	°
Open Loop Gain	OLG	—	85	—	dB

Notes

26. This parameter is guaranteed by process monitoring but it is not production tested.

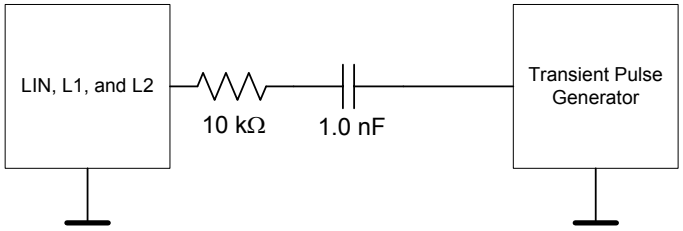
MICROCONTROLLER PARAMETRICS

Table 5. Microcontroller

For a detailed microcontroller description, refer to the MC68HC908EY16 data sheet.

Module	Description
Core	High-Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0 MHz
Timer	Two 16-Bit Timers with 2 Channels (TIM A and TIM B)
Flash	16 K Bytes
RAM	512 Bytes
ADC	10-Bit Analog-to-Digital Converter
SPI	SPI Module
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module

TIMING DIAGRAMS



Note Waveform in accordance with ISO7637 Part 1, Test Pulses 1, 2, 3a, and 3b.

Figure 4. Test Circuit for Transient Test Pulses

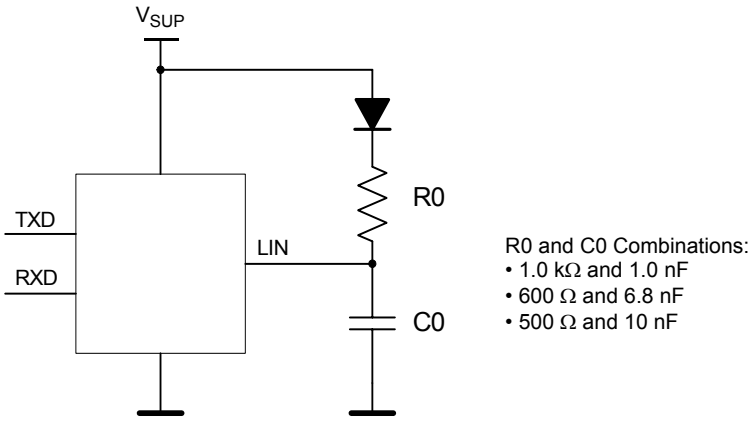


Figure 5. Test Circuit for LIN Timing Measurements

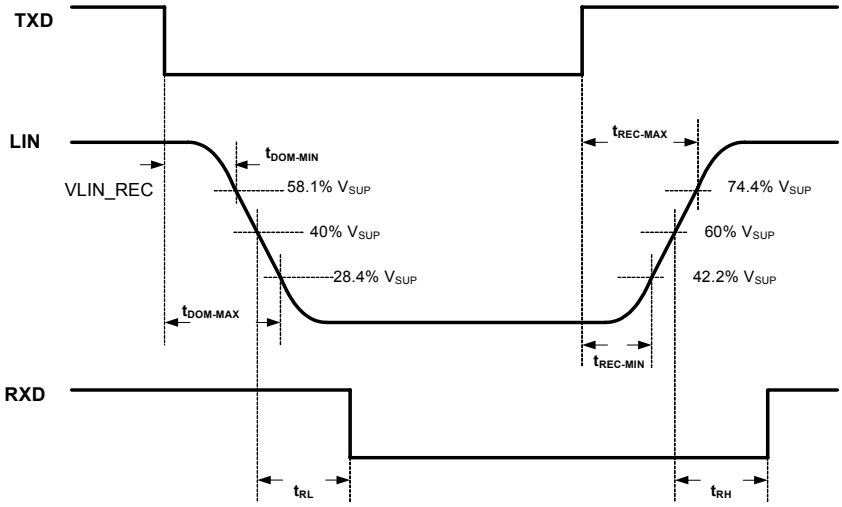


Figure 6. LIN Timing Measurements for Normal Slew Rate

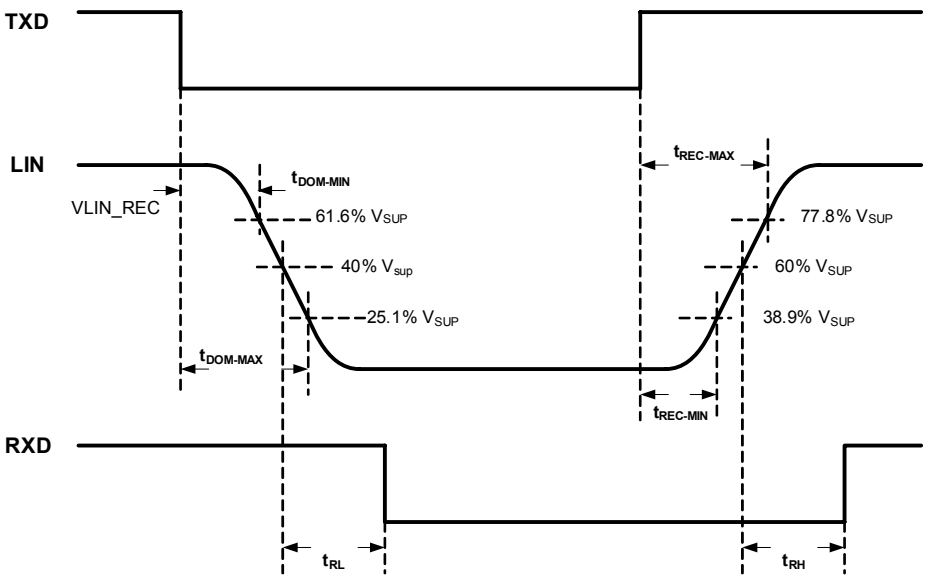


Figure 7. LIN Timing Measurements for Slow Slew Rate

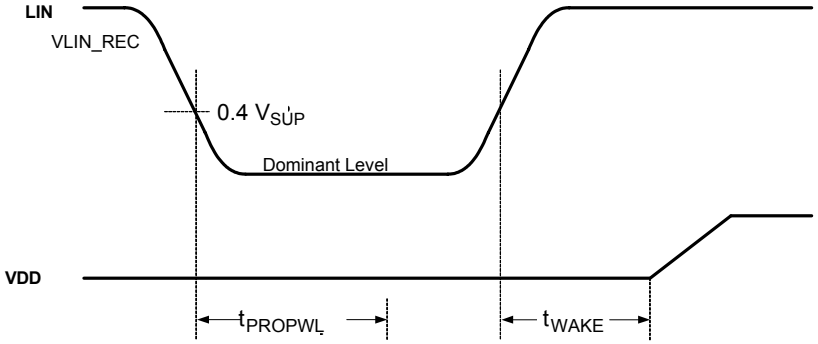


Figure 8. Wake-Up Sleep Mode Timing

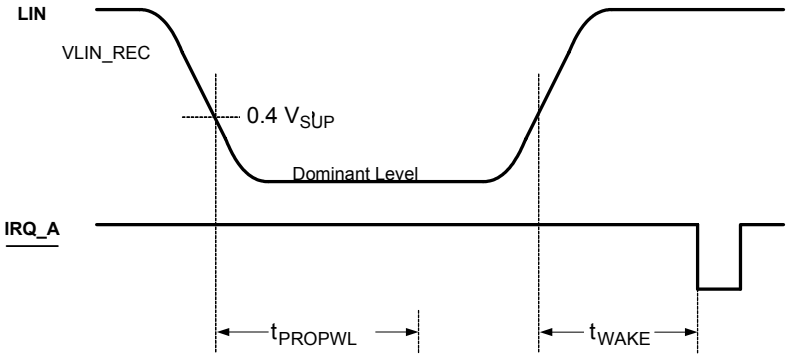


Figure 9. Wake-Up Stop Mode Timing

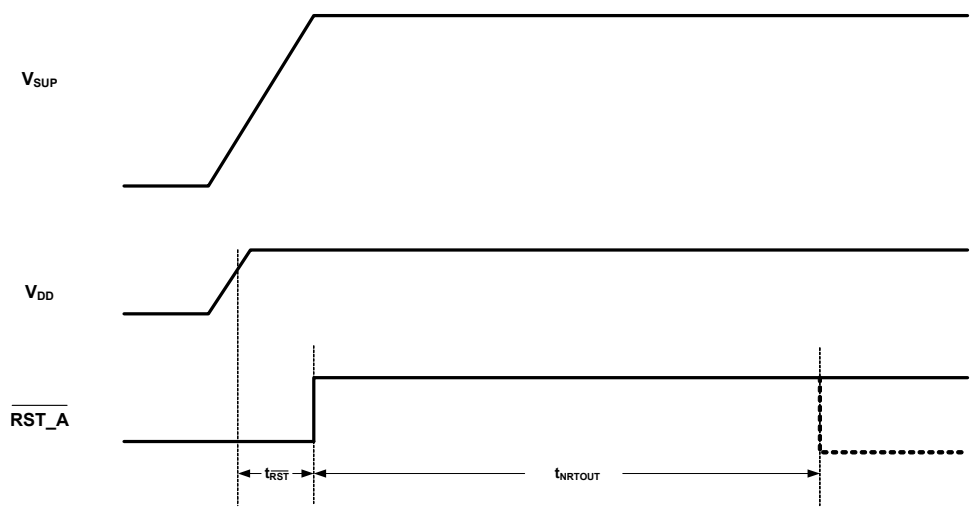


Figure 10. Power On Reset and Normal Request Time-out Timing

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E624 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E624 is well suited to perform relay control in applications like window lift, sunroof, etc., via a three-wire LIN bus.

The device combines an HC908EY16 MCU core with flash memory together with a *SmartMOS* IC chip. The *SmartMOS* IC chip combines power and control in one chip. Power switches are provided on the *SmartMOS* IC configured as high-side outputs. Other ports are also provided, which include a current sense operational amplifier port and two wake-up terminals. An internal voltage regulator provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with three-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

FUNCTIONAL TERMINAL DESCRIPTION

See Figure 1, 908E624 Simplified Application Diagram, page 1, for a graphic representation of the various terminals referred to in the following paragraphs. Also, see the terminal diagram on page 3 for a depiction of the terminal locations on the package.

PORT A I/O TERMINALS (PTA0:4)

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt terminals KBD0:KBD4.

The PTA5/SPSCK terminal is not accessible in this device and is internally connected to the SPI clock terminal of the analog die. The PTA6/$\overline{SS}$ terminal is likewise not accessible.

For details, refer to the 68HC908EY16 data sheet.

PORT B I/O TERMINALS (PTB1:7)

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. All terminals are shared with the ADC module. The PTB6:PTB7 terminals are also shared with the Timer B module.

The PTB0/AD0 and PTB2/AD2 terminals are not accessible in this device.

For details, refer to the 68HC908EY16 data sheet.

PORT C I/O TERMINALS (PTC2:4)

These terminals are special-function, bidirectional I/O port terminals that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI terminals of the analog die.

For details, refer to the 68HC908EY16 data sheet.

PORT D I/O TERMINALS (PTD:0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special-function, bidirectional I/O port terminals that can also be programmed to be timer terminals.

For details, refer to the 68HC908EY16 data sheet.

PORT E I/O TERMINAL (PTE1)

PTE1/RXD and PTE0/TXD are special-function, bidirectional I/O port terminals that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD terminal of the analog die. The connection for the receiver must be done externally.

For details, refer to the 68HC908EY16 data sheet.

EXTERNAL INTERRUPT TERMINAL ($\overline{IRQ}$)

The $\overline{IRQ}$ terminal is an asynchronous external interrupt terminal. This terminal contains an internal pullup resistor that is always activated, even when the $\overline{IRQ}$ terminal is pulled LOW.

For details, refer to the 68HC908EY16 data sheet.

EXTERNAL RESET TERMINAL ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ terminal forces the MCU to a known startup state. It is driven LOW when any internal reset source is asserted.

This terminal contains an internal pullup resistor that is always activated, even when the reset terminal is pulled LOW.

Important To ensure proper operation, do not add any external pullup resistor.

For details, refer to the 68HC908EY16 data sheet.

MCU POWER SUPPLY TERMINALS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground terminals, respectively. The MCU operates from a single-power supply.

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details, refer to the 68HC908EY16 data sheet.

ADC SUPPLY TERMINALS (VDDA AND VSSA)

VDDA and VSSA are the power supply terminals for the analog-to-digital converter (ADC). It is recommended that a high-quality ceramic decoupling capacitor be placed between these terminals.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces. VSSA is the ground terminal for the ADC and should be tied to the same potential as EVSS via separate traces.

For details, refer to the 68HC908EY16 data sheet.

ADC REFERENCE TERMINALS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage terminals for the ADC. It is recommended that a high-quality ceramic decoupling capacitor be placed between these terminals.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSSA via separate traces.

For details, refer to the 68HC908EY16 data sheet.

TEST TERMINAL (FLSVPP)

This terminal is for test purposes only. Do not connect in the application or connect to GND.

PWMIN TERMINAL (PWMIN)

This terminal is the direct PWM input for high-side outputs 1 and 2 (HS1 and HS2). If no PWM control is required, PWMIN must be connected to VDD to enable the HS1 and HS2 outputs.

LIN TRANSCEIVER OUTPUT TERMINAL (RXD)

This terminal is the output of LIN transceiver. The terminal must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD terminal).

RESET TERMINAL ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the reset output terminal of the analog die and must be connected to the $\overline{\text{RST}}$ terminal of the MCU.

Important To ensure proper operation, do not add any external pullup resistor.

INTERRUPT TERMINAL ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output terminal of the analog die indicating errors or wake-up events. This terminal must be connected to the $\overline{\text{IRQ}}$ terminal of the MCU.

WINDOW WATCHDOG CONFIGURATION TERMINAL (WDCONF)

This terminal is the configuration terminal for the internal watchdog. A resistor is connected to this terminal. The resistor value defines the watchdog period. If the terminal is open, the watchdog period is fixed to its default value.

The watchdog can be disabled (e.g., for flash programming or software debugging) by connecting this terminal to GND.

POWER SUPPLY TERMINALS (VSUP1 AND VSUP2)

This VSUP1 power supply terminal supplies the voltage regulator, the internal logic, and LIN transceiver.

This VSUP2 power supply terminal is the positive supply for the high-side switches.

POWER GROUND TERMINAL (GND)

This terminal is the device ground connection.

HIGH-SIDE OUTPUT TERMINALS (HS1 AND HS2)

These terminals are high-side switch outputs to drive loads such as relays or lamps. Each switch is protected with overtemperature and current limit (overcurrent). The output has an internal clamp circuitry for inductive load. The HS1 and HS2 outputs are controlled by SPI and have a direct enabled input (PWMIN) for PWM capability.

HIGH-SIDE OUTPUT TERMINAL (HS3)

This high-side switch can be used to drive small lamps, Hall-effect sensors, or switch pullup resistors. The switch is protected with overtemperature and current limit (overcurrent). The output is controlled only by SPI.

LIN BUS TERMINAL (LIN)

The LIN terminal represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

WAKE-UP TERMINALS (L1 AND L2)

These terminals are high-voltage capable inputs used to sense external switches and to wake up the device from Sleep or Stop mode. During Normal mode the state of these terminals can be read through SPI.

Important If unused these terminals should be connected to VSUP or GND to avoid parasitic transitions. In Low Power Mode this could lead to random wakeup events.

CURRENT SENSE OPERATIONAL AMPLIFIER TERMINALS (E+, E-, OUT, VCC)

These are the terminals of the single-supply current sense operational amplifier.

- The E+ and E- input terminals are the non-inverting and inverting inputs of the current sense operational amplifier, respectively.
- The OUT terminal is the output terminal of the current sense operational amplifier.
- The VCC terminal is the +5.0 V single-supply connection.

Note If the operational amplifier is not used, it is possible to connect all terminals (E+, E-, OUT and VCC) to GND - in this case all of the four terminals must be grounded.

+5.0 V VOLTAGE REGULATOR OUTPUT TERMINAL (VDD)

The VDD terminal is needed to place an external capacitor to stabilize the regulated output voltage. The VDD terminal is intended to supply the embedded microcontroller. The terminal is protected against shorts to GND with an integrated current limit (temperature shutdown could occur).

Important The VDD, EVDD, VDDA, and VREFH terminals must be connected together.

VOLTAGE REGULATOR AND CURRENT SENSE AMPLIFIER GROUND TERMINAL (AGND)

The AGND terminal is the ground terminal of the voltage regulator and the current sense operational amplifier.

Important GND, AGND, VSS, EVSS, VSSA, and VREFL terminals must be connected together.

NO CONNECT TERMINALS (NC)

The NC terminals are not connected internally.

Note Each of the NC terminals can be left open or connected to ground (recommended).

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

908E624 ANALOG DIE MODES OF OPERATION

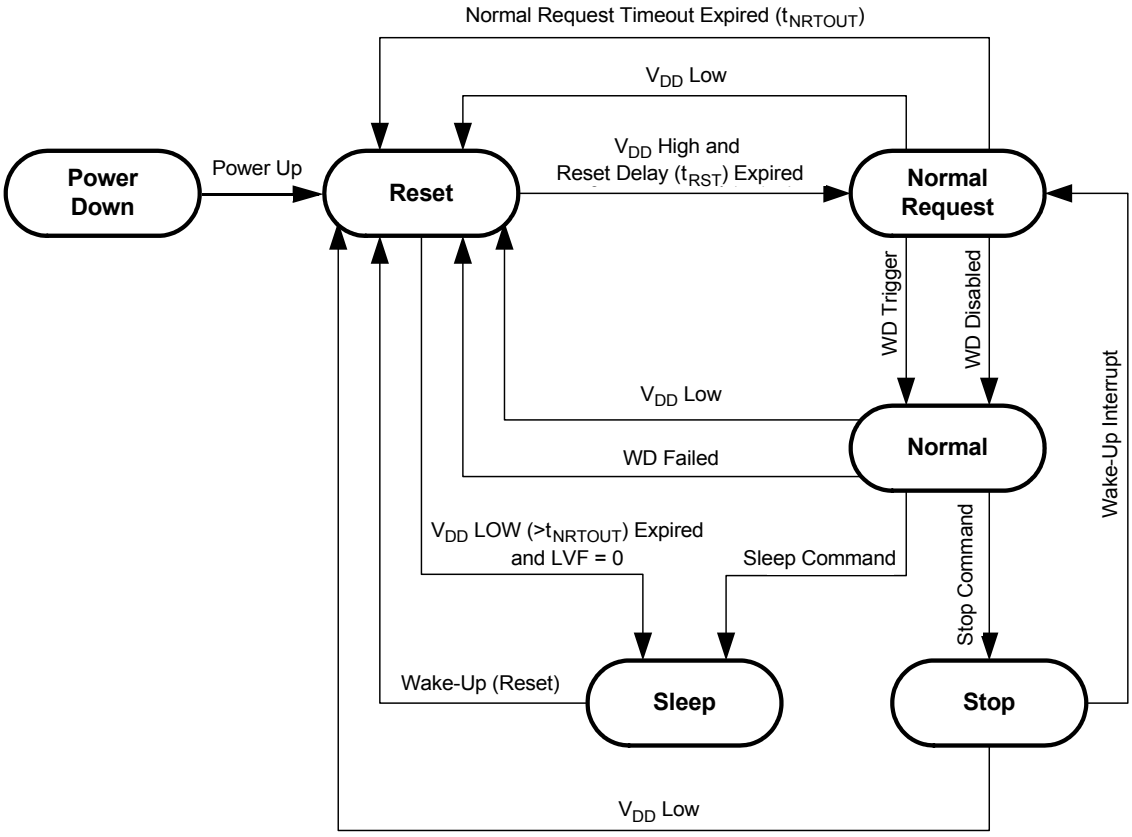
The 908E624 offers three operating modes: Normal (Run), Stop, and Sleep. In Normal mode the device is active and is operating under normal application conditions. The Stop and Sleep modes are low-power modes with wake-up capabilities.

In Stop mode the voltage regulator still supplies the MCU with V_{DD} (limited current capability) and in Sleep mode the voltage regulator is turned off (V_{DD} = 0 V).

Wake-up from Stop mode is initiated by a wake-up interrupt. Wakeup from Sleep mode is done by a reset and the voltage regulator is turned back on.

The selection of the different modes is controlled by the MODE1:2 bits in the SPI Control register.

Figure 11 describes how transitions are done between the different operating modes and Table 6, page 22, gives an overview of the operating mode.



Legend
WD: Watchdog
WD Disabled: Watchdog disabled (WDCONF terminal connected to GND)
WD Trigger: Watchdog is triggered by SPI command
WD Failed: No watchdog trigger or trigger occurs in closed window
Stop Command: Stop command sent via SPI
Sleep Command: Sleep command sent via SPI
Wake-Up: L1 or L2 state change or LIN bus wake-up or $\overline{SS}$ rising edge

Figure 11. Operating Modes and Transitions

Table 6. Operating Modes Overview

Device Mode	Voltage Regulator	Wake-Up Capabilities	$\overline{\text{RST\_A}}$ Output	Watchdog Function	HS1, HS2, and HS3	LIN Interface	Sense Amplifier
Reset	V_{DD} ON	N/A	LOW	Disabled	Disabled	Recessive only	Not active
Normal Request	V_{DD} ON	N/A	HIGH	150 ms time out if WD enabled	Enabled	Transmit and receive	Not active
Normal (Run)	V_{DD} ON	N/A	HIGH	Window WD if enabled	Enabled	Transmit and receive	Active
Stop	V_{DD} ON with limited current capability	LIN wake-up, L1, L2 state change, $\overline{\text{SS}}$ rising edge	HIGH	Disabled	Disabled	Recessive state with wake-up capability	Not active
Sleep	V_{DD} OFF	LIN wake-up L1, L2 state change	LOW	Disabled	Disabled	Recessive state with wake-up capability	Not active

INTERRUPTS

In Normal (Run) mode the 908E624 has four different interrupt sources. An interrupt pulse on the $\overline{\text{IRQ\_A}}$ terminal is generated to report a fault to the MCU. All interrupts are not maskable and cannot be disabled.

After an Interrupt the INTSRC bit in the SPI Status register is set, indicating the source of the event. This interrupt source information is only transferred once, and the INTSRC bit is cleared automatically.

Low-Voltage Interrupt

Low-voltage interrupt (LVI) is related to external supply voltage VSUP1. If this voltage falls below the LVI threshold, it will set the LVF bit in the SPI Status register and an interrupt will be initiated. The LVF bit remains set as long as the Low-voltage condition is present.

During Sleep and Stop mode the low-voltage interrupt circuitry is disabled.

High-Voltage Interrupt

High-voltage interrupt (HVI) is related to external supply voltage VSUP1. If this voltage rises above the HVI threshold, it will set the HVF bit in the SPI Status register and an interrupt will be initiated. The HVF bit remains set as long as the high-voltage condition is present.

During Sleep and Stop mode the high-voltage interrupt circuitry is disabled.

Wake-Up Interrupts

In Stop mode the $\overline{\text{IRQ\_A}}$ terminal reports wake-up events on the L1, L2, or the LIN bus to the MCU. All wake-up interrupts are not maskable and cannot be disabled.

After a wake-up interrupt, the INTSRC bit in the Serial Peripheral Interface (SPI) Status register is set, indicating the source of the event. This wake-up source information is only transferred once, and the INTSRC bit is cleared automatically.

Figure 12, page 23, describes the Stop/Wake-Up procedure.

Voltage Regulator Temperature Prewarning (VDDT)

Voltage regulator temperature prewarning (VDDT) is generated if the voltage regulator temperature is above the T_{PRE} threshold. It will set the VDDT bit in the SPI Status register and an interrupt will be initiated. The VDDT bit remains set as long as the error condition is present.

During Sleep and Stop mode the voltage regulator temperature prewarning circuitry is disabled.

High-Side Switch Thermal Shutdown (HSST)

The high-side switch thermal shutdown HSST is generated if one of the high-side switches HS1:HS3 is above the HSST threshold, it will shutdown all high-side switches, set the HSST flag in the SPI Status register and an interrupt will be initiated. The HSST bit remains set as long as the error condition is present.

During Sleep and Stop mode the high-side switch thermal shutdown circuitry is disabled.

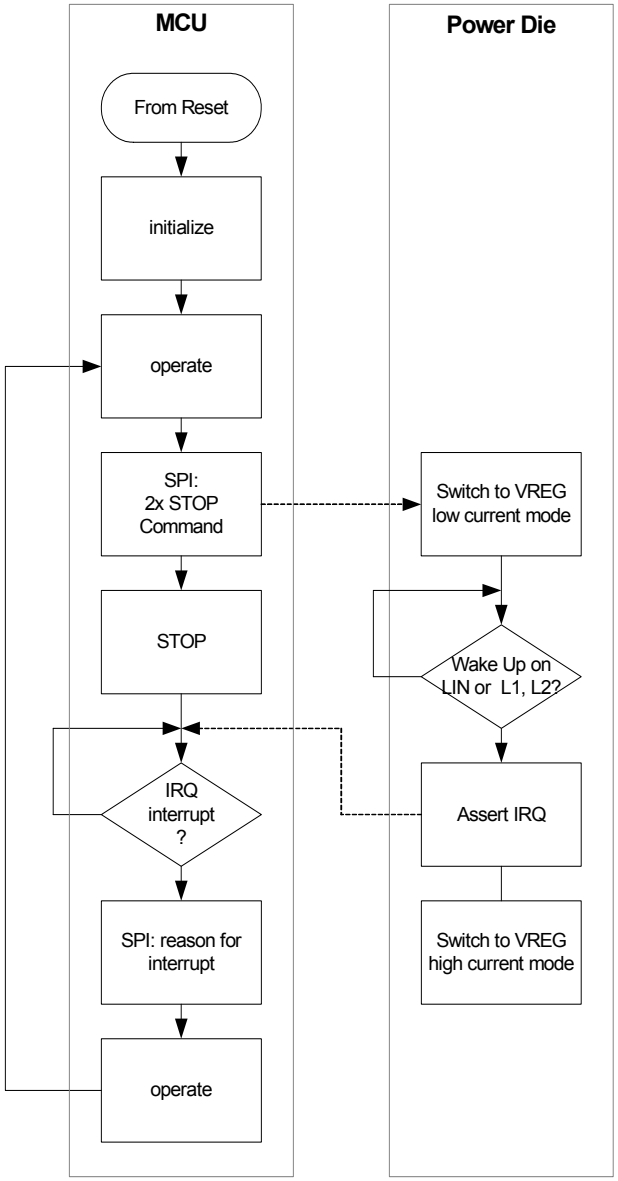


Figure 12. Stop Mode/Wake-Up Procedure

ANALOG DIE INPUTS/OUTPUTS

High-Side Output Terminals HS1 and HS2

These are two high-side switches used to drive loads such as relays or lamps. They are protected with overtemperature and current limit (overcurrent) and include an active internal clamp circuitry for inductive load drive. Control is done using the SPI Control register. PWM capability is offered through the PWMIN input terminal.

The high-side switch is turned on if both the HSxON bit in the SPI Control register is set and the PWMIN input is HIGH (refer to Figure 13, page 24). In order to have HS1 on, the PWMIN must be HIGH and bit HS1ON must be set. The same applies to the HS2 output.

If no PWM control is required, PWMIN must be connected to the VDD terminal.

Current Limit (Overcurrent) Protection

These high-side switches feature current limit to protect them against overcurrent and short circuit conditions.

Overtemperature Protection

If an overtemperature condition occurs on any of the three high-side switches, all high-side switches (HS1, HS2 and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop modes the high-sides are disabled.

High-Side Output HS3

This high-side switch can be used to drive small lamps, Hall-effect sensors, or switch pullup resistors. Control is done using the SPI Control register. No direct PWM control is possible on this terminal (refer to Figure 14, page 25).

Current Limit (Overcurrent) Protection

This high-side feature switch feature current limit to protect it against overcurrent and short circuit conditions.

Overtemperature Protection

If an overtemperature condition occurs on any of the three high-side switches, all high-side switches (HS1, HS2 and HS3) are turned off and latched off. The failure is reported by the HSST bit in the SPI Control register.

Sleep and Stop Mode

In Sleep and Stop mode the high-side is disabled.

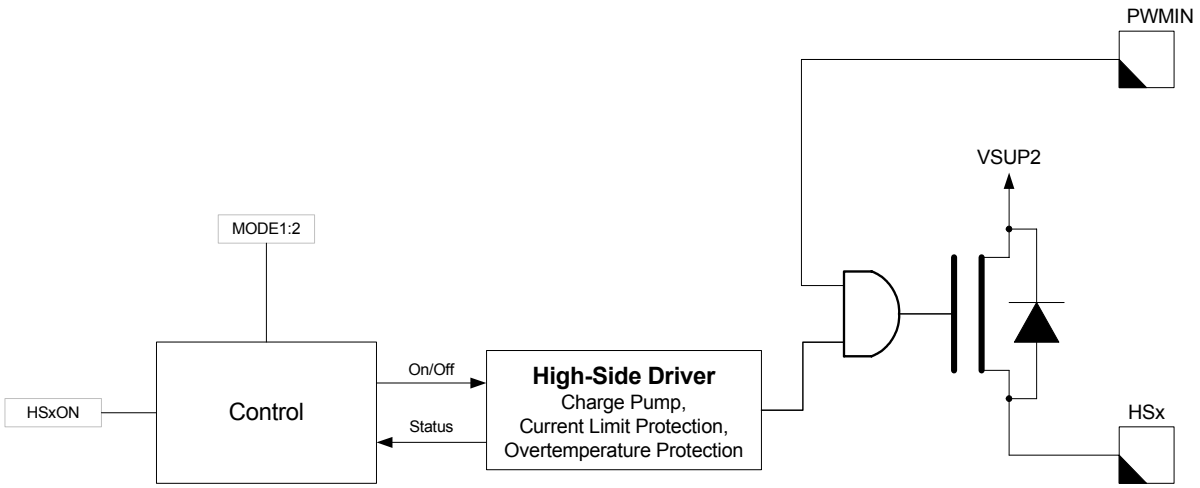


Figure 13. High-Side HS1 and HS2 Circuitry

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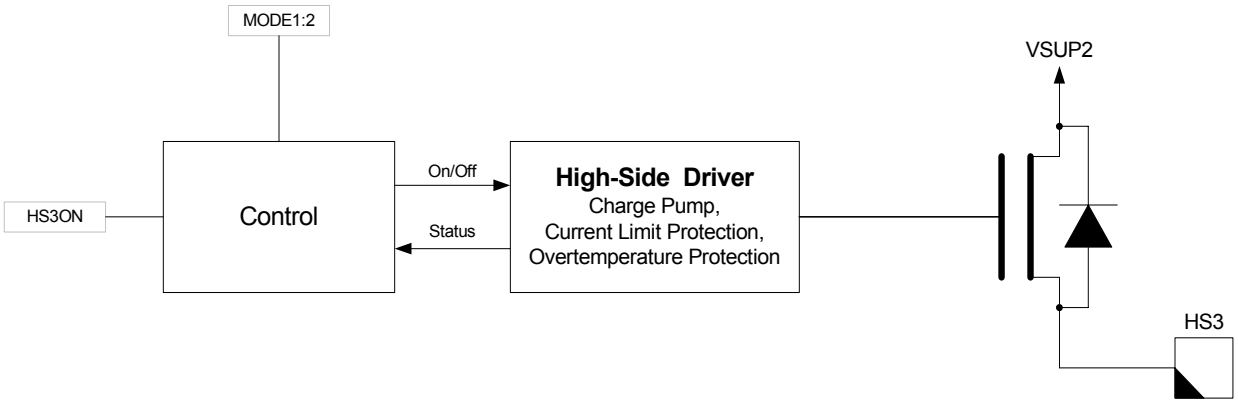


Figure 14. High-Side HS3 Circuitry

LIN PHYSICAL LAYER

The LIN bus terminal provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low-side MOSFET with over current protection and thermal shutdown. An internal pullup resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The slew rate can be selected for optimized operation at 10 and 20kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LINSL2:1 in the SPI Control Register. The initial slew rate is optimized for 20kBit/s.

The LIN terminal offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled in Normal and Normal Request mode.

An over current condition (e.g. LIN bus short to Vbat) or a over temperature in the output low-side FET will shutdown the transmitter and set the LINFAIL flag in the SPI Status Register.

For improved performance and safe behavior in case of LIN bus short to Ground or LIN bus leakage during low power mode the internal pull-up resistor on the LIN terminal can be disconnected, with the LIN-PU bit in the SPI Control Register, and a small current source keeps the LIN bus at recessive level. In case of a LIN bus short to GND, this feature will reduce the current consumption in STOP and SLEEP modes.

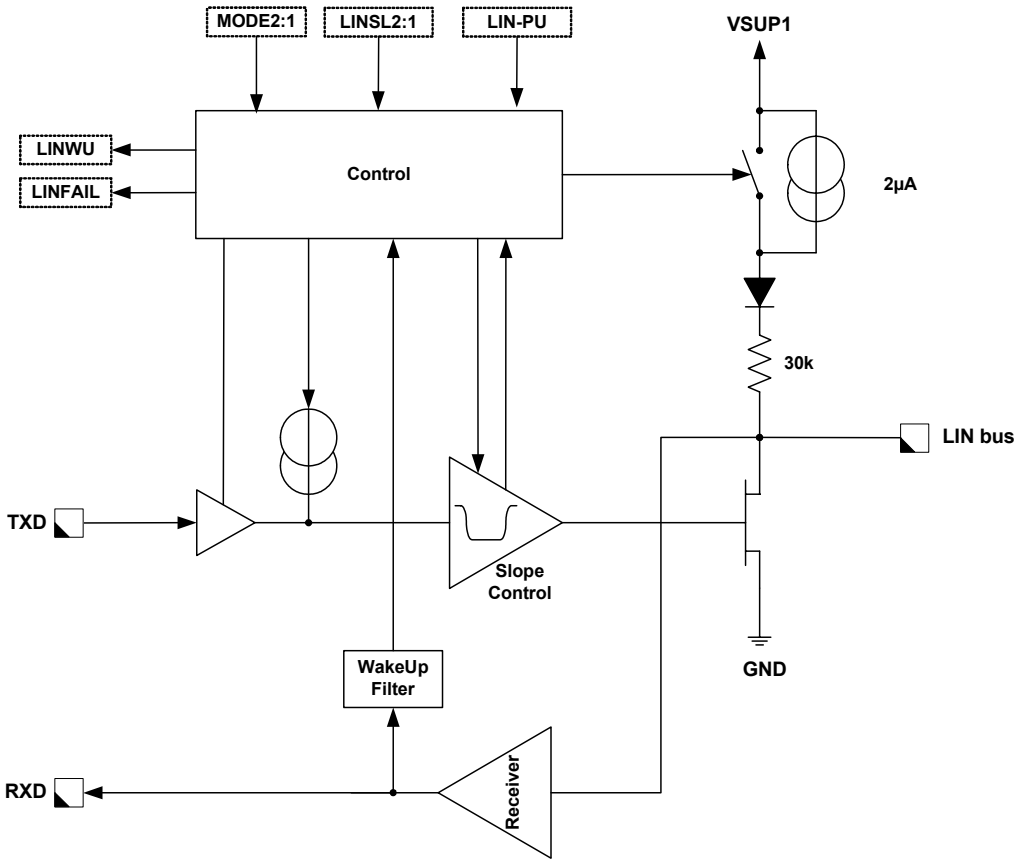


Figure 15. LIN Interface

TXD Terminal

The TXD terminal is the MCU interface to control the state of the LIN transmitter (see Figure 2, page 2). When TXD is LOW, the LIN terminal is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off (recessive state). The TXD terminal has an internal pullup current source in order to set the LIN bus to recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Terminal

The RXD transceiver terminal is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode and Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Stop mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN terminal in recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line.

A dominant level longer than T_{propWL} followed by an rising edge will generate a wake-up interrupt and set the LINWF flag in the SPI Status Register. Also see Figure 9, page 16.

SLEEP Mode and Wake-up Feature

During SLEEP mode operation the transmitter of the physical layer is disabled. In case the bit LIN-PU was set in the Sleep mode sequence the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN terminal in recessive state. The receiver is still active to be able to detect wake-up events on the LIN bus line.

A dominant level longer than T_{propWL} followed by an rising edge will generate a system wake-up (reset) and set the LINWF flag in the SPI Status Register . Also see Figure 8, page 16).

WINDOW WATCHDOG

The window watchdog is configurable using an external resistor at the WDCONF terminal. The watchdog is cleared through by the MODE1:2 bits in the SPI Control register (refer to Table 8, page 29).

A watchdog clear is only allowed in the open window. If the watchdog is cleared in the closed window or has not been cleared at the end of the open window, the watchdog will generate a reset on the $\overline{\text{RST\_A}}$ terminal and reset the whole device.

Note The watchdog clear in Normal request mode (150 ms) (first watchdog clear) has no window.

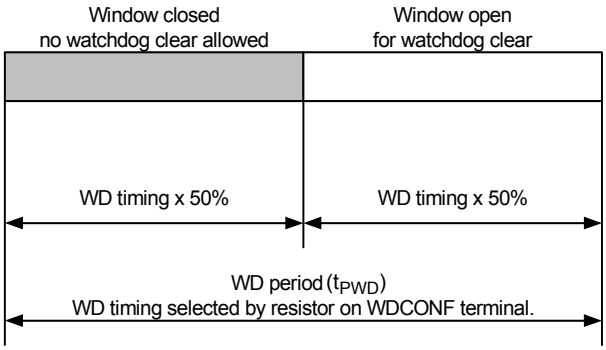


Figure 16. Window Watchdog Operation

Watchdog Configuration

If the WDCONF terminal is left open, the default watchdog period is selected (typ. 150 ms). If no watchdog function is required, the WDCONF terminal must be connected to GND.

The watchdog period is calculated using the following formula:

$$t_{PWD}\ [ms] = 0.991 * R_{EXT}\ [k\Omega] + 0.648$$

VOLTAGE REGULATOR

The 908E624 chip contains a low-power, low dropout voltage regulator to provide internal power and external power for the MCU. The on-chip regulator consist of two elements, the main voltage regulator and the low-voltage reset circuit.

The V_{DD} regulator accepts an unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD terminal to provide the 5.0 V to the microcontroller.

Current Limit (Overcurrent) Protection

The voltage regulator has current limit to protect the device against overcurrent and short circuit conditions.

Overtemperature Protection

The voltage regulator also features an overtemperature protection having an overtemperature warning (Interrupt - VDDT) and an overtemperature shutdown.

Stop Mode

During Stop mode, the Stop mode regulator supplies a regulated output voltage. The Stop mode regulator has a limited output current capability.

Sleep Mode

In Sleep mode the voltage regulator external V_{DD} is turned off.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E624, various parameters (e.g., ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the “empty” (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

The usage of the trim values, located in the flash memory, is explained in the following.

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low-frequency base clock (IBASE), will vary as much as ±25 percent due to process, temperature, and voltage dependencies. To compensate for these dependencies, an ICG trim value is located at address $FDC2. After trimming the ICG, a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100nF) and stabilized (4,7uF) V_{DD} = 5V, $T_{Ambient}$~23°C) and will vary over temperature and voltage (VDD) as indicated in the 68HC908EY16 data sheet.

To trim the ICG, these values have to be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to be copied after every reset.

OPERATING MODES OF THE MCU

For a detailed description of the operating modes of the MCU, refer to the MC68HC908EY16 data sheet.

LOGIC COMMANDS AND REGISTERS

908E624 SPI INTERFACE AND CONFIGURATION

The serial peripheral interface creates the communication link between the microcontroller and the analog die of the 908E624.

The interface consists of four terminals (see Figure 17):

- $\overline{SS}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 8 bits of control information and the slave replies with 8 bits of status data.

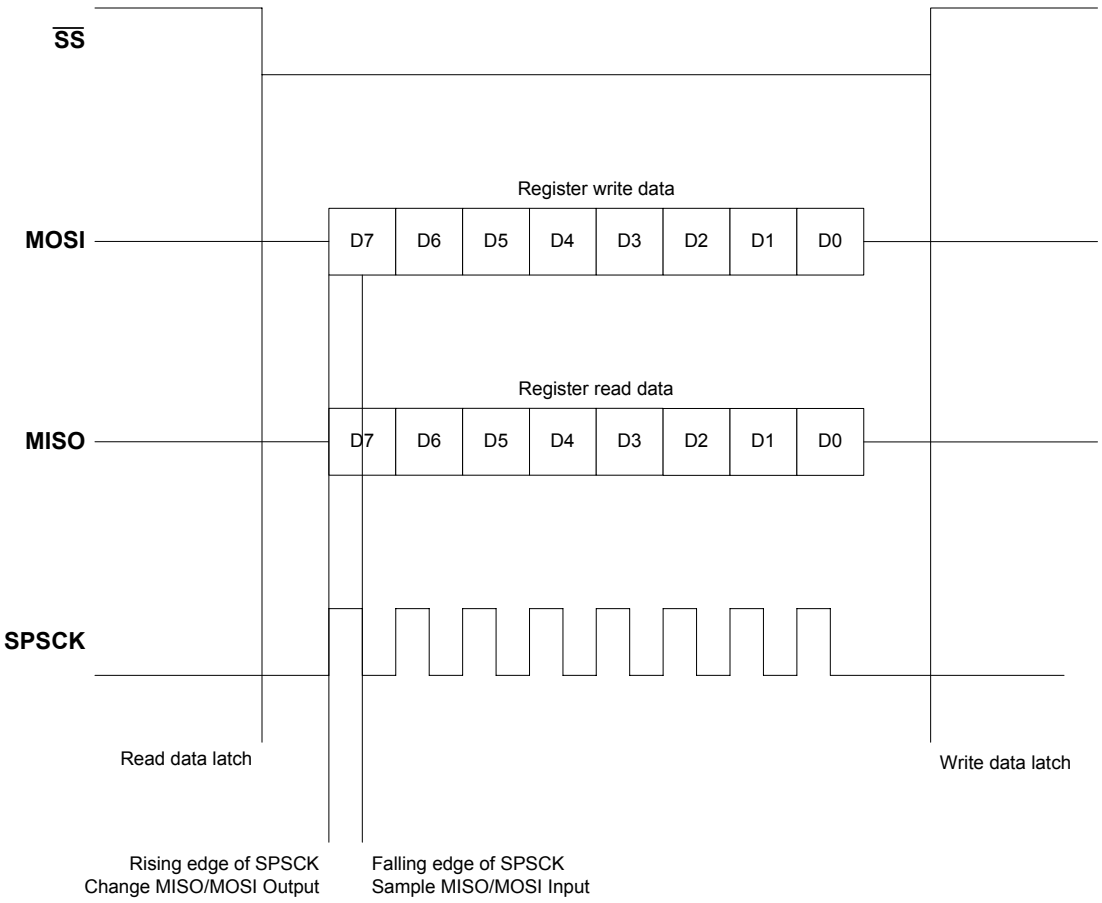


Figure 17. SPI Protocol

During the inactive phase of the $\overline{SS}$ (HIGH), the new data transfer is prepared.

The falling edge of the $\overline{SS}$ indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (Register read data).

With the rising edge of the SPI clock, SPSCK the data is moved to MISO/MOSI terminals. With the falling edge of the SPI clock SPSCK the data is sampled by the Receiver.

The data transfer is only valid if exactly 8 sample clock edges are present in the active (low) phase of $\overline{SS}$.

The rising edge of the slave select $\overline{SS}$ indicates the end of the transfer and latches the write data (MOSI) into the register The $\overline{SS}$ high forces MISO to the high impedance state.

SPI REGISTER OVERVIEW

Table 7 summarizes the SPI Register bit meaning, reset value, and bit reset condition.

Table 7. SPI Register Overview

Read/Write Information	Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
Write	LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
Read	INTSRC (27)	LINWU or LINFAIL	HVF	LVF or BATFAIL (28)	VDDT	HSST	L2	L1
Write Reset Value	0	0	0	0	0	0	—	—
Write Reset Condition	POR, RESET	POR, RESET	POR	POR, RESET	POR, RESET	POR, RESET	—	—

Notes
27. D7 signals interrupts and wake-up interrupts, D6:D0 indicated the source.
28. The first SPI read after reset returns the BATFAIL flag state on bit D4.

SPI Control Register (Write)

Table 8 shows the SPI Control register bits by name.

Table 8. Control Bits Function (Write Operation)

D7	D6	D5	D4	D3	D2	D1	D0
LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1

LINSL2:1—LIN Baud Rate and Low-Power Mode Selection Bits

These bits select the LIN slew rate and requested low-power mode in accordance with Table 9. Reset clears the LINSL2:1 bits.

Table 9. LIN Baud Rate and Low-Power Mode Selection Bits

LINSL2	LINSL1	Description
0	0	Baud Rate up to 20 kbps (normal)
0	1	Baud Rate up to 10 kbps (slow)
1	0	Fast Program Download Baud Rate up to 100 kbps
1	1	Low-Power Mode (Sleep or Stop) Request

LIN-PU—LIN Pullup Enable Bit

This bit controls the LIN pullup resistor during Sleep and Stop modes.

- 1 = Pullup disconnected in Sleep and Stop modes.
- 0 = Pullup connected in Sleep and Stop modes.

In case the Pullup is disconnected a small current source is used to pull the LIN terminal in recessive state. In case of an erroneous short of the LIN bus to ground this will significantly reduce the power consumption, e.g. in combination with STOP/SLEEP mode.

HS3ON:HS1ON—High-Side H3:HS1 Enable Bits

These bits enable the HSx. Reset clears the HSxON bit.

- 1 = HSx switched on (refer to Note below).
- 0 = HSx switched off.

Note If no PWM on HS1 and HS2 is required, the PWMIN terminal must be connected to the VDD terminal.

MODE2:1—Mode Section Bits

The MODE2:1 bits control the operating modes and the watchdog in accordance with Table 10.

Table 10. Mode Selection Bits

MODE2	MODE1	Description
0	0	Sleep Mode (29)
0	1	Stop Mode (29)
1	0	Watchdog Clear (30)
1	1	Run (Normal) Mode

Notes
29. To enter Sleep and Stop mode, a special sequence of SPI commands is implemented.
30. The device stays in Run (Normal) mode.

To safely enter Sleep or Stop mode and to ensure that these modes are not affected by noise issue during SPI transmission, the Sleep/Stop commands require two SPI transmissions.

Sleep Mode Sequence

The Sleep command, as shown in Table 11, must be sent twice.

Table 11. Sleep Command Bits

LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
1	1	0/1	0	0	0	0	0

Stop Mode Sequence

The Stop command, as shown in Table 12, must be sent twice.

Table 12. Stop Command Bits

LINSL2	LINSL1	LIN-PU	HS3ON	HS2ON	HS1ON	MODE2	MODE1
1	1	0/1	0	0	0	0	1

SPI Status Register (Read)

Table 13 shows the SPI Status register bits by name.

Table 13. Control Bits Function (Read Operation)

D7	D6	D5	D4	D3	D2	D1	D0
INTSRC	LINWU or LINFAIL	HVF	LVF or BATFAIL	VDDT	HSST	L2	L1

INTSCR—Register Content Flags or Interrupt Source

This bit indicates if the register contents reflect the flags or an interrupt/wake-up interrupt source.

- 1 = D6:D0 reflects the interrupt or wake-up source.
- 0 = No interrupt occurred. Other SPI bits report real time status.

LINWU/LINFAIL—LIN Status Flag Bit

This bit indicates a LIN wake-up condition.

- 1 = LIN bus wake-up occurred or LIN overcurrent/ overtemperature occurred.
- 0 = No LIN bus wake-up occurred.

In case of a LIN overcurrent/overtemperature condition the LIN transmitter is disabled. To reenable the LIN transmitter, the error condition must be GONE and the LINWU/LINFAIL flag must be cleared.

The flag is cleared by reading the flag when it is set (SPI command).

HVF —High-Voltage Flag Bit

This flag is set on an overvoltage (VSUP1) condition.

- 1 = High-voltage condition has occurred.
- 0 = no High-voltage condition.

LVF/BATFAIL—Low-Voltage Flag Bit

This flag is set on an undervoltage (VSUP1) condition.

- 1 = Low-voltage condition has occurred.
- 0 = No low-voltage condition.

VDDT—Voltage Regulator Status Flag Bit

This flag is set as pre-warning in case of an over-temperature condition on the voltage regulator.

- 1 = Voltage regulator overtemperature condition, pre-warning.
- 0 = No overtemperature detected.

HSST—High-Side Status Flag Bit

This flag is set on overtemperature conditions on one of the high-side outputs.

- 1 = HSx off due to overtemperature.
- 0 = No overtemperature.

In case one of the high-sides has an overtemperature condition all high-side switches are disabled.

To reenable the high-side switches, the flags have to be cleared, by reading the flag when it is set and by writing a one to high-side HSxON bit (two SPI commands are necessary).

L2:L1—Wake-Up Inputs L1, L2 Status Flag Bit

These flags reflect the status of the L2 and L1 input terminals and indicate the wake-up source.

- 1 = L2:L1 input high or wake-up by L2:L1 (first register read after wake-up indicated with INTSRC = 1).
- 0 = L2:L1 input low.

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E624 has the MC68HC908EY16 MCU embedded typically all the development tools available for the MCU also apply for this device, however due to the fact of the additional analog die circuitry and the nominal +12 V supply voltage some additional items have to be considered:

- nominal 12 V rather than 5.0 V or 3.0 V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ terminal, but $\overline{IRQ\_A}$ terminal
- MCU monitoring (Normal request timeout) has to be disabled

For a detailed information on the MCU related development support see the MC68HC908EY16 data sheet - section development support.

The programming is principally possible at two stages in the manufacturing process — first on chip level, before the IC is soldered onto a PCB board and second after the IC is soldered onto the PCB board.

Chip Level Programming

On Chip level the easiest way is to only power the MCU with +5.0 V (see Figure 18) and not to provide the analog chip with VSUP, in this setup all the analog terminal should be left open (e.g. VSUP[1:2]) and interconnections between MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 data sheet - section development support.

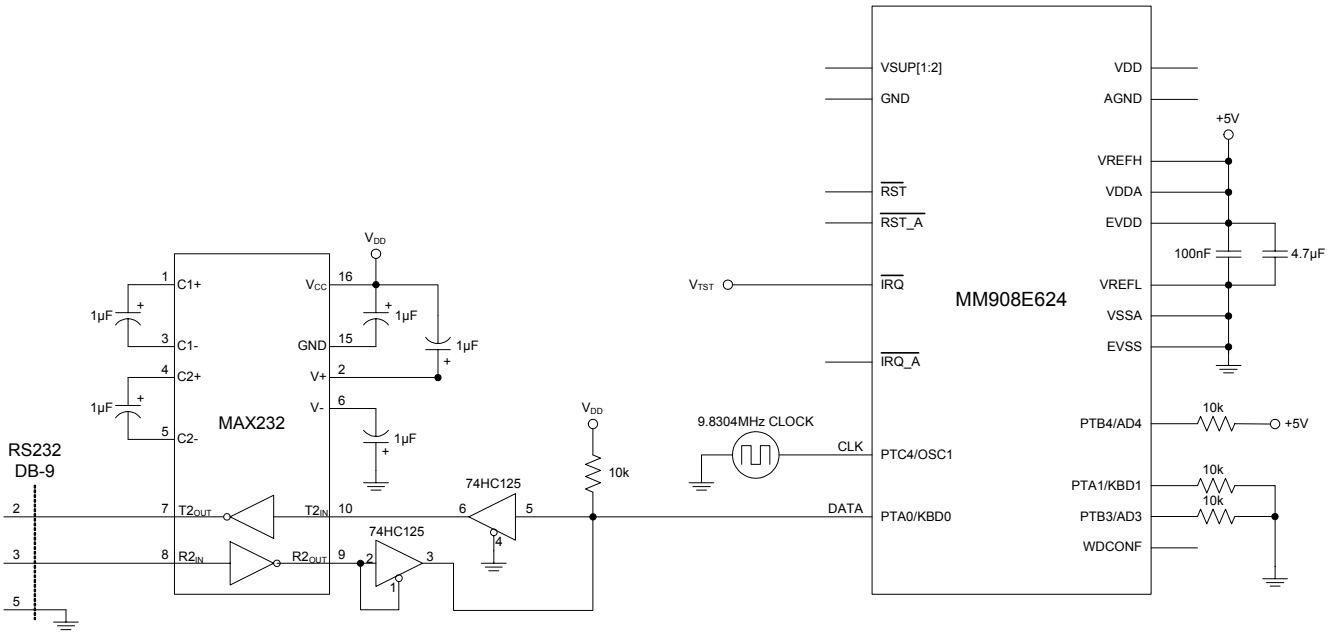


Figure 18. Normal Monitor Mode Circuit (MCU only)

Of course it is also possible to supply the whole system with VSUP (12 V) instead as described in Figure 19, page 32.

PCB Level Programming

If the IC is soldered onto the PCB board it is typically not possible to separately power the MCU with +5.0 V, the whole system has to be powered up providing V_{SUP} (see Figure 19).

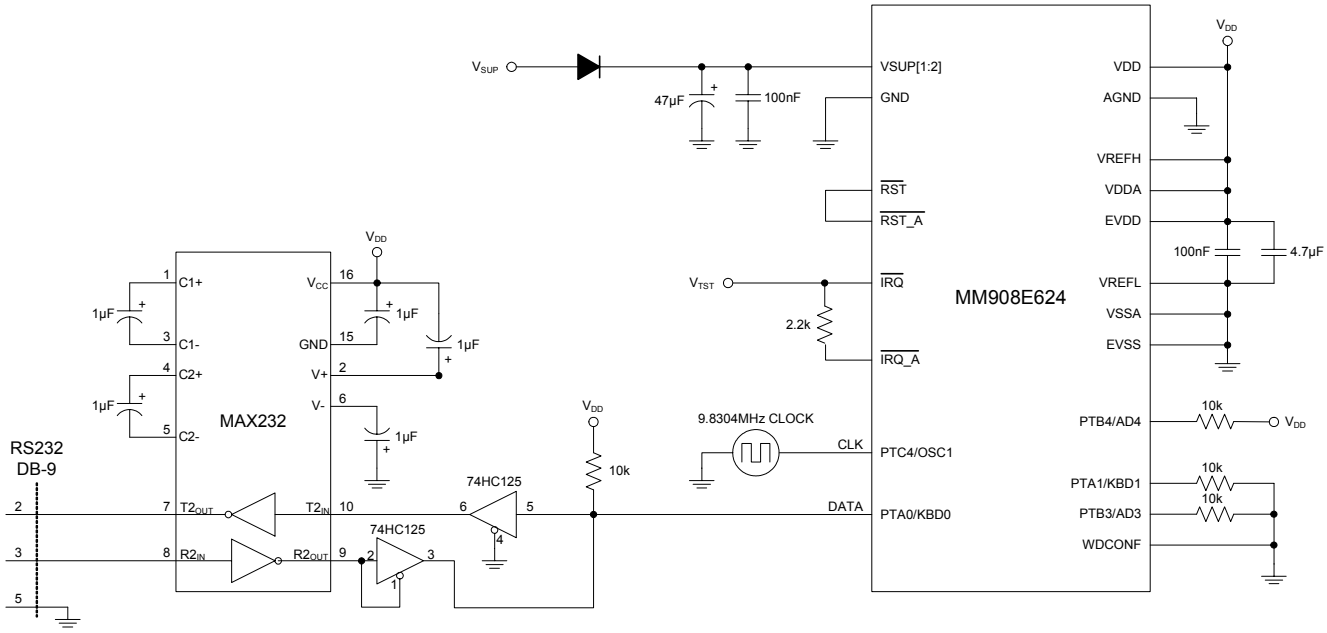


Figure 19. Normal Monitor Mode Circuit

Table 14 summarizes the possible configurations and the necessary setups.

Table 14. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	WDCONF	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Timeout	Communication Speed		
					PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	GND	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	GND	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND								ON	disabled	disabled	—	Nominal 1.6MHz	Nominal 6300
User	V_{DD}	V_{DD}	R_{EXT}	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6MHz	Nominal 6300

Notes

31. PTA0 must have a pullup resistor to V_{DD} in monitor mode.
32. External clock is a 4.9152 MHz, 9.8304 MHz or 19.6608 MHz canned oscillator on OCS1.
33. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256.
34. X = don't care.
35. V_{TST} is a high voltage $V_{DD} + 3.5\ V \le V_{TST} \le V_{DD} + 4.5\ V$.

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be e.g. found on the Freescale website www.freescale.com.

VSUP Terminals (VSUP1 and VSUP2)

Its recommended to place a high-quality ceramic decoupling capacitor close to the VSUP terminals to improve EMC/EMI behavior.

LIN Terminal

For DPI (Direct Power Injection) and ESD (Electro Static Discharge) it is recommended to place a high-quality ceramic decoupling capacitor near the LIN terminal. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage Regulator Output Terminals (VDD and AGND)

Use a high-quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU Digital Supply Terminals (EVDD and EVSS)

Fast signal transitions on MCU terminals place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high-quality ceramic decoupling capacitor be placed between these terminals.

MCU Analog Supply Terminals (VREFH, VDDA and VREFL, VSSA)

To avoid noise on the analog supply terminals it is important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 20 and Figure 21 show the recommendations on schematics and layout level and Table 15 indicates recommended external components and layout considerations.

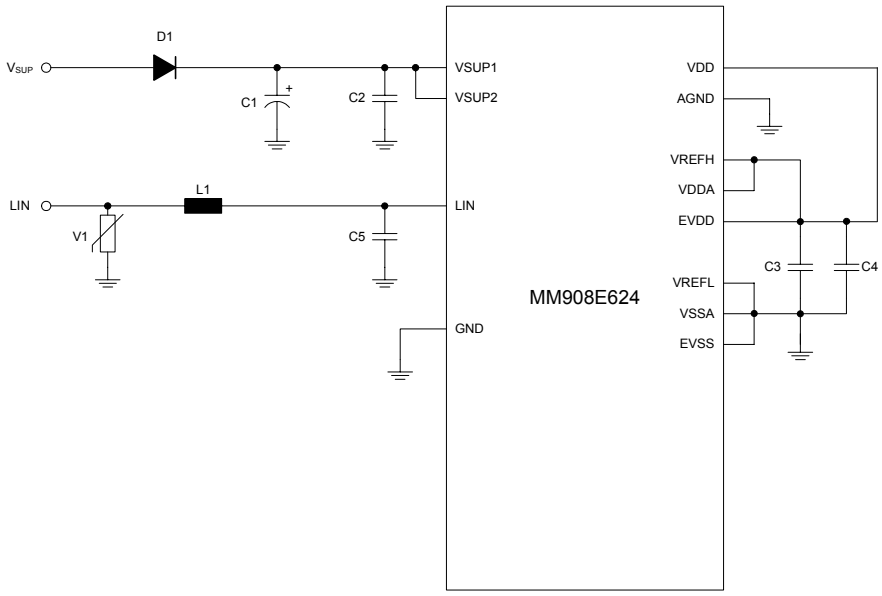


Figure 20. EMC/EMI recommendations

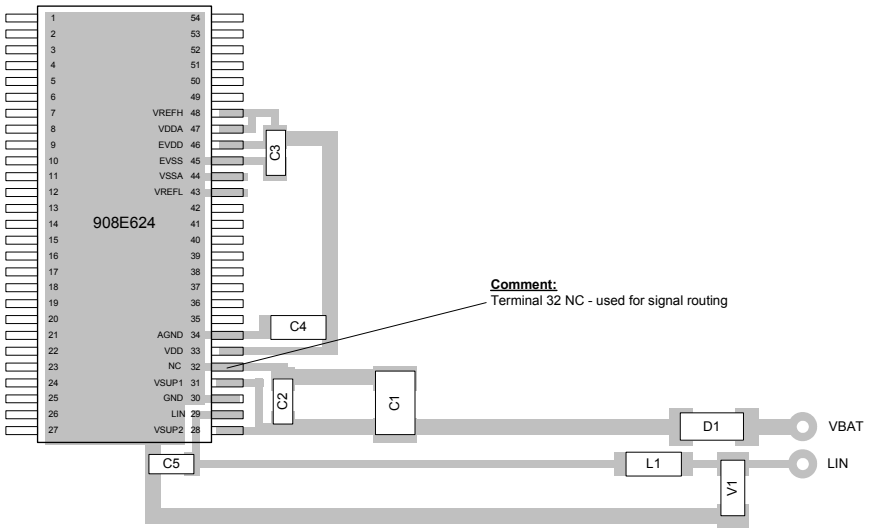


Figure 21. PCB Layout Recommendations

.

Table 15. Component Value Recommendation

Component	Recommended Value[36]	Comments / Signal routing
D1		Reverse battery protection
C1	Bulk Capacitor	
C2	100 nF, SMD Ceramic	Close (<5 mm) to VSUP1, VSUP2 terminals with good ground return
C3	100 nF, SMD Ceramic	Close (<3 mm) to digital supply terminals (EVDD, EVSS) with good ground return. The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4.7 μF, SMD Ceramic or Low ESR	Bulk Capacitor
C5	180 pF, SMD Ceramic	Close (<5 mm) to LIN terminal. Total Capacitance per LIN node has to be below 220 pF. (C_{total} = $C_{LIN-Terminal}$ + C5 + $C_{Varistor}$ ~ 10 pF + 180 pF + 15 pF)
V1[37]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[37]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

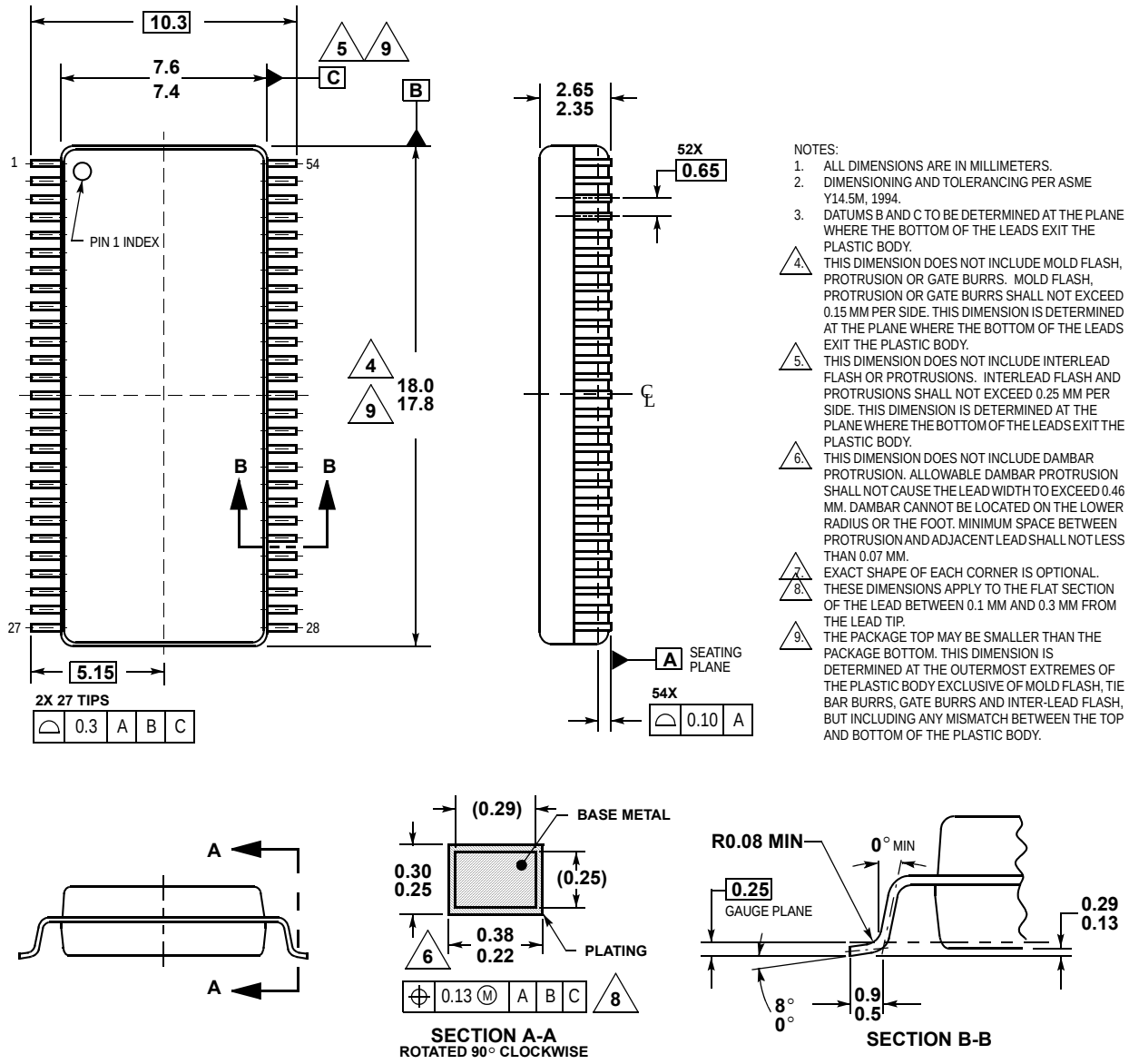
Notes

36. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
37. Components are recommended to improve EMC and ESD performance.

PACKAGING

PACKAGING DIMENSIONS

Important For the most current revision of the package, visit www.freescale.com and do a keyword search on the 98A drawing number below.



DWB SUFFIX
EW SUFFIX (Pb-FREE)
54-TERMINAL SOIC WIDE BODY
PLASTIC PACKAGE
98ASA99294D
ISSUE O

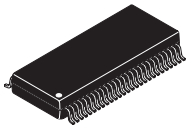
908E624

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 3.0)

908E624

54-TERMINAL SOICW



DWB SUFFIX
EW (Pb-FREE) SUFFIX
98ASA99294D
54-TERMINAL SOICW

Note For package dimensions, refer to the MM908E624 datasheet.

INTRODUCTION

This thermal addendum is provided as a supplement to the MM908E624 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

The MM908E624 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

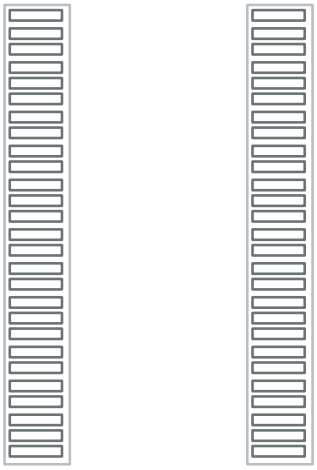
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below

Standards

Table 16. Thermal Performance Comparison

Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	40	31	36
$R_{\theta JBmn}$ (2)(3)	25	16	21
$R_{\theta JAmn}$ (1)(4)	57	47	52
$R_{\theta JCmn}$ (5)	21	12	16

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



54 Terminal SOIC
0.65 mm Pitch
17.9 mm x 7.5 mm Body

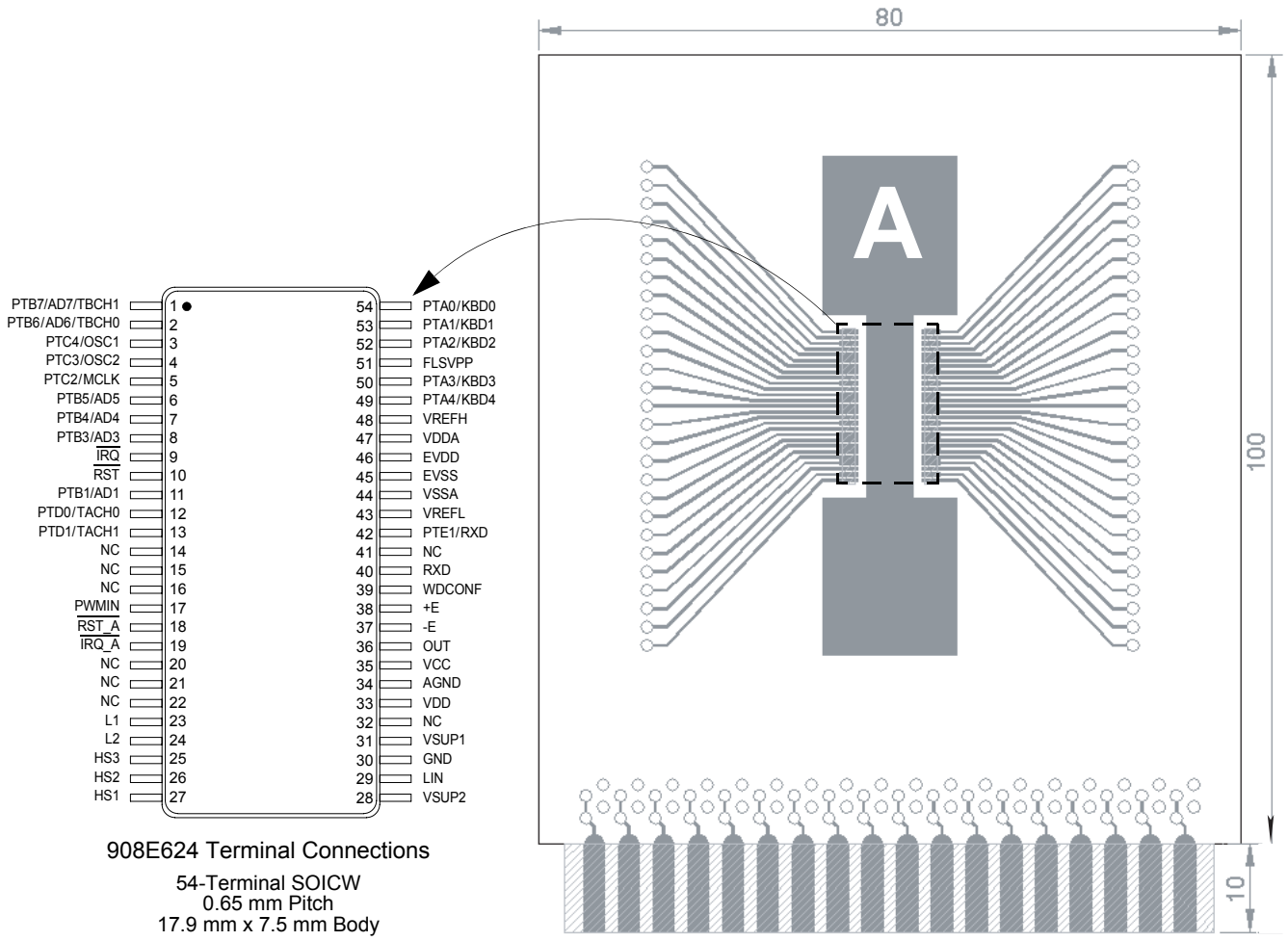


Figure 22. Surface Mount for SOIC Wide Body non-Exposed Pad

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 17. Thermal Resistance Performance

Terminal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1, n = 2** ***m*** **= 2, n = 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$	0	58	48	53
	300	56	46	51
	600	54	45	50

$R_{\theta JAmn}$ is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

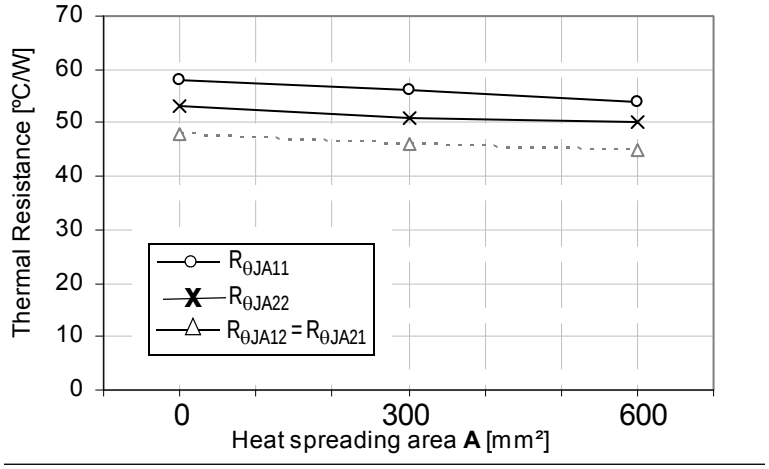


Figure 23. Device on Thermal Test Board

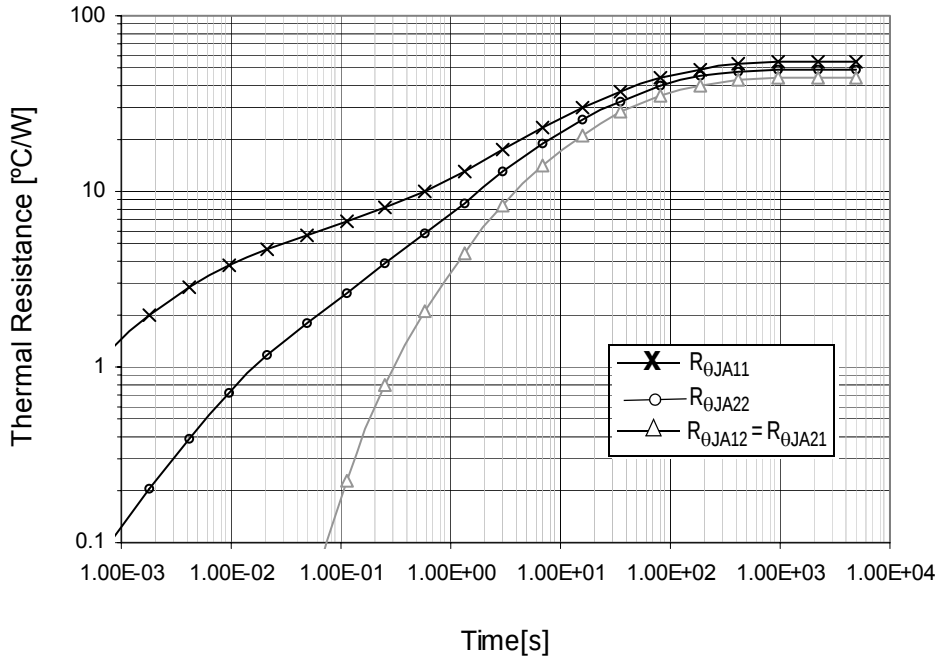


Figure 24. Transient Thermal Resistance $R_{\theta JA}$ (1.0 W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
7.0	5/2006	• Implemented Revision History page • Added Pb-Free package option (Suffix EW) and higher Soldering temperature • Added “Y” temperature (T_J -40°C to 125°C) code option (MM908E624AYEW) and updated condition statement for Static and Dynamic Electrical Characteristics • Corrected Figure 11, Operating Modes and Transitions (“STOP command” for transition from Normal to Stop state) • Updated Figure 21, PCB Layout Recommendations, comment NC Terminal used for signal routing • Updated Table 15, Component Value Recommendation • Corrected Figure 23, Device on Thermal Test Board • Removed reference to Note 11, Voltage Regulator - Dropout Voltage • Added comment “LIN in recessive state” to Supply Current Range in Stop Mode and Sleep Mode • Updated format to match current data sheet standard. • Added Figure 10, Power On Reset and Normal Request Time-out Timing • Added LIN P/L details • Made clarifications on Max Ratings Table for T_A and T_J Thermal Ratings and the accompanying Note
8.0	3/2007	• Removed “Advance Information” watermark from first page.

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