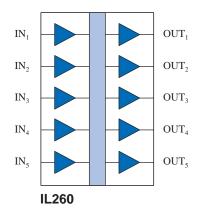
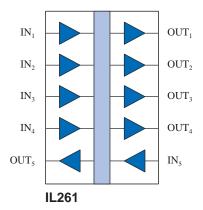


## High Speed Five-Channel Digital Isolators

#### **Functional Diagrams**





#### **Features**

- +5 V / +3.3 V CMOS/TTL Compatible
- High Speed: 110 Mbps
- Extended Temperature Range (-40°C to +85°C)
- 2500 V<sub>RMS</sub> Isolation (1 min.)
- 2 ns Typical Pulse Width Distortion
- 4 ns Typical Propagation Delay Skew
- 10 ns Typical Propagation Delay
- 30 kV/µs Typical Common Mode Rejection
- · 2 ns Channel-to-Channel Skew
- 0.3" and 0.15" 16-pin SOIC Packages
- UL1577 and IEC 61010-2001 Approval

#### **Applications**

- ADCs and DACs
- Multiplexed Data Transmission
- Data Interfaces
- · Board-to-Board Communication
- Digital Noise Reduction
- · Operator Interface
- Ground Loop Elimination
- Peripheral Interfaces
- Parallel Bus
- Logic Level Shifting
- Plasma Displays

#### **Description**

NVE's IL260 and IL261 five-channel high-speed digital isolators are CMOS devices manufactured with NVE's patented\* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, achieving the best specifications of any isolator. The unique fifth channel can be is used to distribute a single, isolated clock to multiple delta-sigma A-D converters. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

Typical transient immunity of 30 kV/ $\mu$ s is unsurpassed. Performance is specified over the temperature range of  $-40^{\circ}$ C to  $+85^{\circ}$ C without derating.

The IL260 and IL261 are available in 0.3" and 0.15" 16-pin SOIC packages. In the 0.15" packages, the five-channel devices provide the highest channel density available.

IsoLoop is a registered trademark of NVE Corporation. \*U.S. Patent number 5,831,426; 6,300,617 and others.



**Absolute Maximum Ratings** 

Parameters	Symbol	Min.	Тур.	Max.	Units	<b>Test Conditions</b>
Storage Temperature	$T_{s}$	-55		150	°C	
Ambient Operating Temperature (1)	$T_{A}$	-55		125	°C	
Supply Voltage	$V_{DD1}$ , $V_{DD2}$	-0.5		7	V	
Input Voltage	$V_{\rm I}$	-0.5		$V_{\rm DD} + 0.5$	V	
Output Voltage	$V_{o}$	-0.5		$V_{\rm DD} + 0.5$	V	
Output Current Drive	$I_{o}$	-10		10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

**Recommended Operating Conditions** 

Parameters	Symbol	Min.	Тур.	Max.	Units	Test Conditions
Ambient Operating Temperature	$T_{A}$	-40		85	°C	
Supply Voltage	$V_{DD1}$ , $V_{DD2}$	3.0		5.5	V	3.3/5.0 V Operation
Logic High Input Voltage	$V_{IH}$	2.4		$V_{\scriptscriptstyle  m DD}$	V	
Logic Low Input Voltage	$V_{\scriptscriptstyle IL}$	0		0.8	V	
Input Signal Rise and Fall Times	$t_{IR}, t_{IF}$			1	μs	

**Insulation Specifications** 

modiation opcomoditions						
Parameters	Symbol	Min.	Тур.	Max.	Units	Test Conditions
Creepage Distance (external)						
0.15" SOIC		4.03			mm	
0.3" SOIC		8.08			mm	
Leakage Current <sup>(5)</sup>			0.2		$\mu A_{\scriptscriptstyle RMS}$	$240 \text{ V}_{\text{RMS}}$
Barrier Impedance <sup>(5)</sup>			>10 <sup>14</sup>   7		$\Omega \parallel pF$	
Capacitance (Input–Output) <sup>(5)</sup>	$C_{I-O}$		5		pF	f = 1  MHz

#### Safety and Approvals

#### IEC61010-2001

TUV Certificate Numbers:

N1502812, N1502812-101

#### **Classification as Reinforced Insulation**

Model	Package	Pollution Degree	Material Group	Max. Working Voltage
IL260, IL261	0.3" 16-pin SOIC	II	III	$300  V_{RMS}$
IL260-3, IL261-3	0.15" 16-pin SOIC	II	III	$150 V_{RMS}$

#### UL 1577

Component Recognition Program File Number: E207481 Rated 2500 V<sub>RMS</sub> for 1 minute (SOIC, PDIP)

#### Soldering Profile

Per JEDEC J-STD-020C, MSL=2

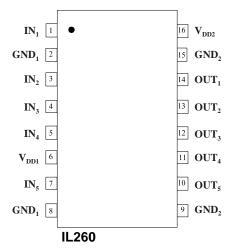
#### Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.



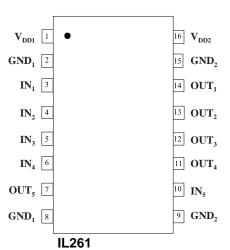
#### **IL260 Pin Connections**

1	IN <sub>1</sub>	Input 1
2	$GND_1$	Ground
3	$IN_2$	Input 2
4	$IN_3$	Input 3
5	$IN_4$	Input 4
6	$V_{DD1}$	Supply Voltage 1
7	$IN_5$	Input 5
8	$GND_1$	Ground
9	$GND_2$	Ground
10	OUT <sub>5</sub>	Output 5
11	OUT <sub>4</sub>	Output 4
12	OUT <sub>3</sub>	Output 3
13	$OUT_2$	Output 2
14	OUT <sub>1</sub>	Output 1
15	GND <sub>2</sub>	Ground
16	$V_{\mathrm{DD2}}$	Supply Voltage 2



#### **IL261 Pin Connections**

1	$V_{\mathrm{DD1}}$	Supply Voltage 1
2	$GND_1$	Ground
3	$IN_1$	Input 1
4	$IN_2$	Input 2
5	$IN_3$	Input 3
6	$IN_4$	Input 4
7	OUT <sub>5</sub>	Output 5
8	$GND_1$	Ground
9	$GND_2$	Ground
10	$IN_5$	Input 5
11	OUT <sub>4</sub>	Output 4
12	OUT <sub>3</sub>	Output 3
13	$OUT_2$	Output 2
14	$OUT_1$	Output 1
15	GND <sub>2</sub>	Ground
16	$V_{DD2}$	Supply Voltage 2





# 3.3 Volt Electrical Specifications Electrical Specifications are $T_{min}$ to $T_{max}$

Parameters	Symbol	Min.	Тур.	Max.	Units	<b>Test Conditions</b>		
Input Quiescent Current IL260	$I_{\mathrm{DD1}}$		30	50	μΑ			
IL261			1.5	2.0	mA			
Output Quiescent Current IL260	T		6.5	10	mA			
IL261	$I_{\mathrm{DD2}}$		5.5	8	mA			
Logic Input Current	$\mathbf{I}_{\mathrm{i}}$	-10		10	μΑ			
Logic High Output Voltage	$V_{\mathrm{OH}}$	V <sub>DD</sub> -0.1	$V_{\mathrm{DD}}$		V	$I_{O} = -20 \mu A, V_{I} = V_{IH}$		
Logic High Output Voltage	<b>▼</b> OH	$0.8 \times V_{DD}$	$0.9 \times V_{DD}$		<b>v</b>	$I_O = -4 \text{ mA}, V_I = V_{IH}$		
Logic Low Output Voltage	$V_{OL}$		0	0.1	v	$I_{O} = 20 \mu A, V_{I} = V_{IL}$		
Logic Low Output Voltage	V OL		0.5	0.8	·	$I_O = 4 \text{ mA}, V_I = V_{IL}$		
	Switching Specifications							
Maximum Data Rate		100	110		Mbps	$C_L = 15 \text{ pF}$		
Minimum Pulse Width	PW	10			ns	50% Points, V <sub>o</sub>		
Propagation Delay Input to Output			12	18	ns	$C_L = 15 \text{ pF}$		
(High to Low)	$t_{ m PHL}$		12	16	118	$C_L = 13 \text{ pF}$		
Propagation Delay Input to Output			12	18	ns	$C_L = 15 \text{ pF}$		
(Low to High)	t <sub>PLH</sub>		12	16	115	-		
Pulse Width Distortion $ t_{PHL}-t_{PLH} ^{(2)}$	PWD		2	3	ns	$C_L = 15 \text{ pF}$		
Propagation Delay Skew <sup>(3)</sup>	$t_{PSK}$		4	6	ns	$C_L = 15 \text{ pF}$		
Output Rise Time (10%–90%)	$t_R$		2	4	ns	$C_L = 15 \text{ pF}$		
Output Fall Time (10%–90%)	$t_{\mathrm{F}}$		2	4	ns	$C_L = 15 \text{ pF}$		
Common Mode Transient Immunity		20	30		1-37/110	V - 200 V		
(Output Logic High to Logic Low) <sup>(4)</sup>	$ CM_H ,  CM_L $	20	30		kV/μs	$V_{CN} = 300 \text{ V}$		
Channel to Channel Skew			2	3	ns	$C_L = 15 \text{ pF}$		
Dynamic Power Consumption <sup>(6)</sup>			140	240	μA/MHz	per channel		

#### **5 Volt Electrical Specifications**

Electrical Specifications are  $T_{min}$  to  $T_{max}$ 

Parameters	Symbol	Min.	Тур.	Max.	Units	Test Conditions		
Input Quiescent Current IL260	ī		30	50	μΑ			
IL261	$I_{\mathrm{DD1}}$		2.5	3.0	mA			
Output Quiescent Current IL260	T		10	15	mA			
IL261	$I_{\mathrm{DD2}}$		8	12	mA			
Logic Input Current	$I_{i}$	-10		10	μΑ			
Logic High Output Voltage	$V_{OH}$	$V_{\rm DD} = 0.1$	$V_{ m DD}$		v	$I_{O} = -20 \mu A, V_{I} = V_{IH}$		
Logic Trigii Output Voltage	V OH	$0.8 \times V_{DD}$	$0.9 \times V_{DD}$		•	$I_O = -4 \text{ mA}, V_I = V_{IH}$		
Logic Low Output Voltage	$V_{OL}$		0	0.1	v	$I_{O} = 20 \mu A, V_{I} = V_{IL}$		
Logic Low Output Voltage	V OL		0.5	0.8	•	$I_O = 4 \text{ mA}, V_I = V_{IL}$		
	Switching Specifications							
Maximum Data Rate		100	110		Mbps	$C_L = 15 \text{ pF}$		
Minimum Pulse Width <sup>(7)</sup>	PW	10			ns	50% Points, V <sub>o</sub>		
Propagations Delay Input to Output	<b>+</b>		10	15	ns	$C_L = 15 \text{ pF}$		
(High to Low)	$t_{ m PHL}$		10	13	118	CL = 13 pr		
Propagations Delay Input to Output	t		10	15	ns	$C_L = 15 \text{ pF}$		
(Low to High)	t <sub>PLH</sub>		10	13	115	CL = 13 pr		
Pulse Width Distortion $ t_{PHL}-t_{PLH} ^{(2)}$	PWD		2	3	ns	$C_L = 15 \text{ pF}$		
Propagation Delay Skew (3)	$t_{PSK}$		4	6	ns	$C_L = 15 \text{ pF}$		
Output Rise Time (10%–90%)	$t_R$		1	3	ns	$C_L = 15 \text{ pF}$		
Output Fall Time (10%–90%)	$t_{\mathrm{F}}$		1	3	ns	$C_L = 15 \text{ pF}$		
Common Mode Transient Immunity		20	30		l <sub>z</sub> V/uc	V = 200 V		
(Output Logic High to Logic Low)	$ CM_H ,  CM_L $	20	30		kV/μs	$V_{CN} = 300 \text{ V}$		
Channel-to-Channel Skew			2	3	ns	$C_L = 15 \text{ pF}$		
Dynamic Power Consumption <sup>(6)</sup>			200	340	μA/MHz	per channel		



#### Notes (apply to both 3.3 V and 5 V specifications):

- 1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
- 2. PWD is defined as  $|t_{PHL} t_{PLH}|$ . %PWD is equal to PWD divided by pulse width.
- 3.  $t_{PSK}$  is the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  between devices at 25°C.
- 4.  $CM_{\rm H}$  is the maximum common mode voltage slew rate that can be sustained while maintaining  $V_{\rm O} > 0.8~V_{\rm DD2}$ .  $CM_{\rm L}$  is the maximum common mode input voltage that can be sustained while maintaining  $V_{\rm O} < 0.8~V$ . The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
- 5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
- 6. Dynamic power consumption numbers are calculated per channel and are supplied by the channel's input side power supply.
- 7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.



#### **Application Information**

#### **Dynamic Power Consumption**

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

#### **Power Supply Decoupling**

Both power supplies to these devices should be decoupled with low ESR 47 nF ceramic capacitors. Ground planes for both  $GND_1$  and  $GND_2$  are highly recommended for data rates above 10 Mbps. Capacitors must be located as close as possible to the  $V_{DD}$  pins.

#### Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

#### **Data Transmission Rates**

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

For example, with data rates of 12.5 Mbps:

PWD% = 
$$\frac{3 \text{ ns}}{80 \text{ ns}}$$
 x 100% = 3.75%

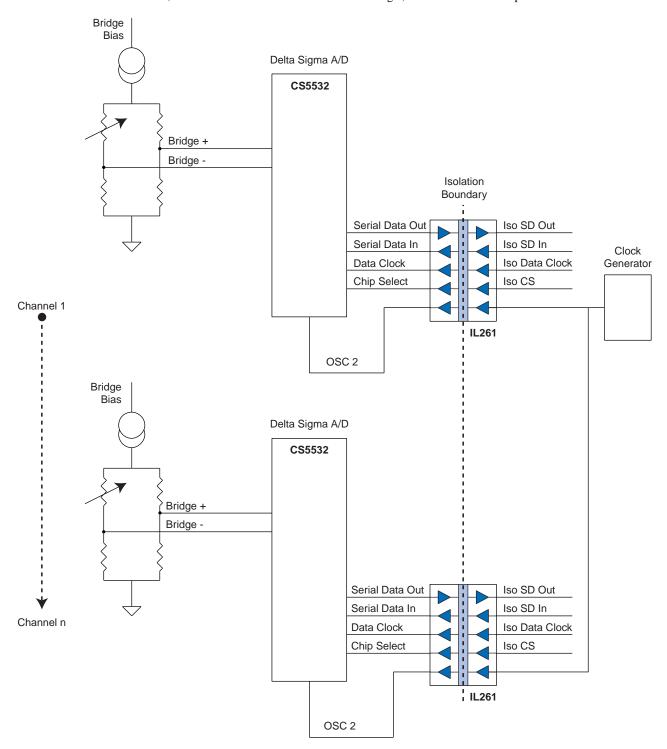
This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in IL260/IL261 Isolators is only 3 ns, which is **ten times** better than any optocoupler. IL260/IL261 Isolators have a maximum propagation delay skew of 6 ns, which is **five times** better than any optocoupler.



### Application Diagram—Multi-Channel Delta-Sigma A/D Converter

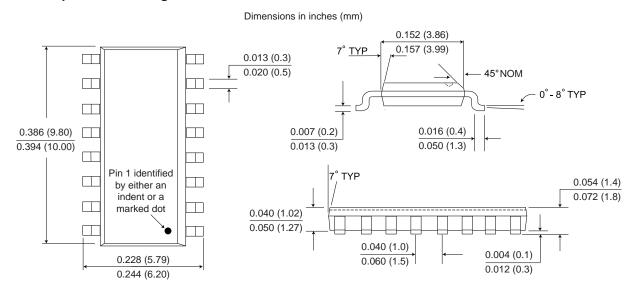
In a typical single-channel delta-sigma ADC, the system clock is located on the isolated side of the system and only four channels of isolation are required. With multiple ADCs configured in a channel-to-channel isolation configuration, however, clock jitter and edge placement accuracy of the system clock must be matched between ADCs. The best solution is to use a single clock on the system side and distribute the clock to each ADC. The five-channel IL261 is ideal, with the fifth channel used to distribute a single, isolated clock to multiple ADCs as shown below:



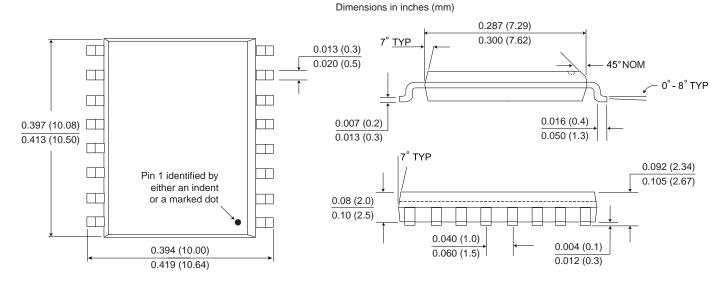


#### Package Drawings, Dimensions and Specifications

#### 0.15" 16-pin SOIC Package

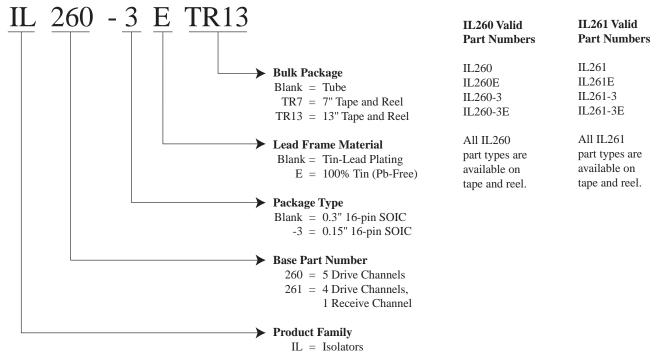


#### 0.3" 16-pin SOIC Package





### **Ordering Information and Valid Part Numbers**





#### **Revision History**

#### ISB-DS-001-IL260/1-E April 2007

Eliminated soldering profile chart

ISB-DS-001-IL260/1-D January 2007

#### Change

Change

- Revised application drawing
- Revised package drawings
- Misc. syntax changes

ISB-DS-001-IL260/1-C

#### Change

Page 2: UL File Number and TUV Certificate Numbers added

Page 9: Soldering Profile added.

ISB-DS-001-IL260/1-B

#### Change

Page 1: Revision letter added Old ISB number removed

- Page 2: Storage temperature changed from 175°C max to 150°C max.
- Page 2: Lead soldering temperature changed from 280°C max to 260°C max.
- Page 2: Absolute Maximum Ratings: Ambient Operation Note (1) added.
- Page 2: Recommended Operating Conditions: Ambient Operation Note (1) removed.
- Page 2: IEC 61010-1 Classification "as Table 1 Reinforced Insulation" added.
- Page 9: Ordering Information. 5 volt only option removed.

  Valid Part Numbers IL260 B, IL260BE, IL260BETR13, IL260BTR13, IL260-3B, IL260-3BETR7, IL260-3BTR13, IL260-3BETR7, IL260-3BETR13, IL261B IL261BE, IL261BETR13, IL261BTR13, IL261-3B, IL261-3BE, IL261-3BTR7, IL261-3BTR13, IL261-3BETR13 removed.



#### **About NVE**

An ISO 9001 Certified Company

NVE Corporation is a high technology components manufacturer having the unique capability to combine spintronic Giant Magnetoresistive (GMR) materials with integrated circuits to make high performance electronic components. Products include Magnetic Field Sensors, Magnetic Field Gradient Sensors (Gradiometer), Digital Magnetic Field Sensors, Digital Signal Isolators and Isolated Bus Transceivers.

NVE is a leader in GMR research and in 1994 introduced the world's first products using GMR material, a line of GMR magnetic field sensors that can be used for position, magnetic media, wheel speed and current sensing.

NVE is located in Eden Prairie, Minnesota, a suburb of Minneapolis. Please visit our Web site at www.nve.com or call (952) 829-9217 for information on products, sales or distribution.

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Specifications shown are subject to change without notice.

ISB-DS-001-IL260/1-E

April 2007